

CMOS 4-BIT MICROCONTROLLER

TMP47C441AN

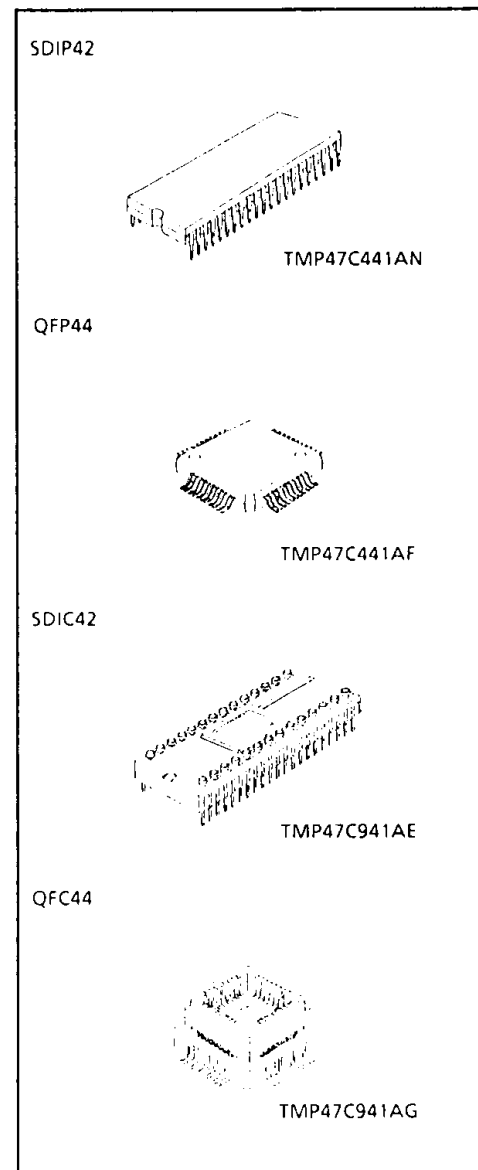
TMP47C441AF

The 47C441A has 8-bit A/D converter, watchdog timer, and high breakdown voltage outputs based on the TLCS-47 CMOS series.

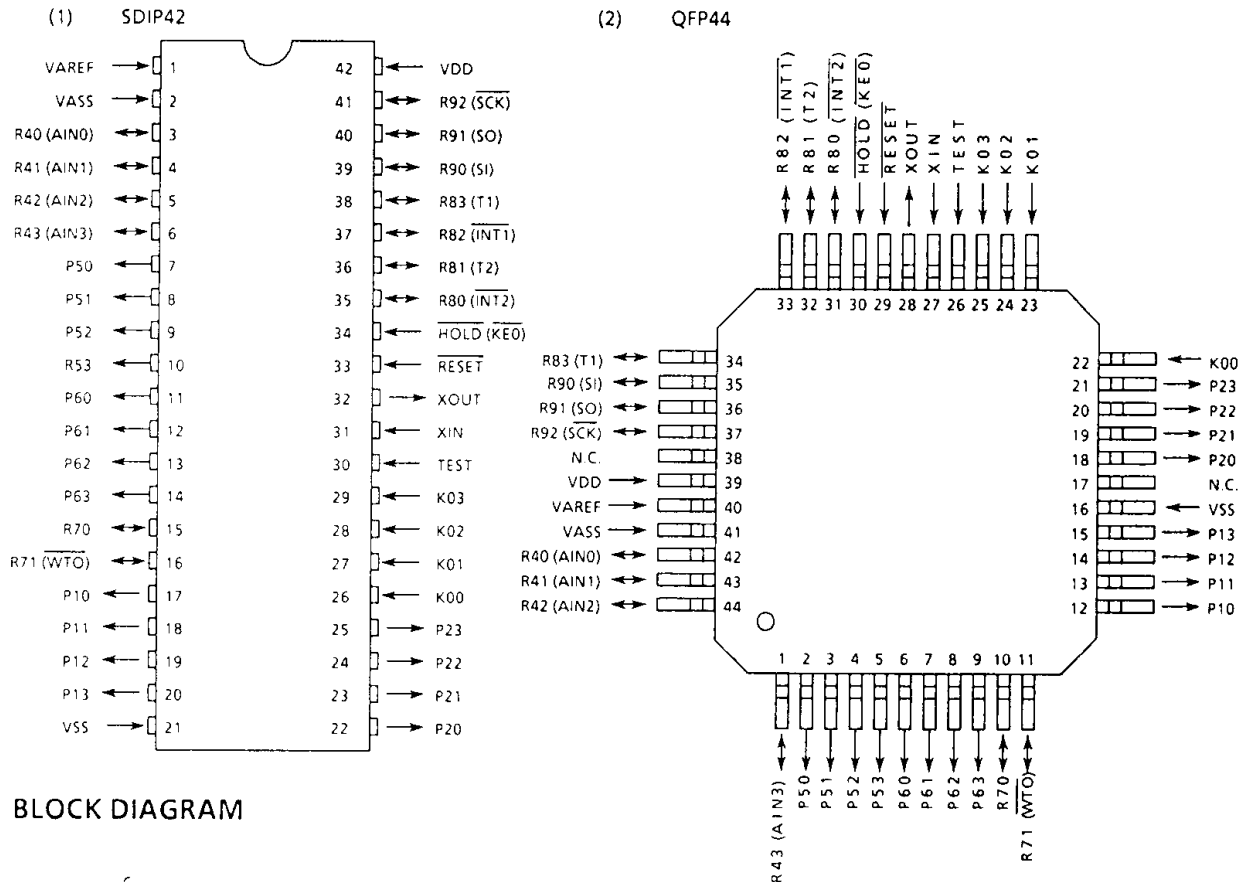
PART No	ROM	RAM	PACKAGE	PIGGYBACK
TMP47C441AN	4096 x 8-bit	256 x 4-bit	SDIP42	TMP47C941AE
TMP47C441AF			QFP44	TMP47C941AG

FEATURES

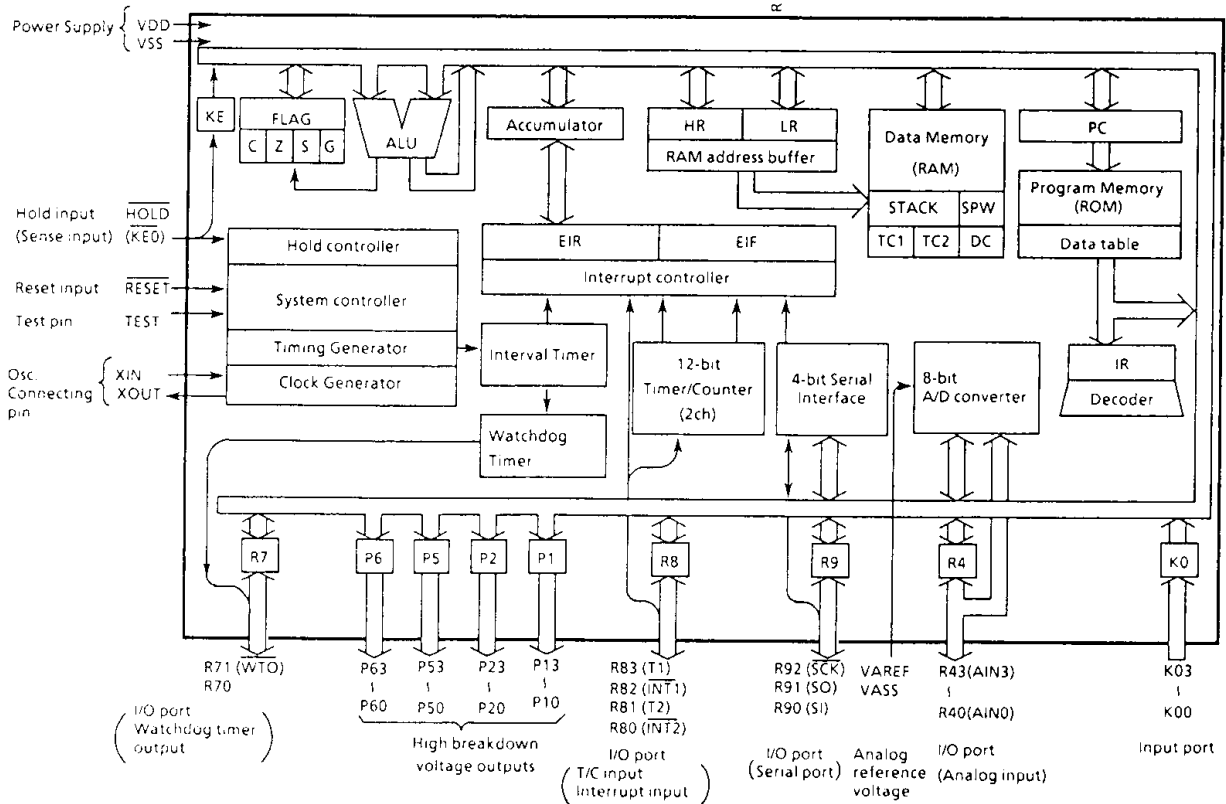
- ◆ 4-bit single chip microcomputer
- ◆ Instruction execution time : 1.9 μ s (at 4.2MHz)
- ◆ 90 basic instructions
- ◆ Table look-up instructions
- ◆ 5-bit to 8-bit data conversion instruction
- ◆ Subroutine nesting : 15 levels max.
- ◆ 6 interrupt sources (External : 2, Internal : 4)
 - All sources have independent latches each, and multiple interrupt control is available
- ◆ I/O port (34 pins)
 - Input 2ports 5pins
 - Output 4ports 16pins
 - I/O 4ports 13pins
- ◆ Interval timer
- ◆ Two 12-bit Timer/Counters
 - Timer, event counter, and pulse width measurement mode
- ◆ Watchdog Timer
- ◆ Serial Interface with 4-bit buffer
 - External/internal clock, leading/trailing edge shift mode
- ◆ 8-bit successive approximate type A/D converter
 - With sample and hold
 - 4 analog inputs
 - Converting time : 48 μ s (4MHz)
- ◆ High breakdown voltage outputs
 - VFT direct drive capability (max. 42V x 16bits)
- ◆ Hold function
 - Battery/Capacitor back-up
- ◆ Real Time Emulator : BM47214A



PIN ASSIGNMENTS (TOP VIEW)



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 - K00	Input	4-bit input port	
P13 - P10	Output	4-bit output port with latch.	
P23 - P20		8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @HL].	
R43 (AIN3) - R40 (AIN0)	I/O (Input)	4-bit I/O port with latch. When using as input port, the latch must be set to "1".	A / D converter analog input
P53 - P50	Output	4-bit output port with latch	
P63 - P60			
R71 (\overline{WTO})	I/O (Output)	2-bit I/O port with latch.	Watchdog timer output
R70	I/O	When using as input port or watchdog timer output, the latch must be set to "1".	
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When using as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 (\overline{SCK})	I/O (I/O)	3-bit I/O port with latch. When using as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
XIN	Input	Resonator connecting pin.	
XOUT	Output	For inputting external clock, XIN is used and XOUT is opened.	
\overline{RESET}	Input	Reset signal input	
\overline{HOLD} ($\overline{KE0}$)	Input (Input)	HOLD request/release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 5V	
VSS		0V (GND)	
VAREF \star		A/D converter analog reference voltage (High)	
VASS		A/D converter analog reference voltage (Low)	

OPERATIONAL DESCRIPTION

Concerning the 47C441A, the hardware configuration and operation are described. As the description is provided with priority on those parts differing from the 47C400A and 47C440A, the technical data sheets for the 47C400A and 47C440A, shall also be referred to.

1. SYSTEM CONFIGURATION

- (1) I/O Ports
- (2) A/D Converter
- (3) Watchdog Timer

2. PERIPHERAL HARDWARE FUNCTION

2.1 Ports

The 47C441A has 10 I/O ports (34 pins).

This section describes ports P1, P2, P5, P6 which are changed from the 47C440A.

Table 2-1 lists the port address assignments and the I/O instructions that can access the ports.

- (1) Ports P1, P2, P5, P6

These are 4-bit high breakdown voltage output ports with latch capable of directly driving vacuum fluorescent tubes (VFT). Latch data are read when the input instruction is executed. During reset, the latch is initialized to "0".

8-bit data can be output through P1 and P2 by using the 5-bit to 8-bit data conversion instruction; therefore, these ports can also be effectively utilized as segment outputs.

Ports P5 and P6 can be set and cleared in 1-bit units using the L-register indirect addressing bit manipulation instruction; therefore, these ports can also be effectively utilized as digit outputs.

Figure 2-2 shows an example of driving a VFT 8-segment x 8-digit display.

Port P* (Port address OP0*/IP0*)

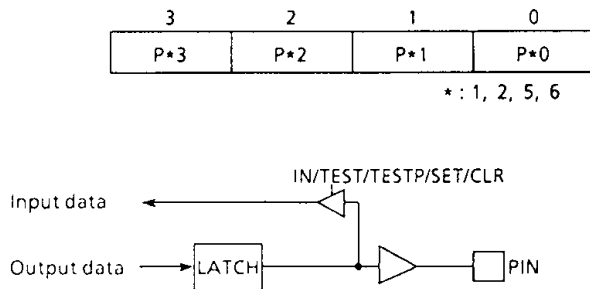


Figure 2-1. Ports P1, P2, P5, P6

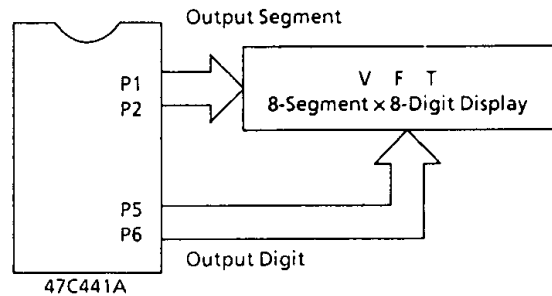


Figure 2-2. Example of driving a VFT

- (2) Port R4 (R43-R40)

Port R4 is 4-bits I/O ports with latch shared by the analog inputs for A/D converter. When used as an input ports or analog inputs, the latch should be set to "1". If other port is used as an output, be careful not to execute the output instruction for any port during A/D conversion in order to keep accuracy of conversion. The latch is initialized to "1" and analog input is selected R40 (AIN0) pin during reset.

Port R4 (Port address OP04/IP04)

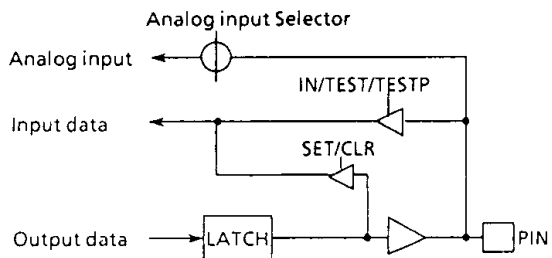
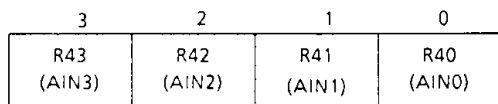


Figure 2-3. Port R4

2.2 A/D Converter

The 47C441A has a 8-bit successive approximate type A/D converter and is capable of processing 4 analog inputs.

2.2.1 Circuit configuration

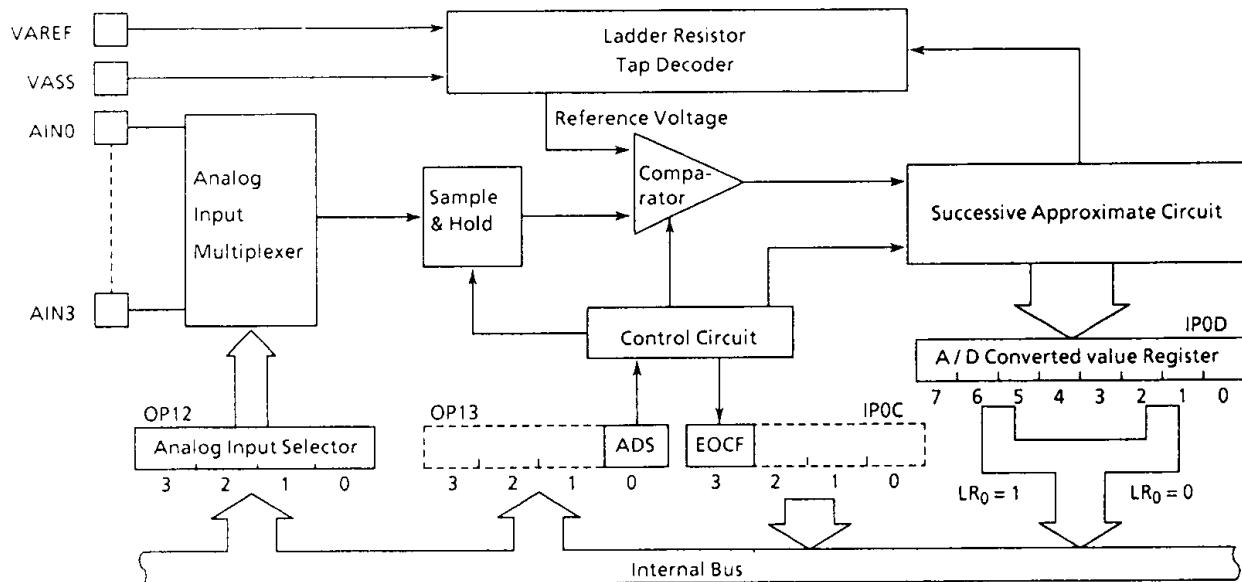


Figure 2-4. Block Diagram of A/D Converter

2.2.2 Control of A/D converter

The operation of A/D converter is controlled by a command. The command register is accessed as port addresses OP12 and OP13. A/D converted value and end of conversion flag (EOCF) can be known by accessing port addresses IPOD and IPOC.

(1) Analog input selector

Analog inputs (AIN0 through AIN3) are selected by values of this register.

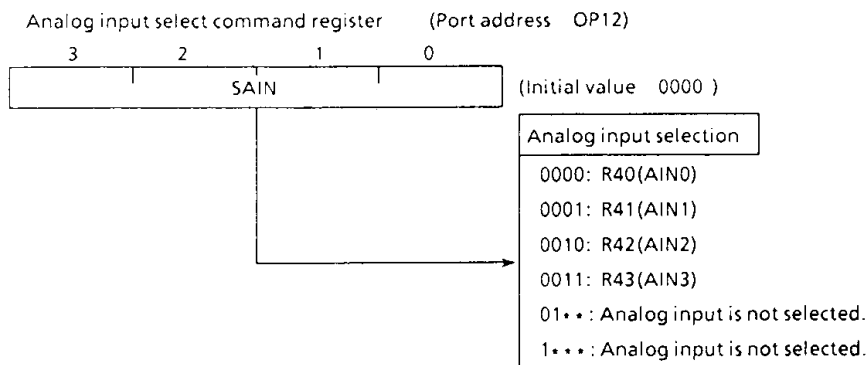


Figure 2-5. Analog input selector

(2) Start of A/D conversion

A/D conversion is started when ADS is set to "1". After the conversion is started, ADS is cleared by hardware. If the restart is requested during the conversion, the conversion is started again at the time.

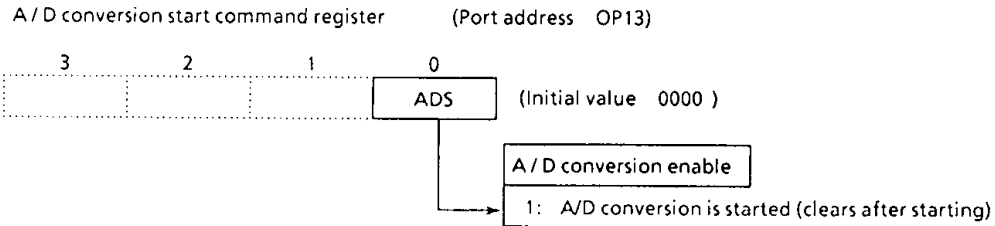


Figure 2-6. A/D conversion start register

(3) A/D converted value register

An A/D converted value is read by accessing port address IP0D. An A/D converted value is read by splitting into upper 4 bits and lower 4 bits by a value of LR₀ (LSB of the L registers).

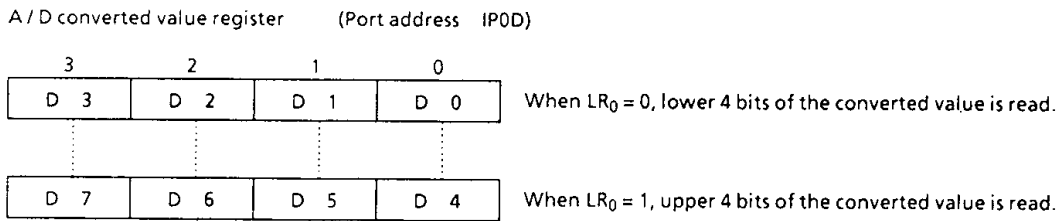


Figure 2-7. A/D converted value register

(4) A/D converter status register

End of conversion flag (EOCF) is a single bit flag showing the end of conversion and is set to "1" when conversion ended. When both upper 4 bits and lower 4 bits of a converted value are read or A/D conversion is started, EOCF is cleared to "0".

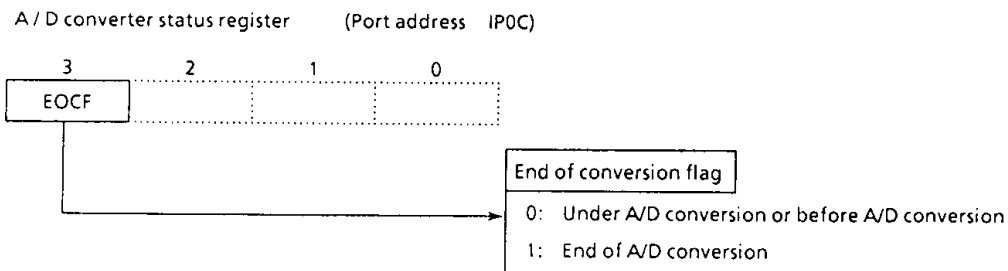


Figure 2-8. A/D converter status register

2.2.3 How to use A/D converter

Apply positive of analog reference voltage to the VAREF pin and negative to the VASS pin. The A/D conversion is carried out by splitting reference voltage between VAREF and VASS to bit corresponding voltage by a ladder resistor and making a judgement by comparing it with analog input voltage.

(1) Start of A / D conversion

Prior to conversion, select one of the analog input AIN0 through AIN3 by the analog input selector. Place output of the analog input, which is to be A/D converted, in the high impedance state by setting "1". If other port is used as an output, be careful not to execute the output instruction for any port during conversion in order to keep accuracy of conversion.

A/D conversion is started by setting ADS (bit 1 of the A/D conversion start register). When conversion ends after 24 instruction cycles, EOCF showing the end of conversion is set to "1".

(2) Reading of an A/D converted value

After the end of conversion, read an A/D converted value is read by splitting into lower 4 bits and upper 4 bits by the A/D converted value register (IP0D).

Lower 4 bits of the A/D converted value can be read when LR₀ = 0 and upper 4 bits when LR₀ = 1. Usually an A/D converted value is stored in RAM by an instruction [IN %p, @HL]. Further, if an A/D converted value is read during the conversion, it becomes an indefinite value.

(3) A / D conversion with HOLD operation

When the HOLD operation is started during the conversion, the conversion is terminated and an A/D converted value becomes indefinite. Therefore, EOCF is kept clear to "0" after release from the HOLD operation. However, if the HOLD operation is started after the end of A/D conversion (after EOCF has been set), A/D converted value and status of EOCF are held.

Example: Selecting analog input (AIN3), starting A/D conversion, monitoring EOCF and storing lower 4 bits and upper 4 bits of a converted value to RAM [10_H] and RAM [11_H] respectively.

```

LD      A, #3           ; Selects analog input (AIN3)
OUT     A, %OP12
LD      A, #1           ; Start of A/D conversion
OUT     A, %OP13
SLOOP : TEST    %IP0C, 3 ; To wait until EOCF goes to "1"
        B       SLOOP
LD      HL, #10H        ; HL ← 10H
IN      %IP0D, @HL     ; RAM [10H] ← Lower 4 bits
INC     L               ; Increment of L registers
IN      %IP0D, @HL     ; RAM [11H] ← Upper 4 bits

```


2.3 Watchdog Timer (WDT)

The purpose of the watchdog timer is to detect the malfunction (runaway) of program due to external noise or other causes and return the operation to the normal condition.

The watchdog timer output is output to R71 must be set to "1". Further, during reset, the output latch of R71 is set to "1", and the watchdog timer becomes disable state.

The initialization at time of runaway will become possible when the \overline{WTO} pin and \overline{RESET} pin are connected each other.

2.3.1 Configuration of Watchdog Timer

The watchdog timer consists of 3-stage binary counter, flip-flop (F/F), and its control circuit. The F/F is set to "1" during reset, and cleared to "0" at the rising edge of the binary counter output.

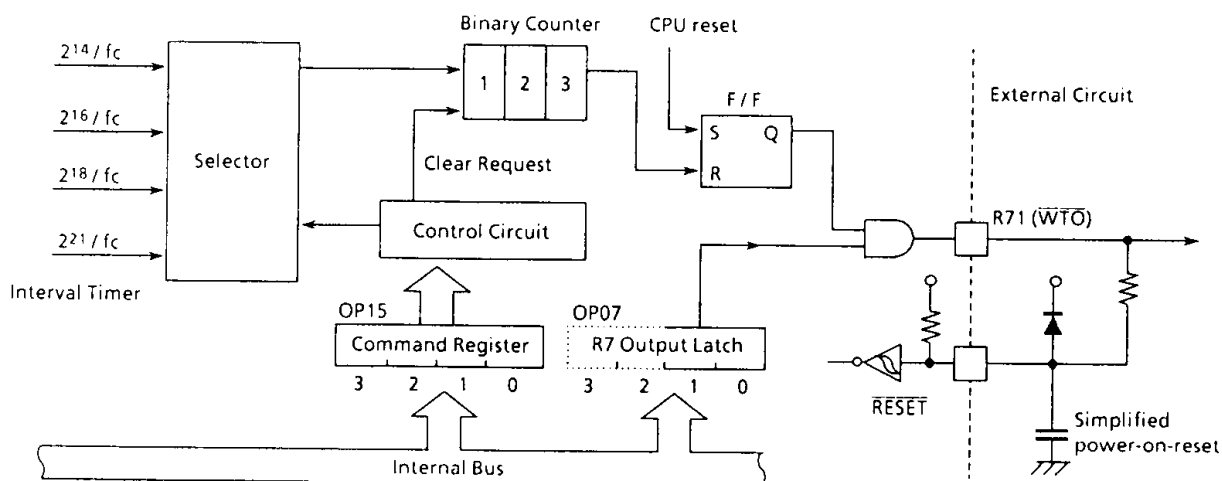


Figure 2-9. Watchdog Timer

2.3.2 Control of watchdog timer

The watchdog timer is controlled by the command register (OP15). This command register is initialized to "1000₈" during reset. The following are procedure to detect the malfunction (runaway) of CPU by the watchdog timer.

- ① At first, detection time of the watchdog timer should be set and binary counter should be cleared.
- ② The watchdog timer should be become enable.
- ③ Binary counter must be cleared before the detection time of the watchdog timer. When the runaway of CPU is taken place for some reason and binary counter is not cleared, the F/F is cleared to "0" at the rising edge of the binary counter and signal of runaway detection is become active (\overline{WTO} output is "L").

Watchdog Timer control command register (Port address OP15)

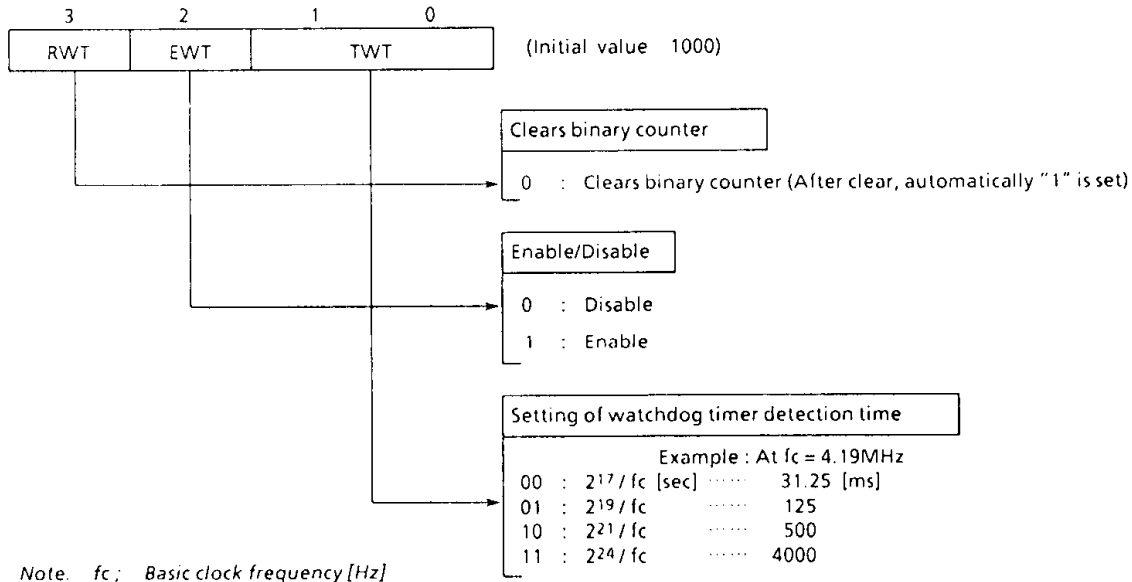


Figure 2-10. Command Register

Example : To set the watchdog detection time ($2^{21}/fc[\text{sec}]$). And to enable the watchdog timer.

```

LD      A, #0010B      ; OP15 ← 0010B
                        (Sets WDT detection time. Clears binary counter)
OUT     A, %OP15
LD      A, #1110B      ; OP15 ← 1110B (Enables WDT)
OUT     A, %OP15
:
:
:
:
LD      A, #0110B      ; OP15 ← 0110B (Clears binary counter)
OUT     A, %OP15
:
:
:
    
```

Within WDT detection time

Note. It is not necessary to set RWT to "1". Note that both EWT (Enable Watchdog Timer) and RWT should not be set to "1" at the same time.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V _{DD}		- 0.5 to 7	V
Input Voltage	V _{IN}		- 0.5 to V _{DD} + 0.5	V
Output Voltage	V _{OUT1}	Except open drain pin	- 0.5 to V _{DD} + 0.5	V
	V _{OUT2}	Ports R7, R8, R9	- 0.5 to 10	
	V _{OUT3}	Analog inputs	- 0.5 to V _{DD} + 0.5	
	V _{OUT4}	Source open drain pin	- 35 to V _{DD} + 0.5	
Output Current (Per 1 pin)	I _{OUT1}	Ports P1, P2	- 10	mA
	I _{OUT2}	Ports P5, P6	- 25	
	I _{OUT3}	Ports R7, R8, R9	3.2	
Output Current (Total)	ΣI _{OUT2}	Ports P5, P6	- 100	mA
Power Dissipation [T _{opr} = 70°C]	PD		600	mW
Soldering Temperature (time)	T _{sld}		260 (10sec)	°C
Storage Temperature	T _{stg}		- 55 to 125	°C
Operating Temperature	T _{opr}		- 30 to 70	°C

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V, T_{opr} = - 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V _{DD}		In the Normal mode	4.5	6.0	V
			In the HOLD mode	2.0		
Input High Voltage	V _{IH1}	Except Hysteresis Input	V _{DD} ≥ 4.5V	V _{DD} × 0.7	V _{DD}	V
	V _{IH2}	Hysteresis Input		V _{DD} × 0.75		
	V _{IH3}		V _{DD} < 4.5V	V _{DD} × 0.9		
Input Low Voltage	V _{IL1}	Except Hysteresis Input	V _{DD} ≥ 4.5V	0	V _{DD} × 0.3	V
	V _{IL2}	Hysteresis Input			V _{DD} × 0.25	
	V _{IL3}		V _{DD} < 4.5V		V _{DD} × 0.1	
Clock Frequency	f _c			0.4	4.2	MHz

Note. Input voltage V_{IH3}, V_{IL3} : in the HOLD mode

D.C. CHARACTERISTICS

 $(V_{SS} = 0V, T_{opr} = -30 \text{ to } 70^{\circ}C)$

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST, RESET, HOLD	$V_{DD} = 5.5V,$ $V_{IN} = 5.5V / 0V$	—	—	± 2	μA
	I_{IN2}	Ports R (open drain)					
Input Resistance	R_{IN1}	Port K0 with pull-up/pull-down		30	70	150	K Ω
	R_{IN2}	RESET		100	220	450	
Output Leakage Current	I_{LO1}	Ports R (Sink open drain)	$V_{DD} = 5.5V, V_{OUT} = 5.5V$	—	—	2	μA
	I_{LO2}	Ports P (Source open drain)	$V_{DD} = 5.5V, V_{OUT} = -32V$	—	—	-2	
Output High Voltage	V_{OH1}	Ports P1, P2	$V_{DD} = 4.5V, I_{OH} = -4mA$	2.4	—	—	V
Output Low Voltage	V_{OL2}	Except XOUT, ports P	$V_{DD} = 4.5V, I_{OL} = 1.6mA$	—	—	0.4	V
High output Current	I_{OH2}	Ports P5, P6	$V_{DD} = 4.5V, V_{OH} = 2.4V$	—	-15	—	mA
Supply Current (in the Normal mode)	I_{DD}		$V_{DD} = 5.5V, f_c = 4MHz$	—	3	6	mA
Supply Current (in the HOLD mode)	I_{DDH}		$V_{DD} = 5.5V$	—	0.5	10	μA

Note 1. Typ. values show those at $T_{opr} = 25^{\circ}C, V_{DD} = 5V$.

Note 2. Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. Supply Current I_{DD}, I_{DDH} ; $V_{IN} = 5.3V / 0.2V$
The K0 port is open when the input resistor is contained. The voltage applied to the R port is within the valid range.

A/D CONVERSION CHARACTERISTICS

 $(T_{opr} = -30 \text{ to } 70^{\circ}C)$

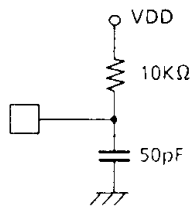
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT	
Analog Reference Voltage	V_{AREF}		$V_{DD} - 1.5$	—	V_{DD}	V	
	V_{ASS}		V_{SS}	—	1.5		
Analog Reference Voltage Range	ΔV_{AREF}	$V_{AREF} - V_{ASS}$	2.5	—	—	V	
Analog Input Voltage	V_{AIN}		V_{ASS}	—	V_{AREF}	V	
Analog Supply Current	I_{REF}		—	0.5	1.0	mA	
Nonlinearity Error		$V_{DD} = 5.0V, V_{SS} = 0.0V$	—	—	± 1	LSB	
Zero Point Error			—	—	± 1		
Full Scale Error			$V_{AREF} = 5.000V$	—	—		± 1
Total Error			$V_{ASS} = 0.000V$	—	—		± 2

A. C. CHARACTERISTICS

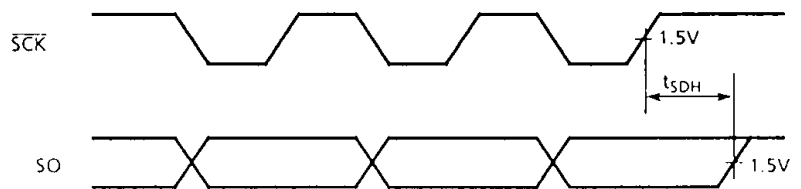
($V_{SS} = 0V$, $V_{DD} = 4.5$ to $6.0V$, $T_{opr} = -30$ to $70^{\circ}C$)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		1.9	—	20	μs
High level Clock pulse Width	t_{WCH}	External clock mode	80	—	—	ns
Low level Clock pulse Width	t_{WCL}					
A/D Sampling Time	$t_{\Delta IN}$	$f_c = 4MHz$	—	4	—	μs
Shift data Hold Time	t_{SDH}		$0.5t_{cy} - 300$	—	—	ns

Note. Shift data Hold Time :
External circuit for \overline{SCK} pin and SO pin



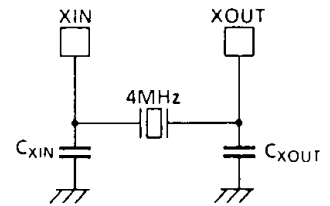
Serial port (completion of transmission)



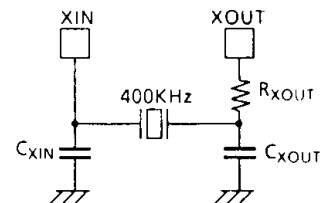
RECOMMENDED OSCILLATING CONDITIONS

($V_{SS} = 0V$, $V_{DD} = 4.5$ to $6.0V$, $T_{opr} = -30$ to $70^{\circ}C$)

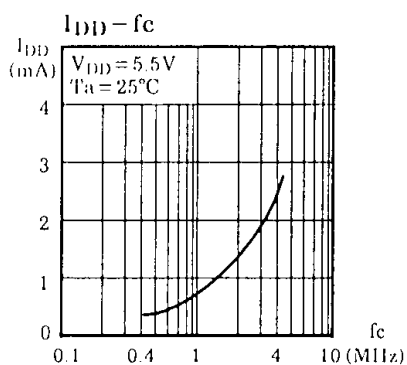
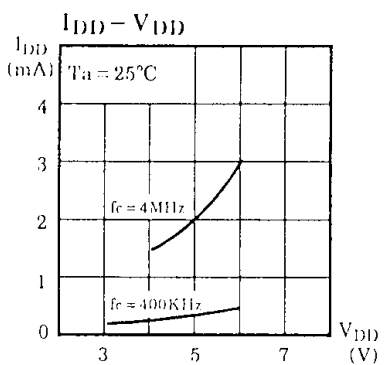
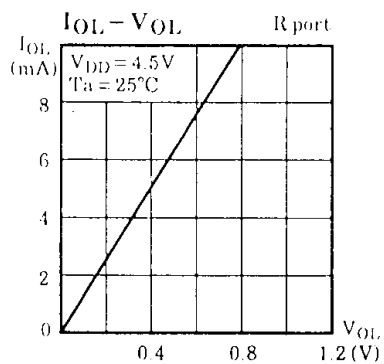
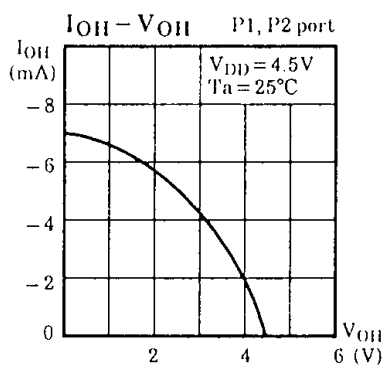
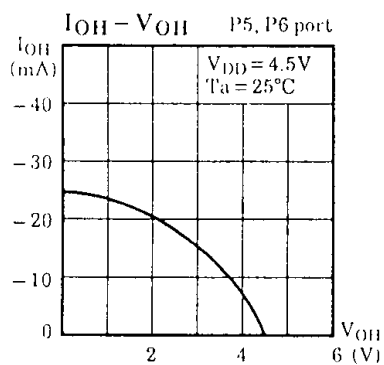
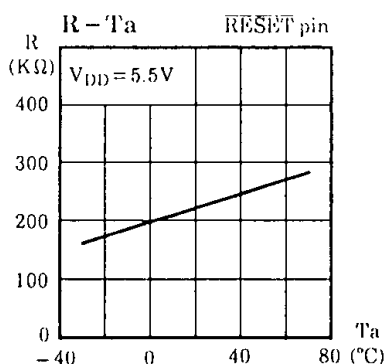
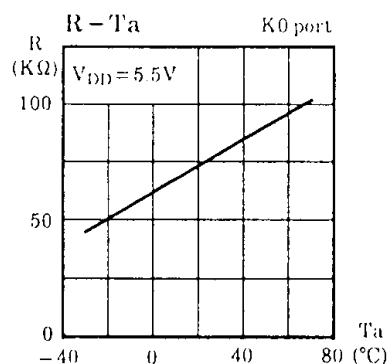
- (1) 4MHz
Ceramic Resonator
CSA4.00MG (MURATA) $C_{XIN} = C_{XOUT} = 30pF$
KBR-4.00MS (KYOCERA) $C_{XIN} = C_{XOUT} = 30pF$
Crystal Oscillator
204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT} = 20pF$



- (2) 400KHz
Ceramic Resonator
CSB400B (MURATA) $C_{XIN} = C_{XOUT} = 220pF$, $R_{XOUT} = 6.8K\Omega$
KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT} = 100pF$, $R_{XOUT} = 10K\Omega$



TYPICAL CHARACTERISTICS



INPUT/OUTPUT CIRCUITRY

(1) Control pins

The input/output circuitries of the 47C441A control pins are similar to that of the 47C400A.

(2) I/O Ports

The input/output circuitries of the 47C441A I/O ports are shown as below, any one of the circuitries can be chosen by a code (TA-TC) as a mask option.

PORT	I/O	INPUT/OUTPUT CIRCUITRY and CODE			REMARKS
		TA	TB	TC	
K0	Input				<p>Pull-up/pull-down resistor</p> <p>$R_{IN} = 70K\Omega$ (typ.)</p> <p>$R = 1K\Omega$ (typ.)</p>
P1 P2 P5 P6	Output				<p>Source open drain output</p> <p>Initial "Hi-Z"</p>
R4	I/O				<p>Sink open drain output</p> <p>Initial "Hi-Z"</p> <p>$R = 1K\Omega$ (typ.)</p> <p>Analog input</p> <p>$R_A = 5K\Omega$ (typ.)</p> <p>$C_A = 12pF$ (typ.)</p>
R7	I/O				<p>Sink open drain output</p> <p>Initial "Hi-Z"</p> <p>$R = 1K\Omega$ (typ.)</p>
R8 R9	I/O				<p>Sink open drain output</p> <p>Initial "Hi-Z"</p> <p>Hysteresis input</p> <p>$R = 1K\Omega$ (typ.)</p>

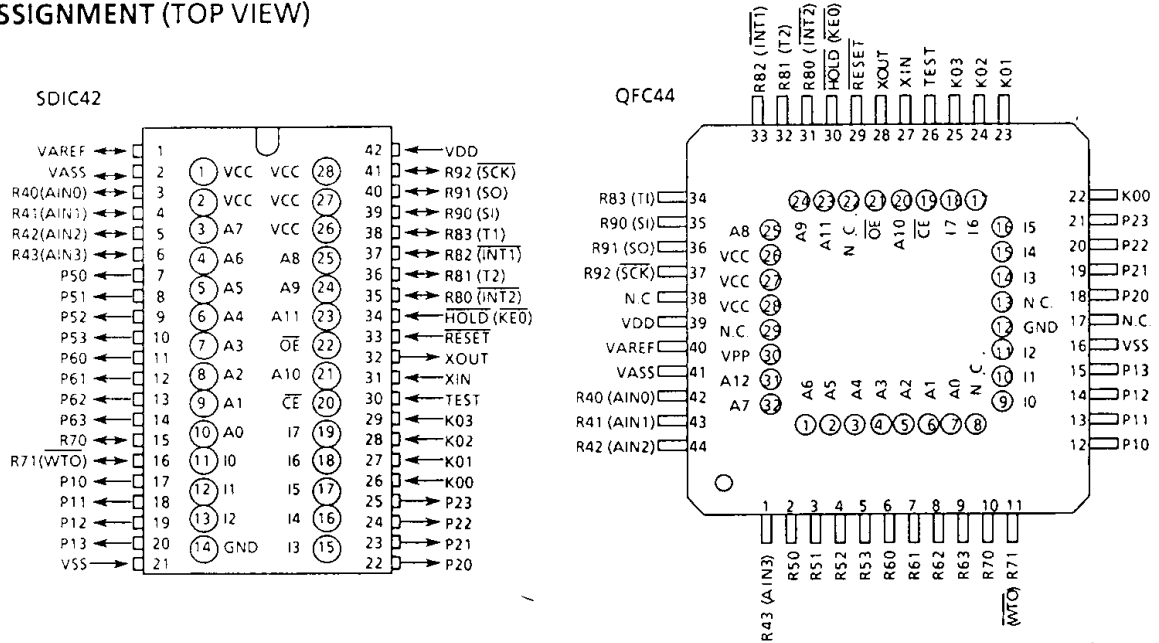
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CMOS 4-BIT MICROCONTROLLER

TMP47C941AE
TMP47C941AG

The 47C941A, which is equipped with an EPROM as program memory, is a piggyback type evaluator chip used for development and operational confirmation of the 47C441A application systems (programs). The 47C941A is pin compatible with the 47C441A which are mask-programmed ROM devices.

PIN ASSIGNMENT (TOP VIEW)



PIN FUNCTION (Top of the package)

PIN NAME	Input / Output	FUNCTIONS
A11 ~ A0	Output	Program memory address output
I7 ~ I0	Input	Program memory data input
\overline{CE}	Output	Chip enable signal output
\overline{OE}		Output enable signal output
VCC	Power supply	+ 5V (connected with VDD)
GND		0V (connected with VSS)

A.C. CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Address Delay Time	t_{AD}	$V_{SS} = 0V, V_{DD} = 4.5 \text{ to } 6.0V$ $C_L = 100pF$ $T_{opr} = -30 \text{ to } 70^\circ C$	-	-	150	ns
Data Setup Time	t_{IS}		150	-	-	ns
Data Hold Time	t_{IH}		50	-	-	ns

NOTES FOR USE

(1) Program memory

The program area are as shown in Figure1.

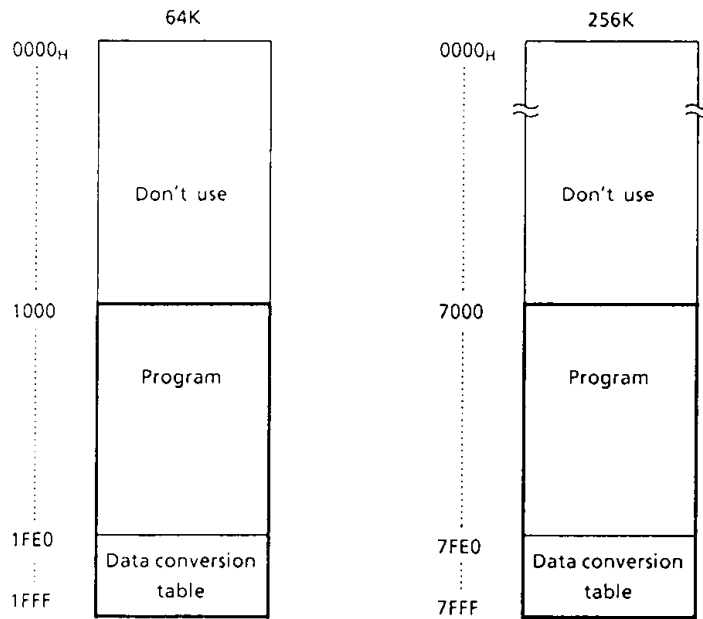


Figure 1. Program area

(2) I/O ports

Input/Output circuitries of I/O ports in the 47C941A are similar to the code TA of the 47C441A. When this chip is used as evaluator with other I/O code, it is necessary to provide the external resistors.

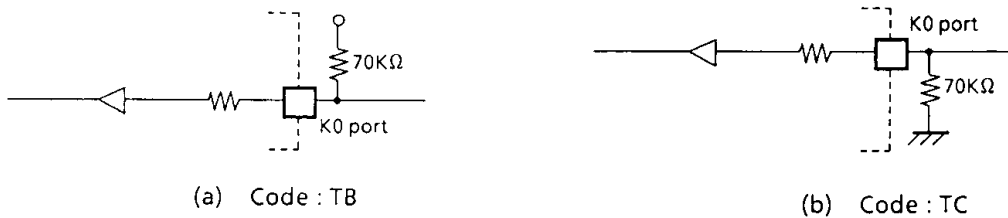


Figure 2. I/O code and external circuitry