

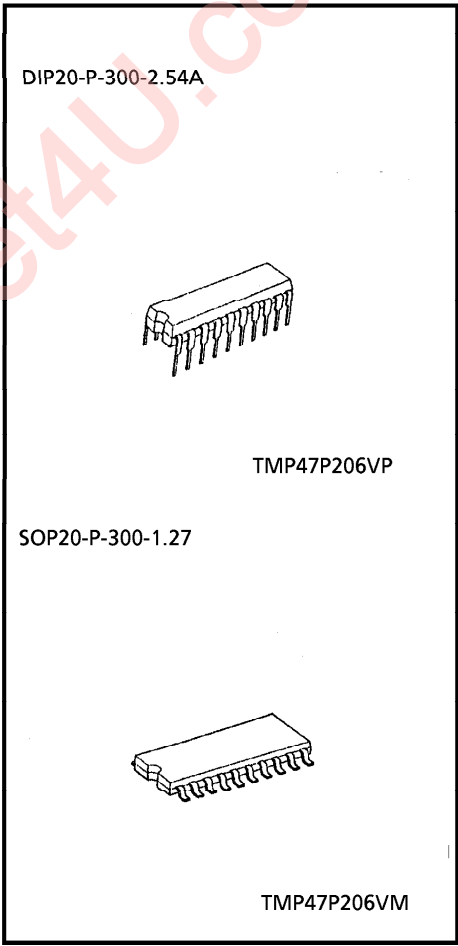
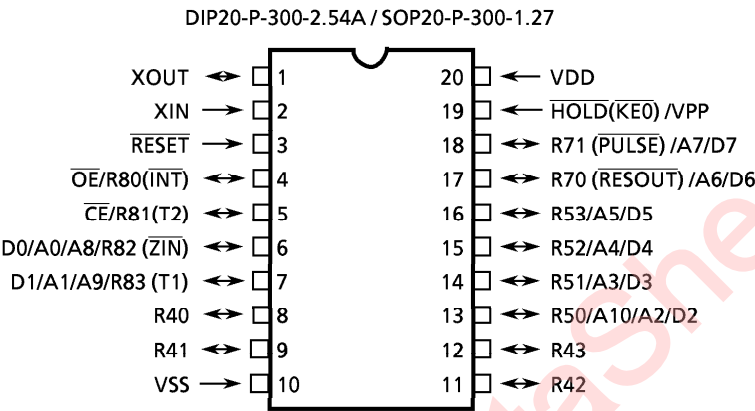
CMOS 4-BIT MICROCONTROLLER

TMP47P206VM/P

The 47P206V is the OTP microcontroller with 16K bits PROM. For program operation, the programming is achieved by using with EPROM programmer (TC57256AD type) and adapter socket. The function of this device is exactly same as the 47C206.

PART No.	ROM	RAM	PACKAGE	ADAPTER SOCKET
TMP47P206VP	OTP	128 × 4-bit	DIP20-P-300-2.54A	BM11125
TMP47P206VM	2048 × 8-bit		SOP20-P-300-1.27	BM11126

PIN ASSIGNMENT (TOP VIEW)



PIN FUNCTION

The 47P206V has MCU mode and PROM mode.

(1) MCU mode

The 47C206 and the 47P206V are pin compatible.

(2) PROM mode

PIN NAME	INPUT / OUTPUT	FUNCTIONS	PIN NAME (MCU mode)
D0 / A0 / A8	I/O	Data inputs / outputs or Address inputs	R82
D1 / A1 / A9			R83
D2 / A2 / A10			R50
D3 / A3			R51
D4 / A4			R52
D5 / A5			R53
D6 / A6			R70
D7 / A7			R71
$\overline{OE}$	Input	Output Enable input	R80
$\overline{CE}$		Chip Enable input	R81
VPP	Power supply	+ 12.5 V / 5 V (Program supply voltage)	$\overline{HOLD}$
VCC		+ 5 V	VDD
VSS		0 V	VSS
R43 to R40	I/O	Be fixed to low level.	
$\overline{RESET}$	Input	Be fixed to non connection.	
XIN	Input	Input the clock from the external oscillator.	
XOUT	Input	PROM control input	

OPERATIONAL DESCRIPTION

The following is an explanation of hardware configuration and operation in relation to the 47P206V. The 47P206V is the same as the 47C206 except that an OTP is used instead of a built-in mask ROM.

1. OPERATION mode

The 47P206V has a MCU mode and a PROM mode.

1.1 MCU mode

The MCU mode is set by attaching a resonator between the XIN and XOUT pins. Operation in the MCU mode is the same as for the 47C206. In the 47P206V, RC oscillation is impossible.

1.1.1 Program Memory

The program storage area is the same as for the 47C206.

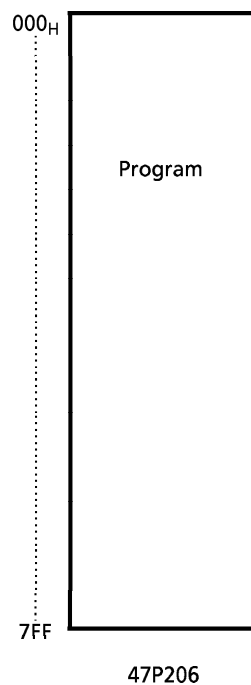


Figure 1-1. Program Area

1.1.2 Data Memory

The 47P206 has 128 × 4-bit of data memory (RAM).

1.1.3 Input / Output Circuitry

(1) Control pins

This is the same as I/O code FB of the 47C206. In the 47P206V, RC oscillator is impossible. Connecting the resonator is required when using as evaluator of I/O code FE.

(2) I/O Ports

The input / output circuit of the 47P206V is the same as the 47C206.

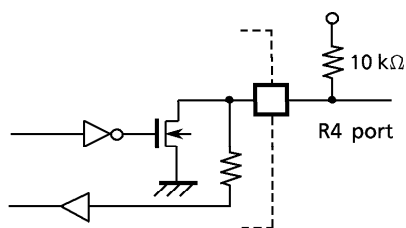
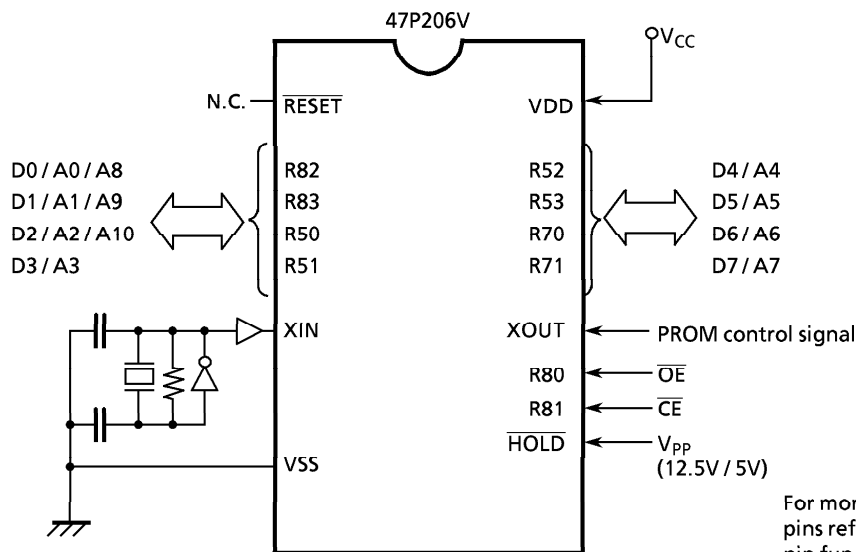


Figure 1-2. I/O code and external circuitry

1.2 PROM mode

The 47P206V enters PROM mode by sending external clock signal from XIN pin when XOUT pin is at low level. In PROM mode, programs can be written or verified using a general-purpose PROM writer with an adapter socket being attached.

With the 47P206V, the PROM address input and data input/output use the same port. PROM mode control signal (XOUT) is used for switching between two functions. XOUT pin becomes control signal input after PROM mode is completed.



For more information on pins refer to the section on pin function.

Figure 1-3. Setting for PROM mode

1.2.1 Program Writing

When writing a program, set a ROM type to "TC57256AD" (programming voltage : 12.5 V) . Since the 47P206V has a 2048 × 8-bit internal PROM (000 to 7FF_H) , set a stop address of a PROM writer to "7FF_H". Please use a general-purpose PROM writer which does not have an electric signature mode or can release from it.

1.2.2 High Speed Programming Mode

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+ 12.5 V) is applied to the V_{PP} terminal with $V_{CC} = 6\text{ V}$ and $\overline{CE} = V_{IH}$.

The programming is achieved by applying a single low level 1ms pulse the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC} = V_{PP} = 5\text{ V}$.

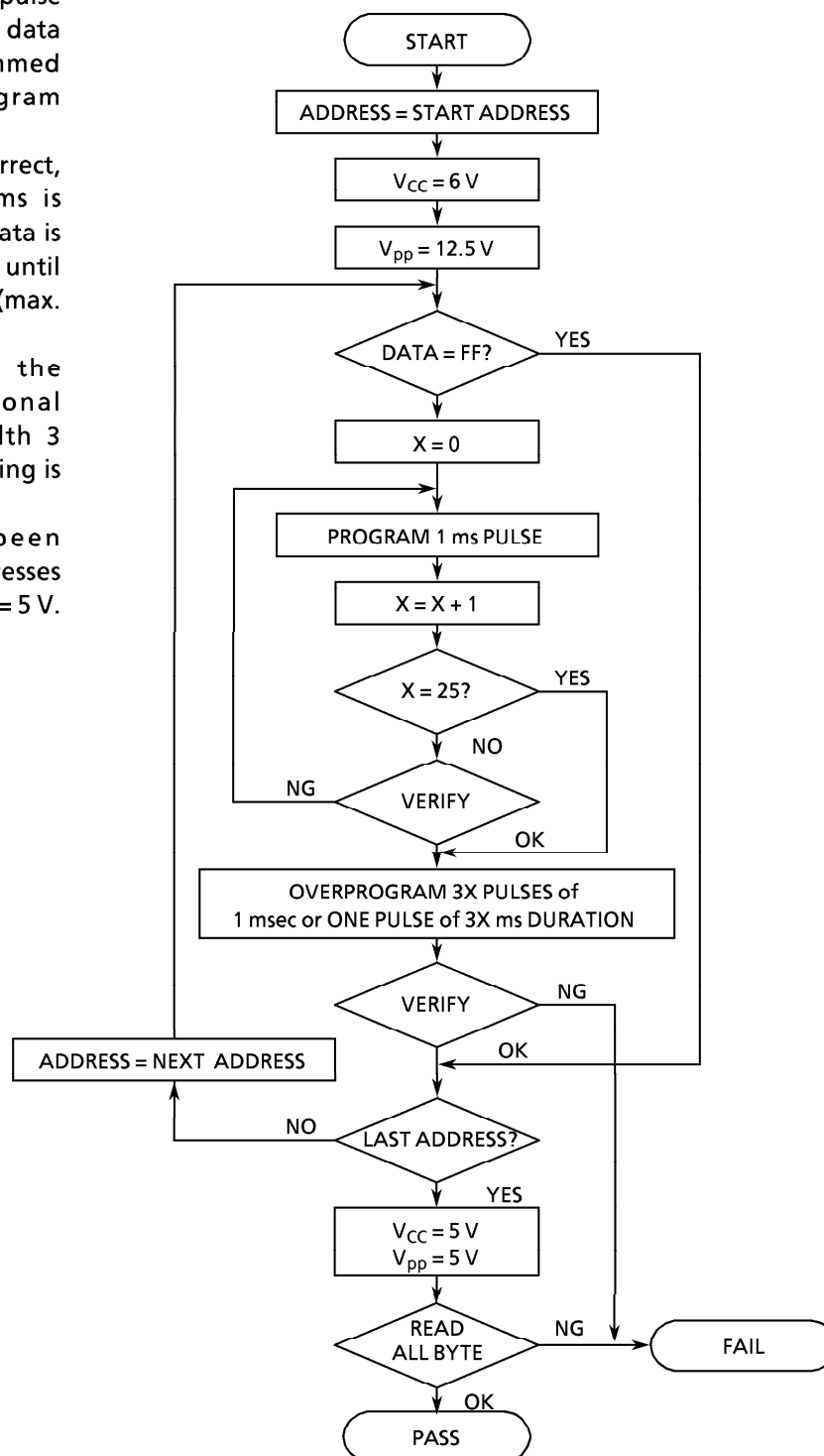


Figure 1-4. Flow Chart

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0 V)

PARAMETER	SYMBOL	PINS	RATINGS	UNIT
Supply Voltage	V _{DD}		– 0.3 to 6.5	V
Program Voltage	V _{PP}	$\overline{\text{HOLD}} / V_{PP}$	– 0.3 to 13.0	V
Input Voltage	V _{IN}		– 0.3 to V _{DD} + 0.3	V
Output Voltage	V _{OUT}		– 0.3 to V _{DD} + 0.3	V
Output Current (Per 1 pin)	I _{OUT1}	Port R4, R50	30	mA
	I _{OUT2}	Port R51 to 53, R8, R70, R71	3.2	mA
Output Current (Total)	ΣI_{OUT1}	Port R4, R50	100	mA
	ΣI_{OUT2}	Port R51 to 53, R8, R70, R71	28.8	
Power Dissipation [T _{opr} = 85 °C]	PD	SOP	150	mW
		DIP	250	
Soldering Temperature (time)	T _{sld}		260 (10 s)	°C
Storage Temperature	T _{stg}		– 55 to 125	°C
Operating Temperature	T _{opr}		– 40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0 V, T_{opr} = – 40 to 85 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V _{DD}	Normal mode	Crystar or ceramic	f _c = 8 MHz	4.0 (2.7) *	V
				f _c = 4.2 MHz	4.0 (2.2) *	
			RC	f _c = 2.5 MHz	4.0 (2.2) *	
		HOLD mode	–	–	4.0 (2.0) *	
Input High Voltage	V _{IH1}	Except Hysteresis Input	In the normal operating area	V _{DD} × 0.7	V _{DD}	V
	V _{IH2}	Hysteresis Input		V _{DD} × 0.75		
	V _{IH3}		In the HOLD mode	V _{DD} × 0.9		
Input Low Voltage	V _{IL1}	Except Hysteresis Input	In the normal operating area	0	V _{DD} × 0.3	V
	V _{IL2}	Hysteresis Input			V _{DD} × 0.25	
	V _{IL3}		In the HOLD mode		V _{DD} × 0.1	
Clock Frequency	f _c	XIN, XOUT	V _{DD} = 2.7 to 5.7 V	1	8	MHz
			V _{DD} = 2.2 to 5.7 V		4.2	
			V _{DD} = 2.2 to 5.7 V (RC)		2.5	

* Note : LVD is initially enable and initial Min. V_{DD} is 4.0 V. After LVD is disabled above 4.0 V. Min. V_{DD} will be 2.7 or 2.2 or 2.0 V.

D.C. CHARACTERISTICS

(V_{SS} = 0 V, T_{opr} = -40 to 85 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V _{HS}	Hysteresis Input		–	0.7	–	V
Input Current	I _{IN1} *1	RESET, HOLD	V _{DD} = 5.7 V, V _{IN} = 5.7 V / 0 V	–	–	± 2	μA
	I _{IN2}	Open drain output ports					
Input Resistance	R _{IN}	RESET		100	220	450	kΩ
Pull down Resistance	R _{PD}	R82		22	70	160	
Input Low Current	I _{IL}	Push-pull output ports	V _{DD} = 5.7 V, V _{IN} = 0.4 V	–	–	– 2	mA
Output Leakage Current	I _{LO}	Open drain output ports	V _{DD} = 5.7 V, V _{OUT} = 5.7 V	–	–	2	μA
Output High Voltage	V _{OH}	Push-pull output ports	V _{DD} = 5 V, I _{OH} = – 100 μA	4.8	–	–	V
			V _{DD} = 4.5 V, I _{OH} = – 200 μA	2.4	–	–	
			V _{DD} = 2.2 V, I _{OH} = – 5 μA	2.0	–	–	
Output Low Voltage	V _{OL1}	Port R8, R7, R51 to 53	V _{DD} = 4.5 V, I _{OL} = 3.3 mA	–	–	1.0	V
			V _{DD} = 4.5 V, I _{OL} = 1.6 mA	–	–	0.4	
			V _{DD} = 2.2 V, I _{OL} = 20 μA	–	–	0.1	
	V _{OL2}	Port R4, R50	V _{DD} = 4.5 V, I _{OL} = 15 mA	–	–	1.0	
			V _{DD} = 4.5 V, I _{OL} = 7 mA	–	–	0.4	
			V _{DD} = 2.2 V, I _{OL} = 50 μA	–	–	0.1	
Output Low Current	I _{OL1}	Port R8, R7, R51 to 53	V _{DD} = 4.5 V, V _{OL} = 1.0 V	3.3	14	–	mA
			V _{DD} = 4.5 V, V _{OL} = 0.4 V	1.6	7	–	
	I _{OL2}	Port R4, R50	V _{DD} = 4.5 V, V _{OL} = 1.0 V	15	34	–	
			V _{DD} = 4.5 V, V _{OL} = 0.4 V	7	17	–	
Supply Current (in the Normal operating mode) *2	I _{DD}		V _{DD} = 5.7 V, f _c = 8 MHz		3	6	mA
			V _{DD} = 5.7 V, f _c = 4 MHz	–	2	4	
			V _{DD} = 3.0 V, f _c = 4 MHz	–	1	2	
			V _{DD} = 3.0 V, f _c = 1 MHz	–	0.6	1.2	
Supply Current (in the HOLD operating mode) *2	I _{DDH}	LVD always Enable	V _{DD} = 5.7 V	–	50	200	μA
		LVD On and Off	V _{DD} = 5.7 V	–	2.5	20	
Injection Current	I _{ZC}	R82		–	–	1	mA

<General Conditions>

Typ. values show those at T_{opr} = 25 °C, V_{DD} = 5 V.Note 1. Input Current I_{IN1} : The current through resistor is not included.Note 2. Supply Current : V_{IN} = 5.5 V / 0.2 V (V_{DD} = 5.7 V) or 2.8 V / 0.2 V (V_{DD} = 3.0 V)

A.C. CHARACTERISTICS

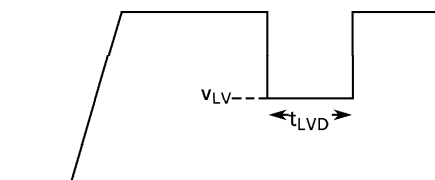
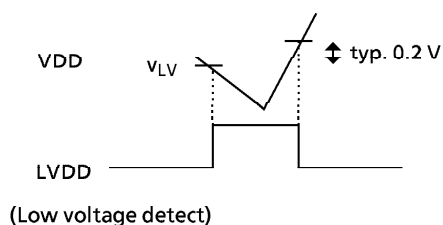
(V_{SS} = 0 V, T_{opr} = – 40 to 85 °C)

PARAMETER	SYMBOL	CONDITIONS		Min.	Typ.	Max.	UNIT
Instruction Cycle Time	tcy		V _{DD} = 2.7 to 5.7 V	1.0	–	8	μs
			V _{DD} = 2.2 to 5.7 V	1.9			
High level Clock pulse Width	t _{WCH}	For external clock operation	V _{DD} ≥ 2.7 V	60	–	–	ns
			V _{DD} < 2.7 V	120			
Low level Clock pulse Width	t _{WCL}		V _{DD} ≥ 2.7 V	60			
			V _{DD} < 2.7 V	120			
Delay Reset Output Signal	t _{rd}	fc = 1 MHz		–	–	16	μs

LOW VOLTAGE DETECTOR CHARACTERISTICS

(V_{SS} = 0 V, T_{opr} = – 40 to 85 °C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
LVD interval time *1	t _{int}		8.5		128	ms
LVD Enable time *1	t _{en}		100			μs
LVD pulse width *1 *2	t _{LVD}		50			μs
Detection Voltage *3	V _{LV}	LVDDTY = 0 LVDD = 0	2.7	3.3	3.8	V
		LVDDTY = 1 LVDD = 0	2.2	2.7	3.3	
LVD Operating Voltage *1	V _{LVD}		2.0			V

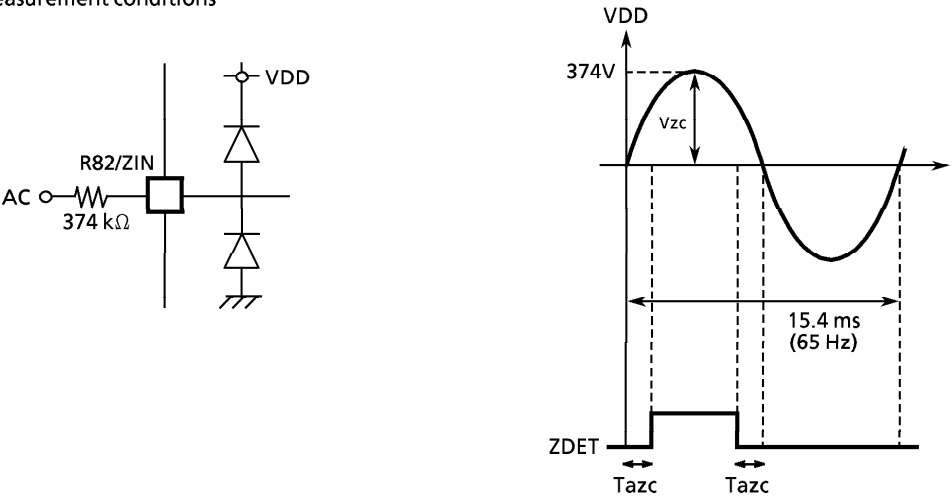
*Note 1 : These parameters are characterized but not tested.**Note 2 : Less than Min. t_{LVD}, CPU will not be reset.**Note 3 : Detection voltage has typ. 0.2V hysteresis.*

ZERO-CROSS DETECTION CHARACTERISTICS

(V_{SS} = 0 V, T_{opr} = - 40 to 85 °C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Zero-cross Accuracy	T _{azc}	f _{zc} = 45 to 65 Hz (*)			90	μs
Injection Current	I _{zc}				1	mA
Pull-down resistance	R _{PD}		22	70	160	kΩ

(*) Measurement conditions



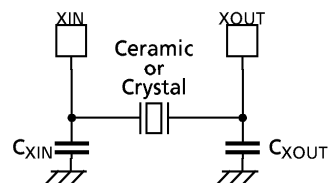
RECOMMENDED OSCILLATING CONDITIONS

 $(V_{SS} = 0\text{ V}, V_{DD} = 2.2\text{ to }5.7\text{ V}, T_{opr} = -40\text{ to }85\text{ }^{\circ}\text{C})$

Recommended oscillating conditions of the 47P206V are equal to the 47C206's but RC oscillation is impossible.

(1) 8MHz

Ceramic Resonator

CSA8.00MGU (MURATA) $C_{XIN} = C_{XOUT} = 30\text{ pF}$ KBR-8.00MS (KYOCERA) $C_{XIN} = C_{XOUT} = 30\text{ pF}$ EFOEC8004A4 (NATIONAL) $C_{XIN} = C_{XOUT} = 30\text{ pF}$ 

(2) 6MHz

Ceramic Resonator

CSA6.00MGU (MURATA) $C_{XIN} = C_{XOUT} = 30\text{ pF}$ KBR-6.00MS (KYOCERA) $C_{XIN} = C_{XOUT} = 30\text{ pF}$ EFOEC6004A4 (NATIONAL) $C_{XIN} = C_{XOUT} = 30\text{ pF}$

(3) 4MHz

Ceramic Resonator

CSA4.00MGU (MURATA) $C_{XIN} = C_{XOUT} = 30\text{ pF}$ KBR-4.00MS (KYOCERA) $C_{XIN} = C_{XOUT} = 30\text{ pF}$ EFOEC4004A4 (NATIONAL) $C_{XIN} = C_{XOUT} = 30\text{ pF}$

Crystal Oscillator

204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT} = 20\text{ pF}$

(4) 1MHz

Ceramic Resonator

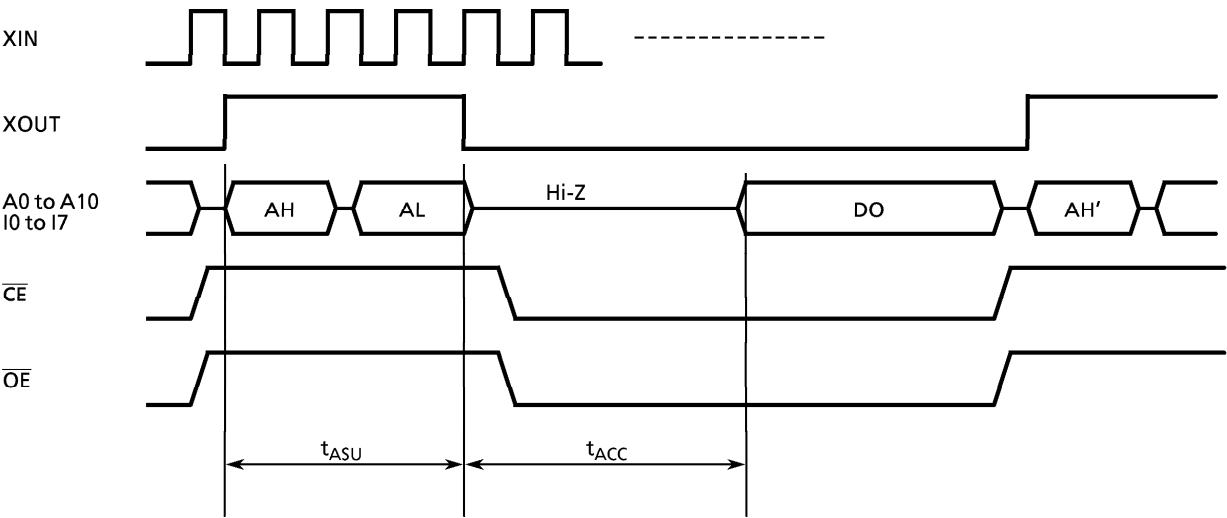
CSA1.00MGU (MURATA) $C_{XIN} = C_{XOUT} = 30\text{ pF}$ KBR-1.00MS (KYOCERA) $C_{XIN} = C_{XOUT} = 30\text{ pF}$ EFOEC1004A4 (NATIONAL) $C_{XIN} = C_{XOUT} = 30\text{ pF}$

DC/AC CHARACTERISTICS

(V_{SS} = 0V)

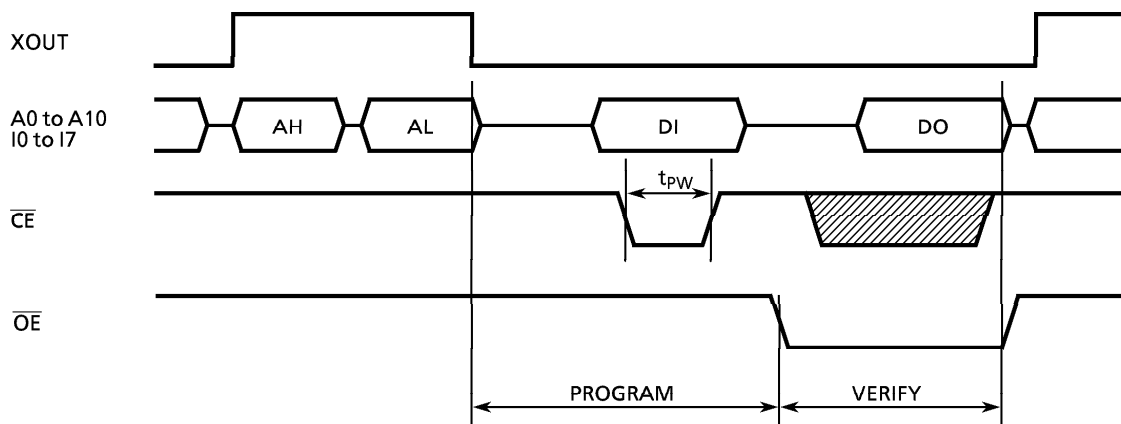
(1) Read Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Output Level High Voltage	V _{IH4}		V _{CC} × 0.7	–	V _{CC}	V
Output Level Low Voltage	V _{IL4}		0	–	V _{CC} × 0.3	V
Supply Voltage	V _{CC}		4.75	–	6.0	V
Programming Voltage	V _{PP}					
Address Set-up Time	t _{ASU}		350	–	–	ns
Address Access Time	t _{ACC}	V _{CC} = 5.0 ± 0.25 V	–	–	300	ns



(2) High Speed Programming Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.3$	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
V_{PP} Power Supply Voltage	V_{PP}		12.25	12.50	12.75	V
Programming Pulse Width	t_{PW}	$V_{CC} = 6.0 \pm 0.25$ V	0.95	1.0	1.05	ms



(Note) DO ; Data output (I0 to I7), AL ; Address input (A0 to A7)
 DI ; Data input (I0 to I7), AH ; Address input (A8 to A10)