GENERAL DESCRIPTION

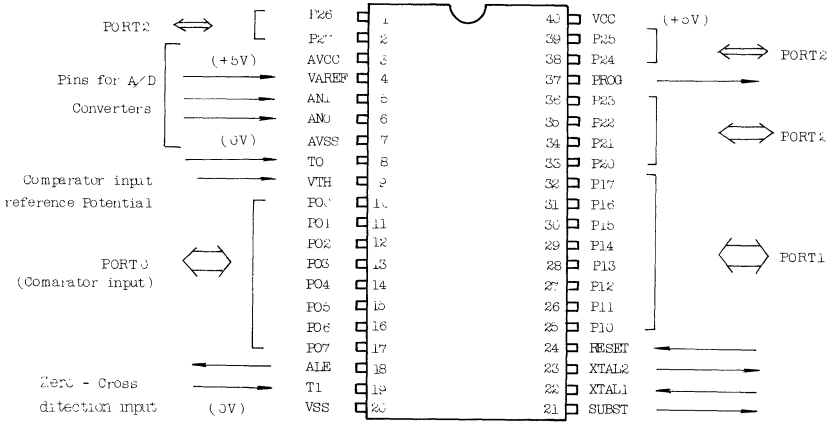
The TMP8022P is one version of the TLCS-84 family, which is an 8-bit single chip microcomputer containing A/D converter.

The CPU, data memory (RAM), program memory (ROM), I/O port, and timer, which are basic functions as a computer, and further, A/D converter, comparator input port, zero-cross ditection circuit, etc. are all integrated on single chip.

FEATURES

- Compatible with Intel's 8022
- 2K × 8 ROM, 64 × 8 RAM, 28 I/O Lines
- 8 Bit Interval Timer/Event Counter
- On-chip 8 Bit A/D Converter; Two Input Channels
- 8 Comparator Inputs (PORT0)
- Zero Cross Detection Capability
- High Current Drive Capability (V_{OL}<2.5V @I_{OL}=7mA)
- 8 Level Subroutine Nesting
- Two Interrupts - External and Timer
- Instructions - 8048 Subset
- 8.38 sec Cycles; All Instructions 1 or 2 Cycles
- Single 5V Supply (4.5V to 6.5V)

PIN CONNECTIONS (TOP VIEW)



PIN NAMES AND DESCRIPTION

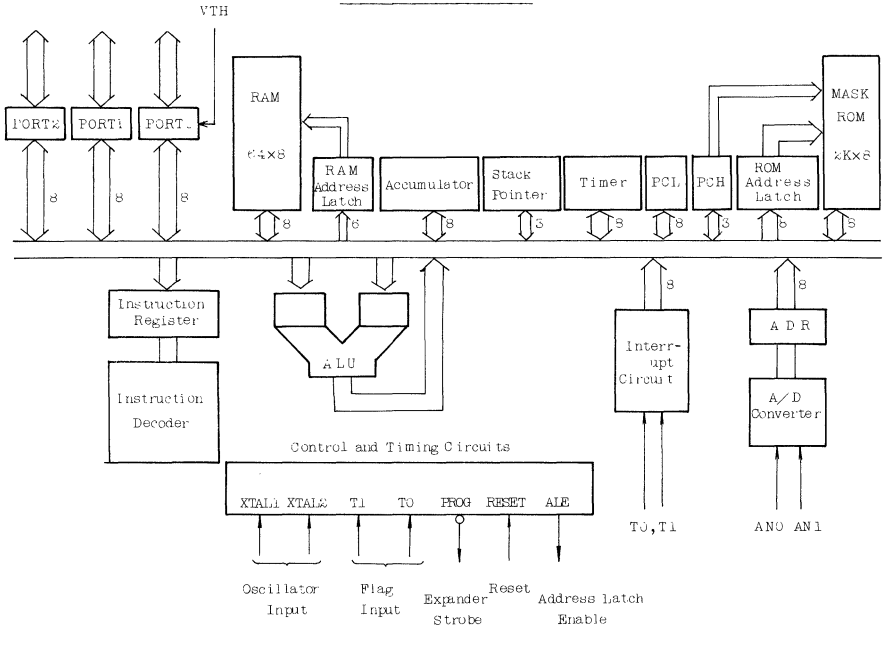
Pin Name	Pin No.	Input/ Output	Function
XTAL1 XTAL2	22 23	Input	A terminal for connecting the oscillator or an input terminal for the external clock.
RESET	24	Input	High active signal and initializes the chip. When a low level voltage is applied to this pin, a program starts from address 0.

Pin Name	Pin No.	Input/ Output	Function
T0	8	Input	Ecternal interrupt input. Since this pin is of a level interrupt type, it is required to be held at low level until an interrupt is accepted. Further, this pin serves as a test flag input for the conditional jump instructions (JT1 and JNT1).
T1	19	Input	This pin is an external clock input for the timer counter at the time of the event counter mode, and has a built-in zero-cross ditection circuit. Further, it serves as a test flag input for the conditional jump instructions (JT1 and JNT1).
ALE	18	Output	Address Latch Enable pin. This pin is a clock output that regards 1 machine cycle (clock cycle x 30) as a cycle. (It is also used for the address latch in the test mode 2.)
PROG	37	Output	Output strobe for the I/O expander 8243.
P00 ∿ P07 (PORT0)	10∿17	I/O	8-bit open drain port. Since this pin has a built-in comparator which regards the voltage applied to VTH pin as a comparison voltage, it can change the input inverse level. It contains a mask option with a pull-up resistor.

Pin Name	Pin No.	Input/ Output	Function
P10 ∿ P27 (PORT1)	25∿32	I/O	8-bit quasi-bidirectional port.
P20 ∿ P27 (PORT2)	33∿36 38,39 1,2	I/O	8-bit-bidirectional port. The lower order 4-bit pins P20 to P23 serve as lines connecting the 4-bit I/O expander 8243.
VTH	9	Input	PORT0 threshold reference pin.
AN0, AN1	6,5	Input	Analog input to A/D converter. This pin switches the channels by use of soft according to SEL AN0 and SEL AN1 instructions. (2 channels)
V_{AREF}	4	Input	The reference voltage of A/D Converter Establishes the upper limit of A/D conversion range.
AVCC	3	Power supply	+5V (For A/D converter section)
AVSS	7	"	+5V (For A/D converter section)
VCC	40	"	+5V
VSS	20	"	+0V
SUBST	21	Output	Substrate potential output pin. This pin is used for the purpose of connecting a bypass capacitor across the VSS pin for improving the accuracy of the A/D converter by stabilizing the substrate potential.

BLOCK DIAGRAM

8022 Block Diagram



DESCRIPTION OF INSTRUCTIONS

o The table of instructions for the TMP8022P is described by use of the following symbols and abbreviations.

A	:	Accumulator
AC	:	Auxiliary carry
addr	:	Lower order 8-bit address
C	:	Carry
CRR	:	A/D conversion result register
data	:	8-bit data
Pp	:	Port p=0, 1, 2 or P=4 ∿ 7
PC	:	Program counter
Rr	:	Register r=0, 1 or r=0 ∿ 7
SP	:	Stack pointer
T	:	Timer
TF	:	Timer flag
T0	:	Test 0
T1	:	Test 1
(x)	:	Contents of x
((x))	:	Contents of address indicated by x
∧	:	AND
∨	:	Logical OR
⊻	:	Exclusive OR

TMP8022 Instruction List (I)

Classification	Mnemonics	Functional description	Effected Flag C	Effected Flag AC	Bytes	Cycles	Operation Code (Hexadecimal)
Accumulator Instruction	ADD A, Rr	(A)←(A)+(Rr) r=0-7	○	○	1	1	68-6F
	ADD A, @Rr	(A)←(A)+((Rr)) r=0,1	○	○	1	1	60, 61
	ADD A, #data	(A)←(A)+data	○	○	2	2	03
	ADDC A, Rr	(A)←(A)+(Rr)+(C) r=0-7	○	○	1	1	78-7F
	ADDC A, @Rr	(A)←(A)+((Rr))+(C) r=0, 1	○	○	1	1	70-71
	ADDC A, #data	(A)←(A)+data+(C)	○	○	2	2	13
	ANL A, Rr	(A)←(A)∧(Rr) r=0-7	-	-	1	1	58-5F
	ANL A, @Rr	(A)←(A)∧((Rr)) r=0, 1	-	-	1	1	50-51
	ANL A, #data	(A)←(A)∧data	-	-	2	2	53
	ORL A, Rr	(A)←(A)∨(Rr) r=0-7	-	-	1	1	48-4F
	ORL A, @Rr	(A)←(A)∨((Rr)) r=0, 1	-	-	1	1	40-41
	ORL A, #data	(A)←(A)∨data	-	-	2	2	43
	XRL A, Rr	(A)←(A)⊻(Rr) r=0-7	-	-	1	1	D8-DF
	XRL A, @Rr	(A)←(A)⊻((Rr)) r=0, 1	-	-	1	1	D0-D1
	XRL A, #data	(A)←(A)⊻data	-	-	2	2	D3
	INC A	(A)←(A)+1	-	-	1	1	17
	DEC A	(A)←(A)-1	-	-	1	1	07
	CLR A	(A)←0	-	-	1	1	27
	CPL A	(A)←NOT(A)	-	-	1	1	37
	DA A	Decimal adjust A	○	-	1	1	57

Classification	Mnemonics	Functional Description	Effected Flag C	Effected Flag AC	Bytes	Cycles	Operation Code (Hexadecimal)
Accumulator Instruction	SWAP A	$(A_{4-7}) \rightleftarrows (A_{0-3})$	-	-	1	1	47
	RL A	$(A_{n+1}) \leftarrow (A_n), (A0) \leftarrow (A7)$ n=0-6	-	-	1	1	E7
	RLC A	$(A_{n+1}) \leftarrow (A_n), (C) \leftarrow (A7)$ n=0-6, $(A0) \leftarrow (C)$	○	-	1	1	F7
	RR A	$(A_n) \leftarrow (A_{n+1}), (A7) \leftarrow (A0)$	-	-	1	1	77
	RRC A	(A_n) $(A_{n+1}), (C) \leftarrow (A0)$ n=0-6 $(A7) \leftarrow (C)$	○	-	1	1	67
I/O Instruction	IN A,Pp	$(A) \leftarrow (Pp)$ p=0,1,2	-	-	1	2	08, 09, 0A
	OUTL Pp,A	$(Pp) \leftarrow (A)$ p=0,1,2	-	-	1	2	90, 39, 3A
	MOVD A, Pp	$(A_{0-3}) \leftarrow (Pp)$ p=4-7 $(A4-7) \leftarrow 0$	-	-	1	2	0C-0F
	MOVD Pp,A	$(Pp) \leftarrow (A_{0-3})$ p=4-7	-	-	1	2	3C-3F
	ANLD Pp,A	$(Pp) \leftarrow (Pp) \wedge (A_{0-3})$ p=4-7	-	-	1	2	9C-9F
	ORLD Pp,A	$(Pp) \leftarrow (Pp) \vee (A_{0-3})$ p=4-7	-	-	1	2	8C-8F
Register Instruction	INC Rr	$(Rr) \leftarrow (Rr)+1$ r=0-7	-	-	1	1	18-1F
	INC @Rr	$((Rr)) \leftarrow ((Rr))+1$ r=0,1	-	-	1	1	10-11
Branch Instruction	JMP addr	$(PC_{0-7}) \leftarrow$ Upper 3-bit of Operation code	-	-	2	2	04,24,44,64 84,A4,C4,E4
	JMPP @A	$(PC_{0-7}) \leftarrow ((A))$	-	-	1	2	B3
	DJNZ Rr,addr	$(Rr) \leftarrow (Rr)-1$, If $(r) \neq 0$ $(PC_{0-7}) \leftarrow$ addr	-	-	2	2	E8-EF
	JC addr	IF (C)=1, $(PC_{0-7}) \leftarrow$ addr	-	-	2	2	F6

Classification	Mnemonics	Functional Description	Effected Flag C	Effected Flag AC	Bytes	Cycles	Operation Code (Hexadecimal)
Branch Instruction	JNC addr	If (C)=0, (PC_{0-7})←addr	-	-	2	2	E6
	JZ addr	If (A)=0, (PC_{0-7})←addr	-	-	2	2	C6
	JNZ addr	If (A)≠0, (PC_{0-7})←addr	-	-	2	2	96
	JT0 addr	If T0=1, (PC_{0-7}) ← addr	-	-	2	2	36
	JNT0 addr	If T0=0, (PC_{0-7}) ← addr	-	-	2	2	26
	JT1 addr	If T1=1, (PC_{0-7}) ← addr	-	-	2	2	56
	JNT1 addr	If T1=0, (PC_{0-7}) ← addr	-	-	2	2	46
	JTF addr	If TF=1, (PC_{0-7}) ← addr	-	-	2	2	16
Subroutine Instruction	CALL addr	((SP))←(PC),(SP)←(SP)+1 (PC_{0-7})←addr (PC_{8-10})←Upper 3-bit of operation code	-	-	1	2	14,34,54,74 94,B4,D4,F4
	RET	(SP) ← (SP)-1 (PC) ← ((SP))	-	-	1	2	83
Flags Instruction	CLR C	(C)←0	○	-	1	1	97
	CPL C	(C)←NOT(C)	○	-	1	1	A7
Data Moves Instruction	MOV A,Rr	(A) ← (Rr) r=0-7	-	-	1	1	F8-FF
	MOV A,@Rr	(A) ← ((Rr)) r=0,1	-	-	1	1	F0-F1
	MOV A,#data	(A) ← data	-	-	2	2	23
	MOV Rr,A	(Rr) ← (A) r=0-7	-	-	1	1	A8-AF
	MOV @Rr,A	((Rr)) ← (A) r=0,1	-	-	1	1	A0-A1
	MOV Rr,#data	(Rr) ← data r=0-7	-	-	2	2	B8-BF
	MOV @Rr,#data	((Rr)) ← data r=0,1	-	-	2	2	B0-B1

Classification	Mnemonics		Functional Description	Effected Flag C	Effected Flag AC	Bytes	Cycles	Operation Code (Hexadecimal)
Data Moves Instruction	XCH	A,Rr	(A) ↔ (Rr) r=0-7	-	-	1	1	28-2F
	XCH	A,@Rr	(A) ↔ ((Rr)) r=0,1	-	-	1	1	20-21
	XCHD	a,@Rr	(A_{0-3}) ↔ ((Rr)) r=0,1	-	-	1	1	30-31
	MOVP	A,@A	(PC_{0-7})←(A) [Note] (A) ← ((PC))	-	-	1	2	A3
Timer/Counter Instruction	MOV	A,T	(A) ← (T)	-	-	1	1	42
	MOV	T,A	(T) ← (A)	-	-	1	1	62
	STRT	T	Start timer	-	-	1	1	55
	STRT	CNT	Start counter	-	-	1	1	45
	STOP	TCNT	Stop timer/counter	-	-	1	1	65
A/D Converter Instruction	RAD		(A) ← (CRR)	-	-	1	2	80
	SEL	AN0	AN0 Selection, Conversion restart	-	-	1	1	85
	SNL	AN1	AN1 " "	-	-	1	1	95
Interrupts Instruction	EI	1	Enable external interrupt	-	-	1	1	05
	DIS	1	Disable external interrupt	-	-	1	1	15
	EN	TCNT1	Enable timer/counter interrupt	-	-	1	1	25
	DIS	TCNT1	Disable timer/counter interrupt	-	-	1	1	35
	RETI		(SP) ← (SP) - 1 (PC) ← ((SP))	-	-	1	2	93
	NOP		No Operation	-	-	1	1	00

Note) MOVP A, @A loads the contents of address indicated by accumulator A in the page, into accumulatorA. After the execution, the contents of PC indicate the next address.

TMP8022P Instruction List (I)

IR0-3 / IR4-7	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP			ADD A,#	JMP	EN I		DEC A	IN A.P0	IN A,P1	IN A,P2		MOVD A,P4	MOVD A,P5	MOVD A,P6	MOVD A,P7
1	INC @R0	INC @R1		ADDC A,#	CALL	DISI	JTF	INC A	INC R0	INC R1	INC R2	INC R3	INC R4	INC R5	INC R6	INC R7
2	XCH A,@R0	XCH A,@R1		MOV A,#	JMP	EN TCNTI	JNTO	CLR A	XCH A,R0	XCH A,R1	XCH A,R2	XCH A,R3	XCH A,R4	XCH A,R5	XCH A,R6	XCH A,R7
3	XCHD A,@R0	XCHD A,@R1			CALL	DIS TCNTI	JTO	CPL A		OUTL P1,A	OUTL P2,A		MOVD P4,A	MOVD P5,A	MOVD P6,A	MOVD P7,A
4	ORL A,@R0	ORL A,@R1	MOV A,T	ORL A,#	JMP	STRT CNT	JNT1	SWAP A	ORL A,R0	ORL A,R1	ORL A,R2	ORL A,R3	ORL A,R4	ORL A,R5	ORL A,R6	ORL A,R7
5	ANL A,@R0	ANL A,@R1		ANL A,#	CALL	STRT T	JT1	DA A	ANL A,R0	ANL A,R1	ANL A,R2	ANL A,R3	ANL A,R4	ANL A,R5	ANL A,R6	ANL A,R7
6	ADD A,@R0	ADD A,@R1	MOV T,A		JMP	STOP TCNT		RRC A	ADD A,R0	ADD A,R1	ADD A,R2	ADD A,R3	ADD A,R4	ADD A,R5	ADD A,R6	ADD A,R7
7	ADDC A,@R0	ADDC A,@R1			CALL			RR A	ADDC A,R0	ADDC A,R1	ADDC A,R2	ADDC A,R3	ADDC A,R4	ADDC A,R5	ADDC A,R6	ADDC A,R7
8	RAD			RET	JMP	SEL AN0							ORLD P4,A	ORLD P5,A	ORLD P6,A	ORLD P7,A
9	OUTL P0,A			RETI	CALL	SEL AN1	JNZ	CLR C					ANLD P4,A	ANLD P5,A	ANLD P5,A	ANLD P7,A
A	MOV @R0,A	MOV @R1,A		MOVP A,@A	JMP			CPL C	MOV R0,A	MOV R1,A	MOV R2,A	MOV R3,A	MOV R4,A	MOV R5,A	MOV R6,A	MOV R7,A
B	MOV @R0,#	MOV @R1,#		JMPP @A	CALL				MOV R0,#	MOV R1,#	MOV R2,#	MOV R3,#	MOV R4,#	MOV R5,#	MOV R6,#	MOV R7,#
C					JMP		JZ									
D	XRL A,@R0	XRL A,@R1		XRL A,#	CALL				XRL A,R0	XRL A,R1	XRL A,R2	XRL A,R3	XRL A,R4	XRL A,R5	XRL A,R6	XRL A,R7
E					JMP		JNC	RL A	DJNZ R0,#	DJNZ R1,#	DJNZ R2,#	DJNZ R3,#	DJNZ R4,#	DJNZ R5,#	DJNZ R6,#	DJNZ R7,#
F	MOV A,@R0	MOV A,@R1			CALL		JC	RLC A	MOV A,R0	MOV A,R1	MOV A,R2	MOV A,R3	MOZ A,R4	MOV A,R5	MOV A,R6	MOV A,R7

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
VCC	Supply Voltage	-0.5 ∿ +7	V
VINA	Input Voltage(Except PRESET,PROG,T1)	-0.5 ∿ +7	V
VINB	Input Voltage (Only PRESET,PROG,T1)	-0.5 ∿ +13	V
P_D	Power Dissipation	1.0	W
T_{opr}	Operating Temperature	0 ∿ 70	°C
T_{stg}	Storage Temperature	-55 ∿ 150	°C

DC CHARACTERISTICS T_{opr} = °C ∿ 70°C, VCC = 5.5V ± 1V, V_{SS} = 0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage	VTH Open	-0.5		0.8	V
VIL	Input Low Voltage (PORT0)		-0.5		VTH -0.1	V
VIH	Input High Voltage (All Except XTAL, RESET)	VCC=5.0V±10% VTH Open	2.0		VCC	V
VIH1	Input High Voltage (All Except XTAL, RESET)	VCC=5.5V±1V VTH Open	3.0		VCC	V
VIH2	Input High Voltage (PORT0)		VTH +0.1		VCC	V
VIH3	Input High Voltage (PRESET,XTALI)		3.0		VCC	V
VTH	PORT0 Threshold Comparison Voltage		0		0.4 VCC	V
VOL	Output Low Voltage	IOL = 1.6mA			0.45	V
VOL1	Output Low Voltage (P10, P11)	IOL = 7 mA			2.5	V
VOH	Output High Voltage (All unless Open Drain Option-Port 0)	IOH = -50μA	2.4			V
IL1	Input Current (T_1)	VSS=0.45V≤VIN≤VCC			±200	μA
IL0	Output Leak Current (Open Drain Option-Port 0)	VSS=0.45V≤VIN≤VCC			±10	μA
ICC	V_{CC} Supply Current		50		100	mA

AC CHARACTERISTICS 1 Ta = 0°C ∿ 70°C V_{CC} = 5.5V ± 1V, V_{SS} = 0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
t_{CY}	Cycle Time	At 3MHz XTAL 10µs	8.38	50.0	µs
V_{ZX}	Zero-cross Detection Input (T1)		1	3	VACpp
A_{ZX}	Zero-cross Acuracy	60Hz Sinewave		±135	mV
F_{ZX}	Zero-cross Detection Input Frequency		0.05	1	KHz

AC CHARACTERISTICS 2 Ta = 0° ∿ 70°C V_{CC} = 5.5V ± 1V, V_{SS} = 0V

SYMBOL		PARAMETER	CONDITION	MIN.	MAX.	UNIT
t_{CP}	Expander Operation	Port Control Setup Before Falling Edge of Prog		0.5		µs
t_{PC}		Port Control Hold After Falling Edge of Prog		0.8		µs
t_{PR}		Prog to Time P2 Input must be Valid			1.0	µs
t_{DP}		Output Data Setup Time		7.0		µs
t_{PD}		Output Data Hold Time		8.3		µs
t_{PF}		Input Data Hold Time		0	150	µs
t_{PP}		PROG Pulse Width		8.3		µs
t_{PRL}	Normal Operation	ALE to Time P2 Input must be Valid			3.6	µs
t_{PL}		Output Data Setup Time		0.8		µs
t_{LP}		Output Data Hold Time		1.6		µs
t_{PFL}		Input Data Hold Time		0		µs
t_{LL}		ALE Pulse Width	Max. at t_{CY}=8.38µs	3.9	23.0	µs

Test Condition t_{CY} = 8.38 µs C_L = 80 pF

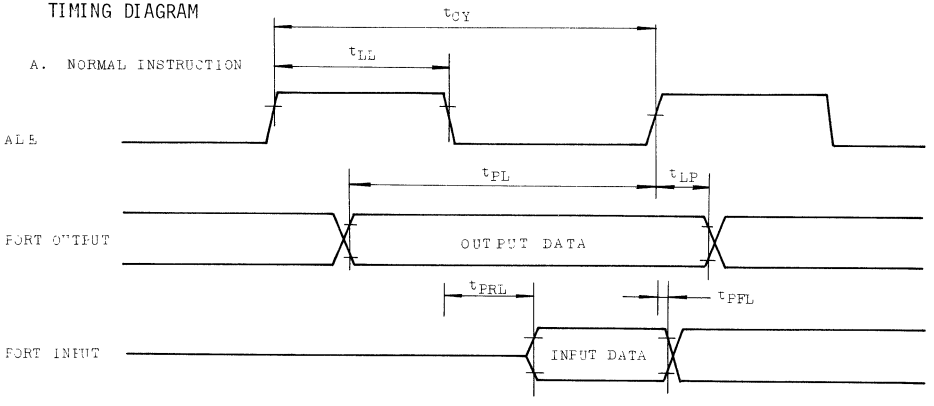
A/D CONVERTER CHARACTERISTICS Ta=0°C 70°C, V_{CC}=5.5V±1V, V_{SS}=0V, AV_{CC}=5.5±1V, AV_{SS}=0V, $AV_{CC}/2 \leq VAREF \leq AV_{CC}$

PARAMETER	MIN.	TYP.	MAX.	UNIT	REMARK
Resolution	8			Bits	
Absolute Accuracy			.8% FST ± 1/2LSB	LSB	Note 1)
Sample Setup Before Falling Edge of ALE (t_{SS})		0.20		t_{CY}	
Sample Hold After Falling Edge of ALE (t_{SH})		0.10		t_{CY}	
Input Capacitance		1		pF	
Conversion Time	4		4	t_{CY}	

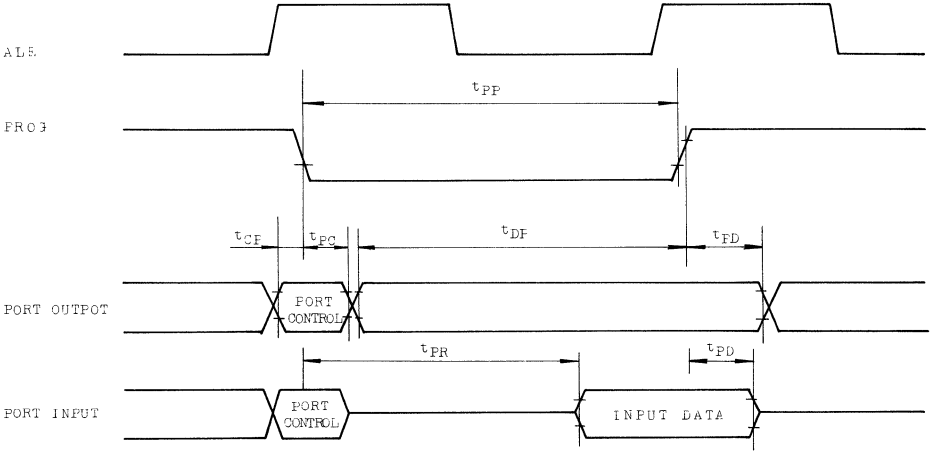
Note 1) It is required that the analog input terminal is kept at a constant voltage during the smapling time (t_{SS} + t_{SH}).

TIMING DIAGRAM

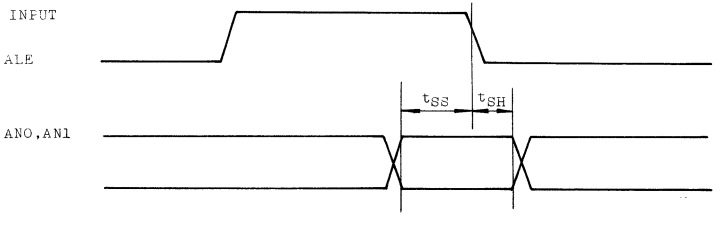
A. NORMAL INSTRUCTION



B. EXPANDER INSTRUCTION



C. ANALOG INPUT



PROGRAM DELIVERY OF TMP8022P

The program delivery of the TMP8022P is performed by using a paper tape of the following format. At the same time, it is required that mask options should be clearly designated. The format of the paper tape is the same as the Intel's type object tape (hexadecimal tape output by Intel MDS system, PROMPT 48 Development Tool, etc.)

(1) Mask Option

It is required that the presence of pull-up resistors is designated as to the 8 bits of PORT0, and the T1 terminal.

It is required that a mask option designation form attached to the ES Order Instruction Sheet is used for designation of mask option.

It is required that the mask option designation form is submitted together with the ES Order Instruction Manual within two weeks before the sumbission date of tape.

Example of mask option designation

0 : Without pull-up register 1 : With pull-up register

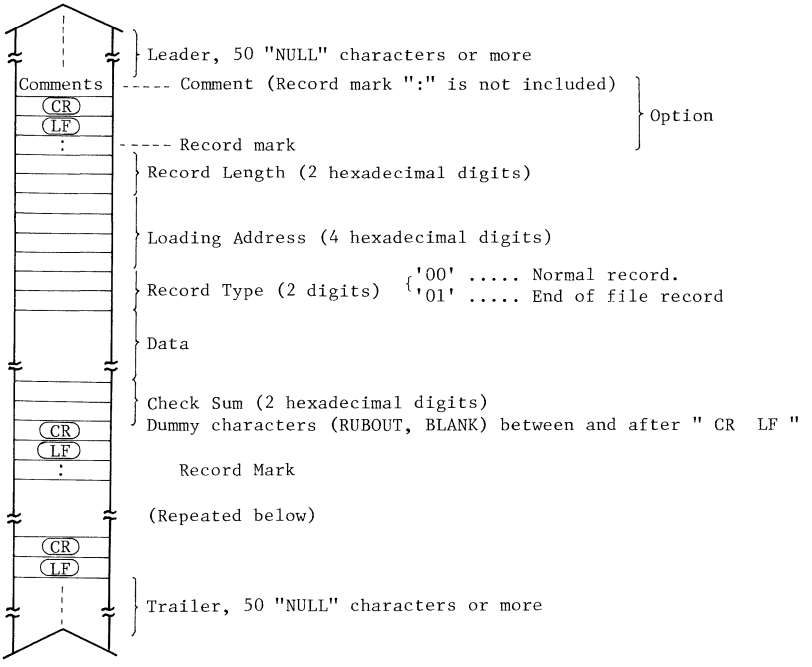
Terminal name / Option designation	PORT0								T1
	7	6	5	4	3	2	1	0	
Presence of pull-up resister	1	0	0	0	1	1	0	0	1

In this case, the presence of pull-up resistors is as follows:

Pins with pull-up resistors ..... P07, P03, P02 and T1

Pins without pull-up resistors ... P06, P05, P04, P01 and P00

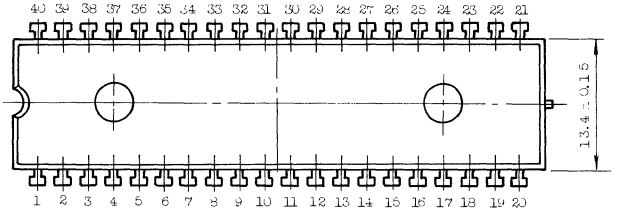
(2) Tape Format

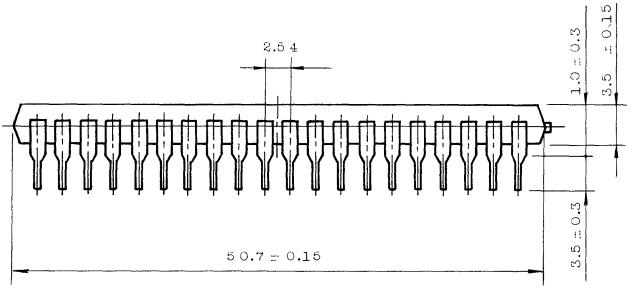


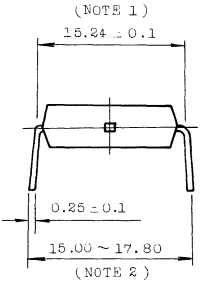
(3) Example of Tape List

```
TOSHIBA MICRO COMPUTER TLSC-84
:100000000665C7D79CF50F3F951FED55A8FF16E570
:1000100088884dde67D31F5D8ABA6DF292F113F5C1
:100020004FF1FB5DFFDAA96A99CF7DF94A346B7C09
:10003000197352F729F12F79AA9C057C5B851EED77
                          :
                          :
                          :
:1003C0005DFDB5E556A67277F61A51C631CF9F0E80
:1003D000BD2F6F20E8BB1977E3FB5AD1E41FDAA7E2
:1003E000B53D42E0EC32546025B7308CDD52063D1D
:1003F000B4BE9E9E345B6138060B20BC372BF60BD6
:00000001FF
```

UNIT : mm







Note: 1. This dimension shows the center of curvature of leads.

2. This dimension shows spread of leads.

3. The pitch of leads is 2.54 and the tolerance is ±0.25 from the theoretical center of each lead obtained No.40 lead as the reference.