PRELIMINARY

TOSHIBA MOS TYPE DIGITAL
INTEGRATED CIRCUIT
TMP80C49P-6, TMP80C39P-6
Silicon Monolithic
CMOS Silicon Gate

8-BIT SINGLE-CHIP MICROCOMPUTER

GENERAL DESCRIPTION

The TMP80C49P-6 is a single chip microcomputer fabricated in Silicon Gate CMOS technology which provides internal 8-bit parallel architecture.

The following basic architectural functions of a computer have been included in a single chip; an 8-bit CPU, 128 × 8 RAM data memory, 2K × 8 ROM program memory, 27 I/O lines and an 8-bit timer/event counter.

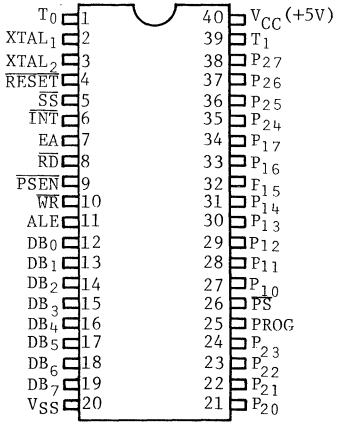
The TMP80C49P-6 is particularly efficient as a controller. It has extensive bit handling capability as well as facilities for both binary and BCD arithmetic.

The TMP80C39P-6 is the equivalent of a TMP80C49P-6 without ROM program memory on chip. By using this device with external EPROM or RAM, software debugging becomes easy.

FEATURES

- Software compatible with TMP8049P/i8049
- CMOS/LSI for low power dissipation - less than 50 mW at 5V, 6MHz
- High Noise Immunity
- 2.5μs Instruction Cycle
- Extended temperature operation:
  -40°C to +85°C
- Single power supply
- 2K × 8 masked ROM
- 128 × 8 RAM
- 27 I/O lines
- Interval Timer/Event Counter
- Power Down Mode

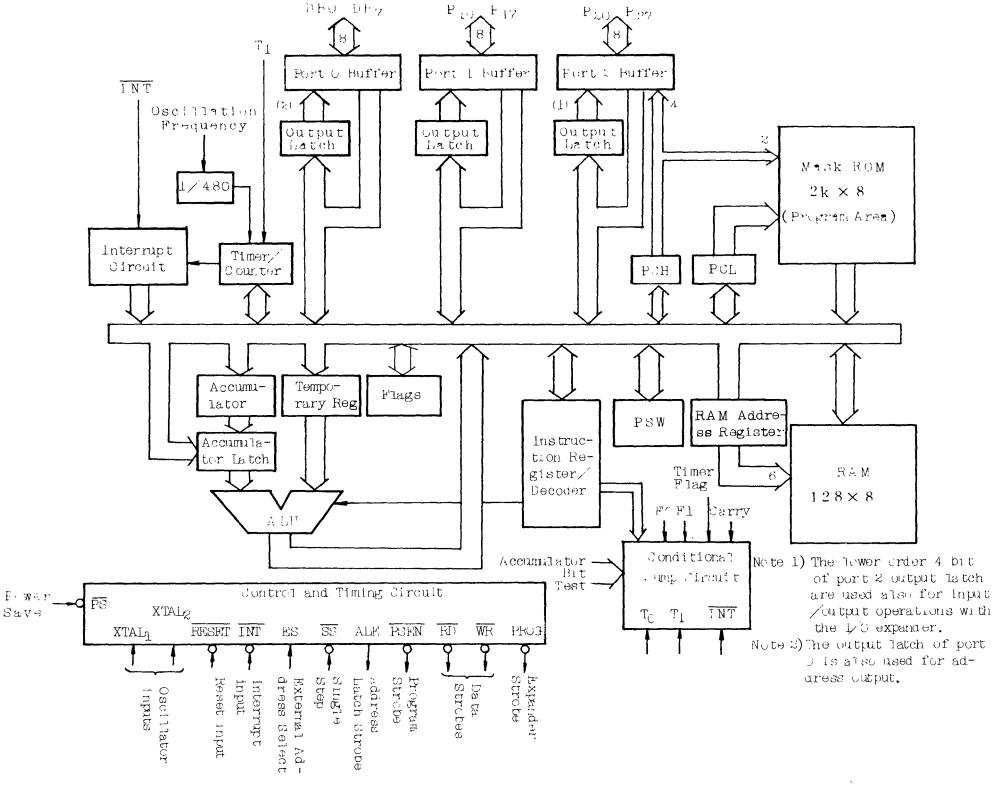
PIN CONNECTIONS (TOP VIEW)



TMP80C49P-6
TMP80C39P-6

PRELIMINARY

BLOCK DIAGRAM



Note 1) The lower order 4 bit of port 2 output latch are used also for input/output operations with the 1/8 expander.

Note 2) The output latch of port 3 is also used for address output.

PIN NAMES AND PIN DESCRIPTION

V_{SS} (Power Supply)
Circuit GND potential

V_{CC} (Power Supply)
+5V during operation

$\overline{PS}$ (Input)
The control signal for the power saving at the power dowen mode (Active Low)

PROG (Output)
Output strobe for the TMP8243P I/O expander.

P10-P17 (Input/Output) Port 1
8-bit quasi-bidirectional port (Internal Pullup ≅ 50KΩ).

P20-P27 (Input/Output) Port 2
8-bit quasi-bidirectional port (Internal Pullup ≅ 50KΩ).

P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for the TMP8243P.

DB0-DB7 (Input/Output, Tri-State)
True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.

T_0 (Input/Output)
Input pin testable using the conditional transfer instructions JT0 and JNT0. T_0 can be designated as a clock output using ENT0 CLK instruction. T_0 is also used during programming.

T_1 (Input)
Input pin testable using the JT1 and JNT1 instruction. Can be designated the event counter input using the timer/STRT CNT instruction.

$\overline{INT}$ (Input)
External interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)

$\overline{RD}$ (Output)
Output strobe activated druing a Bus read. Can be used to enable data onto the Bus from an external device. Used as a Read Strobe to External Data Memory (Active Low).

$\overline{WR}$ (Output)
Output strobe during a Bus write (Active Low). Used as a Write Strobe to External Data Memory.

$\overline{RESET}$ (Input)
Active Low signal which is used to initialize the Processor. Also used during the power down mode.

ALE (Output)
Address Latch Eanble. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.

$\overline{PSEN}$ (Output)
Program Store Enable. This output occurs only during a fetch to external program memory (Active Low).

$\overline{SS}$ (Input)
Single step input can be used in conjunction with ALE to "single step" processor through each instruction when $\overline{SS}$ is low the CPU is placed into a wait state after it has completed the instruction being executed. Also used during the power down mode.

EA (Input)
External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug and essential for testing and program verification. (Active High)

XTAL 1 (Input)
One side of crystal input for internal oscillator. Also input for external source.

XTAL 2 (Input)
Other side of crystal input.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{CC}	V_{CC} Supply Voltage (with respect to GND (V_{SS}))	-0.5V to +7V
V_{INA}	Input Voltage (Except EA)	-0.5V to V_{CC}+0.5V
V_{INB}	Input Voltage (Only EA)	-0.5V to +13V
P_D	Power Dissipation (Ta=85°C)	250mW
T_{SOLDER}	Soldering Temperature (Soldering Time 10 sec)	260°C
T_{STG}	Storage Temperature	-65°C to 150°C
T_{OPR}	Operating Temperature	-40°C to 85°C

DC CHARACTERISTICS (I) T_{OPR}=-40°C to 85°C, V_{CC}=+5V±10%, V_{SS}=0V, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IL}	Input Low Voltage		-0.5	-	0.8	V
V_{IH}	Input High Voltage (Except XTAL1, XTAL2, $\overline{RESET}$, T0, T1)		2.2	-	V_{CC}	V
V_{IH1}	Input High Voltage (XTAL1, XTAL2, $\overline{RESET}$)		0.7V_{CC}	-	V_{CC}	V
V_{IH2}	Input High Voltage (T0, T1)		0.5V_{CC}	-	V_{CC}	V
V_{OL}	Output Low Voltage (Except P10-P17, P20-P27)	I_{OL}=1.6mA	-	-	0.45	V
V_{OL1}	Output Low Voltage (P10-P17, P20-P27)	I_{OL}=1.2mA	-	-	0.45	V
V_{OH11}	Output High Voltage (Except P10-P17, P20-P27)	I_{OH}=-1.6mA	2.4	-	-	V
V_{OH12}	Output High Voltage (Except P10-P17, P20-P27)	I_{OH}=-400μA	V_{CC} -0.8	-	-	V
V_{OH21}	Output High Voltage (P10-P17, P20-P27)	I_{OH}=-50μA	2.4	-	-	V
V_{OH22}	Output High Voltage (P10-P17, P20-P27)	I_{OH}=-25μA	V_{CC} -0.8	-	-	V
I_{LI}	Input Leak Current (T1, $\overline{INT}$, EA, $\overline{PS}$)	$V_{SS} \leq V_{IN} \leq V_{CC}$	-	-	±10	μA
I_{LI1}	Input Leak Current ($\overline{SS}$, $\overline{RESET}$)	$V_{SS} \leq V_{IN} \leq V_{CC}$	-	-	-50	μA
I_{LI2}	Input Leak Current (P10-P17, P20-P27)	V_{SS}+0.45V$\leq V_{IN} \leq V_{CC}$	-	-	-500	μA
I_{LO}	Output Leak Current (BUS, TO) (High impedance condition)	V_{SS}+0.45V$\leq V_{IN} \leq V_{CC}$	-	-	±10	μA
I_{CC}	V_{CC} Supply Current	V_{CC}=5V, f_{XTAL}=6MHz $V_{IH}=V_{CC}$-0.2V V_{IL}=0.2V, C_{X2}=0pF	-	-	10	mA

DC CHARACTERISTICS (II)

T_{OPR}=-40°C to 85°C, V_{CC}=+5V±20%, V_{SS}=0V, Unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IL}	Input Low Voltage		-0.5	-	0.15 V_{CC}	V
V_{IH}	Input High Voltage (Except XTAL1, XTAL2, $\overline{RESET}$, T0, T1)		0.5V_{CC}	-	V_{CC}	V
V_{IH1}	Input High Voltage (XTAL1, XTAL2, $\overline{RESET}$)		0.7V_{CC}	-	V_{CC}	V
V_{IH2}	Input High Voltage (T0, T1)		0.5V_{CC}	-	V_{CC}	V
V_{OL}	Output Low Voltage (Except P10-P17, P20-P27)	I_{OL}=1.6mA	-	-	0.45	V
V_{OL1}	Output Low Voltage (P10-P17, P20-P27)	I_{OL}=1.2mA	-	-	0.45	V
V_{OH12}	Output High Voltage (Except P10-P17, P20-P27)	I_{OH}=-400μA	V_{CC} -0.8	-	-	V
V_{OH22}	Output High Voltage (P10-P17, P20-P27)	I_{OH}=-25μA	V_{CC} -0.8	-	-	V
I_{LI}	Input Leak Current (T1, $\overline{INT}$, EA, $\overline{PS}$)	$V_{SS} \leqq V_{IN} \leqq V_{CC}$	-	-	±10	μA
I_{LI1}	Input Leak Current ($\overline{SS}$, $\overline{RESET}$)	$V_{SS} \leqq V_{IN} \leqq V_{CC}$	-	-	$-\frac{V_{CC}}{0.1}$	μA
I_{LI2}	Input Leak Current (P10-P17, P20-P27)	V_{SS}+0.45V$\leqq V_{IN} \leqq V_{CC}$	-	-	$-\frac{V_{CC}}{0.1}$	μA
I_{LO}	Output Leak Current (BUS, TO) (High impedance condition)	V_{SS}+0.45V$\leqq V_{IN} \leqq V_{CC}$	-	-	±10	μA
I_{CC}	V_{CC} Supply Current	V_{CC}=5V, f_{XTAL}=6MHz $V_{IH}=V_{CC}$-0.2V, V_{IL}=0.2V, C_{X2}=0pF	-	-	10	mA

AC CHARACTERISTICS

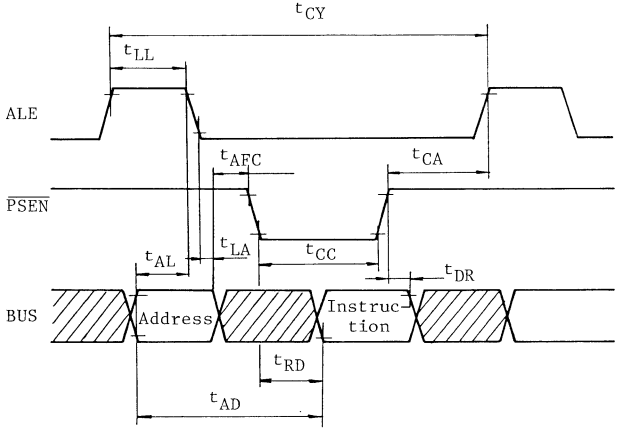
T_{OPR}=-40°C to 85°C, V_{CC}=+5V±20%, V_{SS}=0V, Unless Otherwise Noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
t_{LL}	ALE Pulse Width		400	-	-	ns
t_{AL}	Address Setup Time (ALE)		150	-	-	ns
t_{LA}	Address Hold Time (ALE)		80	-	-	ns
t_{CC}	Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)		700	-	-	ns
t_{DW}	Data Setup Time ($\overline{WR}$)		500	-	-	ns
t_{WD}	Data Hold Time ($\overline{WR}$)	C_L=20pF	120	-	-	ns
t_{CY}	Cycle Time		2.5	-	15.0	μs
t_{DR}	Data Hold Time ($\overline{PSEN}$, $\overline{RD}$)		0	-	200	ns
t_{RD}	Data Input Read Time ($\overline{PSEN}$, $\overline{RD}$)		-	-	500	ns
t_{AW}	Address Setup Time ($\overline{WR}$)		230	-	-	ns
t_{AD}	Address Setup Time (Data Input)		-	-	950	ns
t_{AFC}	Address Float Time ($\overline{RD}$, $\overline{PSEN}$)		0	-	-	ns
t_{CP}	Port Control Setup Time (PROG)		110	-	-	ns
t_{PC}	Port Control Hold Time (PROG)		130	-	-	ns
t_{PR}	Port 2 Input Data Set Time (PROG)		-	-	310	ns
t_{DP}	Output Data Setup Time (PROG)		220	-	-	ns
t_{PD}	Output Data Hold Time (PROG)		65	-	-	ns
t_{PF}	Port 2 Input Data Hold Time (PROG)		0	-	150	ns
t_{PP}	PROG Pulse Width		1510	-	-	ns
t_{PL}	Port 2 I/O Data Setup Time		600	-	-	ns
t_{LP}	Port 2 I/O Data Hold Time		150	-	-	ns

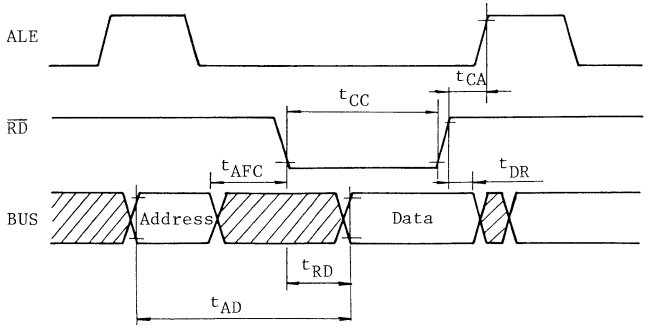
Note : t_{cy}=2.5μs (f_X=6MHz)
Control Outputs ; C_L=80pF, BUS Outputs ; C_L=150pF

TIMING WAVEFORM

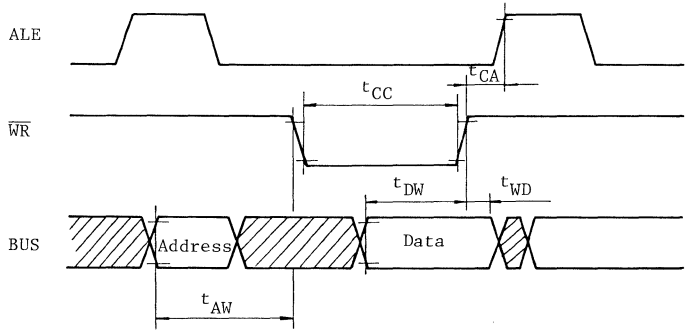
A. Instruction Fetch from External Program Memory



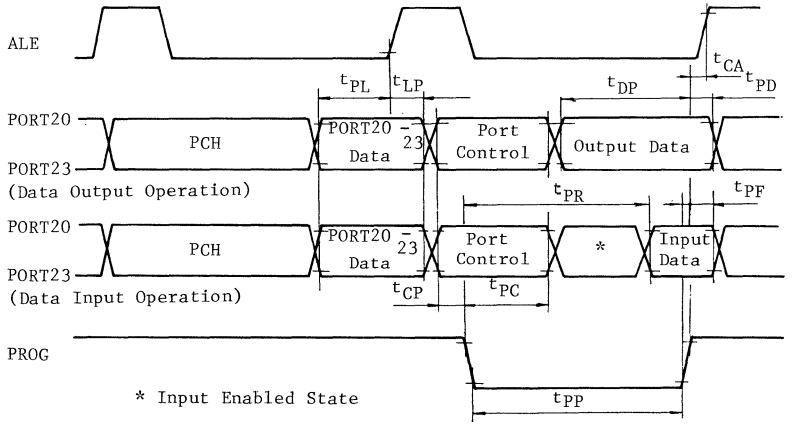
B. Read from External Data Memory



C. Write into External Data Memory



D. Timing of Port 2 during Expander Instruction Execution



POWER DOWN MODE (I) ------ Data Hold Mode in RAM

The operation of oscillation circuit is suspended by setting $\overline{PS}$ terminal to low level after $\overline{RESET}$ terminal has been set to low level. Consequently, all the data in RAM area can be held in low power consumption.

The minimum hold voltage of V_{CC} in this mode is 2V.

$\overline{PS}$ terminal is set to high level to resume osillation after V_{CC} has been reset to 5V, and then $\overline{RESET}$ terminal is set to high level, thus, the normal mode is restarted from the initialize operation (address 0).

DC CHARACTERISTICS (T_{OPR}=-40°C to 85°C, V_{SS}=0V)

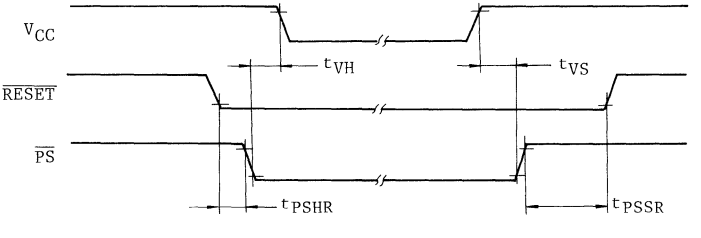
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V_{SB1}	Standby Voltage(1)		2.0	-	6.0	V
I_{SB1}	Standby Current(1)	V_{CC}=5V, V_{IH}=V_{CC}-0.2V, V_{IL}=0.2V	-	0.5	10	μA

AC CHARACTERISTICS (T_{OPR}=-40°C to 85°C, V_{CC}=5V±20%, V_{SS}=0V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{PSHR}	Power Save Hold Time ($\overline{RESET}$)		10	-	-	μS
t_{PSSR}	Power Save Setup Time ($\overline{RESET}$)		10	-	-	mS
t_{VH}	V_{CC} Hold Time ($\overline{PS}$)		5	-	-	μS
t_{VS}	V_{CC} Setup Time ($\overline{PS}$)		5	-	-	μS

Note : t_{cy}=2.5μs (f_x=6MHz)

TIMING WAVEFORM



POWER DOWN MODE (II) ------ All Data Hold Mode

The operation of oscillation circuit is suspended by setting $\overline{PS}$ terminal to low level after $\overline{SS}$ terminal has been set to low level. Consequently, all data can be held in low power consumption.

The minimum hold voltage of V_{CC} in this mode is 3V.

$\overline{PS}$ terminal is set to high level to resume oscillation after V_{CC} has been reset to 5V, and then $\overline{SS}$ terminal is set to high level, thus, the normal mode is restarted continuously from the state just before the power down mode (II).

DC CHARACTERISTICS (T_{OPR}=-40°C to 85°C, V_{SS}=0V)

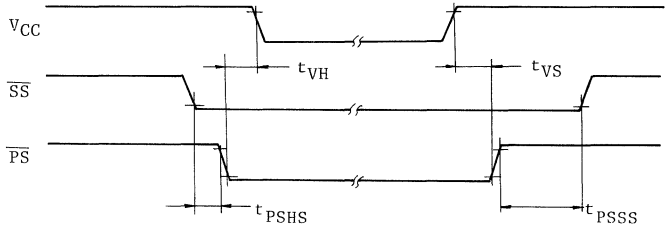
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V_{SB2}	Standby Voltage(2)		3.0	-	6.0	V
I_{SB2}	Standby Current(2)	V_{CC}=5V, V_{IH}=V_{CC}-0.2V, V_{IL}=0.2V	-	0.5	10	μA

AC CHARACTERISTICS (T_{OPR}=-40°C to 85°C, V_{CC}=5V±20%, V_{SS}=0V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{PSHS}	Power Save Hold Time ($\overline{SS}$)		5	-	-	μS
t_{PSSS}	Power Save Setup Time ($\overline{SS}$)		10	-	-	mS
t_{VH}	V_{CC} Hold Time ($\overline{PS}$)		5	-	-	μS
t_{VS}	V_{CC} Setup Time ($\overline{PS}$)		5	-	-	μS

Note : t_{cy}=2.5μs (f_X=6MHz)

TIMING WAVEFORM



PIN STATUS IN THE POWER DOWN MODE

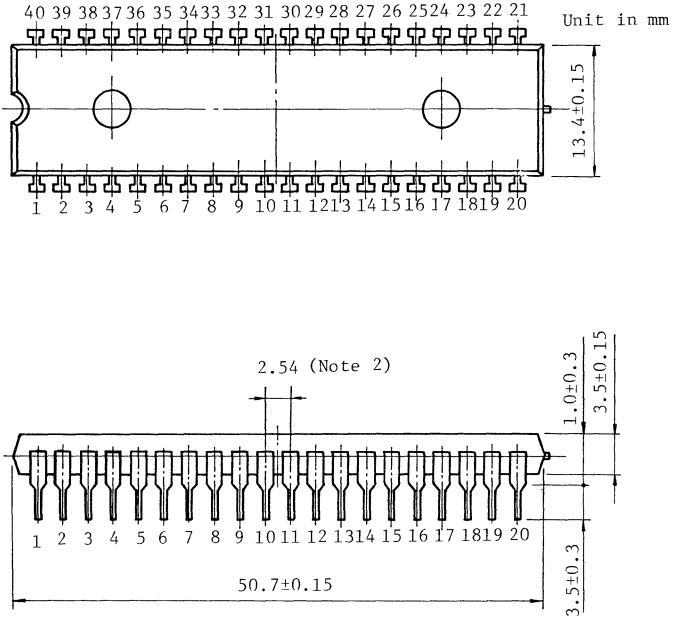
Each pin status in the power down mode (I)/(II) is shown in the following table.

PIN NAME	POWER DOWN MODE (I)	POWER DOWN MODE (II)
DB0 - DB7	High Impedance Input Disabled	High Impedance Input Disabled
P20 - P23	Output "0" (at EA=1) High Impedance (at EA=0) Input Disabled	Output PC_H
P24 - P27	High Impedance Input Disabled	Output the data Contained in the Port (Open Drain)
P10 - P17	High Impedance Input Disabled	Output the data Contained in the Port (Open Drain)
T_0	High Impedance Input Disabled	High Impedance Input Disabled
T_1	Input Disabled	Input Disabled
XTAL1 XTAL2	High Impedance	High Impedance
$\overline{RESET}$, $\overline{SS}$	Input Disabled when oscillator is stopped Pull-up transistor turned off	Input Disabled when oscillator is stopped Pull-up transistor turned off
$\overline{INT}$, EA	Input Disabled when oscillator is stopped	Input Disabled when oscillator is stopped
$\overline{RD}$, $\overline{WR}$	Output "1"	Output "1"
ALE	Output "0"	Output "1"
PROG	Output "1"	Output "1"
$\overline{PSEN}$	Output "0" (at EA=1) Output "1" (at EA=0)	Output "1"

TMP80C49P-6
TMP80C39P-6

PRELIMINARY

OUTLINE DRAWING



Note : 1. This dimension is measured at the center of bending point of leads

2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoritical positions with respect to No.1 and No.42 leads.