TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT

TMP8155P

TMP8156P

N-CHANNEL SILICON GATE MOS

2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

GENERAL DESCRIPTION

The TMP 8155P/8156P are RAM including I/O ports and counter/timer on the chip for using in the TLCS-85A microcomputer system. The RAM portion is designed with 2K bit static cells organized as 256 x 8. The 14 bit programmable counter/timer is the down counter. It provides either a square wave or terminal count pulse for the cpu system depending on timer mode.

The I/O portion is consists of 2 programmable 8 bit I/O ports and 1 programmable 6 bit I/O port. The programmable I/O ports can be operated by BASIC MODE and STROBE MODE.

FEATURES

- Compatible with Intel's 8155/8516
- Single +5 V Power Supply
- Access Time: 400 ns (MAX.)
- Internal Address Latch
- 2 Programmable 8 Bit I/O Ports and 1 Programmable 6 Bit I/O Port.
- 256 Word x 8 Bits RAM
- Programmable 14 Bit Binary Counter/Timer
- Multiplexed Address and Data Bus
- Chip Enable Active High (TMP8156P) or Low (TMP8155P)
- 40 pin DIP

PIN CONNECTION (TOP VIEW)

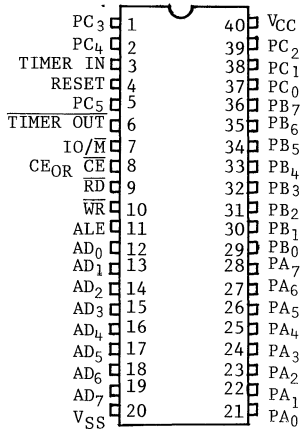


FIGURE 1 TMP8155P/8156P PINOUT DIAGRAM

BLOCK DIAGRAM

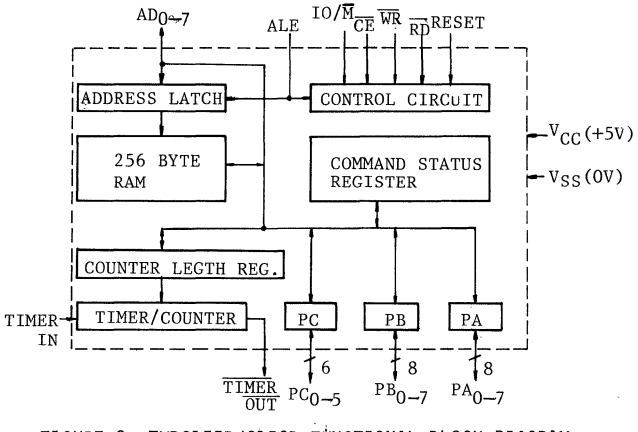


FIGURE 2 TMP8155P/8156P FUNCTIONAL BLOCK DIAGRAM

PIN NAMES AND PIN DESCRIPTION

RESET (INPUT)

The Reset signal is a pulse provided by the TMP8085A to initialize the system. Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two TMP8085A clock cycle times.

$AD_{0\sim7}$ (INPUT / OUTPUT, 3-STATE)

These are 3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latche on the falling edge of the ALE. The address can be applied to the memory section or the I/O section depending on the polarity of the IO/$\overline{M}$ input signal. The 8-bit data is either written into the chip or read from the chip depending on the status of $\overline{WR}$ or $\overline{RD}$ input signal.

CE OR $\overline{CE}$ (INPUT)

Chip Enable: On the TMP8155P, this pin is $\overline{CE}$ and is ACTIVE LOW. On the TMP8156P, this pin is CE and is ACTIVE HIGH.

$\overline{RD}$ (INPUT)

Input low on this line with the Chip Enable active enables the $AD_{0\sim7}$ buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/ status register will be read to the AD bus.

$\overline{WR}$ (INPUT)

Input low on this line with the Chip Enable active causes the data on the AD lines to be written to the RAM or I/O ports and command/status register depending on the polarity of IO/$\overline{M}$.

ALE (INPUT)

Address Latch Enable: This control signal latches both the address on the $AD_{0\sim7}$ lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.

IO/$\overline{M}$ (INPUT)

IO/$\overline{\text{Memory}}$ Select: This line selects the memory if low and selects the I/O and command/status register if high.

$PA_{0\sim7}$ (INPUT/OUTPUT, 3-STATE)

These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command Register.

PB0~7 (INPUT/OUTPUT, 3-STATE)

These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command Register.

PC0~5 (INPUT/OUTPUT, 3-STATE)

These 6 pins can function as either input port, output port, or as control signal for PA and PB. Programming is done through the Command Register. When $PC_{0\sim5}$ are used as control signals, they are defined the following:

PC_0 - A INTR (Port A Interrupt)

PC_1 - A BF (Port A Buffer Full)

PC_2 - A $\overline{STB}$ (Port A Strobe)

PC_3 - B INTR (Port B Interrupt)

PC_4 - B BF (Port B Buffer Full)

PC_5 - B $\overline{STB}$ (Port B Strobe)

TIMER IN (INPUT)

This is the input to the counter-timer.

$\overline{\text{TIMER OUT}}$ (OUTPUT)

This pin is the timer output. This output can be either a square wave or a pulse depending on the timer mode.

V_{CC} (Power)
+5 volt supply

V_{SS} (Power)
Ground Reference

FUNCTIONAL DESCRIPTION

PROGRAMMING OF THE COMMAND REGISTER

The command register consists of eitht latches. Four bits (0-3) define the mode of the ports, two bits (4-5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6-7) are for the timer.

The command register contents can be altered at any time by using the I/O address XXXX000 during a WRITE operation. The function of each bit of the command byte is defined in FUGURE 3.

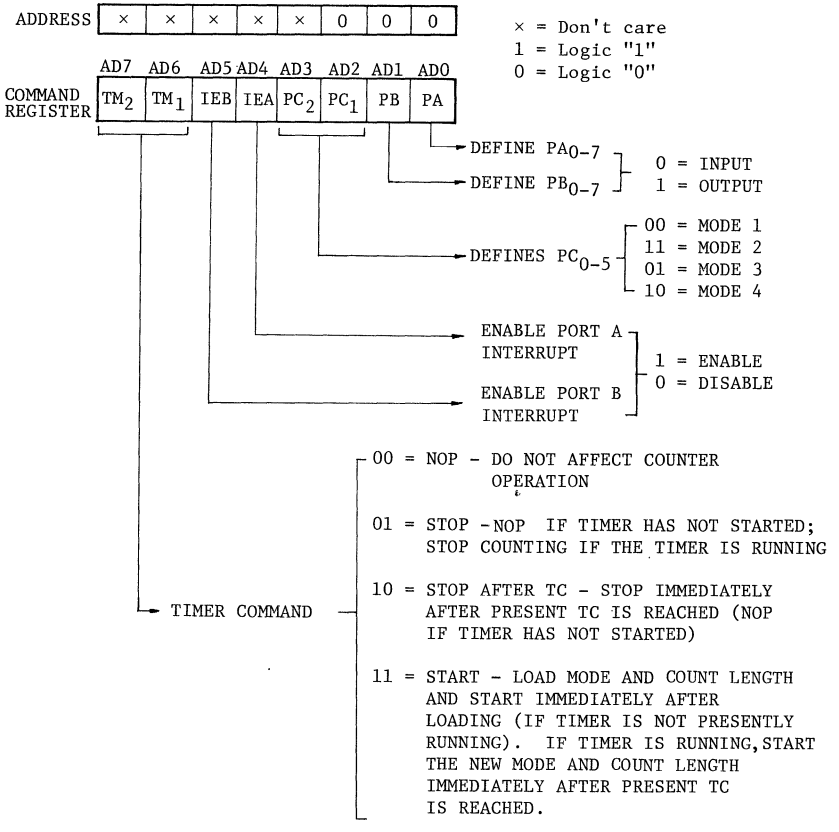


FIGURE 3 COMMAND REGISTER BIT ASSIGNMENT

READING THE STATUS REGISTER

The status register consists of seven latches, one for each bit; six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the Status Register (Address XXXXX000). Status word format is shown in FIGURE 4.

Note that you may never write to the status register since the command register shares the same I/O address and the command register is selected when a write to that address is issued.

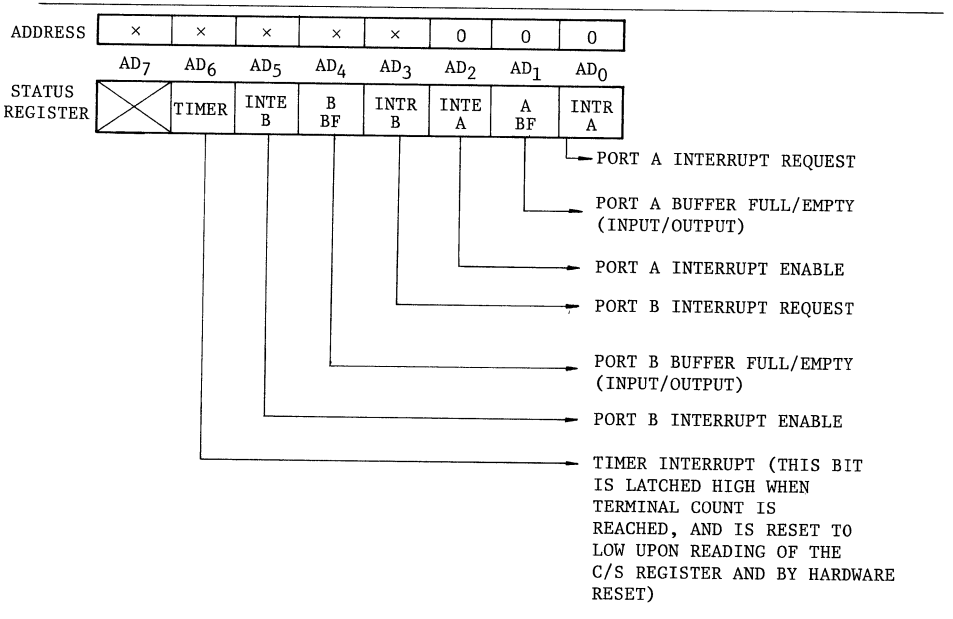


FIGURE 4 STATUS REGISTER BIT ASSIGNMENT

INPUT/OUTPUT SECTION

COMMAND/STATUS REGISTER (C/S)

Both register have the common address ×××××000. When the C/S registers are selected during WRITE operation, a command is written into the C/S register. The contents of this register are not accessible through the pins. When the C/S is selected during a READ operation, the status information of the I/O ports and the timer becomes available on the AD_{0-7} lines.

- PA Register — This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register. Also depending on the command, this port can operate in either the basic mode or the strobed mode (See timing diagram). The I/O pins assigned in relation to this register are PA_{0-7}. The address of this register is XXXXX001.

- PB Register — This register functions the same as PA Register. The I/O pins assigned are PB_{0-7}. The address of this register is XXXXX010.

- PC Register — This register has the address XXXXX011 and contains only 6-bits. The 6-bits can be programmed to be either input ports, output ports or as control signals for PA and PB by properly programming the AD_2 and AD_3 bits of the C/S register.

When PC_{0-5} is used as a control port, 3-bits are assigned for Port A and 3 for Port B. The first bit is an interrupt that the TMP8155P/8156P issues. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. See Table 2.

When the port C is programmed to either MODE 3 or MODE 4, the control signals for PA and PB are initialized as follows:

MODE \ CONTROL	BF	INTR	$\overline{STB}$
INPUT MODE	Low	Low	Input Control
OUTPUT MODE	Low	High	Input Control

To summarize, the register's assignments are shown TABLE 1.

TABLE 1 I/O PORT ADDRESSING SCHEME

I/O ADDRESS								PINOUTS	SELECTION	NO. OF BITS
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0			
X	X	X	X	X	0	0	0	Internal	Command/Status Register	8
X	X	X	X	X	0	0	1	PA_{0-7}	General Purpose I/O Port A	8
X	X	X	X	X	0	1	0	PB_{0-7}	General Purpose I/O Port B	8
X	X	X	X	X	0	1	1	PC_{0-7}	General Purpose I/O Port or Control	6
X	X	X	X	X	1	0	0		Low-Order 8 bits of Timer Count	
X	X	X	X	X	1	0	1		High 6 bits/2 bits of Timer Count	

TABLE 2 TABLE OF PORT CONTROL ASSIGNMENT

Pin	MODE 1	MODE 2	MODE 3	MODE 4
PC0	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A $\overline{\text{STB}}$ (Port A strobe)	A $\overline{\text{STB}}$ (Port A Strobe)
PC3	Input Port	Output Port	Output Port	B INTR (Port B Interrupt)
PC4	Input Port	Output Port	Output Port	B BF (Port B Buffer Full)
PC5	Input Port	Output Port	Output Port	B $\overline{\text{STB}}$ (Port B Strobe)

TIMER SECTION

The timer is a 14-bit down-counter that counts the 'timer input' pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register.

To program the timer, the COUNT LENGTH REGISTER is loaded first, one byte at a time, by selecting the timer addresses. Bits 0-13 will specify the length of the next count and bits 14-15 will specify the timer output mode. The value loaded into the count length register can have any value from 2_H through $3FFF_H$ in bits 0-13.

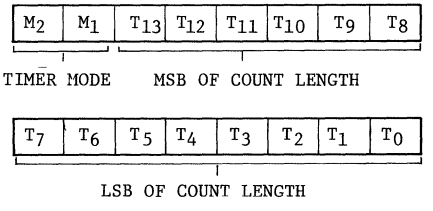


FIGURE 5 TIMER FROMAT

There are four timer modes which are defined by M2 and M1.

M2	M1	
0	0	Put out low during second half of count.
0	1	Continuous square wave; The period of the square-wave equals the count length programmed with automatic reload at terminal count.
1	0	Single pulse upon TC being reached.
1	1	Continuous pulses.

Note: In case of an odd-numbered count, the first half-cycle of the square-wave output, which is high, is one count longer than the second (low) half-cycle as shown in FIGURE 6.

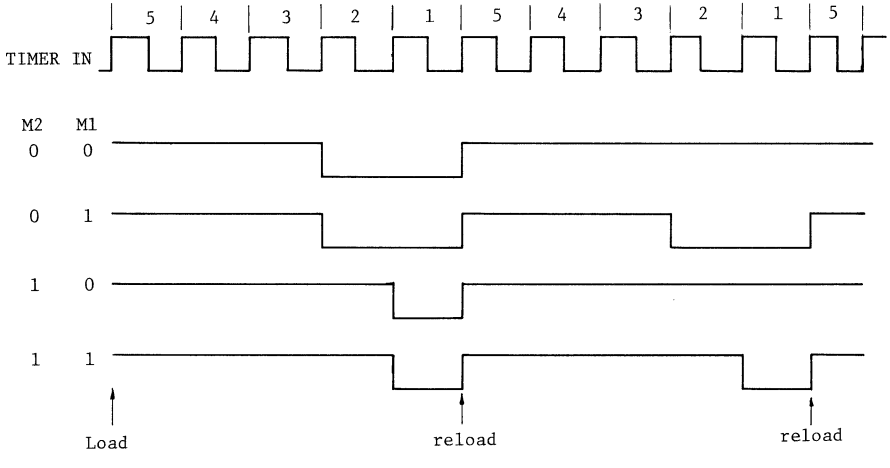


FIGURE 6 ASYMMETRICAL SQUARE-WAVE OUTPUT RESULTING FROM COUNT OF 5

Bits 6-7 (TM2 and TM1) of command register contents are used to start and stop the counter. There are four commands to choose from;

TM2	TM1	
0	0	NOP: Do not affect counter operation.
0	1	STOP: NOP if timer has not started; stop counting if the timer is running.
1	0	STOP AFTER TC: Stop immediately after present TC is reached. (NOP if timer has not started)
1	1	START: Load mode and count length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and count length immediately after present TC is reached.

Note that while the counter is counting, you may load a new count and mode into the count length registers. Before the new count and mode will be used by the counter, you must issue a START command to the counter. This applies even though you may only want to change the count and use the previous mode.

The counter in the TMP8155P/8156P is not initialized to any particular mode or count when hardware RESET occurs, but RESET does stop the counting. Therefore you must issue a START command via the C/S register, because counting cannot begin following RESET.

Please note that the timer circuit on the TMP8155P/8156P chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by twos twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. You cannot load an initial value of 1 into the count register and cause the timer to operate, as its terminal count value is 10 (binary). After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses required to complete the timer cycle if desired. To obtain the remaining count, perform the following operations in order:

1. Stop the count.
2. Read in the 16-bit value from the count length registers.
3. Reset the upper two mode bits.
4. Reset the carry and rotate right one position all 16 bits through carry.
5. If carry is set, add 1/2 of the full original count (1/2 full count-1 if full count is odd.)

Note: If you started with an odd count and you read the count length register before the third count pulse occurs, you will not be able to discern whether one or two counts has occurred. Regardless of this, the TMP8155P/8156P always counts out the right number of pulses in generating the $\overline{\text{TIMER OUT}}$ waveforms.

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating
V_{CC}	V_{CC} Supply Voltage with Respect to V_{SS}	-0.5V to +7.0V
V_{IN}	Input Voltage with Respect to V_{SS}	-0.5V to +7.0V
V_{OUT}	Output Voltage with Respect to V_{SS}	-0.5V to +7.0V
P_D	Power Dissipation	1.5W
T_{SOLDER}	Soldering Temperature (Soldering Time 10 sec.)	260°C
T_{STG}	Storage Temperature	-55°C to +150°C
T_{OPR}	Operating Temperature	0°C to +70°C

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}+0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -400μA	2.4			V
I_{IL}	Input Leakage	V_{IN} = V_{CC} to 0V			±10	μA
I_{LO}	Output Leakage Current	0.45V ≤ V_{OUT} ≤ V_{CC}			±10	μA
I_{CC}	V_{CC} Supply Current				180	mA
$I_{IL(CE)}$	Chip Enable Leakage 8155 8156	V_{IN} = V_{CC} to 0V.			 +100 -100	 μA μA

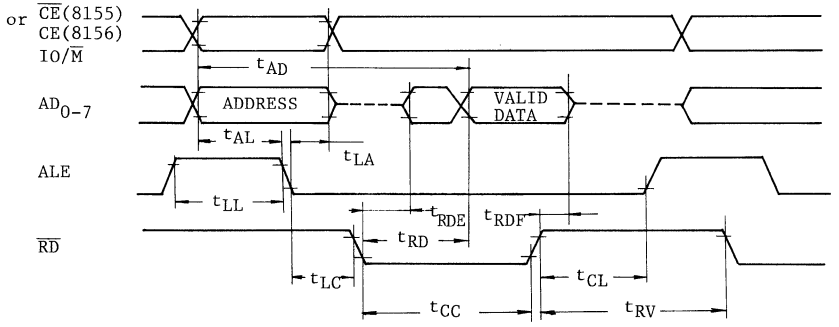
A.C. CHARACTERISTICS

T_A=0°C to +70°C, V_{CC}=+5V±5%

Symbol	Parameters	Test Condition	Min.	Typ.	Max.	Units
t_{AL}	Address to Latch Set Up Time	150pF Load	50			ns
t_{LA}	Address Hold Time after Latch		80			ns
t_{LC}	Latch to READ/WRITE Control		100			ns
t_{RD}	Valid Data out Delay from READ Control				170	ns
t_{AD}	Address Stable to Data Out Valid				400	ns
t_{LL}	Latch Enable Width		100			ns
t_{RDF}	Data Bus Float After READ		0		100	ns
t_{CL}	READ/WRITE control Latch Enable		20			ns
t_{CC}	READ/WRITE Control Width		250			ns
t_{DW}	Data In to WRITE Set Up Time		150			ns
t_{WD}	Data in Hold Time After WRITE		0			ns
t_{RV}	Recovery Time Between Controls		300			ns
T_{WP}	WRITE to Port Output				400	ns
T_{PR}	Port Input Setup Time		70			ns
t_{RP}	Port Input Hold Time		50			ns
t_{SBF}	Strobe to Buffer Full				400	ns
t_{SS}	Strobe Width		200			ns
t_{RBE}	READ to Buffer Empty				400	ns
t_{SI}	Strobe to INTR On				400	ns
t_{RDI}	READ to INTR Off				400	ns
t_{PSS}	Port Setup Time to Strobe		50			ns
t_{PHS}	Port Hold Time After Strobe		120			ns
t_{SBE}	Strobe to Buffer Empty				400	ns
t_{WBF}	WRITE to Buffer Full				400	ns
t_{WI}	WRITE to INTR Off				400	ns
t_{TL}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low				400	ns
t_{TH}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ High				400	ns
t_{RDE}	Data Bus Enable from READ Control		10			ns
t_L	TIMER-IN Low Time		80			ns
t_H	TIMER-IN High Time		120			ns

TIMING WAVEFORMS

A. READ CYCLE



B. WRITE CYCLE

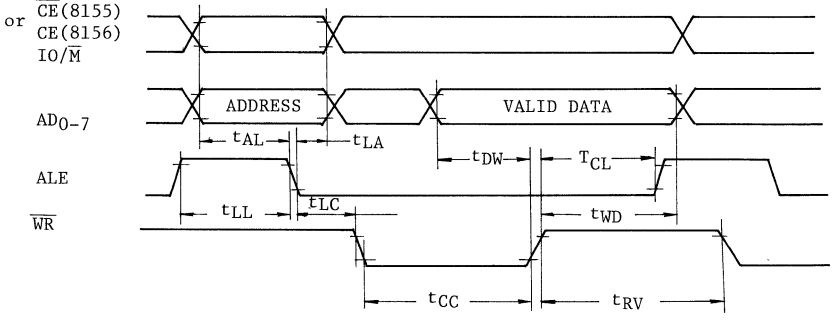
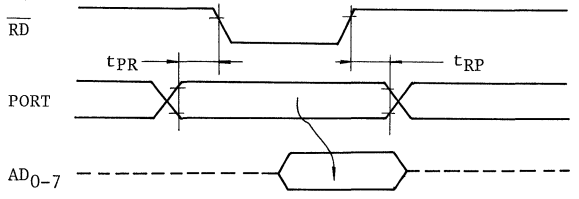


FIGURE 7 READ/WRITE TIMING DIAGRAMS

A. BASIC INPUT MODE



B. BASIC OUTPUT MODE

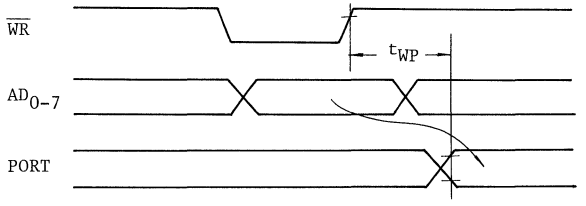
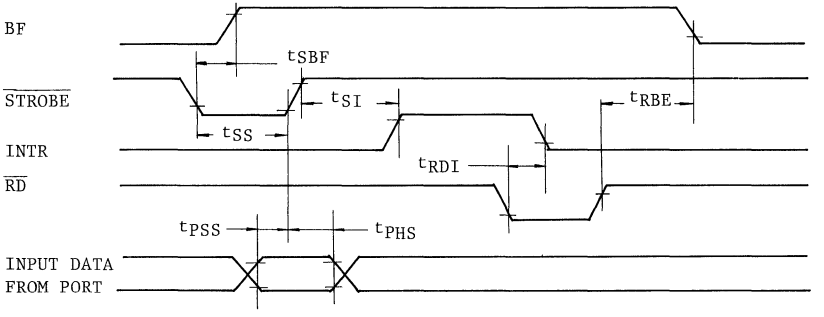


FIGURE 8 BASIC I/O TIMING WAVEFORM

A. STROBED INPUT MODE



B. STROBED OUTPUT MODE

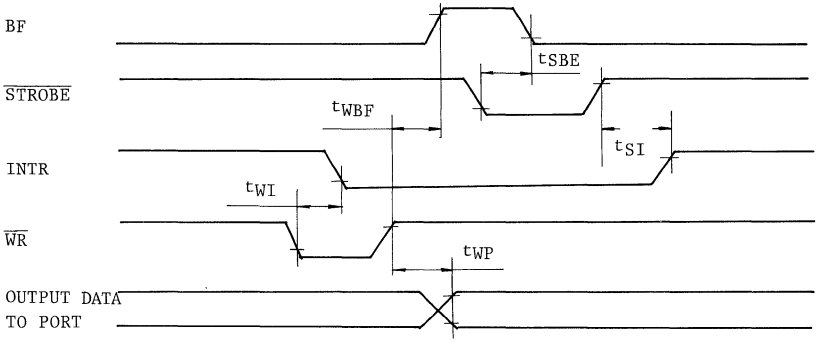
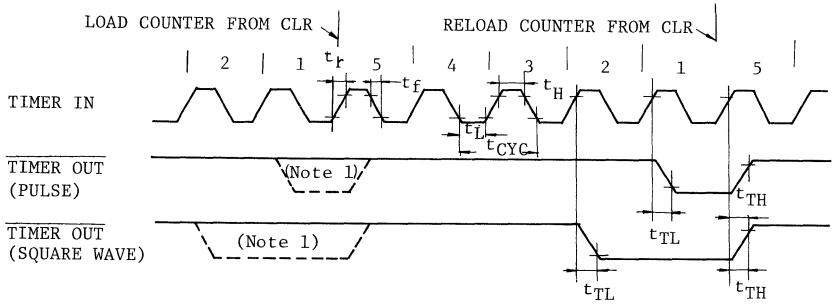


FIGURE 9 STROBED I/O TIMING WAVEFORM



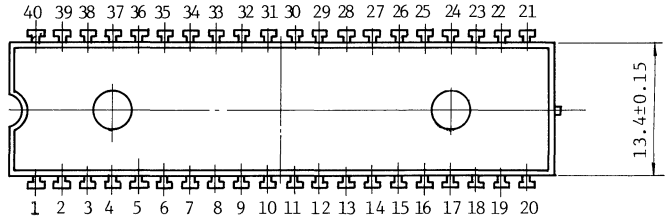
Note 1: The timer output is periodic if in an automatic reload mode (M_1 Mode Bit = 1)

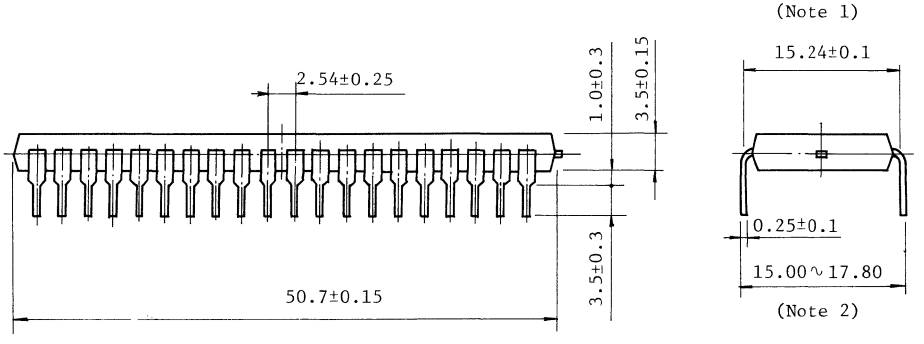
FIGURE 10 TIMER OUTPUT WAVEFORM COUNTDOWN FROM 5 TO 1

OUTLINE DRAWING

40 Pins Plastic Package

Unit in mm





Note: 1. This dimension shows the center of curvature of leads.
2. This dimension shows spread of leads.
3. All dimensions are in millimeters.