Comparison table of TMP86C829B/H29B/M29B/PM29A/PM29B/C929AXB and TMP86FM29 ☐ Difference

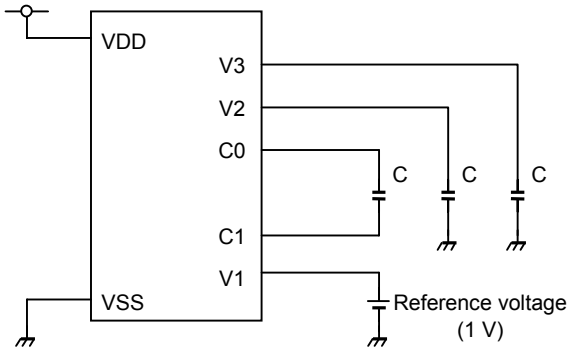
	TMP86C829B TMP86CH29B TMP86CM29B	TMP86PM29A TMP86PM29B	TMP86C929AXB (Emulation chip) (Note 3)	TMP86FM29F
ROM	8 K (Mask ROM) 16 K (Mask ROM) 32 K (Mask ROM)	32 K (OTP)	–	32 K (Flash)
RAM	512 1.5 K 1.5 K	1.5 K	–	2 K
I/O	42 pin		42 pin (MCU part)	42 pin
External Interrupt	5 pin			5 pin
AD Converter	10-bit AD converter × 8 ch			10-bit AD converter × 8 ch
Timer Counter	18-bit timer × 1 ch 8-bit timer × 4 ch			18-bit timer × 1 ch 8-bit timer × 4 ch
Serial Interface	8-bit UART / SIO × 1 ch			8-bit UART / SIO × 1 ch
LCD	32 seg × 4 com			32 seg × 4 com (Note 2)
Key-on Wakeup	4 ch			4 ch
Operating Voltage in MCU Mode	1.8 to 5.5 V at 4.2 MHz 2.7 to 5.5 V at 8 MHz 4.5 to 5.5 V at 16 MHz		1.8 to 5.25 V at 4.2 MHz 2.7 to 5.25 V at 8 MHz 4.5 to 5.25 V at 16 MHz	1.8 to 3.6 V at 4.2 MHz (External clock) 1.8 to 3.6 V at 8 MHz (Resonator) 2.7 to 3.6 V at 16 MHz
Operating Temperature in MCU Mode	−40 to 85°C		0 to 60°C	−40 to 85°C
Writing to Flash Memory	–			2.7 to 3.6V at 16 MHz 25°C ± 5°C
CPU Wait (Note 1)	N/A			Available

Note 1: The CPU wait is a CPU halt function for stabilizing of power supply of Flash memory. The CPU wait period is as follows. In the CPU wait period except RESET, CPU is halted but peripheral functions are not halted. Therefore, if the interrupt occurs during the CPU wait period, the interrupt latch is set. In this case, if the IMF has been set to "1", the interrupt service routine is executed after CPU wait period. For details refer to 2.14 "Flash Memory" in TMP86FM29 data sheet.

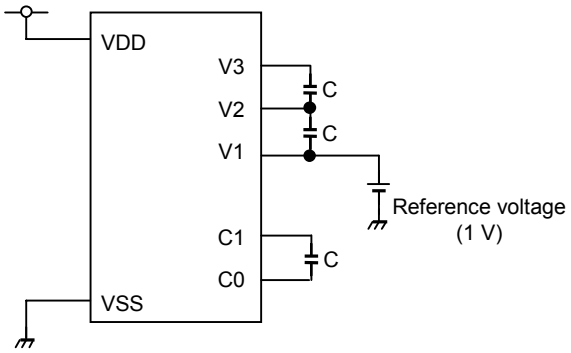
Thus, even if the same software is executed in 86FM29 and 86C829B/H29B/M29B/PM29A/PM29B /C929AXB, the operation process is not the same. Therefore, when the final operating confirmation on target application is executed for software development of Mask ROM Product (86C829B/H29B/M29B), not the Flash product (86FM29) but the OTP product (86PM29A/PM29B) should be used.

Condition	Wait Time	Halt/Operate	
		CPU	Peripherals
After reset release	2^{10}/fc[s]	Halt	Halt
Changing from STOP mode to NORMAL mode (at EEPCR<MNPWDW> = "1")	2^{10}/fc[s]	Halt	Operate
Changing from STOP mode to SLOW mode (at EEPCR<MNPWDW> = "1")	2^{3}/fs[s]	Halt	Operate
Changing from IDLE0/1/2 mode to NORMAL mode (at EEPCR<ATPWDW> = "0")	2^{10}/fc[s]	Halt	Operate
Changing from SLEEP0/1/2 mode to SLOW mode (at EEPCR<ATPWDW> = "0")	2^{3}/fs[s]	Halt	Operate

Note 2: The 86FM29 can not drive the 5V LCD panel because the electrical characteristics in 86FM29 is altered from 86C829B/H29B/M29B/PM29A/PM29B/C929AXB. The recommended operating condition of V3 pin in TMP86FM29 is 3.6V(max). For details, refer to “Electrical Characteristics”.
When the LCD booster circuit is used in 86FM29, connect the reference voltage and capacitor as shown in "case2". Though the method of "case1" has been recommended in 86C829B /H29B/M29B/PM29A/PM29B datasheets, the 86FM29 should not use method of "case1". Even if the method of "case1" is used in the 86C829B/H29B/M29B/PM29A/PM29B/C929AXB, the function and operation are not issue at all. However, if the "case2" is used, the booster ability becomes higher than "case1". Therefore, when the application board is designed newly in future, the method of "case2" is also recommended in 86C829B/H29B/M29B/PM29A/PM29B/C929AXB.



Case 1
(For 86C829B/H29B/M29B/PM29A/PM29B/C929AXB)



Case 2
(For 86FM29 and 86C829B/H29B/M29B/
PM29A/PM29B/C929AXB)

Note 3: Flash function, CPU wait period and serial PROM mode cannot be emulated in the 86C929AXB. If the software including the flash function is executed in 86C929AXB, the operation process differs from 86FM29.

CMOS 8-Bit Microcontroller

TMP86FM29UG/FG

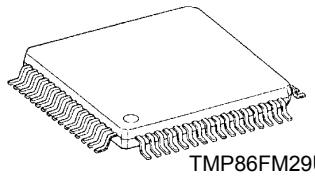
The TMP86FM29 is the high-speed, high-performance and low power consumption 8-bit microcomputer, including FLASH, RAM, LCD driver, multi-function timer/counter, serial interface (UART/SIO), a 10-bit AD converter and two clock generators on chip.

Product No.	FLASH	RAM	Package	Emulation Chip
TMP86FM29UG	32768 × 8 bits	1536 × 8 bits	P-LQFP64-1010-0.50E	TMP86C929AXB
TMP86FM29FG			P-QFP64-1414-0.80C	

Feautures

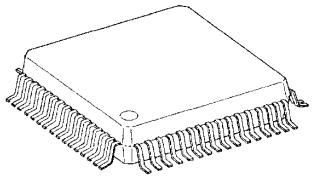
- 8-bit single chip microcomputer TLCS-870/C series
- Instruction execution time: 0.25 μs (at 16 MHz)
  122 μs (at 32.768 kHz)
- 132 types and 731 basic instructions
- 19 interrupt sources (External: 5, Internal: 14)
- Input/Output ports (39 pins)
  (Out of which 24 pins are also used as SEG pins)
- 18-bit timer counter: 1 ch
  - Timer, Event counter,
    Pulse width measurement,
    Frequencymeasurement modes
- 8-bit timer counter: 4 ch
  - Timer, Event counter,
    PWM output, Programmable divider output,
    PPG output modes
- Time Base Timer
- Divider output function

P-LQFP64-1010-0.50E



TMP86FM29UG

P-QFP64-1414-0.80C



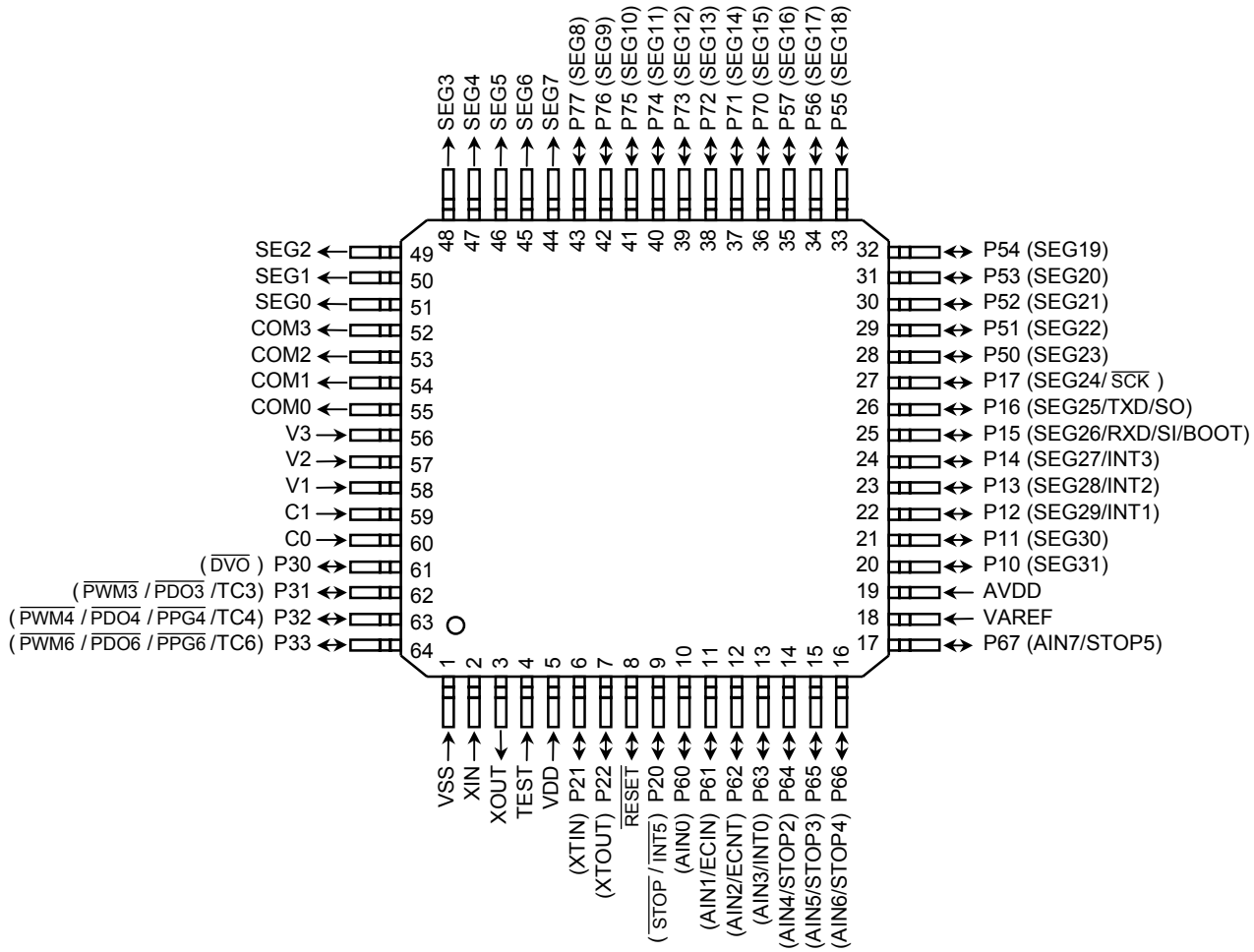
TMP86FM29FG

030619EBP1

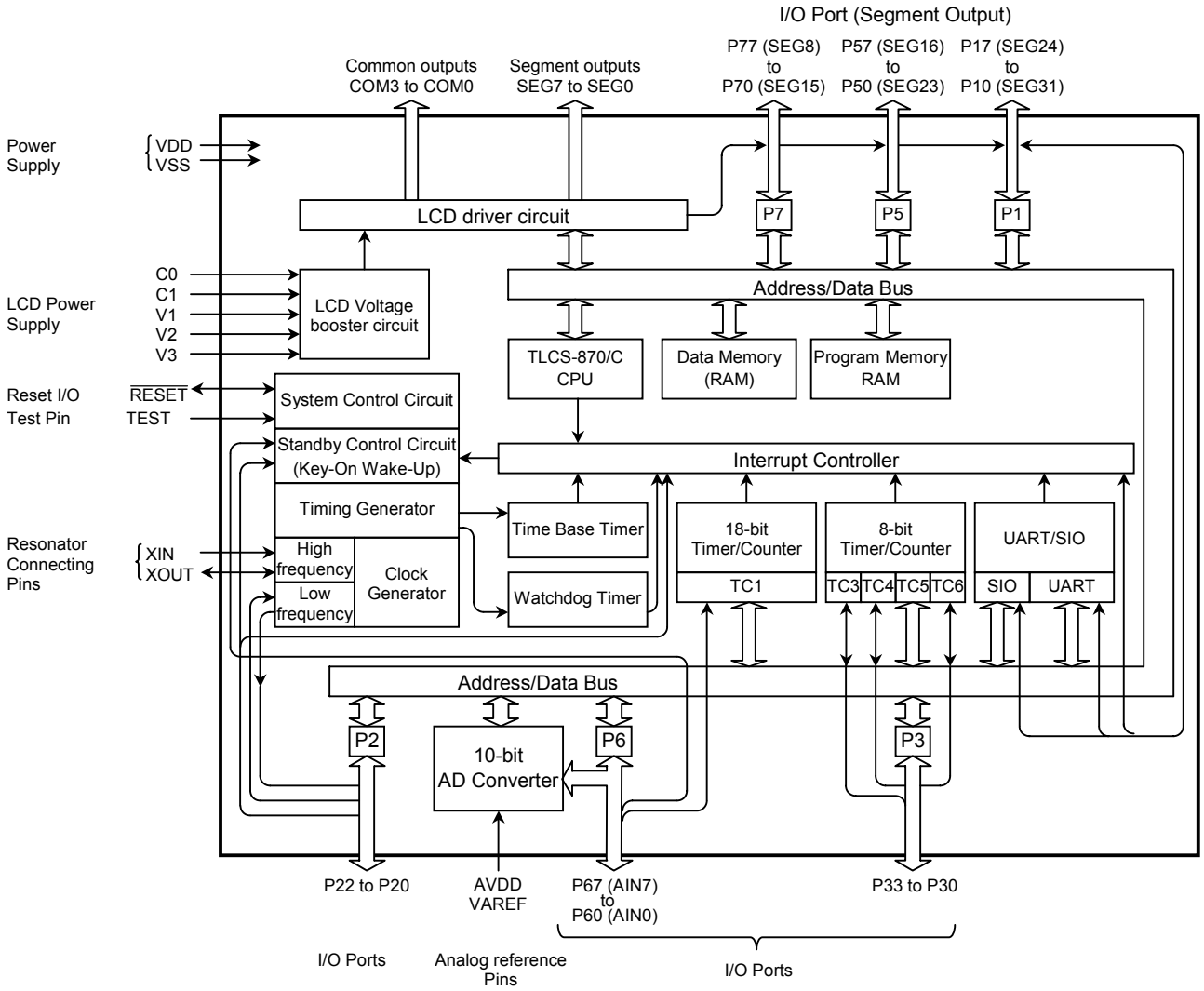
- Watchdog Timer
  - Interrupt source/reset output (programmable)
- Serial interface
  - 8-bit UART/SIO: 1ch
- 10-bit successive approximation type AD converter
  - Analog input: 8 ch
- Four Key-On Wake-Up pins
- LCD driver/controller
  - Built-in voltage booster for LCD driver
  - With displaymemory
  - LCD direct drive capability (max 32 seg × 4 com)
  - 1/4, 1/3, 1/2duties or static drive are programmably selectable
- Dual clock operation
  - Single/Dual-clock mode
- Nine power saving operating modes
  - STOP mode : Oscillation stops. Battery/Capacitor back-up. Port output hold/High-impedance.
  - SLOW 1, 2 mode : Low power consumption operation using low-frequency clock (32.768 kHz)
  - IDLE 0 mode : CPU stops, and peripherals operate using high-frequency clock of Time-Base-Timer. Release by falling edge of TBTCR <TBTCK> setting.
  - IDLE 1 mode : CPU stops, and peripherals operate using high-frequency clock. Release by interruputs.
  - IDLE 2 mode : CPU stops, and peripherals operate using high and low frequency clock. Release by interruputs.
  - SLEEP 0 mode : CPU stops, and peripherals operate using low-frequency clock of Time-Base-Timer. Release by falling edge of TBTCR <TBTCK> setting.
  - SLEEP 1 mode : CPU stops, and peripherals operate using low-frequency clock. Release by interrupts.
  - SLEEP 2 mode : CPU stops, and peripherals operate using high and low frequency clock. Release by interrupts.
- Wide operating voltage: 1.8 to 3.6 V at 8 MHz/32.768 kHz
  2.7 to 3.6 V at 16 MHz/32.768 kHz

Pin Assignments (Top View)

P-LQFP64-1010-0.50E
P-QFP64-1414-0.80C



Block Diagram



Pin Functions

Pin Name	Input/Output	Functions		
P17 (SEG24, $\overline{SCK}$)	I/O (I/O)	8-bit input/output port with latch. When used as input port, an external interrupt input, serial interface input/output and UART data input/output, the P1LCR must be set to "0" after setting output latch to "1". When used as a LCD segment output, the P1LCR must be set to "1".	Serial clock input/output	LCD segment outputs.
P16 (SEG25, TxD, SO)	I/O (Output)		UART data output Serial data output	
P15 (SEG26, RxD, SI BOOT)	I/O (I/O)		UART data input Serial data input Serial PROM mode control input	
P14 (SEG27, INT3)	I/O (I/O)		External interrupt 3 input	
P13 (SEG28, INT2)	I/O (I/O)		External interrupt 2 input	
P12 (SEG29, INT1)	I/O (I/O)		External interrupt 1 input	
P11 (SEG30)	I/O (Output)			
P10 (SEG31)	I/O (Output)			
P22 (XTOUT)	I/O (Output)	3-bit input/output port with latch. When used as an input port, the output latch must be set to "1".	Resonator connecting pins (32.768 kHz) For inputting external clock, XTIN is used and XOUT is opened.	
P21 (XTIN)	I/O (Input)			
P20 ($\overline{INT5}$, $\overline{STOP}$)	I/O (Input)		External interrupt input 5 or STOP mode release signal input	
P33 ($\overline{PWM6}$, $\overline{PDO6}$ $\overline{PPG6}$, TC6)	I/O (I/O)	4-bit programmable input/output port (Nch high current output). When used as a timer/counter output or divider output, the output latch must be set to "1". When used as an input port or timer/counter input, the P3OUTCR must be set to "0" after P3DR is set to "1".	Timer counter 6 input/output	
P32 ($\overline{PWM4}$, $\overline{PDO4}$ $\overline{PPG4}$, TC4)	I/O (I/O)		Timer counter 4 input/output	
P31 ($\overline{PWM3}$, $\overline{PDO3}$, TC3)	I/O (I/O)		Timer counter 3 input/output	
P30 ($\overline{DVO}$)	I/O (Output)		Divider output	
P57 (SEG16) to P50 (SEG23)	I/O (Output)	8-bit input/output port with latch. When used as a LCD segment output, the P5LCR must be set to "1".	LCD segment outputs	
P67 (AIN7, STOP5)	I/O (Input)	8-bit programmable input/output port (tri-state). Each bit of this port can be individually configured as an input or an output under software control. When used as an analog input, the P6CR must be set to "0" after setting output latch to "0". When used as an input port, a key on wake up input, an external interrupt input and timer/ counter input, the P6CR must be set to "0" after setting output latch to "1".	STOP 5 input	AD converter analog inputs
P66 (AIN6, STOP4)	I/O (Input)		STOP 4 input	
P65 (AIN5, STOP3)	I/O (Input)		STOP 3 input	
P64 (AIN4, STOP2)	I/O (Input)		STOP 2 input	
P63 (AIN3, $\overline{INT0}$)	I/O (Input)		External interrupt 0 input	
P62 (AIN2, ECNT)	I/O (Input)		Timer/Counter 1 input	
P61 (AIN1, ECIN)	I/O (Input)			
P60 (AIN0)	I/O (Input)			
P77 (SEG8) to P70 (SEG15)	I/O (Output)	8-bit input/output port with latch. When used as a LCD segment output, the P7LCR must be set to "1".	LCD segment outputs	
SEG7 to SEG0	Output	LCD segment outputs		
COM3 to COM0		LCD common outputs		
V3 to V1	LCD voltage booster pin	LCD voltage booster pin. Capacitors are required between C0 and C1 pin and V1/V2/V3 pin and GND.		
C1 to C0				
XIN, XOUT	Input Output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.		
$\overline{RESET}$	I/O	Reset signal input or watchdog timer output/address-trap-reset output/system clock reset output		
TEST	Input	Test pin for out-going test, and the serial PROM mode control pin. Usually be fixed to low level. When the serial PROM mode starts, be fixed to "1".		
VDD, VSS	Power Supply	+5 V, 0 (GND)		
VAREF		Analog reference voltage inputs (High)		
AVDD		AD circuit power supply		

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

1.1 Memory Address Map

The TMP86FM29 memory consists of 5 blocks: FLASH memory, BOOT ROM, RAM, DBR (Data buffer register) and SFR (Special function register). They are all mapped in 64-Kbyte address space. Figure 1.1.1 shows the TMP86FM29 memory address map. The general-purpose registers are not assigned to the RAM address space.

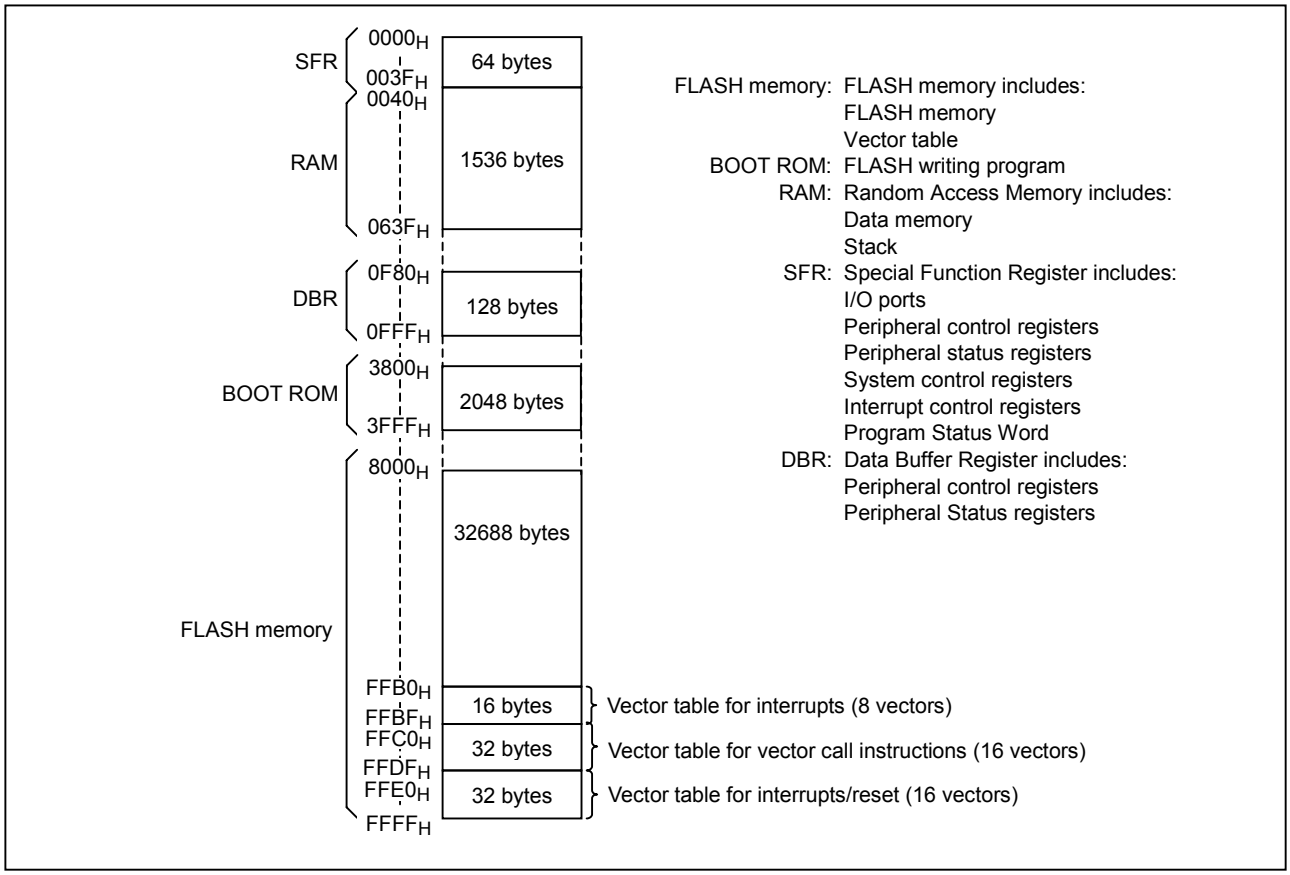


Figure 1.1.1 Memory Address Maps

1.2 Program Memory (FLASH)

The TMP86FM29 has a 32 K × 8 bits (Address 8000_H to $FFFF_H$) of Flash memory.

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Rating	Unit
Supply voltage	V_{DD}		−0.3 to 4.0	V
	V_{LCD}	V3 pin	−0.3 to 4.0	
Input voltage	V_{IN}		−0.3 to V_{DD} + 0.3	
Output voltage	V_{OUT1}		−0.3 to V_{DD} + 0.3	
Output current (Per 1 pin)	I_{OUT1}	P3, P6 ports	−1.8	mA
	I_{OUT2}	P1, P2, P5, P6, P7 ports	3.2	
	I_{OUT3}	P3 ports	30	
Output current (Total)	ΣI_{OUT2}	P1, P2, P5, P6, P7 ports	60	
	ΣI_{OUT3}	P3 ports	80	
Power dissipation [Topr = 85°C]	PD		350	mW
Soldering temperature (Time)	Tsld		260 (10 s)	°C
Storage temperature	Tstg		−55 to 125	
Operating temperature	Topr		−40 to 85	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition-1 (MCU mode) (V_{SS} = 0 V, Topr = −40 to 85°C)

Parameter	Symbol	Pins	Condition		Min	Max	Unit
Supply voltage	V_{DD}		fc = 16 MHz	NORMAL1, 2 mode	2.7	3.6	V
				IDLE0, 1, 2 mode			
			fc = 8 MHz (In case of connecting the resonator)	NORMAL1, 2 mode	1.8		
				IDLE0, 1, 2 mode			
			fc = 4.2 MHz (In case of external clock input)	NORMAL1, 2 mode			
				IDLE0, 1, 2 mode			
			fs = 32.768 kHz	SLOW1, 2 mode	1.8		
				SLEEP0, 1, 2 mode			
				STOP mode			
Input high level	V_{IH1}	Except Hysteresis input	$V_{DD} \geq 2.7$ V		$V_{DD} \times 0.70$	V_{DD}	
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 2.7$ V		$V_{DD} \times 0.90$		
Input low level	V_{IL1}	Except Hysteresis input	$V_{DD} \geq 2.7$ V		0	$V_{DD} \times 0.30$	
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 2.7$ V			$V_{DD} \times 0.10$	
Clock frequency (In case of connecting the resonator)	fc	XIN, XOUT	V_{DD} = 1.8 to 3.6 V		1.0	8.0	MHz
			V_{DD} = 2.7 to 3.6 V			16.0	
	fs	XTIN, XTOUT	V_{DD} = 1.8 to 3.6 V		30.0	34.0	kHz
Clock frequency (In case of external clock input)	fc	XIN, XOUT	V_{DD} = 1.8 to 3.6 V		1.0	4.2	MHz
			V_{DD} = 2.7 to 3.6 V			16.0	
	fs	XTIN, XTOUT	V_{DD} = 1.8 to 3.6 V		30.0	34.0	kHz
LCD reference voltage	V1		Booster circuit is enable ($V3 \geq V_{DD}$)		0.8	1.2	V
Capacity for LCD booster circuit	C_{LCD}		LCD booster circuit is enable ($V3 \geq V_{DD}$)		0.1	0.47	μF

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (Supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Recommended Operating Condition-2 (Serial PROM mode) (V_{SS} = 0 V, Topr = 25°C ± 5°C)

Parameter	Symbol	Pins	Condition	Min	Max	Unit
Supply voltage	VDD		2 MHz ≤ fc ≤16 MHz	2.7	3.6	V
Clock frequency	fc	XIN, XOUT	VDD = 2.7 to 3.6 V	2.0	16.0	MHz

Note: The operating temperature area of serial PROM mode is 25°C ± 5°C and the operating area of high frequency of serial PROM mode is different from MCU mode.

DC Characteristics (V_{SS} = 0 V, Topr = –40 to 85°C)

Parameter	Symbol	Pins	Condition	Min	Typ.	Max	Unit
Hysteresis voltage	V_{HS}	Hysteresis input	V_{DD} = 3.3 V	–	0.4	–	V
Input current	I_{IN1}	TEST	V_{DD} = 3.6 V, V_{IN} = 0 V	–	–	–5	μA
	I_{IN2}	Sink open drain, Tri-state	V_{DD} = 3.6 V, V_{IN} = 3.6 V/0 V	–	–	±5	
	I_{IN3}	$\overline{RESET}$	V_{DD} = 3.6 V, V_{IN} = 3.6 V	–	–	+5	
Input resistance	R_{IN1}	TEST pull down	V_{DD} = 3.6 V, V_{IN} = 3.6 V	–	70	–	kΩ
	R_{IN2}	$\overline{RESET}$ pull up	V_{DD} = 3.6 V, V_{IN} = 0 V	100	220	450	
High frequency feedback resistor	R_{FB}	XOUT	V_{DD} = 3.6 V	–	3	–	MΩ
Low frequency feedback resistor	R_{FBT}	XTOUT	V_{DD} = 3.6 V	–	20	–	
Output leakage current	I_{LO}	Sink open drain, Tri-state	V_{DD} = 3.6 V V_{OUT} = 3.4V/0.2 V	–	–	±10	μA
Output high voltage	V_{OH}	CMOS, Tri-state	V_{DD} = 3.6 V, I_{OH} = –0.6 mA	3.2	–	–	V
Output low voltage	V_{OL}	Except XOUT, P3 port	V_{DD} = 3.6 V, I_{OL} = 0.9 mA	–	–	0.4	
Output low current	I_{OL}	P3 port	V_{DD} = 3.6 V, V_{OL} = 1.0 V	–	6	–	mA
LCD output voltage (LCD booster is enable)	$V_{2\text{-}3OUT}$	V2 pin	V3 ≥ V_{DD} Reference supply pin: V1 SEG/COM pin: No load	–	V1 x 2	–	V
		V3 pin		–	V1 x 3	–	
Supply current in NORMAL 1, 2 mode		Fetch area: Flash area	V_{DD} = 3.6 V V_{IN} = 3.4 V/0.2 V fc = 16 MHz fs = 32.768 kHz	MNP = "1"	–	5.3	7.3	mA
		Fetch area: RAM area		MNP = "0"	–	3.4	5.2	
Supply current in IDLE 0, 1, 2 mode				MNP•ATP = "1"	–	3.1	5.2	
				MNP•ATP = "0"	–	2.2	4.2	
Supply current in SLOW 1 mode		Fetch area: Flash area	V_{DD} = 3.0 V V_{IN} = 2.8 V/0.2 V fs = 32.768 kHz	MNP = "1"	–	850	1200	μA
		Fetch area: RAM area		MNP = "0"	–	7	19	
Supply current in SLEEP 1 mode				MNP•ATP = "1"	–	850	1200	
				MNP•ATP = "0"	–	5.5	17	
Supply current in SLEEP 0 mode				MNP•ATP = "1"	–	850	1200	
				MNP•ATP = "0"	–	4.5	15	
Supply current in STOP mode			V_{DD} = 3.6 V V_{IN} = 3.4 V/0.2 V		–	0.5	10	

Note 1: Typical values show those at Topr = 25°C.

Note 2: Input current (I_{IN1}, I_{IN2}): The current through pull-up or pull-down resistor is not included.

Note 3: I_{DD} does not include I_{REF} current.

Note 4: The supply currents of SLOW2 and SLEEP2 modes are equivalent to IDLE0, IDLE1, IDLE2.

Note 5: MNP (MNPWDW) shows bit0 in EEPCR register and ATP (ATPWDW) shows bit1 in EEPCR register.

Note 6: "Fetch" means reading operation of FLASH data as an instruction by CPU.

AD Conversion Characteristics (V_{SS} = 0.0 V, 2.7 V ≤ V_{DD} ≤ 3.6 V, Topr = –40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage	V_{AREF}		A_{VDD} – 1.0	–	A_{VDD}	V
Power supply voltage of analog control circuit	A_{VDD}		V_{DD}			
Analog reference voltage range (Note 4)	ΔV_{AREF}		2.5	–	–	
Analog input voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power supply current of analog reference voltage	I_{REF}	V_{DD} = A_{VDD} = V_{AREF} = 3.6 V V_{SS} = 0.0 V	–	0.35	0.61	mA
Non linearity error		V_{DD} = A_{VDD} = 2.7 V V_{SS} = 0.0 V V_{AREF} = 2.7 V	–	–	±2	LSB
Zero point error			–	–	±2	
Full scale error			–	–	±2	
Total error			–	–	±2	

(V_{SS} = 0.0 V, 2.0 V ≤ V_{DD} < 2.7 V, Topr = –40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage	V_{AREF}		A_{VDD} – 0.6	–	A_{VDD}	V
Power supply voltage of analog control circuit	A_{VDD}		V_{DD}			
Analog reference voltage range (Note 4)	ΔV_{AREF}		2.0	–	–	
Analog input voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power supply current of analog reference voltage	I_{REF}	V_{DD} = A_{VDD} = V_{AREF} = 2.0V V_{SS} = 0.0 V	–	0.20	0.34	mA
Non linearity error		V_{DD} = A_{VDD} = 2.0 V V_{SS} = 0.0 V V_{AREF} = 2.0 V	–	–	±4	LSB
Zero point error			–	–	±4	
Full scale error			–	–	±4	
Total error			–	–	±4	

(V_{SS} = 0.0 V, 1.8 V ≤ V_{DD} < 2.0 V, Topr = –10 to 85°C) (Note 5)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage	V_{AREF}		A_{VDD} – 0.1	–	A_{VDD}	V
Power supply voltage of analog control circuit	A_{VDD}		V_{DD}			
Analog reference voltage range (Note 4)	ΔV_{AREF}		1.8	–	–	
Analog input voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power supply current of analog reference voltage	I_{REF}	V_{DD} = A_{VDD} = V_{AREF} = 1.8 V V_{SS} = 0.0 V	–	0.18	0.31	mA
Non linearity error		V_{DD} = A_{VDD} = 1.8 V V_{SS} = 0.0 V V_{AREF} = 1.8 V	–	–	±4	LSB
Zero point error			–	–	±4	
Full scale error			–	–	±4	
Total error			–	–	±4	

Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.

Note 2: Conversion time is different in recommended value by power supply voltage.
About conversion time, please refer to “2.15.2 Register configration”.

Note 3: Please use input voltage to AIN input Pin in limit of VAREF – VSS.
When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.

Note 4: Analog Reference Voltage Range: ΔVAREF = VAREF – VSS

Note 5: When AD is used with VDD < 2.0 V, the guaranteed temperature range varies with the operating voltage.

Note 6: When AD converter is not used, fix the AVDD pin and VAREFpin on the V_{DD} level.

AC Characteristics (V_{SS} = 0 V, V_{DD} = 2.7 to 3.6 V, Topr = –40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine cycle time	tcy	NORMAL1, 2 mode	0.25	–	4	μs
		IDLE1, 2 mode				
		SLOW1, 2 mode	117.6	–	133.3	
		SLEEP1, 2 mode				
High Level clock pulse width	twcH	For external clock operation (XIN input), fc = 16 MHz	–	31.25	–	ns
Low level clock pulse width	twcL					
High level clock pulse width	twcH	For external clock operation (XTIN input), fs = 32.768 kHz	–	15.26	–	μs
Low level clock pulse width	twcL					

(V_{SS} = 0 V, V_{DD} = 1.8 to 3.6 V, Topr = –40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine cycle time	tcy	NORMAL1, 2 mode	0.5	–	4	μs
		IDLE1, 2 mode				
		SLOW1, 2 mode	117.6	–	133.3	
		SLEEP1, 2 mode				
High level clock pulse width	twcH	For external clock operation (XIN input), fc = 4.2 MHz	–	119.04	–	ns
Low level clock pulse width	twcL					
High level clock pulse width	twcH	For external clock operation (XTIN input), fs = 32.768 kHz	–	15.26	–	μs
Low level clock pulse width	twcL					

Timer Counter 1 input (ECIN) Characteristics (V_{SS} = 0 V, Topr = -40 to 85°C)

Parameter	Symbol	Condition		Min	Typ.	Max	Unit
TC1 input (ECIN input)	t_{TC1}	Frequency measurement mode V_{DD} = 2.7 to 3.6 V	Single edge count	–	–	16	MHz
			Both edge count				
		Frequency measurement mode V_{DD} = 1.8 to 2.7 V	Single edge count	–	–	8	
			Both edge count				

Flash Characteristics (V_{SS} = 0 V)

Parameter	Condition	Min	Typ.	Max	Unit
Number of guaranteed writes (page writing) to Flash memory in serial PROM mode	V_{DD} = 2.7 to 3.6 V, 2 MHz ≤ fc ≤ 16 MHz (Topr = 25°C ± 5°C)	–	–	10^5	Times

Recommended Oscillating Conditions

Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.

Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following http://www.murata.co.jp/search/index.html