CMOS 8-Bit Microcontroller

TMP86FH46N

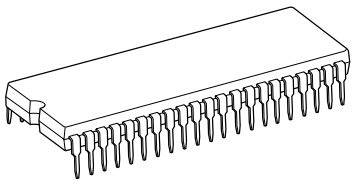
The TMP86FH46 is a high-speed, high-performance 8-bit microcomputer built around the TLCS-870/C Series core with built-in 16-Kbyte flash memory and it is pin compatible with its mask ROM version, the TMP86C846/H46. Writing programs in the built-in flash memory enables this microcomputer to perform the same operations as the TMP86C846/H46. The built-in flash memory can be rewritten on board (without removing it from the PCB) by a built-in boot program.

Product No.	Flash Memory	RAM	Package
TMP86FH46N	16384 × 8 bits	512 × 8 bits	P-SDIP42-600-1.78

Feautures

- 8-bit single chip microcomputer TLCS-870/C series
- Instruction execution time: 0.25 μs (at 16 MHz)
  122 μs (at 32.768 kHz)
- 132 types and 731 basic instructions
- 18 interrupt sources (External: 6, Internal: 12)
- Input/output ports (33 pins)
- 8-bit timer counter: 2 ch
  - Timer, PWM, PPG, PDO, Event counter modes
- Time base timer
- Watchdog timer
  - Interrupt sources/reset output (Programmable)
- Serial interface
  - 8-bit SIO: 1 ch
  - 8-bit UART: 1 ch

P-SDIP42-600-1.78



TMP86FH46N

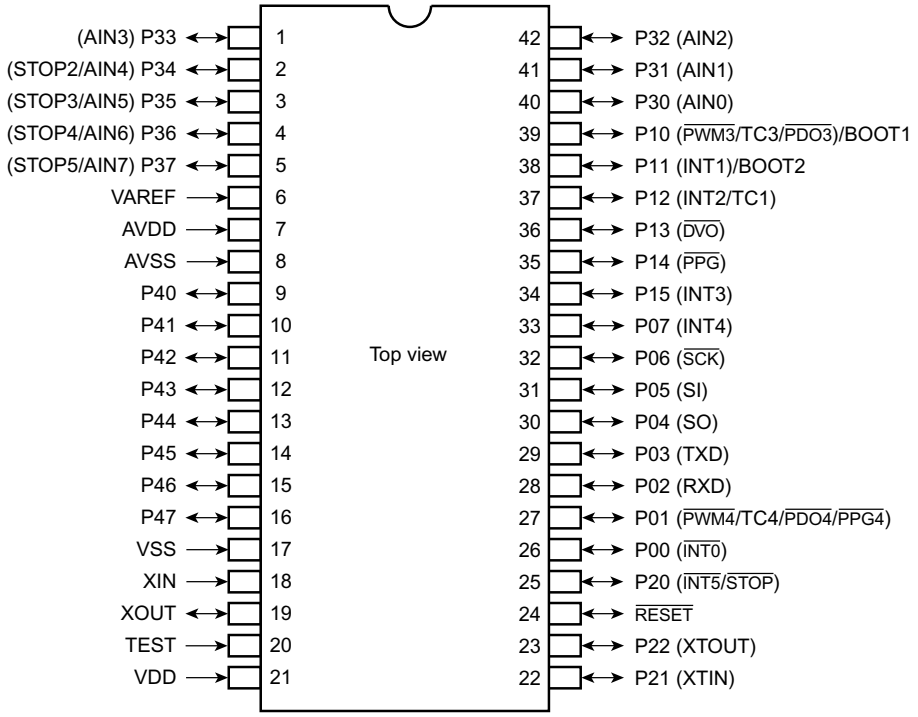
030619EBP1

- 10-bit successive approximation type AD converter
  - Analog input: 8 ch
- 16-bit timer counter: 1 ch
  - Timer, event counter, pulse width measurment, programmable pulse generator (PPG), external-triggered timer, window modes
- Key-on wakeup: 4 ch
- Dual clock operation
  - Single/dual-clock mode
- Nine power saving operating modes
  - STOP mode: Oscillation stops. Battery/capacitor backup. Port output hold/high-impedance.
  - SLOW 1, 2 mode: Low power consumption operation using low-frequency clock (32.768 kHz)
  - IDLE 0 mode: CPU stops, and peripherals operate using high-frequency clock of time-base-timer. Release by INTTBT interrupt.
  - IDLE 1 mode: CPU stops, and peripherals operate using high-frequency clock. Release by interrupts.
  - IDLE 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release by interrupts.
  - SLEEP 0 mode: CPU stops, and peripherals operate using low-frequency clock of time-base-timer. Release by INTTBT interrupt.
  - SLEEP 1 mode: CPU stops, and peripherals operate using low-frequency clock. Release by interrupts.
  - SLEEP 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release by interrupts.
- Wide operating voltage: 4.5 to 5.5 V at 16 MHz/32.768 kHz
  2.7 to 5.5 V at 8 MHz/32.768 kHz

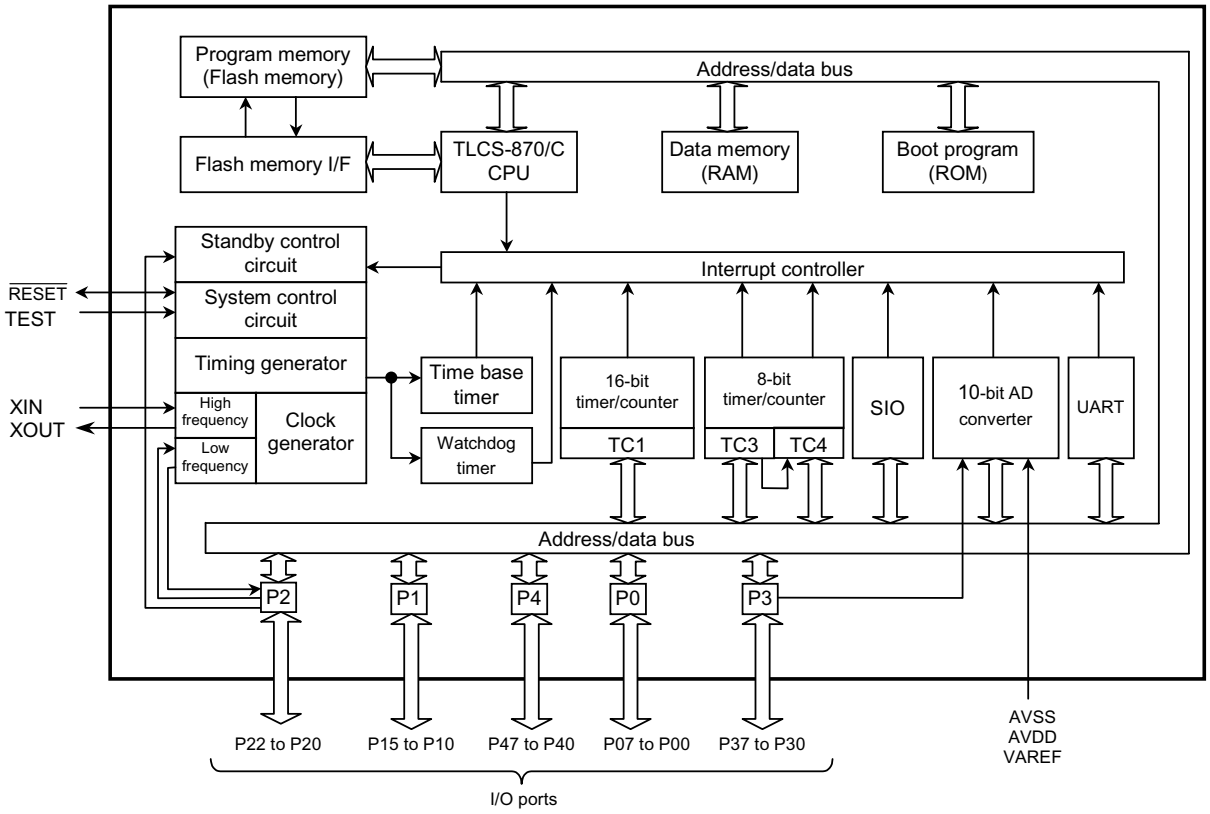
Note: The operating voltage, the operating temperature and the operating current are different between TMP86FH46 and TMP86C846/H46.
About details, please refer to electrical characteristics of each products.

Pin Assignments (Top view)

P-SDIP42-600-1.78



Block Diagram



Pin Function

The TMP86FH46 has MCU mode and serial PROM mode.

(1) MCU mode

In the MCU mode, the TMP86FH46 is a pin compatible with the TMP86C846/H46 (Make sure to fix the TEST pin to low level).

(2) Serial PROM mode

The serial PROM mode is set by fixing TEST pin, P10 and P11 at "high" respectively when $\overline{\text{RESET}}$ pin is fixed "low".

After release of reset, the built-in BOOT ROM program is activated and the built-in flash memory is rewritten by serial I/F (UART).

Pin Name (Serial PROM mode)	Input/ Output	Functions	Pin Name (MCU mode)
BOOT1/RXD	Input/Input	Fix "High" during reset. This pin is used as RXD pin after releasing reset.	P10
BOOT2/TXD	Input/Output	Fix "High" during reset. This pin is used as TXD pin after releasing reset.	P11
TEST	Input	Fix to "High".	
$\overline{\text{RESET}}$	I/O	Reset signal input or an internal error reset output.	
VDD, AVDD	Power supply	5 V	
VSS, AVSS, VAREF		0 V	
P07 to P00, P15 to P12, P22 to P20, P37 to P30, P47 to P40		Fix to "Low" or "High".	
XIN	Input	Self oscillation with resonator (2 MHz, 4 MHz, 8 MHz, 16 MHz)	
XOUT	Output		

Operation

This section describes the functions and basic operational blocks of TMP86FH46.

The TMP86FH46 has flash memory in place of the mask ROM which is included in the TMP86C846/H46. The configuration and function are the same as the TMP86C846/H46. For TMP86C845, however, some functions have been partially changed or deleted. For the functions of TMP86FH46 in details, see the section of TMP86C846/H46.

1. Operating Mode

The TMP86FH46 has MCU mode and serial PROM mode.

1.1 MCU Mode

The MCU mode is set by fixing the TEST pin to the low level.

In the MCU mode, the operation is the same as the TMP86C846/H46 (TEST pin cannot be used open because it has no built-in pull-down resistor).

1.1.1 Program memory

The TMP86FH46 has a 16-Kbyte built-in flash memory (Addresses C000H to FFFFH in the MCU mode).

When using TMP86FH46 for evaluation of TMP86C846/H46, the program is written by the serial PROM mode.

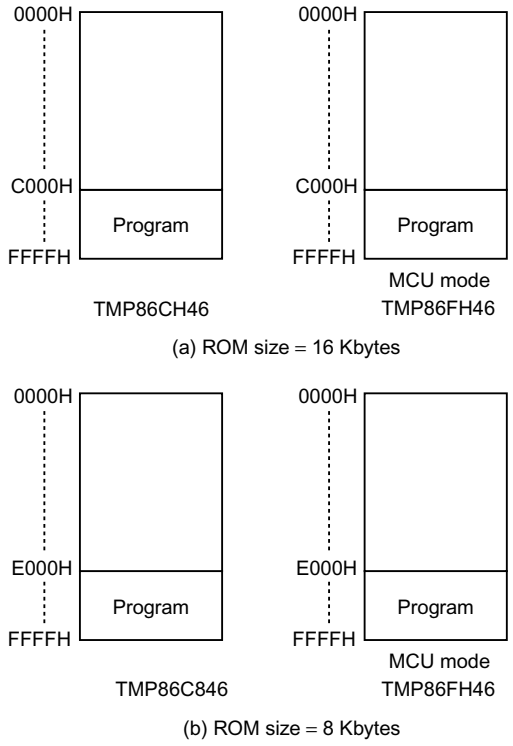


Figure 1.1.1 Program Memory Area

Note: The area that is not in use should be set data to FFH.

1.1.2 Data Memory

TMP86FH46 has a built-in 512-byte data memory (Static RAM).

1.1.3 Input/Output Circuitry

(1) Control pins

The control pins of the TMP86FH46 are the same as those of the TMP86C846/H46 except that the TEST pin does not have a built-in pull-down resistor.

(2) I/O ports

The I/O circuitries of TMP86FH46 I/O ports are the same as the those of TMP86C846/H46.

2. Serial PROM Mode

2.1 Outline

The TMP86FH46 has a 2-Kbyte BOOT ROM for programming to flash memory. This BOOT ROM is a mask ROM that contains a program to write the flash memory on-board. The BOOT ROM is available in a serial PROM mode and it is controlled by TEST pin and $\overline{\text{RESET}}$ pin and 2 I/O pins, and is communicated with UART. There are four operation modes in a serial PROM mode: flash memory writing mode, RAM loader mode, flash memory SUM output mode and product discrimination code output mode. Operating area of serial PROM mode differs from that of MCU mode. The operating area of serial PROM mode shows in Table 2.1.1.

Table 2.1.1 Operating Area of Serial PROM Mode

Parameter	Symbol	Min	Max	Unit
Operating voltage	V_{DD}	4.5	5.5	V
High frequency	fc	2, 4, 8, 16		MHz
Temperature	Topr	25 ± 5		°C

2.2 Memory Mapping

The BOOT ROM is mapped in address F800H to FFFFH. The BOOT ROM can't be accessed in MCU mode. The Figure 2.2.1 shows a memory mapping.

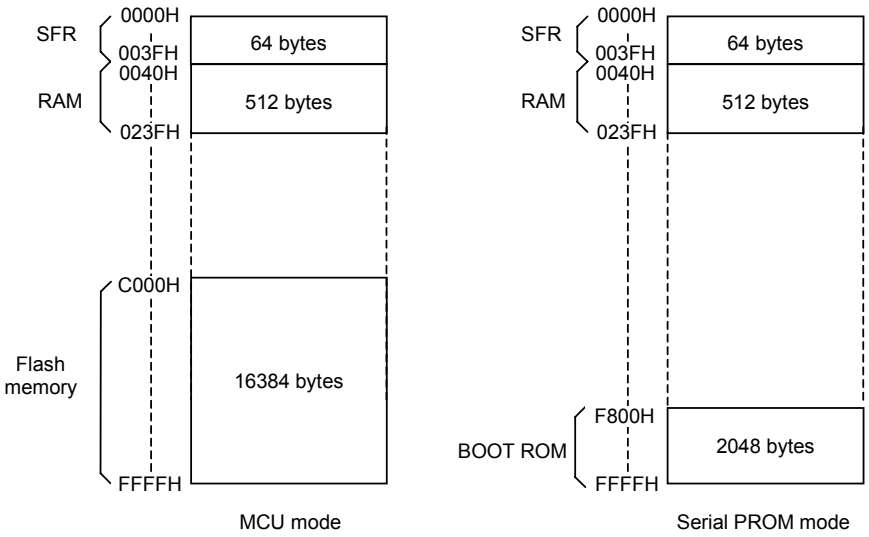


Figure 2.2.1 Memory Address Maps

2.3 Serial PROM Mode Setting

2.3.1 Serial PROM Mode Control Pins

To execute on-board programming, start the TMP86FH46 in serial PROM mode. Setting of a serial PROM mode is shown in Table 2.3.1.

Table 2.3.1 Serial PROM Mode Setting

Pin	Setting
TEST pin	High
BOOT1 (RXD) (Note)	High
BOOT2 (TXD) (Note)	High
$\overline{\text{RESET}}$ pin	↑

Note: BOOT1 is RXD pin and BOOT2 is TXD pin during a serial PROM mode.

2.3.2 Pin Function

In the serial PROM mode, TXD (P11) and RXD (P10) pins are used as a serial interface pin. Therefore, if the programming is executed on-board after mounting, these pins should be released from the other devices for communication in serial PROM mode.

Pin Name (Serial PROM mode)	Input/ Output	Functions	Pin Name (MCU mode)
BOOT1/RXD	Input/Input	Fix “High” during reset. This pin is used as RXD pin after releasing reset.	P10
BOOT2/TXD	Input/Output	Fix “High” during reset. This pin is used as TXD pin after releasing reset.	P11
TEST	Input	Fix to “High”.	
$\overline{\text{RESET}}$	I/O	Reset signal input or an internal error reset output.	
VDD, AVDD	Power supply	5 V	
VSS, AVSS, VAREF		0 V	
P07 to P00, P15 to P12, P22 to P20, P37 to P30, P47 to P40		Fix to “low” or “high”.	
XIN	Input	Self oscillation with resonator (2 MHz, 4 MHz, 8 MHz, 16 MHz)	
XOUT	Output		

Note: When the device is used as on-board writing and other parts are already mounted in place, be careful not to affect these communication control pins.

To set a serial PROM mode, connect device pins as shown in Figure 2.3.1.

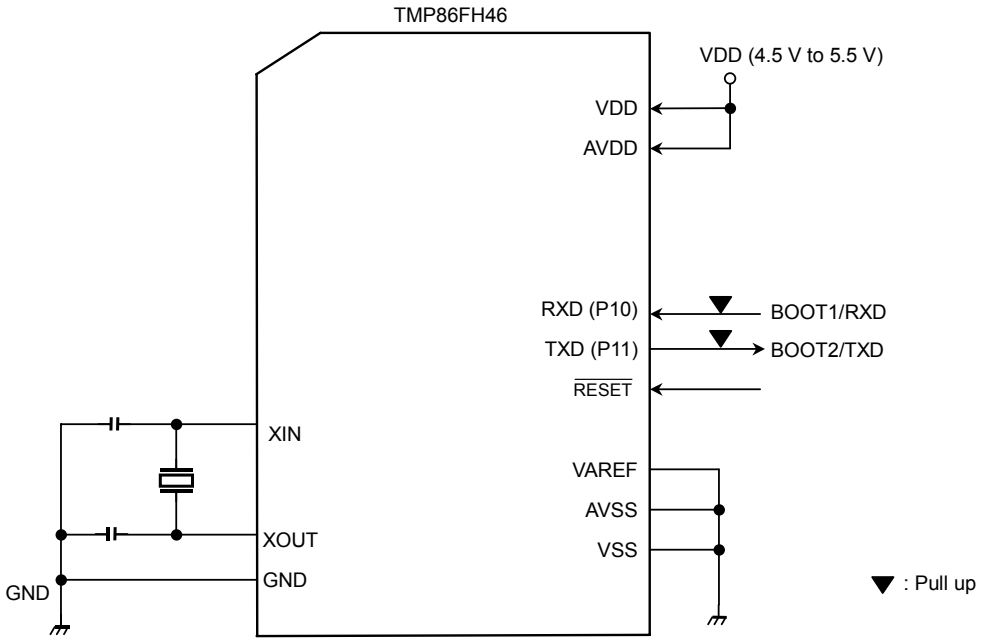


Figure 2.3.1 Serial PROM Mode Port Setting

2.3.3 Activating Serial PROM Mode

The following is a procedure of setting of serial PROM mode. Figure 2.3.2 shows a serial PROM mode timing.

(1) Turn on the power to the VDD pin.

(2) Set the $\overline{\text{RESET}}$ to low level.

(3) Set the TEST, BOOT1 and BOOT2 pin to high level.

(4) Wait until the power supply and clock sufficiently stabilize.

(5) Release the $\overline{\text{RESET}}$ (Set to high level).

(6) Input a matching data (5AH) to BOOT1/RXD pin after waiting for setup sequence. For details of the setup timing, refer to 2.14 “UART Timing”.

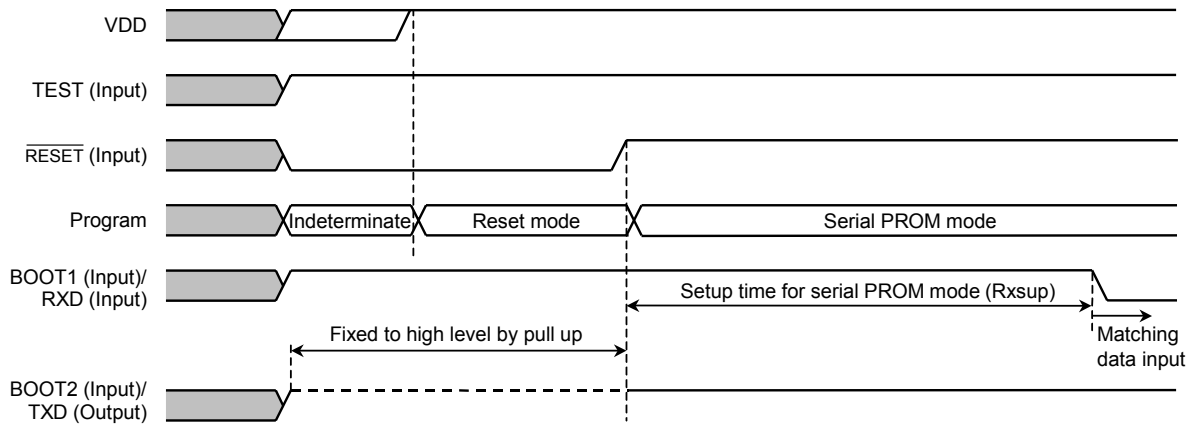


Figure 2.3.2 Serial PROM Mode Timing

2.4 Interface Specifications for UART

The following shows the UART communication format used in serial PROM mode.

Before on-board programming can be executed, the communication format on the external controller side must also be setup in the same way as for this product.

Note that although the default baud rate is 9,600 bps, it can be changed to other values as shown in Table 2.4.1. The Table 2.4.2 shows an operating frequency and baud rate in serial PROM mode. Except frequency which is not described in Table 2.4.2 can not use in serial PROM mode.

Baud rate (Default): 9,600 bps
Data length: 8 bits
Parity addition: None
Stop bit length: 1 bit

Table 2.4.1 Baud Rate Modification Data

Baud Rate Modification Data	05H	07H	0AH	18H	28H
Baud Rate (bps)	62500	38400	31250	19200	9600

Table 2.4.2 Operating Frequency and Baud Rate in Serial PROM Mode

Reference Baud Rate (Baud)	62500		38400		31250		19200		9600	
Baud Rate Modification Data	05H		07H		0AH		18H		28H	
Reference Frequency (MHz)	(bps)	(%)	(bps)	(%)	(bps)	(%)	(bps)	(%)	(bps)	(%)
2	–	–	–	–	–	–	–	–	9615	+0.16
4	–	–	–	–	31250	0.00	19231	+0.16	9615	+0.16
8	62500	0.00	38462	+0.16	31250	0.00	19231	+0.16	9615	+0.16
16	62500	0.00	38462	+0.16	31250	0.00	19231	+0.16	9615	+0.16

Note: "Reference Frequency" shows the high-frequency area supported in serial PROM mode. Except the above frequency can not be supported in serial PROM mode.

2.5 Command

There are five commands in serial PROM mode. After reset release, the TMP86FH46 waits a matching data (5AH).

Table 2.5.1 Command in Serial PROM Mode

Command Data	Operation Mode	Remarks
5AH	Setup	Matching data. Always start with this command after reset release.
30H	Flash memory writing	Writing to area from C000H to FFFFH is enable.
60H	RAM loader	Writing to area from 0050H to 0230H is enable.
90H	Flash memory SUM output	The checksum of entire flash memory area (from C000H to FFFFH) is output in order of the upper byte and the lower byte.
C0H	Product discrimination code output	Product discrimination code, that is expressed by 13 bytes data, is output.

2.6 Operation Mode

There are four operating modes in serial PROM mode: Flash memory writing mode, RAM loader mode, flash memory SUM output mode and product discrimination code output mode. For details about these modes, refer to (1) Flash memory writing mode through (4) Product discrimination code output mode.

(1) Flash memory writing mode

The data are written to the specified flash memory addresses. The controller should send the write data in the Intel Hex format (Binary). For details of writing data format, refer to 2.7 “Flash Memory Writing Data Format”.

If no errors are encountered till the end record, the SUM of 16 Kbytes of flash memory is calculated and the result is returned to the controller.

To execute the flash memory writing mode, the TMP86FH46 checks the passwords except a blank product. If the passwords did not match, the program is not executed.

(2) RAM loader mode

The RAM loader transfers the data into the internal RAM that has been sent from the controller in Intel Hex format. When the transfer has terminated normally, the RAM loader calculates the SUM and sends the result to the controller before it starts executing the user program. After sending of SUM, the program jumps to the start address of RAM in which the first transferred data has been written. This RAM loader function provides the user's own way to control on-board programming.

To execute the RAM loader mode, the TMP86FH46 checks the passwords except a blank product. If the passwords did not match, the program is not executed.

(3) Flash memory SUM output mode

The SUM of 16 Kbytes of flash memory is calculated and the result is returned to the controller.

The BOOT ROM does not support the reading function of the flash memory. Instead, it has this SUM command to use. By reading the SUM, it is possible to manage Revisions of application programs.

(4) Product discrimination code output mode

The product discrimination code is output as a 13-byte data, that includes the start address and the end address of ROM. (In case of TMP86FH46, the start address is C000H and the end address is FFFFH.) Therefore, the controller can recognize the device information by using this function.

2.6.1 Flash Memory Writing Mode (Operation command: 30H)

Table 2.6.1 shows flash memory writing mode process.

Table 2.6.1 Flash Memory Writing Mode Process

	Number of Bytes Transferred	Transfer Data from External Controller to TMP86FH46	Baud Rate	Transfer Data from TMP86FH46 to External Controller
BOOT ROM	1st byte 2nd byte	Matching data (5AH) –	9600 bps 9600 bps	– (Baud rate auto set) OK: Echo back data (5AH) Error: Nothing transmitted
	3rd byte 4th byte	Baud rate modification data (See Table 2.4.1) –	9600 bps 9600 bps	– OK: Echo back data Error: A1H × 3, A3H × 3, 62H × 3 (Note 1)
	5th byte 6th byte	Operation command data (30H) –	Changed new baud rate Changed new baud rate	– OK: Echo back data (30H) Error: A1H × 3, A3H × 3, 63H × 3 (Note 1)
	7th byte 8th byte	Address 15 to 08 in which to store Password count (Note 4)	Changed new baud rate Changed new baud rate	– OK: Nothing transmitted Error: A1H × 3, A3H × 3 (Note 1)
	9th byte 10th byte	Address 07 to 00 in which to store Password count (Note 4)	Changed new baud rate Changed new baud rate	– OK: Nothing transmitted Error: A1H × 3, A3H × 3 (Note 1)
	11th byte 12th byte	Address 15 to 08 in which to start Password comparison (Note 4)	Changed new baud rate Changed new baud rate	– OK: Nothing transmitted Error: A1H × 3, A3H × 3 (Note 1)
	13th byte 14th byte	Address 07 to 00 in which to start Password comparison (Note 4)	Changed new baud rate Changed new baud rate	– OK: Nothing transmitted Error: A1H × 3, A3H × 3 (Note 1)
	15th byte : m'th byte	Password string (Note 5) –	Changed new baud rate Changed new baud rate	– OK: Nothing transmitted Error: A1H × 3, A3H × 3 (Note 1)
	m'th + 1 byte : n'th – 2 byte	Extended Intel format (Binary) (Note 2, 6)	Changed new baud rate	–
	n'th – 1 byte	–	Changed new baud rate	OK: SUM (High) (Note 3) Error: Nothing transmitted
	n'th byte	–	Changed new baud rate	OK: SUM (Low) (Note 3) Error: Nothing transmitted
	n'th + 1 byte	(Wait for the next operation) (Command data)	Changed new baud rate	–

Note 1: "xxH × 3" denotes that operation stops after sending 3 bytes of xxH. For details, refer to 2.8 "Error Code".

Note 2: Refer to 2.10 "Intel Hex Format (Binary)".

Note 3: Refer to 2.9 "Checksum (SUM)".

Note 4: Refer to 2.11 "Passwords".

Note 5: If all data of vector area are "00H" or "FFH", the passwords comparison is not executed because the device is considered as blank product. However, it is necessary to specify the password count storage addresses and the password comparison start address even though it is a blank product. If a password error occurs, the UART function of TMP86FH46 stops without returning error code to the controller. Therefore, when a password error occurs, the TMP86FH46 should be reset by $\overline{\text{RESET}}$ pin input.

Note 6: The time between data records needs over 1 ms.

Description of flash memory writing mode

1. The receive data in the 1st byte is the matching data. When the boot program starts in serial PROM mode, TMP86FH46 (Mentioned as "device" hereafter) waits for the matching data (5AH) to receive. Upon receiving the matching data, it automatically adjusts the UART's initial baud rate to 9,600bps.
2. When the device has received the matching data, the device transmits the data "5AH" as an echo back to the controller. If the device can not receive the matching data, the device does not transmit the echo back data and waits for the matching data again with changing baud rate. Therefore, the controller should send the matching data continuously until the device transmits the echo back data.
3. The receive data in the 3rd byte is the baud rate modification data. The six kinds of baud rate modification data shown in Table 2.4.1 are available. Even if baud rate changing is no need, be sure to send the initial baud rate data (28H: 9,600 bps). The changing of baud rate is executed after transmitting the echo back data.
4. When the 3rd byte data is one of the baud rate modification data corresponding to the device's operating frequency, the device sends the echo back data which is the same as received baud rate modification data. Then the baud rate is changed. If the 3rd byte data does not correspond to the baud rate modification data, the device stops UART function after sending 3 bytes of baud rate modification error code: (62H).
5. The receive data in the 5th byte is the command data (30H) to write the flash memory.
6. When the 5th byte is one of the operation command data shown in Table 2.5.1, the device sends the echo back data which is the same as received operation command data (in this case, 30H). If the 5th byte data does not correspond to the operation command data, the device stops UART function after sending 3 bytes of operation command error code: (63H).
7. The 7th byte is used as an upper bit (Bit15 to bit8) of the password count storage address. When the receiving is executed correctly (No error), the device does not send any data. If the receiving error occurs, the device stops UART function after sending 3 bytes of receiving error code: (A1H or A3H).
8. The 9th byte is used as a lower bit (Bit7 to bit0) of the password count storage address. When the receiving is executed correctly (No error), the device does not send any data. If the receiving error occurs, the device stops UART function after sending 3 bytes of receiving error code: (A1H or A3H).
9. The 11th byte is used as an upper bit (Bit15 to bit8) of the password comparison start address. When the receiving is executed correctly (No error), the device does not send any data. If the receiving error occurs, the device stops UART function after sending 3 bytes of receiving error code: (A1H or A3H).
10. The 13th byte is used as a lower bit (Bit7 to bit0) of the password comparison start address. When the receiving is executed correctly (No error), the device does not send any data. If the receiving error occurs, the device stops UART function after sending 3 bytes of receiving error code: (A1H or A3H).
11. The 15th through the m'th bytes are the password data. The number of passwords is the data (N) indicated by the password count storage address. The password data are compared for N entries beginning with the password comparison start address. The controller should send N bytes of password data to the device. If the passwords do not match, the device stops UART function without returning error code to the controller. If the data of vector addresses (FFE0H to FFFFH) are all "FFH", the comparison of passwords is not executed because the device is considered as a blank product.

12. The receive data in the m'th + 1 through n'th – 2 byte are received as binary data in Intel Hex format. No received data are echoed back to the controller. The data which is not the start mark (3AH for ":") in Intel Hex format is ignored and does not send an error code to the controller until the device receives the start mark. After receiving the start mark, the device receives the data record, that consists of length of data, address, record type, writing data and checksum. After receiving the checksum of data record, the device waits the start mark data (3AH) again. The data of data record is temporarily stored to RAM and then, is written to specified flash memory by page (32 bytes) writing. For details of an organization of flash memory, refer to 2. "Serial PROM Mode". Since after receiving an end record, the device starts to calculate the SUM, the controller should wait the SUM after sending the end record. If receive error or Intel Hex format error occurs, the device stops UART function without returning error code to the controller.
13. The n'th – 1 and the n'th bytes are the SUM value that is sent to the controller in order of the upper byte and the lower byte. For details on how to calculate the SUM, refer to 2.9 "Checksum (SUM)". The SUM calculation is performed after detecting the end record, but the calculation is not executed when receive error or Intel Hex format error has occurred. The time required to calculate the SUM of the 16 Kbytes of flash memory area is approximately 100 ms at fc = 16 MHz. After the SUM calculation, the device sends the SUM data to the controller. After sending the end record, the controller can judge that the transmission has been terminated correctly by receiving the checksum.
14. After sending the SUM, the device waits for the next operation command data.

2.6.2 RAM Loader Mode (Operation command: 60H)

Table 2.6.2 shows RAM loader mode process.

Table 2.6.2 RAM Loader Mode Process

	Number of Bytes Transferred	Transfer Data from External Controller to TMP86FH46	Baud Rate	Transfer Data from TMP86FH46 to External Controller
BOOT ROM	1st byte	Matching data (5AH)	9600 bps	– (Baud rate auto set)
	2nd byte	–	9600 bps	OK: Echo back data (5AH) Error: Nothing transmitted
	3rd byte	Baud rate modification data (See Table 2.4.1)	9600 bps	–
	4th byte	–	9600 bps	OK: Echo back data Error:A1H × 3, A3H × 3, 62H × 3 (Note 1)
	5th byte	Operation command data (60H)	Changed new baud rate	–
	6th byte	–	Changed new baud rate	OK: Echo back data (60H) Error: A1H × 3, A3H × 3, 63H × 3 (Note 1)
	7th byte	Address 15 to 08 in which to store Password count (Note 4)	Changed new baud rate	–
	8th byte		Changed new baud rate	OK: Nothing transmitted Error: A1H × 3, A3H × 3 (Note 1)
	9th byte	Address 07 to 00 in which to store Password count (Note 4)	Changed new baud rate	–
	10th byte		Changed new baud rate	OK: Nothing transmitted Error: A1H × 3, A3H × 3 (Note 1)
	11th byte	Address 15 to 08 in which to start Password comparison (Note 4)	Changed new baud rate	–
	12th byte		Changed new baud rate	OK: Nothing transmitted Error: A1H × 3, A3H × 3 (Note 1)
	13th byte	Address 07 to 00 in which to start Password comparison (Note 4)	Changed new baud rate	–
	14th byte		Changed new baud rate	OK: Nothing transmitted Error: A1H × 3, A3H × 3 (Note 1)
	15th byte	Password string (Note 5)	Changed new baud rate	–
	:			
	m'th byte	–	Changed new baud rate	OK: Nothing transmitted Error: A1H × 3, A3H × 3 (Note 1)
	m'th + 1 byte	Extended Intel format (Binary) (Note 2)	Changed new baud rate	–
	:			
	n'th – 2 byte			
	n'th – 1 byte	–	Changed new baud rate	OK: SUM (High) (Note 3) Error: Nothing transmitted
	n'th byte	–	Changed new baud rate	OK: SUM (Low) (Note 3) Error: Nothing transmitted
RAM	–	The program jumps to the start address of RAM in which the first transferred data has been written.		

Note 1: "xxH × 3" denotes that operation stops after sending 3 bytes of xxH. For details, refer to 2.8 "Error Code".

Note 2: Refer to 2.10 "Intel Hex Format (Binary)".

Note 3: Refer to 2.9 "Checksum (SUM)".

Note 4: Refer to 2.11 "Passwords".

Note 5: If all data of vector area are “00H” or “FFH”, the passwords comparison is not executed because the device is considered as blank product. However, it is necessary to specify the password count storage addresses and the password comparison start address even though it is a blank product. If a password error occurs, the UART function of TMP86FH46 stops without returning error code to the controller. Therefore, when a password error occurs, the TMP86FH46 should be reset by $\overline{\text{RESET}}$ pin input.

Note 6: Do not send only end record after transferring of password string. If the TMP86FH46 receives the end record only after reception of password string, it does not operate correctly.

Description of RAM loader mode

1. The process of the 1st byte through the 4th byte are the same as flash memory writing mode.
2. The receive data in the 5th byte is the RAM loader command data (60H) to write the user’s program to RAM.
3. When the 5th byte is one of the operation command data shown in Table 2.5.1, the device sends the echo back data which is the same as received operation command data (in this case, 60H). If the 5th byte data does not correspond to the operation command data, the device stops UART function after sending 3 bytes of operation command error code: (63H).
4. The process of the 7th byte through the m’th byte are the same as flash memory writing mode.
5. The receive data in the m’th + 1 through n’th – 2byte are received as binary data in Intel Hex format. No received data are echoed back to the controller.
   The data which is not the start mark (3AH for “:”) in Intel Hex format is ignored and does not send an error code to the controller until the device receives the start mark. After receiving the start mark, the device receives the data record, that consists of length of data, address, record type, writing data and checksum. After receiving the checksum of data record, the device waits the start mark data (3AH) again. The data of data record is written to specified RAM by the receiving data. Since after receiving an end record, the device starts to calculate the SUM, the controller should wait the SUM after sending the end record. If receive error or Intel Hex format error occurs, the UART function of TMP86FH46 stops without returning error code to the controller.
6. The n’th – 1 and the n’th bytes are the SUM value that is sent to the controller in order of the upper byte and the lower byte. For details on how to calculate the SUM, refer to 2.9 “Checksum (SUM)”. The SUM calculation is performed after detecting the end record, but the calculation is not executed when receive error or Intel Hex format error has occurred.
   The SUM is calculated by the data written to RAM, but the length of data, address, record type and checksum in Intel Hex format are not included in SUM.
7. The boot program jumps to the first address that is received as data in Intel Hex format after sending the SUM to the controller.

2.6.3 Flash Memory Memory SUM Output Mode (Operation command: 90H)

Table 2.6.3 shows flash memory SUM output mode process.

Table 2.6.3 Flash Memory Memory SUM Output Process

	Number of Bytes Transferred	Transfer Data from External Controller to TMP86FH46	Baud Rate	Transfer Data from TMP86FH46 to External Controller
BOOT ROM	1st byte	Matching data (5AH)	9600 bps	– (Baud rate auto set)
	2nd byte	–	9600 bps	OK: Echo back data (5AH) Error: Nothing transmitted
	3rd byte	Baud rate modification data (See Table 2.4.1)	9600 bps	–
	4th byte	–	9600 bps	OK: Echo back data Error: A1H × 3, A3H × 3, 62H × 3 (Note 1)
	5th byte	Operation command data (90H)	Changed new baud rate	–
	6th byte	–	Changed new baud rate	OK: Echo back data (90H) Error: A1H × 3, A3H × 3, 63H × 3 (Note 1)
	7th byte	–	Changed new baud rate	OK: SUM (High) (Note 2) Error: Nothing transmitted
	8th byte	–	Changed new baud rate	OK: SUM (Low) (Note 2) Error: Nothing transmitted
	9th byte	(Wait for the next operation) (Command data)	Changed new baud rate	–

Note 1: "xxH × 3" denotes that operation stops after sending 3 bytes of xxH. For details, refer to 2.8 "Error Code".

Note 2: Refer to 2.9 "Checksum (SUM)"

Description of flash memory SUM output mode

1. The process of the 1st byte through the 4th byte are the same as flash memory writing mode.
2. The receive data in the 5th byte is the flash memory SUM command data (90H) to calculate the entire flash memory.
3. When the 5th byte is one of the operation command data shown in Table 2.5.1, the device sends the echo back data which is the same as received operation command data (in this case, 90H). If the 5th byte data does not correspond to the operation command data, the device stops UART function after sending 3 bytes of operation command error code: (63H).
4. The 7th and the 8th bytes are the SUM value that is sent to the controller in order of the upper byte and the lower byte. For details on how to calculate the SUM, refer to 2.9 "Checksum (SUM)".
5. After sending the SUM, the device waits for the next operation command data.

2.6.4 Product Discrimination Code Output Mode (Operation command: C0H)

Table 2.6.4 shows product discrimination code output mode process.

Table 2.6.4 Product Discrimination Code Output Process

	Number of Bytes Transferred	Transfer Data from External Controller to TMP86FH46	Baud Rate	Transfer Data from TMP86FH46 to External Controller	
BOOT ROM	1st byte	Matching data (5AH)	9600 bps	– (Baud rate auto set)	
	2nd byte	–	9600 bps	OK: Echo back data (5AH) Error: Nothing transmitted	
	3rd byte	Baud rate modification data (See Table 2.4.1)	9600 bps	–	
	4th byte	–	9600 bps	OK: Echo back data Error: A1H × 3, A3H × 3, 62H × 3 (Note 1)	
	5th byte	Operation command data (C0H)	Changed new baud rate	–	
	6th byte	–	Changed new baud rate	OK: Echo back data (C0H) Error: A1H × 3, A3H × 3, 63H × 3 (Note 1)	
	7th byte		Changed new baud rate	3AH	Start mark
	8th byte		Changed new baud rate	0AH	The number of transfer data (from 9th to 18th byte)
	9th byte		Changed new baud rate	02H	Length of address (2 bytes)
	10th byte		Changed new baud rate	03H	Reserved data
	11th byte		Changed new baud rate	00H	Reserved data
	12th byte		Changed new baud rate	00H	Reserved data
	13th byte		Changed new baud rate	00H	Reserved data
	14th byte		Changed new baud rate	01H	The number of ROM block (1 block)
	15th byte		Changed new baud rate	C0H	First address of ROM (Upper 8 bits)
	16th byte		Changed new baud rate	00H	First address of ROM (Lower 8 bits)
	17th byte		Changed new baud rate	FFH	End address of ROM (Upper 8 bits)
	18th byte		Changed new baud rate	FFH	End address of ROM (Lower 8 bits)
	19th byte		Changed new baud rate	3CH	Checksum of transferred data (from 9th to 18th byte)
	20th byte	(Wait for the next operation) (Command data)	Changed new baud rate	–	

Note: "xxH × 3" denotes that operation stops after sending 3 bytes of xxH. For details, refer to 2.8 "Error Code".

Description of product discrimination code output mode

1. The process of the 1st byte through the 4th byte are the same as flash memory writing mode.
2. The receive data in the 5th byte is the product discrimination code output command data (C0H).
3. When the 5th byte is one of the operation command data shown in Table 2.5.1, the device sends the echo back data which is the same as received operation command data (in this case, C0H). If the 5th byte data does not correspond to the operation command data, the device stops UART function after sending 3 bytes of operation command error code: (63H).
4. The 7th and the 19th bytes are the product discrimination code. For details, refer to 2.12 "Product Discrimination Code".
5. After sending the SUM, the device waits for the next operation command data.

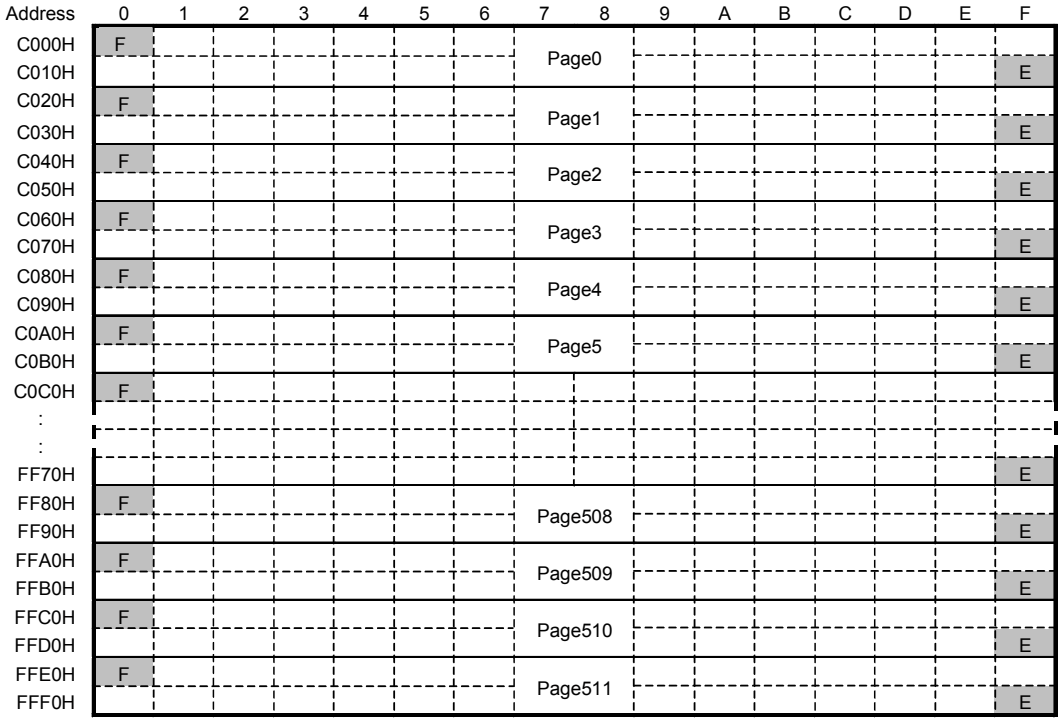
2.7 Flash Memory Writing Data Format

Flash memory area of TMP86FH46 consists of 512 pages and one page size is 32 bytes.

Writing to flash memory is executed by page writing. Therefore, it is necessary to send 32 bytes data (for one page) even though only a few bytes data are written. Figure 2.7.1 shows an organization of flash memory area. When the controller sends the writing data to the device, be sure to keep the format described below.

1. The address of data after receiving the flash memory writing command should be the first address of page. For example, in case of page 2, the first address should be C040H.
2. If the last data's address of data record is not end address of page, the address of the next data record should be the address + 1 and the last data's address must point to the last address of this page. For example, if the last data's address is C00FH (Page0), the address of the next data record should be C010H (Page0) and the address of the last data should be C01FH (Page0).
3. The last data's address of data record immediately before sending the end record should be the last address of page. For example, in case of page 1, the last data's address of data record should be C03FH.

Note: Do not write only the vector area (FFF0H to FFFFH) when all data of flash memory are the same data. If the vector area is only written, the next operation can not be executed because of password error.



Note: "F" shows the first address of each page and "E" shows the last address of each page.

Figure 2.7.1 Organization of Flash Memory Area

2.8 Error Code

When the device detects an error, the error codes are sent to the controller.

Table 2.8.1 Error Code

Transmit Data	Meaning of Transmit Data
62H, 62H, 62H	Baud rate modification error occurred.
63H, 63H, 63H	Operating command error occurred.
A1H, A1H, A1H	Framing error in received data occurred.
A3H, A3H, A3H	Overrun error in received data occurred.

2.9 Checksum (SUM)

(1) Calculation method

SUM consists of byte + byte.... + byte, the checksum of which is returned in word as the result.

Namely, data is read out in byte and checksum of which is calculated, with the result returned in word.

Example:

A1H
B2H
C3H
D4H

If the data to be calculated consists of the four bytes shown to the left, SUM of the data is

A1H + B2H + C3H + D4H = 02EAH
SUM (HIGH) = 02H
SUM (LOW) = EAH

The SUM returned when executing the flash memory write command, RAM loader command, or flash memory SUM command is calculated in the manner shown above.

(2) Calculation data

The data from which SUM is calculated are listed in Table 2.9.1 below.

Table 2.9.1 Checksum Calculation Data

Operating Mode	Calculation Data	Remarks
Flash memory writing mode	Data in the entire area (16 Kbytes) of flash memory	Even when written to part of the flash memory area, data in the entire memory area (16 Kbytes) is calculated. The length of data, address, record type and checksum in Intel Hex format are not included in SUM.
Flash memory Checksum output mode		
RAM loader mode	Data written to RAM	The length of data, address, record type and checksum in Intel Hex format are not included in SUM.

2.10 Intel Hex Format (Binary)

1. After receiving the SUM of a record, the device waits for the start mark data (3AH for ":") of the next record. Therefore, the device ignores the data, which does not match the start mark data after receiving the SUM of a record.
2. Make sure that once the controller program has finished sending the SUM of the end record, it does not send anything and waits for two bytes of data to be received (Upper and lower bytes of SUM). This is because after receiving the SUM of the end record, the boot program calculates the SUM and returns the calculated SUM in two bytes to the controller.
3. If a receive error or Intel Hex format error occurs, the UART function of TMP86FH46 stops without returning error code to the controller. In the following cases, an Intel Hex format error occurs:
   - When the record type is not 00H, 01H, or 02H
   - When a SUM error occurred
   - When the data length of an extended record (Type = 02H) is not 02H
   - When the address of an extended record (Type = 02H) is larger than 1000H and after that, receives the data record
   - When the data length of the end record (Type = 01H) is not 00H

2.11 Passwords

The area in which passwords can be specified is located at addresses C000H to FF9FH. The vector area (from FFF0H to FFFFH) can not be specified as passwords area. The device compares the stored passwords with the passwords, which are received from the controller. If all data of vector area are "00H" or "FFH", the passwords comparison is not executed because the device is considered as blank product. It is necessary to specify the password count storage addresses and the password comparison start address even though it is a blank product.

1. Password count storage addresses (PNSA).

   The content of the address specified by PNSA is the password count (N). In the following cases, a password error occurs:

   - PNSA < address C000H
   - Address FF9F < PNSA
   - N < 8

   Note: If it is considered as a blank product, the comparison of N < 8 is not executed.

2. Password comparison start address (PCSA)

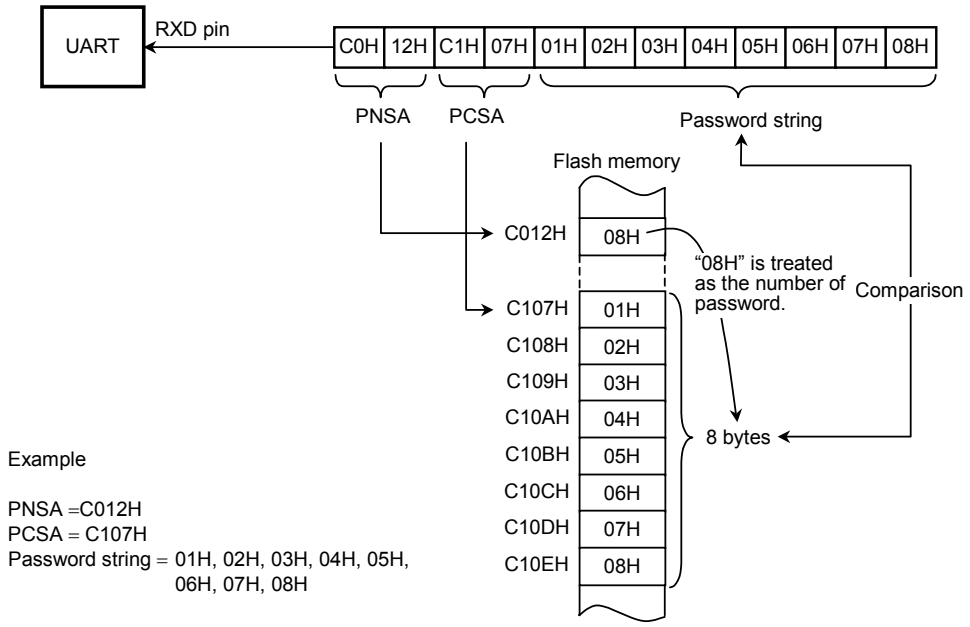
   The passwords are compared beginning with the address specified by PCSA. The specified password area is from PCSA to PCSA + N – 1. In the following cases, a password error occurs:

   - PCSA < address C000H
   - Address FF9FH < PCSA + N – 1
   - When the specified password area contains three or more consecutive bytes of the same data

3. Password string

A string of passwords in the received data are compared with the data in the flash memory. In the following cases, a password error occurs:

- When the received data does not match the data in the flash memory



4. Handling of password error

If a password error occurs, the UART function of TMP86FH46 stops without returning error code to the controller. Therefore, when a password error occurs, the TMP86FH46 should be reset by $\overline{\text{RESET}}$ pin input.

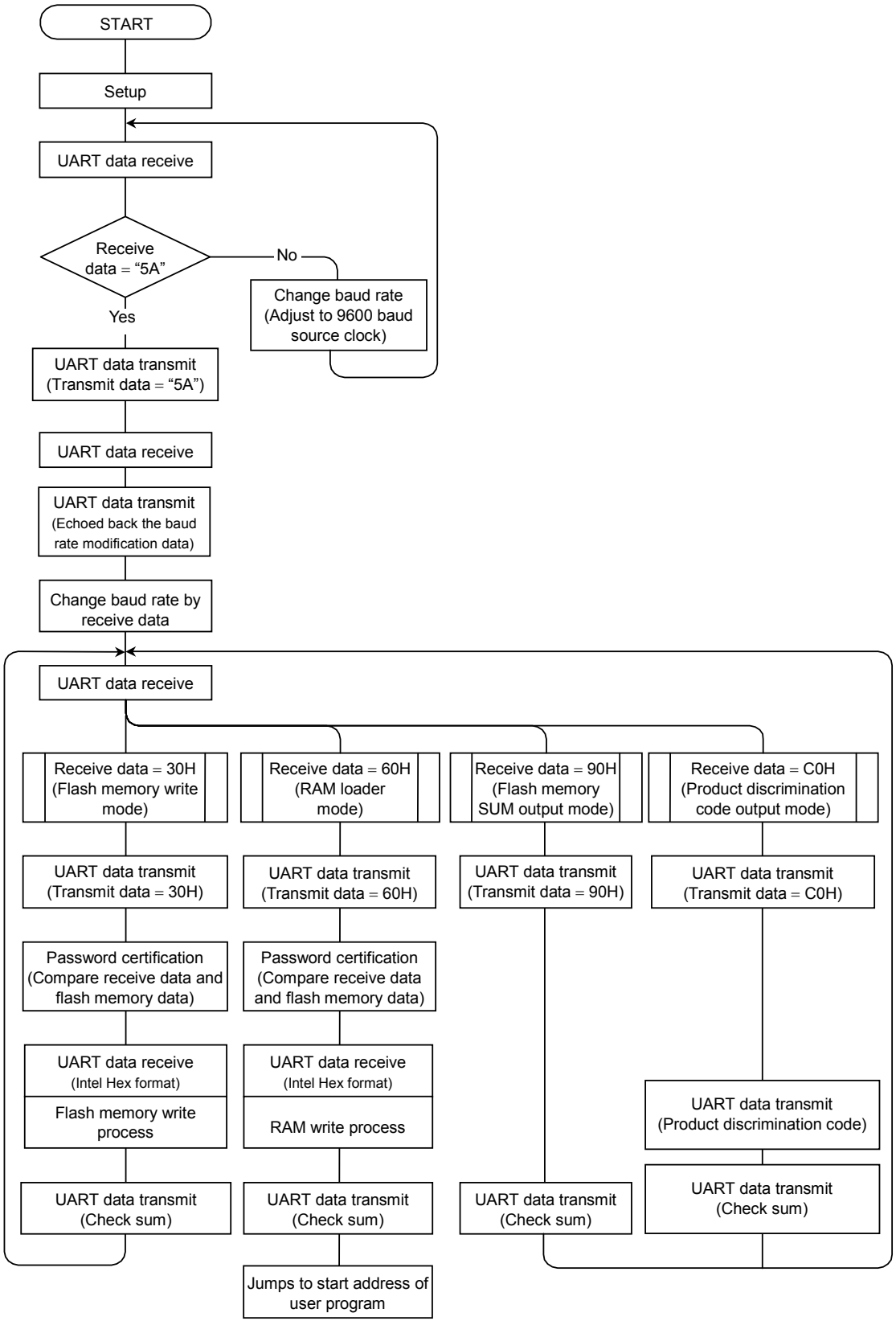
2.12 Product Discrimination Code

The product discrimination code is a 13-byte data, that includes the start address and the end address of ROM. Table 2.12.1 shows the product discrimination code format.

Table 2.12.1 Product Discrimination Code Format

Data	The Meaning of Data	In Case of TMP86FH46
1st	Start mark (3AH)	3AH
2nd	The number of transfer data (from 3rd to 13th byte)	0AH
3rd	Length of address	02H
4th	Reserved data	03H
5th	Reserved data	00H
6th	Reserved data	00H
7th	Reserved data	00H
8th	The number of ROM block	01H
9th	The upper byte of the first address of ROM	C0H (Depends on the product)
10th	The lower byte of the first address of ROM	00H (Depends on the product)
11th	The upper byte of the end address of ROM	FFH (Depends on the product)
12th	The lower byte of the end address of ROM	FFH (Depends on the product)
13th	Checksum of transferred data (from 3rd to 12th byte)	3CH (Depends on the product)

2.13 Flowchart



2.14 UART Timing

Table 2.14.1 UART Timing-1 (VDD = 4.5 V to 5.5 V, fc = 2 MHz, 4 MHz, 8 MHz, 16 MHz, Topr = 20 to 30°C)

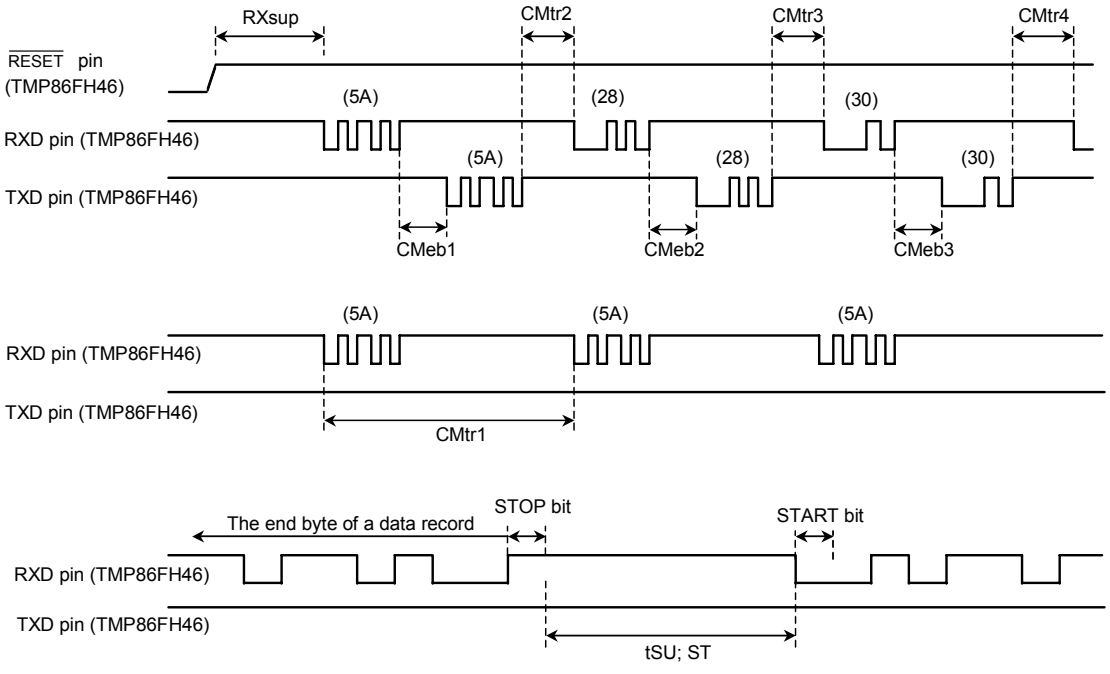
Parameter	Symbol	The Number of Clock (fc)	Required Minimum Time	
			At fc = 2 MHz	At fc = 16 MHz
Time from the reception of a matching data until the output of an echo back	CMeb1	Approx. 600	300 μs	37.5 μs
Time from the reception of a baud rate modification data until the output of an echo back	CMeb2	Approx. 500	250 μs	31.3 μs
Time from the reception of an operation command until the output of an echo back	CMeb3	Approx. 500	250 μs	31.3 μs
Calculation time of checksum	CKsm	Approx. 1573000	786.5 ms	98.3 ms

Table 2.14.2 UART Timing-2 (VDD = 4.5 V to 5.5 V, fc = 2 MHz, 4 MHz, 8 MHz, 16 MHz, Topr = 20 to 30°C)

Parameter	Symbol	The Number of Clock (fc)	Required Minimum Time	
			At fc = 2 MHz	At fc = 16 MHz
Time from reset release until acceptance of start bit of RXD pin	RXsup	25000	12.5 ms	1.56 ms
Time between a matching data and the next matching data	CMtr1	28500	14.3 ms	1.8 ms
Time from the echo back of matching data until the acceptance of baud rate modification data	CMtr2	400	200 μs	25 μs
Time from the output of echo back of baud rate modification data until the acceptance of an operation command	CMtr3	500	250 μs	31.3 μs
Time from the output of echo back of operation command until the acceptance of Password count storage addresses	CMtr4	2600	1.3 ms	163 μs

Table 2.14.3 UART Timing-3 (VDD = 4.5 V to 5.5 V, fc = 2 MHz, 4 MHz, 8 MHz, 16 MHz, Topr = 20 to 30°C)

Parameter	Symbol	Min.	Max.	Unit
Time from the stop bit of the previous data record to start bit of the next data record	tSU; ST	1	–	ms



Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Rating	Unit
Supply voltage	V_{DD}		−0.3 to 5.5	V
Input voltage	V_{IN}		−0.3 to V_{DD} + 0.3	
Output voltage	V_{OUT}		−0.3 to V_{DD} + 0.3	
Output current (Per 1 pin)	I_{OUT1} I_{OH}	P1, P3, P4 ports	−1.8	mA
	I_{OUT2} I_{OL}	P1, P3 ports	3.2	
	I_{OUT3} I_{OL}	P0, P2, P4 ports	30	
Output current (Total)	ΣI_{OUT1}	P1, P3 ports	60	
	ΣI_{OUT2}	P0, P2, P4 ports	80	
Power dissipation [Topr = 70°C]	PD		250	mW
Soldering temperature (time)	Tsld		260 (10 s)	°C
Storage temperature	Tstg		−55 to 125	
Operating temperature	Topr		−40 to 70 (MCU mode)	
			20 to 30 (Serial PROM mode)	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition

1) MCU mode (V_{SS} = 0 V, Topr = −40 to 70°C)

Parameter	Symbol	Pins	Condition		Min	Max	Unit
Supply voltage	V_{DD}		fc = 16 MHz	NORMAL1, 2 mode	4.5	5.5	V
				IDLE0, 1, 2 mode			
			fc = 8 MHz	NORMAL1, 2 mode	2.7		
				IDLE0, 1, 2 mode			
				STOP mode			
Input high level	V_{IH1}	Except hysteresis input	$V_{DD} \geq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input low level	V_{IL1}	Except hysteresis input	$V_{DD} \geq 4.5$ V		0	$V_{DD} \times 0.30$	
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V		1.0	16.0	MHz
			V_{DD} = 2.7 to 5.5 V			8.0	
	fs	XTIN, XTOUT			30.0	34.0	kHz

2) Serial PROM mode (V_{SS} = 0 V, Topr = 20 to 30°C)

Parameter	Symbol	Pins	Condition	Min	Max	Unit
Supply voltage	V_{DD}		fc = 2 MHz, 4 MHz, 8 MHz, 16 MHz	4.5	5.5	V
Input high level	V_{IH1}	Except hysteresis input	V_{DD} = 4.5 to 5.5 V	$V_{DD} \times 0.70$	V_{DD}	
	V_{IH2}	Hysteresis input		$V_{DD} \times 0.75$		
Input low level	V_{IL1}	Except hysteresis input	V_{DD} = 4.5 to 5.5 V	0	$V_{DD} \times 0.30$	
	V_{IL2}	Hysteresis input			$V_{DD} \times 0.25$	
Clock frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V	2.0, 4.0, 8.0, 16		MHz

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (Supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics (V_{SS} = 0 V, Topr = –40 to 70°C)

Parameter	Symbol	Pins	Condition		Min	Typ.	Max	Unit
Hysteresis voltage	V_{HS}	Hysteresis input			–	0.9	–	V
Input current	I_{IN1}	TEST	V_{DD} = 5.5 V, V_{IN} = 5.5/0 V		–	–	±2	μA
	I_{IN2}	Sink open drain, tri-state						
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$						
Input resistance	R_{IN2}	$\overline{RESET}$ pull up			100	200	450	kΩ
Output leakage current	I_{LO1}	Sink open drain	V_{DD} = 5.5 V, V_{OUT} = 5.5 V		–	–	2	μA
	I_{LO2}	Tri-state	V_{DD} = 5.5 V, V_{OUT} = 5.5/0 V		–	–	±2	
Output high voltage	V_{OH}	Tri-state	V_{DD} = 4.5 V, I_{OH} = –0.7 mA		4.1	–	–	V
Output low voltage	V_{OL}	Except XOUT, P0, P4 and P2 ports	V_{DD} = 4.5 V, I_{OL} = 1.6 mA		–	–	0.4	
Output low current	I_{OL}	High current port (P0, P2, P4 port)	V_{DD} = 4.5 V, V_{OL} = 1.0 V		–	20	–	mA
Supply current in NORMAL 1, 2 mode	I_{DD}		V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V fc = 16 MHz fs = 32.768 kHz		–	8.0	12.5	
Supply current in IDLE1, 2 mode					–	6.0	9.0	
Supply current in IDLE0 mode					–	4.5	9.0	
Supply current in SLOW1 mode			V_{DD} = 3.0 V V_{IN} = 2.8 V/0.2 V fs = 32.768 kHz	When a program operates on flash memory	–	300	600	μA
				When a program operates on RAM	–	8.0	27	
Supply current in SLEEP1 mode					–	7.0	25	
Supply current in SLEEP0 mode					–	6.0	24	
Supply current in STOP mode			V_{DD} = 5.0 V V_{IN} = 5.3 V/0.2 V		–	0.5	10	

Note 1: Typical values show those at Topr = 25°C, V_{DD} = 5 V.

Note 2: Input current (I_{IN3}); The current through pull-up resistor is not included.

Note 3: I_{DD} does not include I_{REF} current.

AD Conversion Characteristics (V_{SS} = 0 V, 4.5 V ≤ V_{DD} ≤ 5.5 V, Topr = –40 to 70°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage	V_{AREF}		A_{VDD} – 1.0	–	A_{VDD}	V
Power supply voltage of analog control circuit	A_{VDD}		V_{DD}			
Analog reference voltage range (Note 4)	ΔV_{AREF}		3.5	–	–	
Analog input voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power supply current of analog reference voltage	I_{REF}	$V_{DD} = A_{VDD} = V_{AREF}$ = 5.5 V $V_{SS} = A_{VSS}$ = 0.0 V	–	0.6	1.0	mA
Non linearity error		$V_{DD} = A_{VDD}$ = 5.0 V $V_{SS} = A_{VSS}$ = 0.0 V V_{AREF} = 5.0 V	–	–	±2	LSB
Zero point error			–	–	±2	
Full scale error			–	–	±2	
Total error			–	–	±2	

(V_{SS} = 0 V, 2.7 V ≤ V_{DD} < 4.5 V, Topr = –40 to 70°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage	V_{AREF}		A_{VDD} – 1.0	–	A_{VDD}	V
Power supply voltage of analog control circuit	A_{VDD}		V_{DD}			
Analog reference voltage range (Note 4)	ΔV_{AREF}		2.5	–	–	
Analog input voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power supply current of analog reference voltage	I_{REF}	$V_{DD} = A_{VDD} = V_{AREF}$ = 4.5V $V_{SS} = A_{VSS}$ = 0.0 V	–	0.5	0.8	mA
Non linearity error		$V_{DD} = A_{VDD}$ = 2.7 V V_{SS} = 0.0 V V_{AREF} = 2.7 V	–	–	±2	LSB
Zero point error			–	–	±2	
Full scale error			–	–	±2	
Total error			–	–	±2	

Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.

Note 2: Conversion time is different in recommended value by power supply voltage.
About conversion time, please refer to “10-Bit AD Converter”.

Note 3: Please use input voltage to AIN input pin in limit of $V_{AREF} - V_{SS}$.
When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.

Note 4: Analog reference voltage range: $\Delta V_{AREF} = V_{AREF} - V_{SS}$

Note 5: The A_{VDD} pin should be fixed on the V_{DD} level even though AD converter is not used.

AC Characteristics (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = –40 to 70°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine cycle time	tcy	NORMAL1, 2 mode	0.25	–	4	μs
		IDLE1, 2 mode				
		SLOW1, 2 mode	117.6	–	133.3	
		SLEEP1, 2 mode				
High level clock pulse width	twcH	For external clock operation (XIN input), fc = 16 MHz	–	31.25	–	ns
Low level clock pulse width	twcL					
High level clock pulse width	twcH	For external clock operation (XTIN input), fs = 32.768 kHz	–	15.26	–	μs
Low level clock pulse width	twcL					

(V_{SS} = 0 V, V_{DD} = 2.7 to 4.5 V, Topr = –40 to 70°C)

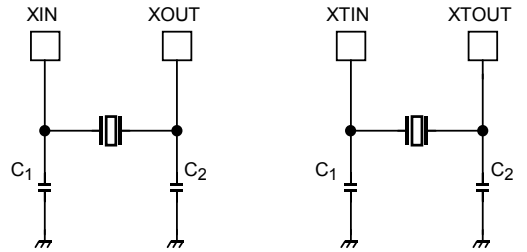
Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine cycle time	tcy	NORMAL1, 2 mode	0.5	–	4	μs
		IDLE1, 2 mode				
		SLOW1, 2 mode	117.6	–	133.3	
		SLEEP1, 2 mode				
High level clock pulse width	twcH	For external clock operation (XIN input), fc = 8 MHz	–	62.5	–	ns
Low level clock pulse width	twcL					
High level clock pulse width	twcH	For external clock operation (XTIN input), fs = 32.768 kHz	–	15.26	–	μs
Low level clock pulse width	twcL					

Recommended Oscillating Conditions-1 (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = –40 to 85°C)

Parameter	Oscillator	Oscillation Frequency	Recommened Oscillator		Recommended Constant C_1	Recommended Constant C_2
High-frequency Oscillation	Ceramic Resonator	16 MHz	MURATA	CSA16.00MXZ040	10 pF	10 pF
		8 MHz	MURATA	CSA8.00MTZ	30 pF	30 pF
				CST8.00MTW	30 pF (built-in)	30 pF (built-in)
		4.19 MHz	MURATA	CSA4.19MG	30 pF	30 pF
				CST4.19MGW	30 pF (built-in)	30 pF (built-in)
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	SII	VT-200	6 pF	6 pF

Recommended Oscillating Conditions-2 (V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = –40 to 85°C)

Parameter	Oscillator	Oscillation Frequency	Recommened Oscillator		Recommended Constant C_1	Recommended Constant C_2
High-frequency Oscillation	Ceramic Resonator	8 MHz	MURATA	CSA8.00MTZ	30 pF	30 pF
				CST8.00MTW	30 pF (built-in)	30 pF (built-in)
		4.19 MHz	MURATA	CSA4.19MG	30 pF	30 pF
				CST4.19MGW	30 pF (built-in)	30 pF (built-in)



High-frequency oscillation Low-frequency oscillation

Note 1: When using the device (Oscillator) in places exposed to high electric fields such as cathode-ray tubes, we recommend electrically shielding the package in order to maintain normal operating condition.

Note 2: To ensure stable oscillation, the resonator position, load capacitance, etc. must be appropriate. Because there factors are greatly affected by board patterns, please be sure to evaluate operation on the board on which the device will actually be mounted.

Note 3: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL: http://www.murata.co.jp/search/index.html