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ROCESSORS

16,384 BIT EPROM WITH I/O PORTS

N-CHANNEL SILICON GATE MOS

TMP8755AC

GENERAL DESCRIPTION

The TMP8755AC is an erasable and electrically reprogrammable ROM (EPROM) and I/O chip to be used in the TLCS-85A microcomputer system. The RPOM portion is organized as 2,048 words by 8 bits.

The I/O portion consists of two general purpose I/O ports. Each I/O port has eight port lines, and each I/O port line is individually programmable as input or output.

FEATURES

- U.V. Erasable and Electrically Reprogrammable ROM (2,048 x 8)
- Single +5V Power Supply (V_{CC})
- Internal Address Latch
- 2 General Purpose 8 bit I/O Ports
- Access Time: 450 ns (MAX.)
- Each I/O Port Line Individually Programmable as Input or Output
- Multiplexed Address and Data Bus
- 40 pin DIP
- Compatible with Intel's 8755A

PIN CONNECTIONS (TOP View)

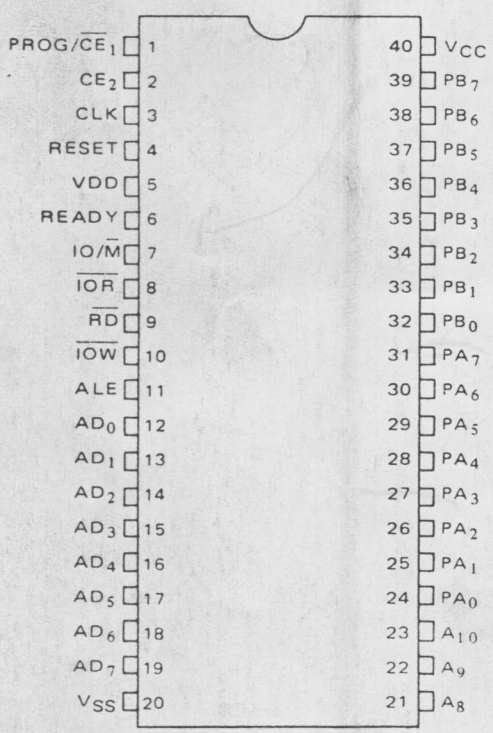


Fig. 1 TMP8755AC Pinout Diagram

BLOCK DIAGRAM

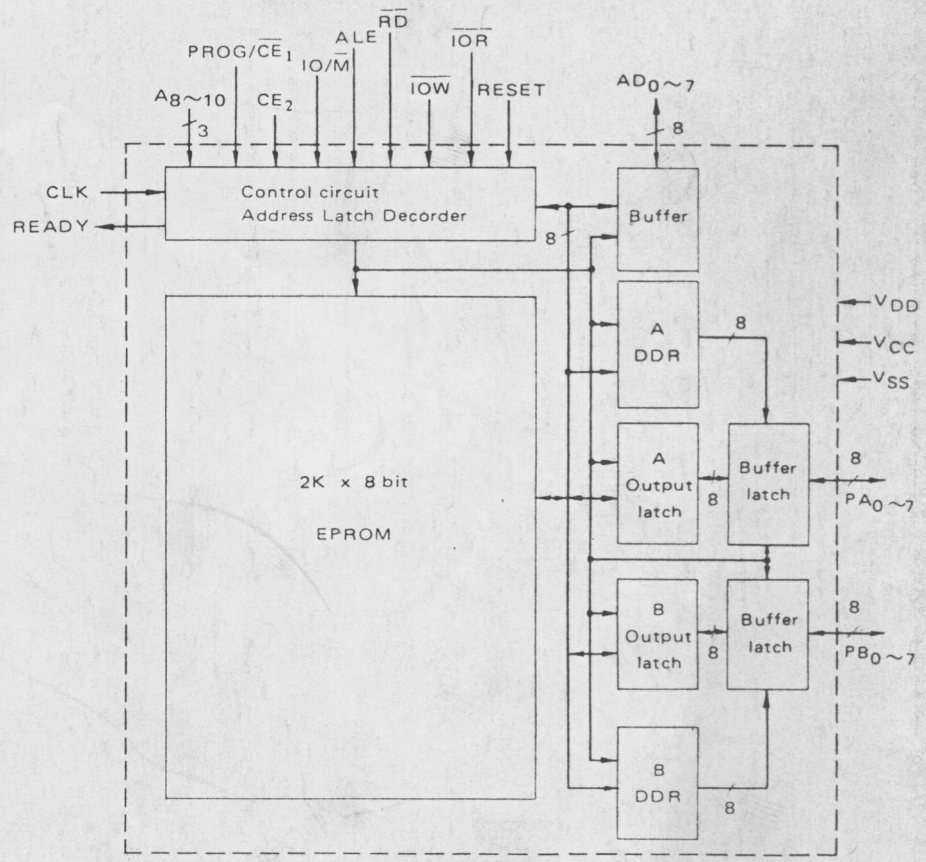


Fig. 2 TMP8755AC Functional Block Diagram

TOSHIBA

PIN NAMES AND PIN DESCRIPTION

ALE (Input)

When Address Latch Enable goes high, AD_{0-7}, $IO/\overline{M}$, A_{8-10}, CE_2, and $\overline{CE}_1$ enter the address latches. The signals (AD_{0-7}, $IO/\overline{M}$, A_{8-10}, CE) are latched in at the trailing edge of ALE.

AD_{0-7} (Input/Output, 3-state)

Bi-directional Address/Data bus. The lower 8-bits of the PROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle, Port A or B are selected based on the latched value of AD_0. If $\overline{RD}$ or $\overline{IOR}$ is low when the latched Chip Enables are active, the output buffers present data to the bus.

A_{8-10} (Input)

These are the high order bits of the PROM address. They do not affect I/O operations.

PROG/$\overline{CE_1}$, CE_2 (Input)

CHIP ENABLE INPUTS: $\overline{CE}_1$ is active low and CE_2 is active high.
Both chip enables must be active to permit accessing the PROM. $\overline{CE}_1$ is also used as a programming pin.

$IO/\overline{M}$ (Input)

If the latched $IO/\overline{M}$ is high when $\overline{RD}$ is low, the output data comes from an I/O port. If it is low the output data comes from the EPROM.

$\overline{RD}$ (Input)

If the latched Chip Enables are active when $\overline{RD}$ goes low, the AD_{0-7} output buffers are enabled and outputs either the selected PROM location or I/O ports. When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD_{0-7} output buffers are 3-stated.

$\overline{IOW}$ (Input)

If the latched Chip Enables are active, a low on $\overline{IOW}$ causes the output port pointed to by the latched value of AD_0 to be written with the data on AD_{0-7}. The state of $IO/\overline{M}$ is ignored.

CLK (Input)

The CLK is used to force the READY into its high impedance state after it has been forced low by $\overline{CE}_1$ low, CE_2 high, and ALE high.

READY (Output, 3-state)

READY is a 3-state output controlled by $\overline{CE}_1$, CE_2, ALE and CLK.
READY is forced low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK.

$PA_0 - PA_7$ (Input/Output, 3-state)

These are general purpose I/O pins. Their input/output direction is determined by the contents of Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active and $\overline{IOW}$ is low and a 0 was previously latched from AD_0, AD_1.
Read operation is selected by either $\overline{IOR}$ low and active Chip Enables and AD_0 and AD_1 low, or $IO/\overline{M}$ high, $\overline{RD}$ low, active Chip Enables, and AD_0 and AD_1 low.

$PB_0 - PB_7$ (Input/Output, TR1-state)

This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD_0 and a 0 from AD_1.

RESET (Input)

In normal operation, an input high on RESET causes all pins in Ports A and B to assume input mode (clear DDR register)

$\overline{IOR}$ (Input)

When the Chip Enables are active, a low on $\overline{IOR}$ will output the selected I/O port onto the AD bus. $\overline{IOR}$ low performs the same function as the combination of $IO/\overline{M}$ high and $\overline{RD}$ low. When $\overline{IOR}$ is not used in a system, $\overline{IOR}$ should be tied to V_{CC} "1".

V_{CC} (Power)

+5 volt supply

V_{SS} (Power)

Ground Reference

V_{DD} (Power)

V_{DD} is a programming voltage and must be tied to +5V when the TMP8755AC is being read. For programming, a high voltage is supplied with V_{DD} = 25V, typical.

FUNCTIONAL DESCRIPTION

PROM SECTION

The TMP8755AC contains an 8-bit address latch which allows it to interface directly to TLCS-85A microcomputer system without additional hardware.

The PROM portion of the chip is addressed by the 11-bit address (A_{8-10}, AD_{0-7}) and CE. The address, IO/$\overline{M}$ and CE are latched into the address latches on falling edge of ALE. If the Chip Enables (CE_2 and $\overline{CE}_1$) are active and IO/$\overline{M}$ is low when $\overline{RD}$ goes low, the contents of the EPROM location addressed by latched address are output onto the AD_{0-7} lines.

I/O SECTION

The I/O port portion consists of two 8-bit I/O ports and two 8-bit Data Direction Registers (DDR).

The I/O portion of the chip is addressed by the latched value of AD_0 and AD_1.

Contents of Port A and Port B can be read and written, but the contents of DDR's cannot be read. A port can be read out when the latched Chip Enables are active and either $\overline{RD}$ goes low with IO/$\overline{M}$ high, or $\overline{IOR}$ goes low.

The two 8-bit DDR's (DDRA and DDRB) are used to determine the input/output status of each pin in the corresponding port.

A "0" specifies an input mode and a "1" specifies an output mode.

The two 8-bit DDR's are cleared by RESET signal. The table 1 summarize Port and DDR designation.

Table 1. Selection of Port and DDR Designation

AD_1	AD_0	Selection
0	0	Port A
0	1	Port B
1	0	Port A Data Direction Register (DDR A)
1	1	Port B Data Direction Register (DDR B)

ERASE CHARACTERISTICS

The TMP8755AC can be erased by applying light with wavelengths shorter than 4000 Å. (1Å = 10^{-8} cm). Sunlight and the fluorescent lamps may include 300 ~ 4000 Å wavelength components consequently when used under such lighting for extended periods of time, an opaque seal will be required to protect the TMP8755AC. Generally, ultraviolet light with a wavelength of 2537 Å is recommended for TMP-8755AC erasing, and in this case the integrated dose (ultraviolet light intensity [W/cm^2] x time [sec]) should be over 15 [w. sec/cm^2].

If the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1-cm from the lamp surface, erasure should be completed in about 60 minutes.

And using a lamp whose ultraviolet light intensity is a 12000 [μW/cm^2] will reduce the exposure time to about 20 minutes. (In this case the integrated dose should be 12000 [μW/cm^2] x (20 x 60) [sec] $\cong$ 15 [W. sec/cm^2].)

PROGRAMMING

Initially when received by customers all bits of the TMP8755AC are in the "1" state which is the erased state. Therefore programming is carried out by electrically writing in the "0" state at the desired bit locations.

A programmed "0" can only by changed to a "1" by ultraviolet erasure.

The program mode itself consists of programming a single address at a time, giving a single 50 ms pulse for every address.

Preliminary timing diagrams and parameter values pertaining to the TMP8755 AC programming operation are contained in Figure 7.

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating
V_{CC}	V_{CC} Supply Voltage Respect to V_{SS}	−0.5V to +7.0V
V_{DD}	V_{DD} Supply Voltage for Programming Respect to V_{SS}	−0.5V to +26.5V
P_D	Power Dissipation	1.5W
T_{SOLDER}	Soldering Temperature (Soldering Time 10 sec.)	260°C
T_{STG}	Storage Temperature	−55°C to +150°C
T_{OPR}	Operating Temperature	0°C to +70°C

D.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = V_{CC} \pm 0.6V$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input Low Voltage		−0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = 400μA	2.4			V
V_{IL}	Input Leakage Current	$V_{IN} = V_{CC}$ to 0V			± 10	μA
V_{LO}	Output Leakage Current	$0.45 \leqslant V_{out} \leqslant V_{CC}$			± 10	μA
I_{CC}	V_{CC} Supply Current				180	mA

A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = V_{CC} \pm 0.6V$

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
t_{CYC}	Clock Cycle time		320			ns
t_L	CLK Low Width		80			ns
t_H	CLK High Width		120			ns
t_r, t_f	CLK Rise and Fall Time				30	ns
t_{AL}	Address to Latch Set Up Time		50			ns
t_{LA}	Address Hold Time after Latch		80			ns
t_{LC}	Latch to READ/WRITE Control		100			ns
t_{RD}	Valid Data Out Delay from READ Control				170	ns
t_{AD}	Address Stable to Data Out Valid				450	ns
t_{LL}	Latch Enable Width		100			ns
t_{RDF}	Data Bus Float after READ	150pF	0		100	ns
t_{CL}	READ/WRITE Control to Latch Enable	Load	20			ns
t_{CC}	READ/WRITE Control Width		250			ns
t_{DW}	Data In to WRITE Set Up Time		150			ns
t_{WD}	Data In Hold Time after WRITE		30			ns
t_{WP}	WRITE to Port Output				400	ns
t_{PR}	Port Input Set Up Time		50			ns
t_{RP}	Port Input Hold Time		50			ns
t_{RYH}	READY HOLD TIME		0		160	ns
t_{ARY}	Address (CE) to READY				160	ns
t_{RV}	Recovery Time between Controls		300			ns
t_{RDE}	Data Out Delay from READ Controls		10			ns
t_{LD}	ALE to Data Out Valid (Preliminary)				350	ns
t_{LCK}	ALE Low during CLK high		100			ns

D.C. CHARACTERISTICS FOR PROGRAMMING

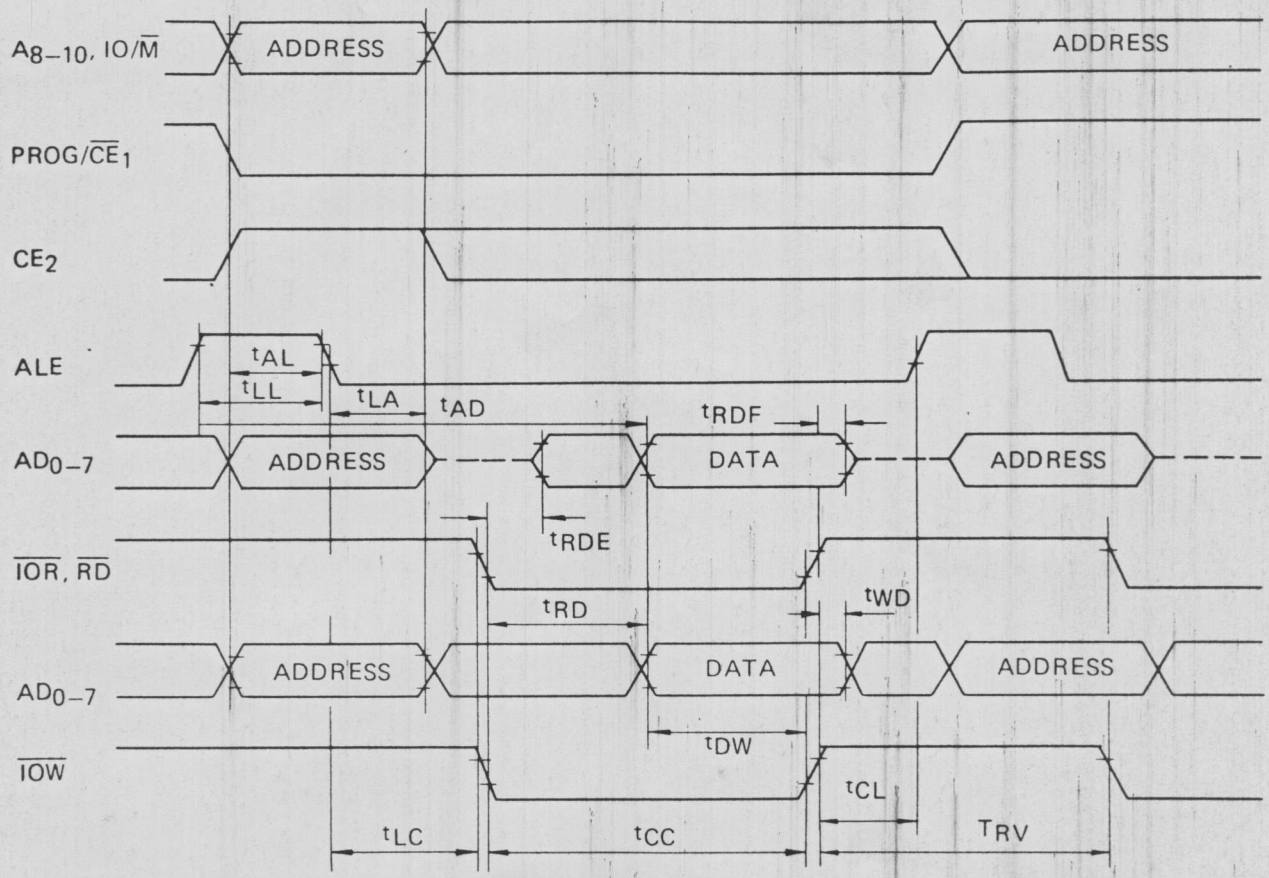
$T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage for programming	24	25	26	V
I_{DD}	I_{DD} Supply Current			30	mA

A.C. CHARACTERISTICS FOR PROGRAMMING

$T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$

Symbll	Parameter	Min.	Typ.	Max.	Units
t_{PS}	Data Set Up Time	10			ns
t_{PD}	Data Hold Time	0			ns
t_S	Program Pulse Set Up Time	2			μs
t_H	Program Pulse Hold Time	2			μs
t_{PR}	Program Pulse Rise Time	10	2000		ns
t_{PF}	Program Pulse Fall Time	10	2000		ns
t_{PRG}	Program Pulse Width	45	50		ms



Note: CE_1 must remain low for the entire cycle.

Fig. 3 PROM Read, I/O Read, and Write Timing

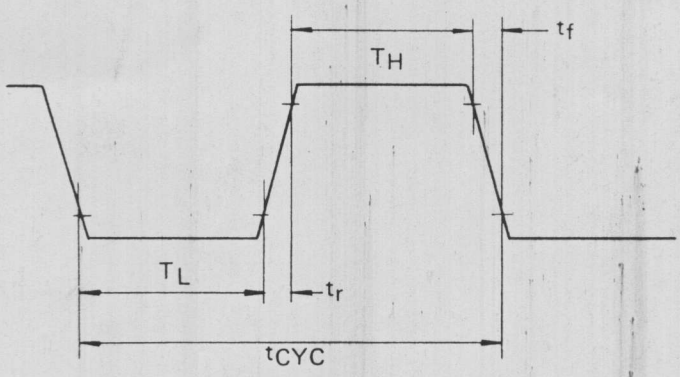


Fig. 4 Clock Specification for TMP8755AC

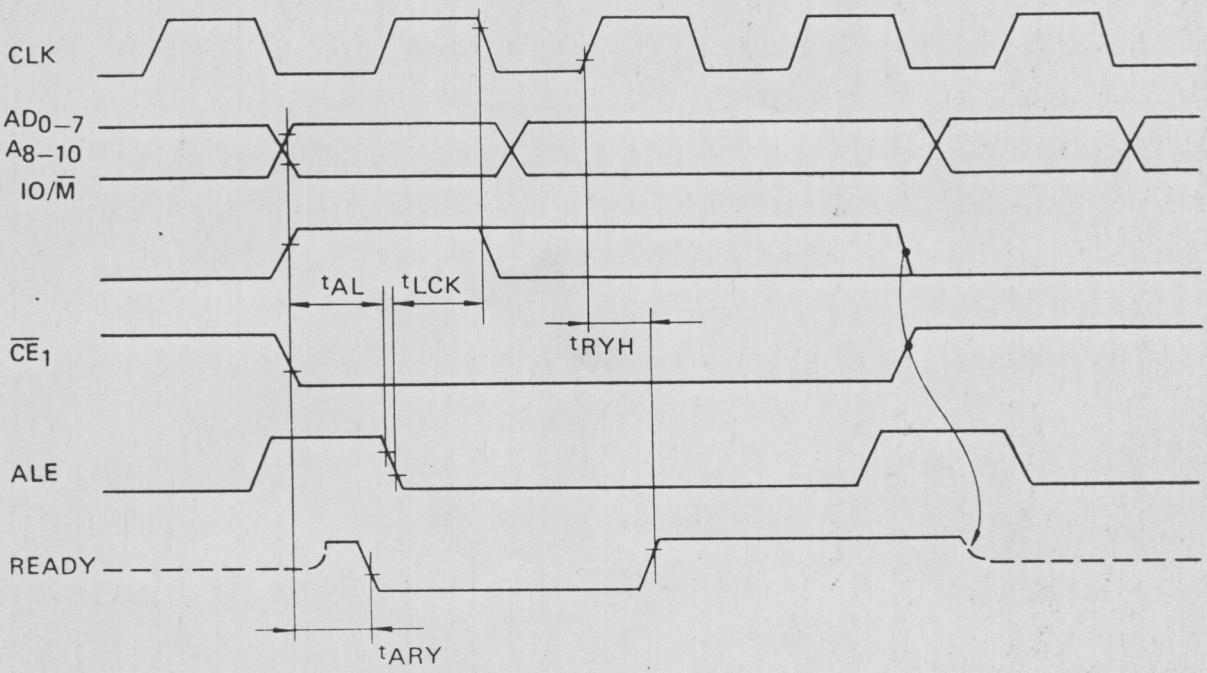


Fig. 5 Wait State Timing (Ready = 0)

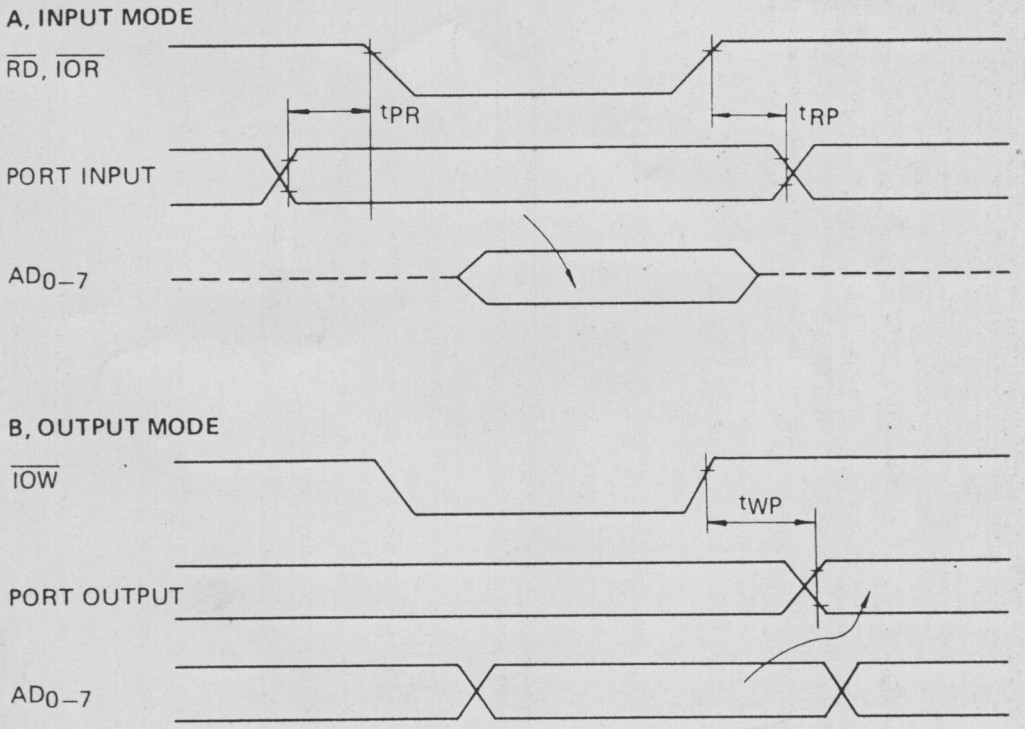
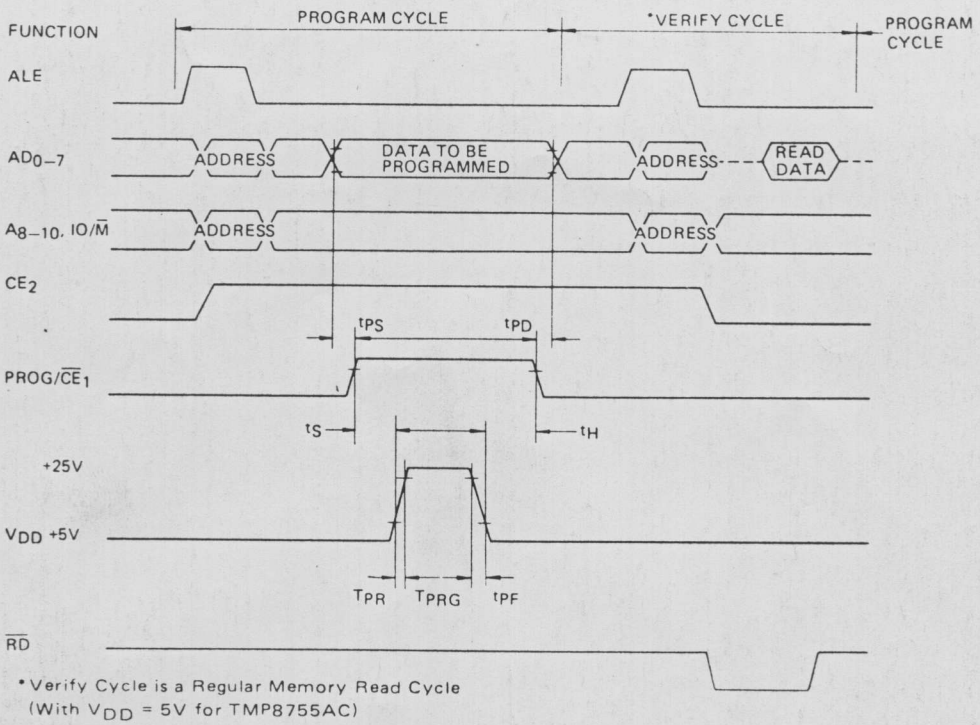


Fig. 6 I/O Port Timing

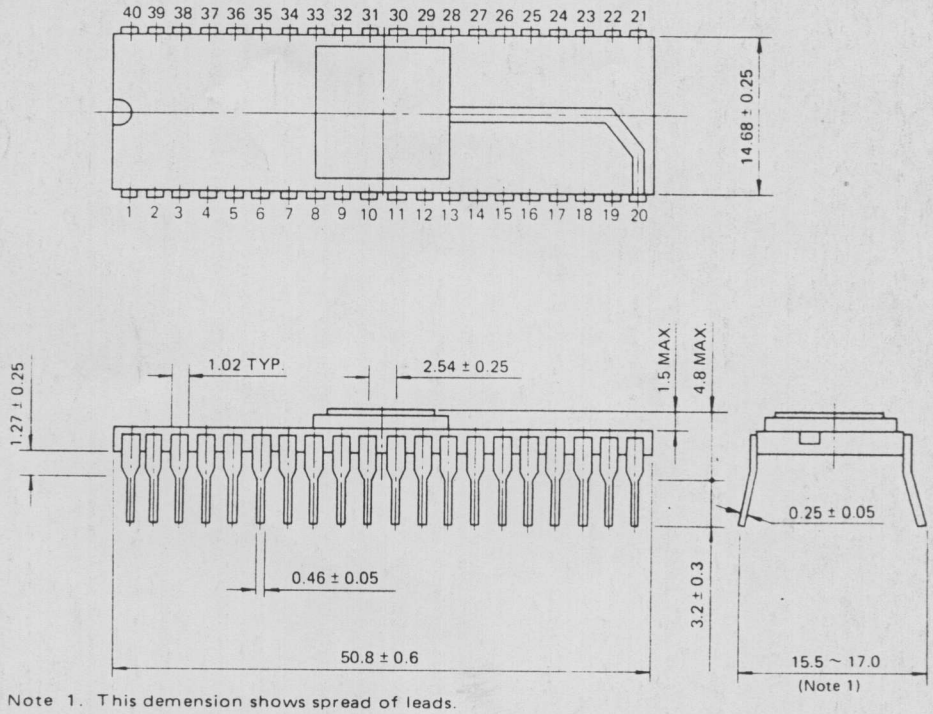


*Verify Cycle is a Regular Memory Read Cycle
(With V_{DD} = 5V for TMP8755AC)

Fig. 7 Program Mode Timing Diagram

OUTLINE DRAWING

40 Pins Ceramic Package



Note 1. This demension shows spread of leads.
2. All dimensions are in millimeters.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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