TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/L1 Series

TMP91C016

TOSHIBA CORPORATION

Semiconductor Company

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, “Points of Note and Restrictions”.
Especially, take care below cautions.

****CAUTION****
How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, INT0 to INT3, INTRTC, INTALM0 to INTALM4, INTKEY, INTVLD0 to INTVLD2), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 5 clocks of f_{FPH}) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

CMOS 16-Bit Microcontrollers

TMP91C016F/JTMP91C016S

1. Outline and Features

TMP91C016 is a high-speed 16-bit microcontroller designed for the control of various mid- to large-scale equipment.

TMP91C016F comes in a 100-pin flat package. JTMP91C016S is a 100-pad chip product.

Listed below are the features.

(1) High-speed 16-bit CPU (900/L1 CPU)

- Instruction mnemonics are upward compatible with TLCS-90/900
- 16 Mbytes of linear address space
- General-purpose registers and register banks
- 16-bit multiplication and division instructions; bit transfer and arithmetic instructions
- Micro DMA: 4 channels (592ns/ 2bytes at 27MHz)

(2) Minimum instruction execution time: 148 ns (at 27 MHz)

(3) Built-in RAM: None
Built-in ROM: None

(4) External memory expansion
- Expandable up to 105 Mbytes (Shared program/data area)
- Can simultaneously support 8-/16-bit width external data bus: Dynamic data bus sizing
- Separate bus system

(5) 8-bit timers: 4 channels

(6) General-purpose serial interface: 2 channels

Channel 0
- UART mode
- IrDA Ver.1.0 (115.2 kbps) mode selectable

Channel 1
- UART mode
- Synchronous mode selectable

(7) LCD controller
- Adapt to both Shift register type and Built-in RAM type LCD driver

(8) Timer for real time clock (RTC)
- Based on TC8521A

(9) Key-on wakeup (Interrupt key input)

(10) Watchdog timer

(11) Melody/alarm generator
- Melody: Output of clock 4 to 5461 Hz
- Alarm: Output of the 8 kinds of alarm pattern
- Output of the 5 kinds of interval interrupt

(12) Chip select/wait controller: 4 channels

(13) MMU
- Expandable up to 105 Mbytes (4 local area/8 bank method)

(14) Display data reciprocal conversion function between the vertical and horizontal (8 × 8)

(15) Interrupts: 40 interrupts
- 9 CPU interrupts: Software interrupt instruction and illegal instruction
- 25 internal interrupts: 7 priority levels are selectable
- 9 external interrupts: 7 priority levels are selectable
  (among 4 interrupts are selectable edge mode)

(16) Input/output ports: 31 pins (at External 16-bit data bus memory)

(17) Standby function
Three HALT modes: IDLE2 (Programmable), IDLE1 and STOP

(18) DRAM controller
- $\overline{2CAS}$ mode

(19) Voltage compare circuit: 3 channels

(20) Triple-clock controller
- Clock doubler (DFM) circuit is inside
- Clock gear function: Select a high-frequency clock fc/1 to fc/16
- Slow mode (fs = 32.768 kHz)

(21) Operating voltage

- VCC = 2.7 V to 3.6 V (fc max = 27 MHz)
- VCC = 1.8 V to 3.6 V (fc max = 10 MHz)

(22) Package

- 100-pin QFP: P-LQFP100-1414-0.50F
- Chip form supply also available. For details, contact your local Toshiba sales representative.

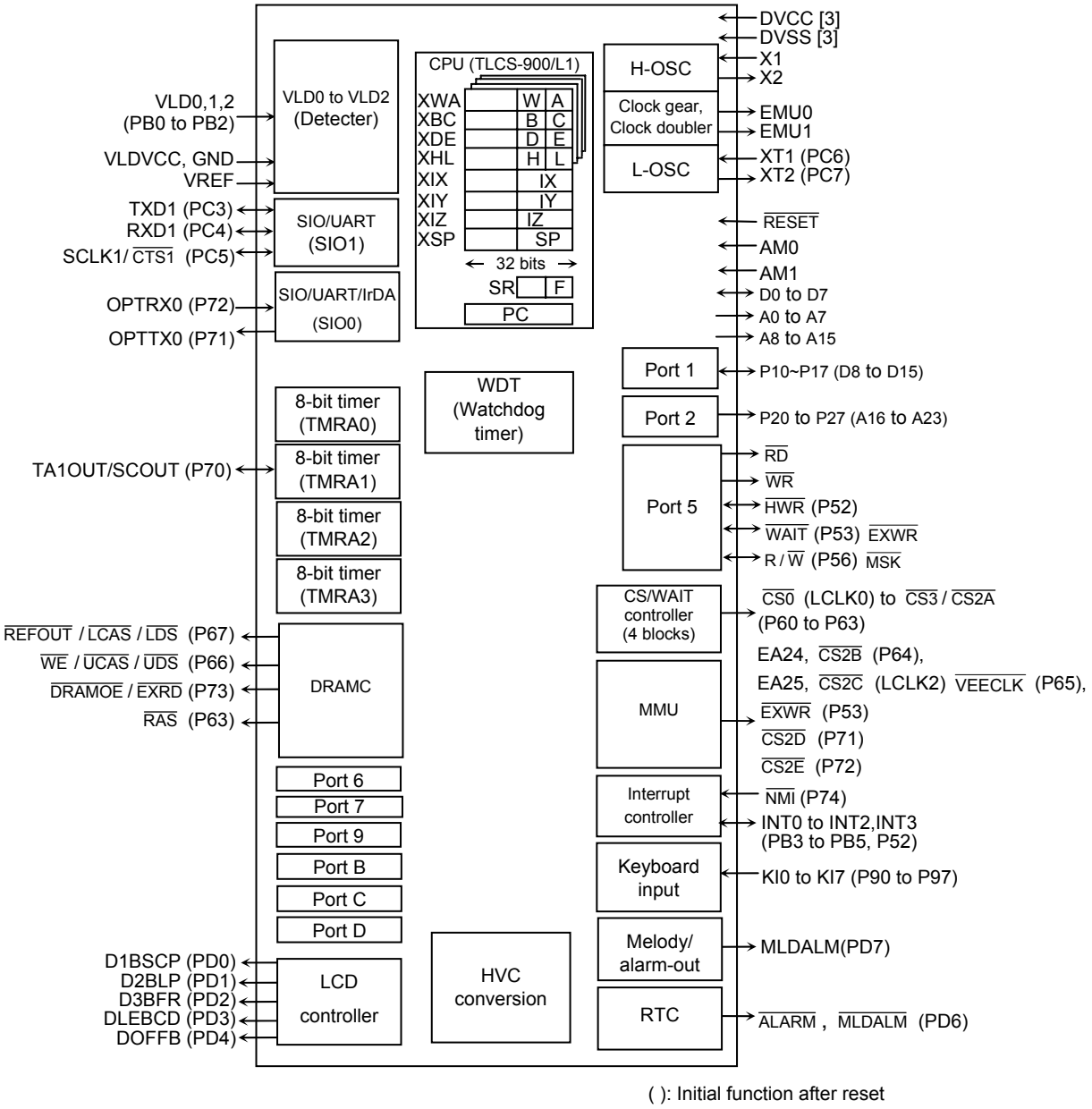


Figure 1.1 TMP91C016 Block Diagram

2. Pin Assignment and Pin Functions

The assignment of input/output pins for the TMP91C016, their names and functions are as follows:

2.1 Pin Assignment Diagram

Figure 2.1.1 shows the pin assignment of the TMP91C016F.

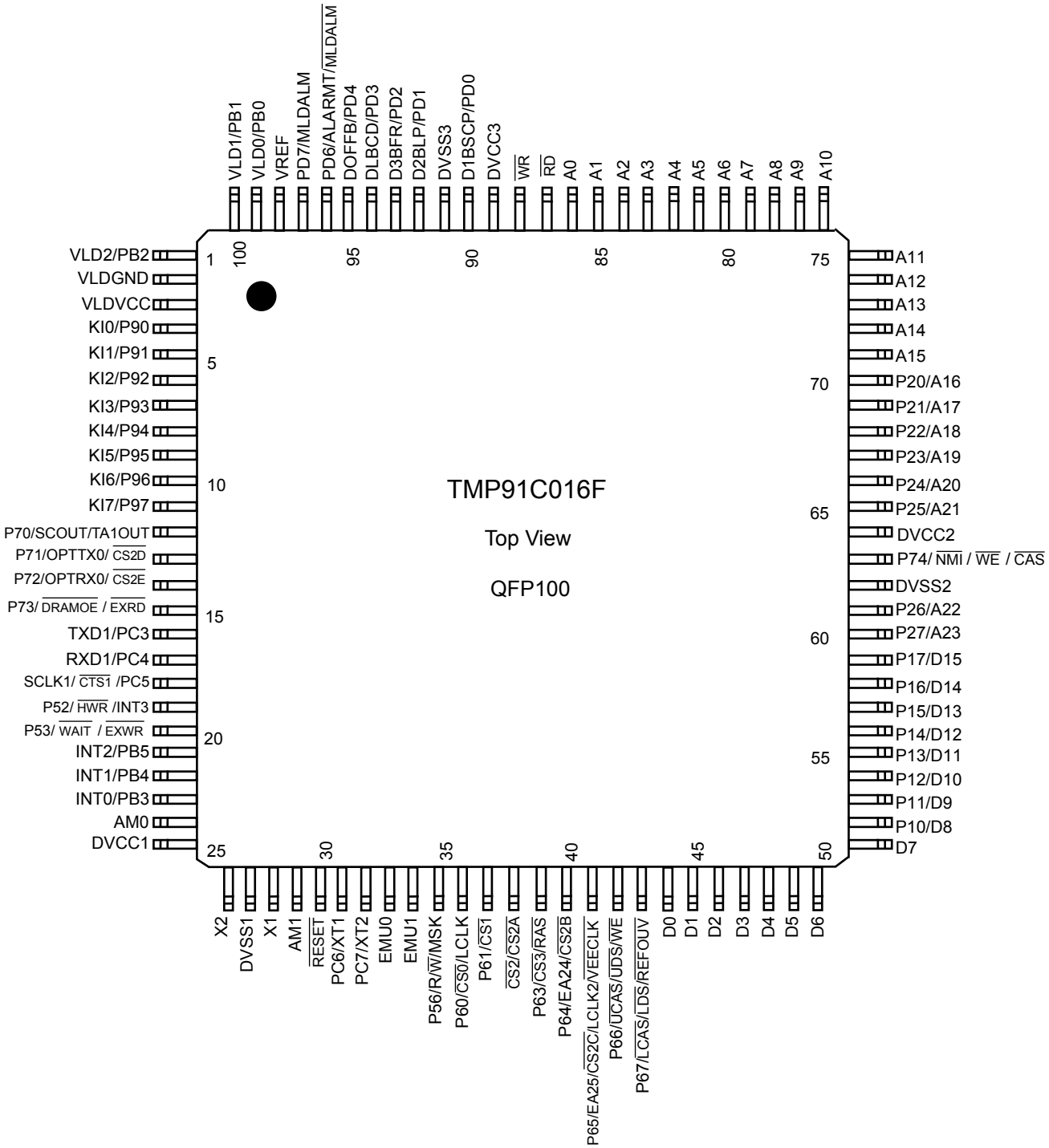


Figure 2.1.1 Pin Assignment Diagram (100-pin QFP)

2.1.1 Pad Layout

Table 2.1.1 PAD Layout

(Chip size 4.38 mm × 4.43 mm) Unit: μm

Pin No	Name	X Point	Y Point	Pin No	Name	X Point	Y Point	Pin No	Name	X Point	Y Point
1	PB2	−2057	1531	35	P56	−239	−2082	69	P21	2053	850
2	VLDGND	−2057	1417	36	P60	−125	−2082	70	P20	2053	964
3	VLDVCC	−2057	1303	37	P61	−11	−2082	71	A15	2053	1078
4	P90	−2057	990	38	P62	103	−2082	72	A14	2053	1192
5	P91	−2057	876	39	P63	217	−2082	73	A13	2053	1306
6	P92	−2057	762	40	P64	331	−2082	74	A12	2053	1420
7	P93	−2057	648	41	P65	479	−2082	75	A11	2053	1534
8	P94	−2057	534	42	P66	593	−2082	76	A10	1503	2082
9	P95	−2057	420	43	P67	707	−2082	77	A9	1389	2082
10	P96	−2057	306	44	D0	821	−2082	78	A8	1275	2082
11	P97	−2057	192	45	D1	935	−2082	79	A7	1160	2082
12	P70	−2057	55	46	D2	1049	−2082	80	A6	1046	2082
13	P71	−2057	−59	47	D3	1163	−2082	81	A5	932	2082
14	P72	−2057	−174	48	D4	1277	−2082	82	A4	818	2082
15	P73	−2057	−290	49	D5	1391	−2082	83	A3	704	2082
16	PC3	−2057	−404	50	D6	1505	−2082	84	A2	590	2082
17	PC4	−2057	−521	51	D7	2053	−1534	85	A1	476	2082
18	PC5	−2057	−638	52	P10	2053	−1420	86	A0	362	2082
19	P52	−2057	−755	53	P11	2053	−1306	87	$\overline{RD}$	248	2082
20	P53	−2057	−870	54	P12	2053	−1192	88	$\overline{WR}$	134	2082
21	PB5	−2057	−991	55	P13	2053	−1078	89	DVCC3	20	2082
22	PB4	−2057	−1105	56	P14	2053	−964	90	PD0	−180	2082
23	PB3	−2057	−1219	57	P15	2053	−850	91	DVSS3	−294	2082
24	AM0	−2057	−1333	58	P16	2053	−736	92	PD1	−408	2082
25	DVCC1	−2057	−1447	59	P17	2053	−606	93	PD2	−522	2082
26	X2	−1507	−2082	60	P27	2053	−450	94	PD3	−638	2082
27	DVSS1	−1342	−2082	61	P26	2053	−295	95	PD4	−752	2082
28	X1	−1176	−2082	62	DVSS2	2053	−140	96	PD6	−866	2082
29	AM1	−1060	−2082	63	P74	2053	17	97	PD7	−980	2082
30	$\overline{RESET}$	−946	−2082	64	DVCC2	2053	171	98	VREF	−1274	2082
31	PC6	−831	−2082	65	P25	2053	326	99	PB0	−1388	2082
32	PC7	−583	−2082	66	P24	2053	482	100	PB1	−1506	2082
33	EMU0	−467	−2082	67	P23	2053	622				
34	EMU1	−353	−2082	68	P22	2053	736				

2.2 Pin Names and Functions

The names of the input/output pins and their functions are described below.

Pin Name	Number of Pins	I/O	Functions
D0 to D7	8	I/O	Data (Lower): Bits 0 to 7 of data bus
P10 to P17	8	I/O	Port 1: I/O port that allows I/O to be selected at the bit level (When used to the external 8-bit bus)
D8 to D15		I/O	Data (Upper): Bits 8 to15 of data bus
P20 to P27	8	Output	Port 2: Output port
A16 to A23		Output	Address: Bits 16 to 23 of address bus
A8 to A15	8	Output	Address: Bits 8 to 15 of address bus
A0 to A7	8	Output	Address: Bits 0 to 7 of address bus
$\overline{RD}$	1	Output	Read: Strobe signal for reading external memory. P5 <RDE>=0, output RD when reading internal area.
$\overline{WR}$	1	Output	Write: Strobe signal for writing data to pins D0 to D7
P52	1	I/O	Port 52: I/O port (with pull-up resistor)
$\overline{HWR}$		Output	High Write: Strobe signal for writing data to pins D8 to D15
$\overline{INT3}$		Input	Interrupt request pin 3: Interrupt request pin with programmable rising/falling edge
P53	1	I/O	Port 53: I/O port (with pull-up resistor)
$\overline{WAIT}$		Input	Wait: Pin used to request CPU bus wait ((1 + N) WAIT mode)
$\overline{EXWR}$		Output	Ex write: Strobe signal for writing data for RAM
P56	1	I/O	Port 56: I/O port (with pull-up resistor)
R / $\overline{W}$		Output	Read/write: 1 represents read or dummy cycle; 0 represents write cycle.
$\overline{MSK}$		Input	Request VEECLK clock for external LCD-driver.
P60	1	I/O	Port 60: I/O port (with pull-up resistor)
$\overline{CS0}$		Output	Chip select 0: Outputs 0 when address is within specified address area.
LCLK0		Output	Lcd CLK: Command controll C/S for S/R type lcdd.
P61	1	I/O	Port 61: I/O port (with pull-up resistor)
$\overline{CS1}$		Output	Chip select 1: Outputs 0 when address is within specified address area
CS2	1	Output	Chip select 2: Outputs 0 when address is within specified address area
$\overline{CS2A}$		Output	Expand chip select: 2A: Outputs 0 when address is within specified address area
P63	1	I/O	Port 63: I/O port (with pull-up resistor)
CS3		Output	Chip select 3: Outputs 0 when address is within specified address area
$\overline{RAS}$		Output	Row address strobe: RAS strobe row address area for DRAM
P64	1	I/O	Port 64: I/O port (with pull-up resistor)
EA24		Output	Chip select 24: Outputs 0 when address is within specified address area
$\overline{CS2B}$		Output	Expand chip select 2B: Outputs 0 when address is within specified address area
P65	1	I/O	Port 65: I/O port (with pull-up resistor)
EA25		Output	Chip select 25: Outputs 0 when address is within specified address area
$\overline{CS2C}$		Output	Expand chip select 2C: Outputs 0 when address is within specified address area
LCLK2		Output	Lcd CLK: Command controll C/S for S/R type lcdd.
$\overline{VEECLK}$		Output	Pomp-up CLK for external LCD driver
P66	1	I/O	Port 66: I/O port (with pull-up resistor)
$\overline{UCAS}$		Output	Upper column address strobe: Upper CAS strobe for 2CAS type DRAM.
$\overline{UDS}$		Output	Upper data enable strobe
$\overline{WE}$		Output	Write strobe for DRAM (only 8-bit access)
P67	1	I/O	Port 67: I/O port (with pull-up resistor)
$\overline{LCAS}$		Output	Lower column address strobe: Upper CAS strobe for 2CAS type DRAM.
$\overline{LDS}$		Output	Lower data enable strobe
$\overline{REFOUT}$		Output	Refresh cycle state singanl for DRAM (only 8-bit access)

Pin Name	Number of Pins	I/O	Functions
P70 SCOUT TA1OUT	1	I/O Output Output	Port 70: I/O port (with pull-up resistor) System clock output: Selectable f_{FPH} or fs 8-bit timer output: Timer 0 or timer 1 out
P71 OPTTX0 $\overline{CS2D}$	1	I/O Output Output	Port 71: I/O port (with pull-up resistor) SIO0 trance port Expond chip select 2D: Outputs 0 when address is within specified address area
P72 OPTRX0 $\overline{CS2E}$	1	I/O Input Output	Port 72: I/O port (Shummit input, with pull-up/pull-down resistor) SIO0 receive port Expond chip select 2E: Outputs 0 when address is within specified address area
P73 $\overline{DRAMOE}$ $\overline{EXRD}$	1	I/O Output Output	Port 73: I/O port (with pull-up resistor) DRAMOE: Strobe signal for reading external DRAM External read: Strobe signal for reading external memory
P74 $\overline{NMI}$ $\overline{WE}$ $\overline{CAS}$	1	I/O Input Output Output	Port 74: I/O port (with pull-up resistor) Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge level or with both edge levels programmable Strobe signal for writing data for DRAM (only 2CAS) Coulmn address strobe: Outputs 0 when address is within specified DRAM column address area (only 8 bits access)
P90 to P97 KI0 to KI7	8	Input Input	Port: 90 to 97 port: Pin used to input ports Key input 0 to 7: Pin used of key on wake-up 0 to 7 (Schmitt input, with pull-up resistor)
PB0 VLD0	1	I/O Input	Port B0: I/O port (with pull-up resistor) Voltage level detector 0: For main battery, Interrupt request with edge, too
PB1 VLD1	1	I/O Input	Port B1: I/O port (with pull-up resistor) Voltage level detector 1: For back up battery, Interrupt request with edge, too
PB2 VLD2	1	I/O Input	Port B2: I/O port (with pull-up resistor) Voltage level detector 2: For micon battery, Interrupt request with edge, too
PB3 INT0	1	I/O Input	Port B3: I/O port (Schmitt input, with pull-up resistor) Interrupt request pin 0: Interrupt request pin with programmable level/rising/falling edge
PB4 to PB5 INT1 to INT2	2	I/O Input	Port B4 to B5: I/O port (Schmitt input, with pull-down resistor) Interrupt request pin 1 to 2: Interrupt request pin with programmable rising/falling edge
PC3 TXD1	1	I/O Output	Port C3: I/O port (with pull-up resistor) Serial 1 send data: Open-drain output pin by programmable
PC4 RXD1	1	I/O Input	Port C4: I/O port (Schmitt input, with pull-up/pull-down resistor) Serial 1 recive data
PC5 SCLK1 $\overline{CTS1}$	1	I/O I/O Input	Port C5: I/O port (Schmitt input, with pull-up/pull-down resistor) Serial clock I/O 1 Clear to send
PC6 XT1	1	I/O Input	Port C6: I/O port (Open-drain output) Low-frequency oscillator connection pins
PC7 XT2	1	I/O Output	Port C7: I/O port (Open-drain output) Low-frequency oscillator connection pins

Pin Name	Number of Pins	I/O	Functions
PD0 D1BSCP	1	I/O Output	Port D0: I/O port (with pull-up resistor) LCD driver output pin
PD1 D2BLP	1	I/O Output	Port D1: I/O port (with pull-up resistor) LCD driver output pin
PD2 D3BFR	1	I/O Output	Port D2: I/O port (with pull-up resistor) LCD driver output pin
PD3 DLEBCD	1	I/O Output	Port D3: I/O port (with pull-up resistor) LCD driver output pin
PD4 DOFFB	1	I/O Output	Port D4: I/Ot port (with pull-up resistor) LCD driver output pin
PD6 $\overline{\text{ALARM}}$ $\overline{\text{MLDALM}}$	1	I/O Output Output	Port D6: I/O port (with pull-up resistor) RTC alarm output pin Logical invert for Melody/alarm output pin
PD7 MLDALM	1	I/O Output	Port D7: I/O port (with pull-up resistor) Melody/alarm output pin
AM0 to AM1	2	Input	Operate mode: Fixed to AM1 = 0, AM0 = 1 16-bit external bus or 8-/16-bit dynamic sizing. Fixed to AM1 = 0, AM0 = 0 8-bit external bus fixed.
EMU0	1	Output	Open pin
EMU1	1	Output	Open pin
$\overline{\text{RESET}}$	1	Input	Reset: Initializes TMP91C016. (with pull-up resistor)
VREF	1	Input	Power supply pin for Low-frequency oscillator, RTC and VLD.
VLDVCC	1		For VLD power supply pin
VLDVSS	1		For VLD: GND pins (0 V) (All pins should be connected with GND (0 V).)
X1/X2	2		High-frequency oscillator connection pins
DVCC	3		Power supply pins (All Vcc pins should be connected with the power Supply pin).
DVSS	3		GND pins (0 V) (All pins should be connected with GND (0V).)

3. Operation

This following describes block by block the functions and operation of the TMP91C016.

Notes and restrictions for eatch book are outlined in 6. “Points of Note and Restrictions” at the end of this manual.

3.1 CPU

The TMP91C016 incorporates a high-performance 16-bit CPU (The 900/L1-CPU). For CPU operation, see the TLCS-900/L1 CPU.

The following describe the unique function of the CPU used in the TMP91C016; these functions are not covered in the TLCS-900/L1 CPU section.

3.1.1 Reset

When resetting the TMP91C016 microcontroller, ensure that the power supply voltage is within the operating voltage range, and that the internal high-frequency oscillator has stabilized. Then set the $\overline{\text{RESET}}$ input to low level at least for 10 system clocks (12 μs at 27 MHz).

Thus when turn on the switch, be set to the power supply voltage is within the operating voltage range, and that the internal high-frequency oscillator has stabilized. Then hold the $\overline{\text{RESET}}$ input to low level at least for 10 system clocks.

Clock gear is initialized 1/16 mode by reset operation. It means that the system clock mode f_{SYS} is set to fc/32 (= fc/16 × 1/2).

When the reset is accept, the CPU:

- Sets as follows the program counter (PC) in accordance with the reset vector stored at address FFFF00H to FFFF02H:

  PC<0:7> ← Value at FFFF00H address

  PC<15:8> ← Value at FFFF01H address

  PC<23:16> ← Value at FFFF02H address
- Sets the stack pointer (XSP) to 100H.
- Sets bits <IFF2:0> of the status register (SR) to 111 (Sets the interrupt level mask register to level 7).
- Sets the <MAX> bit of the status register (SR) to 1 (Max mode).
  (Note: As this product does not support Min mode, do not write a 0 to the <MAX>)
- Clears bits <RFP2:0> of the status register (SR) to 000 (Sets the register bank to 0).

When reset is released, the CPU starts executing instructions in accordance with the program counter settings. CPU internal registers not mentioned above do not change when the reset is released.

When the reset is accepted, the CPU sets internal I/O, ports, and other pins as follows.

- Initializes the internal I/O registers.
- Sets the port pins, including the pins that also act as internal I/O, to general-purpose input or output port mode.

Note: The CPU internal register (except to PC, SR, XSP) and internal RAM data do not change by resetting.

Figure 3.1.1 is a reset timing chart of the TMP91C016.

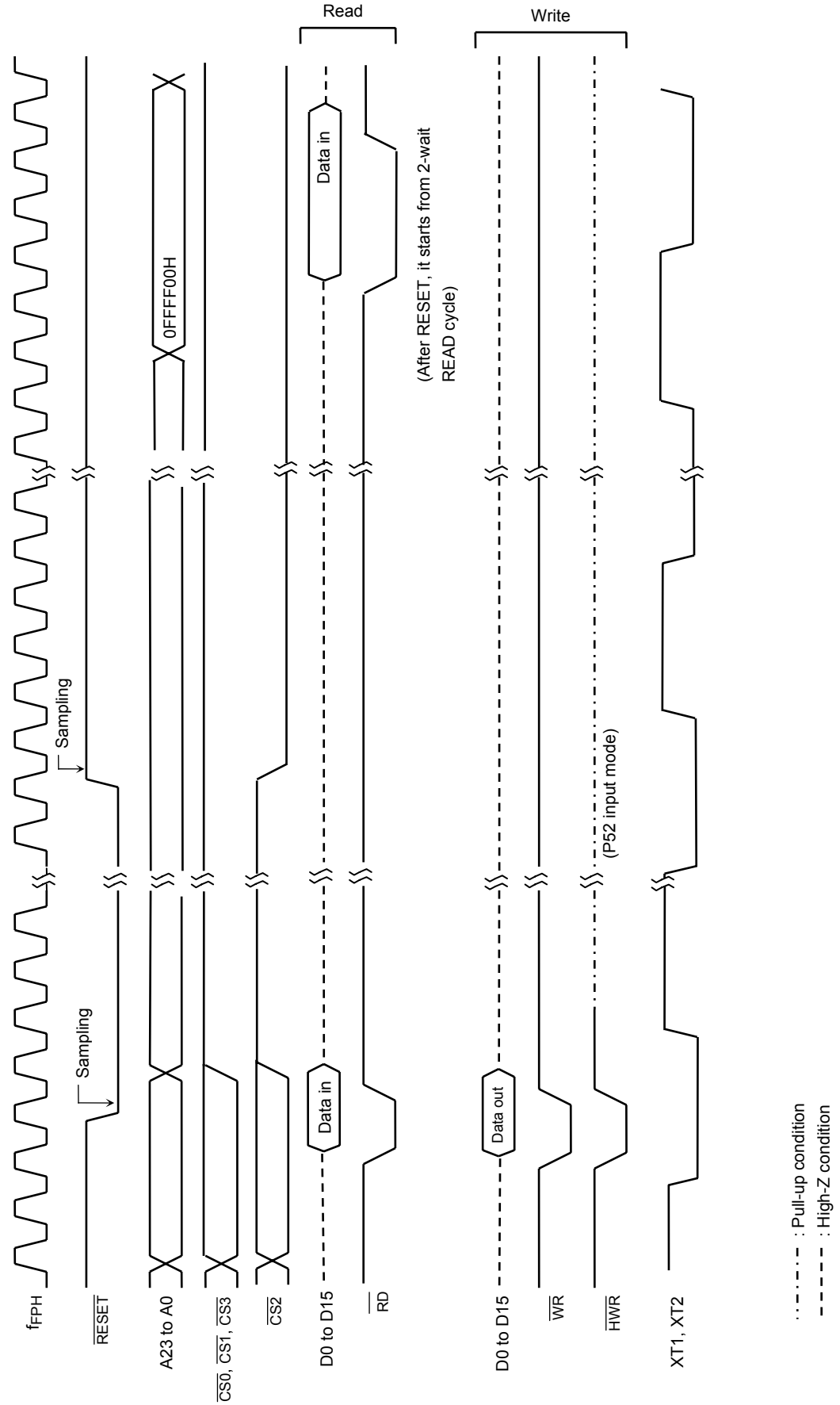


Figure 3.1.1 TMP91C016 Reset Timing Chart

3.2 Memory Map

Figure 3.2.1 is a memory map of the TMP91C016.

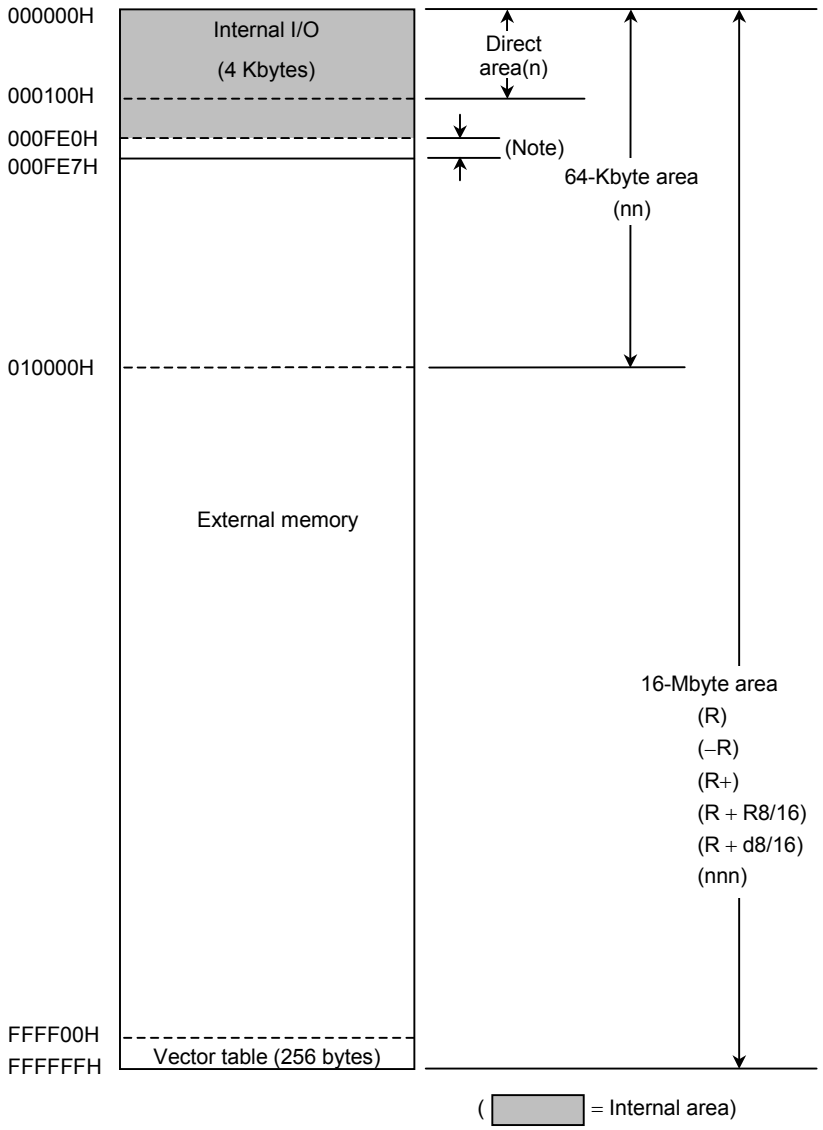


Figure 3.2.1 Memory Map

Note: Address 000FE0H to 00FE7H are assigned for the external memory area of built-in RAM type LCD driver.

4. Electrical Characteristics

4.1 Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	Vcc	−0.5 to 4.0	V
Input voltage	VIN	−0.5 to Vcc + 0.5	
Output current	IOL	2	mA
Output current	IOH	−2	
Output current (total)	ΣIOL	80	
Output current (total)	ΣIOH	−80	
Power dissipation (Ta = 85°C)	PD	600	mW
Soldering temperature (10 s)	TSOLDER	260	°C
Storage temperature	TSTG	−65 to 150	
Operating temperature	TOPR	−10 to 70	

Note: The maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2)

Parameter		Symbol	Condition		Min	Typ. (Note 1)	Max	Unit
Power supply voltage (AVCC = DVCC) (AVSS = DVSS = 0 V)		VCC	fc = 2 to 27 MHz	fs = 30 to 34 kHz	2.7		3.6	V
			fc = 2 to10 MHz		1.8			
Power supply voltage		VREF	3.6 ≥ Vcc ≥ 1.8 V		–	1.5	–	
Input low voltage	D0 to D15	VIL	Vcc ≥ 2.7 V		−0.3		0.6	
			Vcc < 2.7 V				0.2 Vcc	
	P52 to PD7 (except $\overline{\text{RESET}}$, P52, P72, P74, P9, PB3, PB4, PB5, PC4, PC5)	VIL1	Vcc ≥ 2.7 V				0.3 Vcc	
			Vcc < 2.7 V				0.2 Vcc	
	$\overline{\text{RESET}}$, P52, P72, P74, P9, PB3, PB4, PB5, PC4, PC5	VIL2	Vcc ≥ 2.7 V				0.25 Vcc	
			Vcc < 2.7 V				0.15 Vcc	
	AM0 to AM1	VIL3	Vcc ≥ 2.7 V				0.3	
			Vcc < 2.7 V				0.3	
	X1	VIL4	Vcc ≥ 2.7 V				0.2 Vcc	
			Vcc < 2.7 V				0.1 Vcc	
Input high voltage	D0 to D15	VIH	3.6 ≥ Vcc ≥ 3.3 V		2.4		Vcc + 0.3	
			3.3 > Vcc ≥ 2.7 V		2.0			
			Vcc < 2.7 V		0.7 Vcc			
	P52 to PD7 (except $\overline{\text{RESET}}$, P52, P72, P74, P9, PB3, PB4, PB5, PC4, PC5)	VIH1	Vcc ≥ 2.7 V		0.7 Vcc			
			Vcc < 2.7 V		0.8 Vcc			
	$\overline{\text{RESET}}$, P52, P72, P74, P9, PB3, PB4, PB5, PC4, PC5	VIH2	Vcc ≥ 2.7 V		0.75 Vcc			
			Vcc < 2.7 V		0.85 Vcc			
	AM0 to AM1	VIH3	Vcc ≥ 2.7 V		Vcc − 0.3			
			Vcc < 2.7 V		Vcc − 0.3			
	X1	VIH4	Vcc ≥ 2.7 V		0.8 Vcc			
			Vcc < 2.7 V		0.9 Vcc			
Output low voltage		VOL	IOL = 1.6 mA	Vcc ≥ 2.7 V			0.45	
			IOL = 0.4 mA	Vcc < 2.7 V			0.15 Vcc	
Output high voltage		VOH	IOH = −400 μA	Vcc ≥ 2.7 V	Vcc − 0.3			
			IOH = −200 μA	Vcc < 2.7 V	0.8 Vcc			

4.2 DC Characteristics (2/2)

Parameter	Symbol	Condition	Min	Typ. (Note 1)	Max	Unit
Input leakage current	ILI	0.0 ≤ VIN ≤ Vcc		0.02	±5	μA
Output leakage current	ILO	0.2 ≤ VIN ≤ Vcc − 0.2		0.05	±5	
$\overline{\text{RESET}}$ pull-up resistor	RRST	2.7 ≤ Vcc ≤ 3.6 V	80		400	kΩ
		Vcc = 2 V ± 10%	200		1000	
Pin capacitance	CIO	fc = 1 MHz			10	pF
Schmitt width ($\overline{\text{RESET}}$, INT3, OPTRX0, $\overline{\text{NMI}}$, KI0 to KI7, INT0, INT1, INT2, RXD1, SCLK1/ $\overline{\text{CTS1}}$)	VTH	Vcc ≥ 2.7 V	0.4	0.9		V
		Vcc < 2.7 V	0.3	0.7		
Programmable pull-up resistor (P53, P56, P60 toP67, P70 to P71, P73, PD0 to P7)	RKH1	2.7 ≤ Vcc ≤ 3.6 V	80	200	400	kΩ
		Vcc = 2 V ± 10%	200		1000	
Programmable pull-up resistor (P90 to P97, PB0 to PB2, PB4 to PB5, P52, P72, PC4 to PC5)	RKH2	2.7 ≤ Vcc ≤ 3.6 V	60	180	350	
		Vcc = 2 V ± 10%	180		900	
Programmable pull-up resistor (PB3 at Vcc)	RKH3	2.7 ≤ Vcc ≤ 3.6 V	50	167	280	
		Vcc = 2 V ± 10%	120		900	
Programmable pull-up resistor (PB3 at Vss)		2.7 ≤ Vcc ≤ 3.6 V	400	1000	2000	
		Vcc = 2 V ± 10%	800		4500	
Programmable pull-down resistor (P72, PB4 to PB5, PC4 to PC5)	RKL	2.7 ≤ Vcc ≤ 3.6 V	80	200	600	
		Vcc = 2 V ± 10%	200		1000	
NORMAL (Note 2)	Icc	2.7 ≤ Vcc ≤ 3.6 V fc = 27 MHz		11.0	15.0	mA
IDLE2				4.5	6.7	
IDLE1				1.5	2.9	
NORMAL (Note 2)		Vcc = 2 V ± 10% fc = 10 MHz (Typ.: Vcc = 2.0 V)		2.5	3.5	mA
IDLE2				1.0	1.4	
IDLE1				0.3	0.6	
SLOW (Note 2)		2.7 ≤ Vcc ≤ 3.6 V fs = 32.768 kHz		15.0	30.0	μA
IDLE2				6.0	23.0	
IDLE1				2.5	20	
SLOW (Note 2)		Vcc = 2V ± 10% fs = 32.768 kHz (Typ.: Vcc = 2.0 V)		9.0	20	μA
IDLE2				4.0	15	
IDLE1				1.0	10	
STOP		1.8 ≤ Vcc ≤ 3.6 V		0.3	10	μA
XT: VREF power operation	Icc Iref	VREF = 1.5 V		0.8	1.2	μA

Note 1: Typical values are for when Ta = 25°C and Vcc = 3.3 V unless otherwise noted.

Note 2: Icc measurement conditions (Normal, Slow):
All functions are operational; output pins are open and input pins are fixed. Data and address bus CL = 30 pF loaded.

Note 3: All Icc specifications are VREF = 1.5 V and fs power = VREF condition.

4.3 AC Characteristics

(1) Vcc = 2.7 to 3.6 V

No.	Parameter	Symbol	Variable		f_{FPH} = 27 MHz		Unit
			Min	Max	Min	Max	
1	f_{FPH} period (= x)	t_{FPH}	37.0	31250	37.0		ns
2	A0 to A23 valid → $\overline{RD}$ / $\overline{WR}$ fall	t_{AC}	x – 23		14		ns
	SR mode (LCDC DMA case: READ only)		1.5x – 13		32		ns
3	$\overline{RD}$ rise → A0 to A23 hold	t_{CAR}	0.5x – 13		5		ns
4	$\overline{WR}$ rise → A0 to A23 hold	t_{CAW}	x – 13		24		ns
	$\overline{DS}$ rise → A0 to A23 hold		x – 13		24		ns
5	A0 to A23 valid → D0 to D15 input	t_{AD}		3.5x – 24		105	ns
6	$\overline{RD}$ fall → D0 to D15 input	t_{RD}		2.5x – 24		68	ns
	SR mode (LCDC DMA case)			2.0x – 24		50	ns
7	$\overline{RD}$ low width	t_{RR}	2.5x – 15		77		ns
	SR mode (LCDC DMA case)		2.0x – 15		59		ns
8	$\overline{RD}$ rise → D0 to A15 hold	t_{HR}	0		0		ns
9	$\overline{WR}$ low width	t_{WW}	2.0x – 15		59		ns
	$\overline{DS}$ Low Width		2.0x – 15		59		ns
10	D0 to D15 valid → $\overline{WR}$ rise	t_{DW}	1.5x – 35		20		ns
	D0 to D15 valid → $\overline{DS}$ rise		1.5x – 35		20		ns
11	$\overline{WR}$ rise → D0 to D15 hold	t_{WD}	x – 25		12		ns
	$\overline{DS}$ rise → D0 to D15 hold		x – 25		12		ns
12	A0 to A23 valid → $\overline{WAIT}$ input (1 + N) WAIT mode	t_{AW}		3.5x – 60		69	ns
13	$\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ hold (1 + N) WAIT mode	t_{CW}	2.5x + 0		92		ns
	SR mode (LCDC DMA case: READ only)		2.0x + 0		74		ns
14	A0 to A23 valid → Port input	t_{APH}		3.5x – 89		40	ns
15	A0 to A23 valid → Port hold	t_{APH2}	3.5x		129		ns
16	A0 to A23 valid → Port valid	t_{APO}		3.5x + 60		189	ns

AC measuring conditions

- Output level: High = 0.7 Vcc, Low = 0.3 Vcc, CL = 50 pF
- Input level: High = 0.9 Vcc, Low = 0.1 Vcc

Note: Symbol “x” in the above table means the period of clock “f_{FPH}”, it’s half period of the system clock “f_{SYS}” for CPU core. The period of f_{FPH} depends on the clock gear setting or the selection of high/low oscillator frequency.

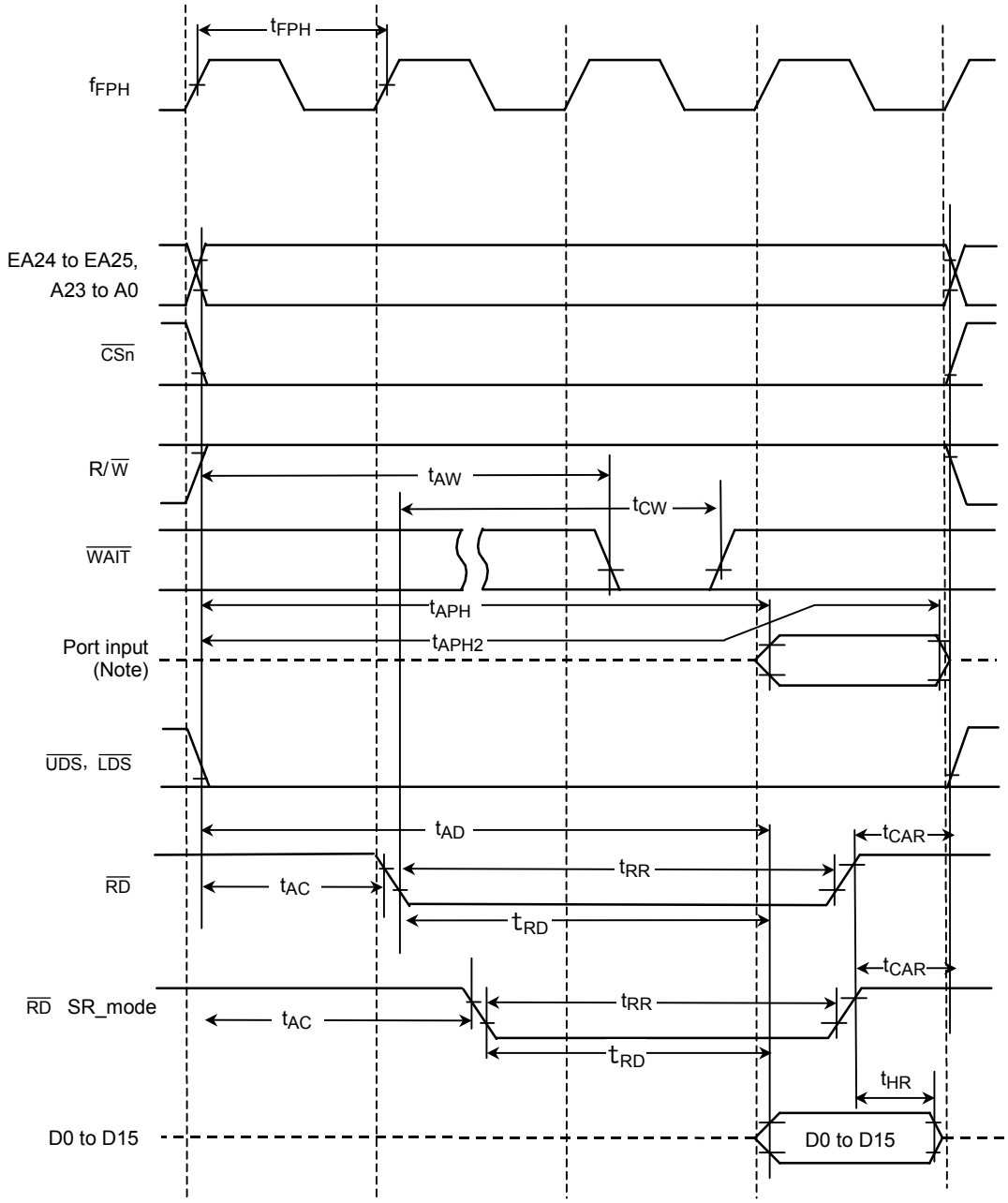
(2) Vcc = 2.0 V ± 10%

No.	Parameter	Symbol	Variable		f_{FPH} = 10 MHz		Unit
			Min	Max	Min	Max	
1	f_{FPH} period (= x)	t_{FPH}	100	31250	100		ns
2	A0 to A23 valid → $\overline{RD}$ / $\overline{WR}$ fall	t_{AC}	x – 46		54		ns
	SR mode (LCDC DMA case: READ only)		1.5x – 46		104		ns
3	$\overline{RD}$ rise → A0 to A23 hold	t_{CAR}	0.5x –30		20		ns
4	$\overline{WR}$ rise → A0 to A23 hold	t_{CAW}	x – 26		74		ns
	$\overline{DS}$ rise → A0 to A23 hold		x – 26		74		ns
5	A0 to A23 valid → D0 to D15 input	t_{AD}		3.5x – 48		302	ns
6	$\overline{RD}$ fall → D0 to D15 input	t_{RD}		2.5x – 48		202	ns
	SR mode (LCDC DMA case)			2.0x – 48		152	ns
7	$\overline{RD}$ low width	t_{RR}	2.5x – 30		220		ns
	SR mode (LCDC DMA case)		2.0x – 30		170		ns
8	$\overline{RD}$ rise → D0 to A15 hold	t_{HR}	0		0		ns
9	$\overline{WR}$ low width	t_{WW}	2.0x – 30		170		ns
	$\overline{DS}$ low width		2.0x – 30		170		ns
10	D0 to D15 valid → $\overline{WR}$ rise	t_{DW}	1.5x – 70		80		ns
	D0 to D15 valid → $\overline{DS}$ rise		1.5x – 70		80		ns
11	$\overline{WR}$ rise → D0 to D15 hold	t_{WD}	x – 50		50		ns
	$\overline{DS}$ rise → D0 to D15 hold		x – 50		50		ns
12	A0 to A23 valid → $\overline{WAIT}$ input (1 + N) WAIT mode	t_{AW}		3.5x – 120		230	ns
13	$\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ hold (1 + N) WAIT mode	t_{CW}	2.5x + 0		250		ns
	SR mode (LCDC DMA case: READ only)		2.0x + 0		200		ns
14	A0 to A23 valid → Port input	t_{APH}		3.5x – 178		172	ns
15	A0 to A23 valid → Port hold	t_{APH2}	3.5x		350		ns
16	A0 to A23 valid → Port valid	t_{APO}		3.5x + 120		470	ns

AC measuring conditions

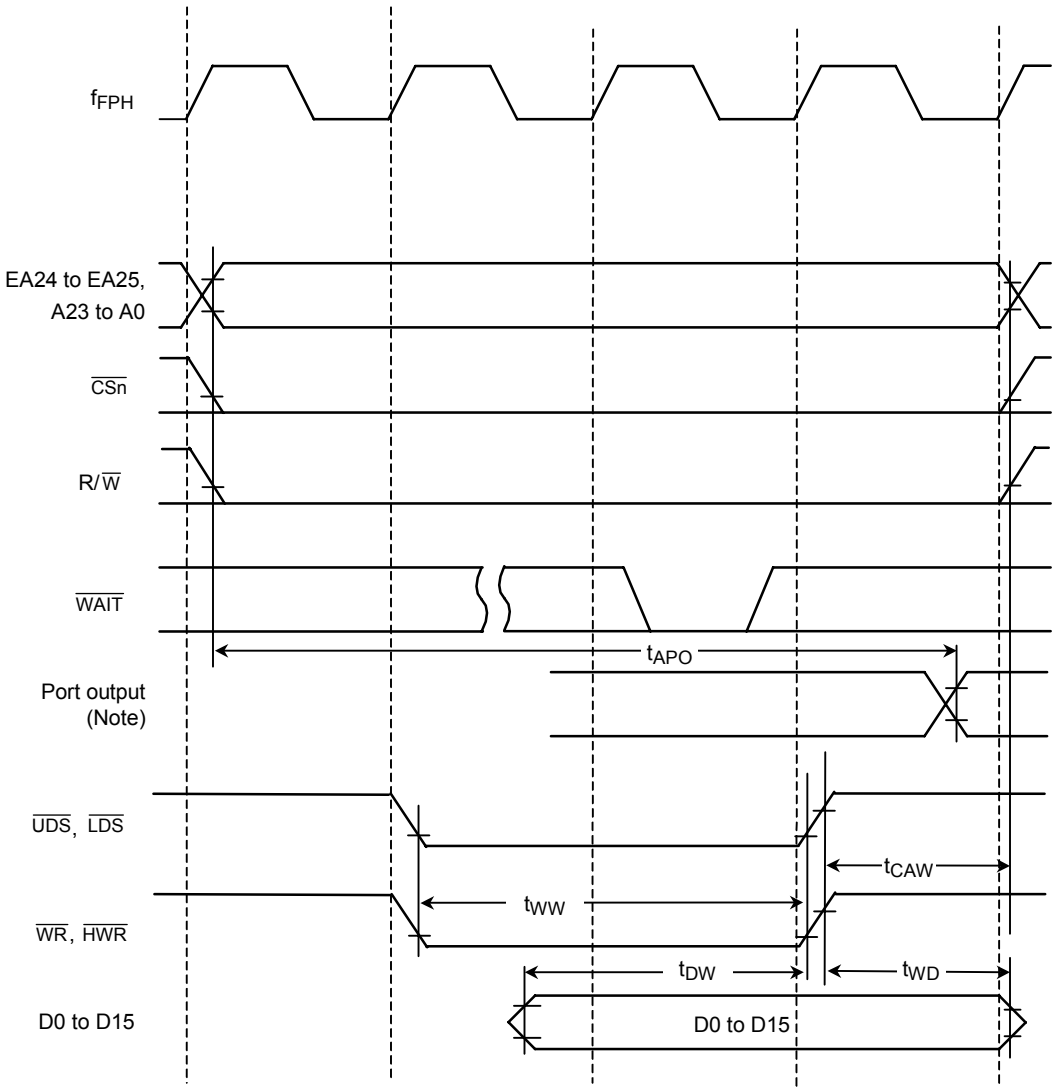
- Output level: High = 0.7 V, Low = 0.3 V, CL = 50 pF
- Input level: High = 0.9 V, Low = 0.1 V

(3) Read cycle



Note: Since the CPU accesses the internal area to read data from a port, the control signals of external pins such as $\overline{RD}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

(4) Write cycle



Note: Since the CPU accesses the internal area to write data to a port, the control signals of external pins such as $\overline{WR}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

(5) Vcc = 3.0 to 3.6 V

No.	Parameter	Symbol	Variable		27 MHz		Unit
			Min	Max	Min	Max	
1	$\overline{RAS}$ cycle time	t_{RC}	4.0x		148		ns
2	$\overline{RAS}$ access time	t_{RAC}		3.0x – 35		76	ns
3	$\overline{CAS}$ access time	t_{CAC}		1.5x – 30		26	ns
4	Column address access time	t_{AA}		2.5x – 45		48	ns
5	After $\overline{UCAS}$, $\overline{LCAS}$ data hold time	t_{OFF1}	0		0		ns
6	$\overline{RAS}$ pre-charge time	t_{RP}	1.5x – 4		52		ns
7	$\overline{RAS}$ pulse width	t_{RAS}	2.5x – 20		73		ns
8	$\overline{RAS}$ hold time	t_{RSH}	1.0x – 15		22		ns
9	$\overline{CAS}$ hold time	t_{CSH}	3.0x – 35		76		ns
10	$\overline{CAS}$ pulse width	t_{CAS}	1.5x – 15		41		ns
11	$\overline{RAS}$ – $\overline{CAS}$ delay time	t_{RCD}	1.5x – 30	1.5x	26	55	ns
12	$\overline{RAS}$ column address delay time	t_{RAD}	0.5x – 3	0.5x + 20	16	38	ns
13	$\overline{CAS}$ – $\overline{RAS}$ pre-charge time	t_{CRP}	1.0x – 25		12		ns
14	$\overline{CAS}$ pre-charge time	t_{CPD}	2.5x – 35		58		ns
15	Row address setup time	t_{ASR}	0.5x – 15		4		ns
16	Row address hold time	t_{RAH}	0.5x – 7		12		ns
17	Column address setup time	t_{ASC}	1.0x – 25		12		ns
18	Column address hold time	t_{CAH}	2.0x – 50		24		ns
19	Column address $\overline{RAS}$ read time	t_{RAL}	2.0x – 30		44		ns
20	Write command $\overline{CAS}$ read time	t_{CWL}	2.0x – 35		39		ns
21	Data output setup time	t_{DS}	0.5x – 17		2		ns
22	Data output hold time	t_{DH}	2.0x – 35		39		ns
23	Write command setup time	t_{WCS}	0.5x – 18		0		ns
24	$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}*1	2.0x – 50		24		ns
25	$\overline{RAS}$ pre-charge $\overline{CAS}$ active time	t_{RPC}	1.5x – 30		26		ns
26	$\overline{CAS}$ setup time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}*	0.5x – 2		17		ns
27	$\overline{RAS}$ pre-charge time (Self refresh)	t_{RPS}*2	4.0x – 16		132		ns
28	$\overline{CAS}$ hold time (Self refresh)	t_{CHS}*2	0		0		ns
29	Refresh setup time	t_{CFL}*	1.0x – 10		27		ns
30	Refresh hold time	t_{CFH}*	1.0x – 15		22		ns
31	Write command pulse width	t_{WP}	2.0x – 40		34		ns
32	Write command hold time	t_{WCH}	1.5x – 35		21		ns
33	$\overline{OE}$ access time 1	t_{OAC1}		2.5x – 50		43	ns
	$\overline{OE}$ access time 2	t_{OAC2}		2.0x – 40		34	ns
34	After $\overline{OE}$ input data hold time	t_{OFF2}	0		0		ns

AC measuring conditions

- Output level: High = 0.7 V, Low = 0.3 V, CL = 50 pF
- Input level: High = 0.9 V, Low = 0.1 V

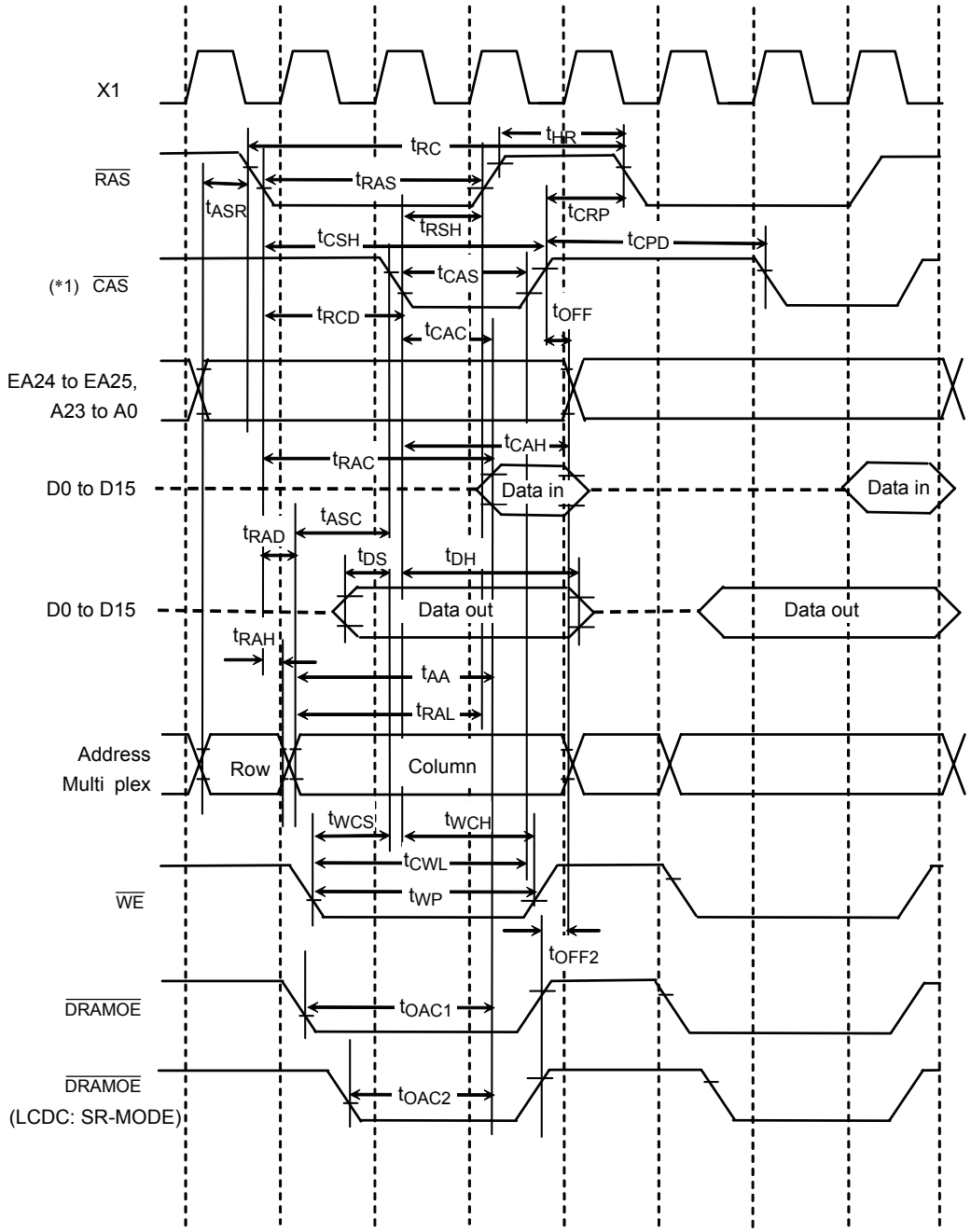
(6) Vcc = 2.7 to 3.6 V

No.	Parameter	Symbol	Variable		27 MHz		Unit
			Min	Max	Min	Max	
1	$\overline{RAS}$ cycle time	t_{RC}	4.0x		148		ns
2	$\overline{RAS}$ access time	t_{RAC}		3.0x – 38		73	ns
3	$\overline{RAS}$ access time	t_{CAC}		1.5x – 38		23	ns
4	Column address access time	t_{AA}		2.5x – 48		45	ns
5	After $\overline{UCAS}$, $\overline{LCAS}$ data hold time	t_{OFF1}	0		0		ns
6	$\overline{RAS}$ pre-charge time	t_{RP}	1.5x – 6		50		ns
7	$\overline{RAS}$ pulse width	t_{RAS}	2.5x – 22		71		ns
8	$\overline{RAS}$ hold time	t_{RSH}	1.0x – 18		19		ns
9	$\overline{CAS}$ hold time	t_{CSH}	3.0x – 33		74		ns
10	$\overline{CAS}$ pulse width	t_{CAS}	1.5x – 13		39		ns
11	$\overline{RAS}$ – $\overline{CAS}$ delay time	t_{RCD}	1.5x – 32	1.5x	24	53	ns
12	$\overline{RAS}$ column address delay time	t_{RAD}	0.5x – 5	0.5x + 20	13	36	ns
13	$\overline{CAS}$ – $\overline{RAS}$ pre-charge time	t_{CRP}	1.0x – 27		10		ns
14	$\overline{CAS}$ pre-charge time	t_{CPD}	2.5x – 37		56		ns
15	Row address setup time	t_{ASR}	0.5x – 16		3		ns
16	Row address hold time	t_{RAH}	0.5x – 8		10		ns
17	Column address setup time	t_{ASC}	1.0x – 27		10		ns
18	Column address hold time	t_{CAH}	2.0x – 52		22		ns
19	Column address $\overline{RAS}$ read time	t_{RAL}	2.0x – 32		42		ns
20	Write command $\overline{CAS}$ read time	t_{CWL}	2.0x – 37		37		ns
21	Data output setup time	t_{DS}	0.5x – 17		2		ns
22	Data output hold time	t_{DH}	2.0x – 37		37		ns
23	Write command setup time	t_{WCS}	0.5x – 18		0		ns
24	$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}*1	2.0x – 52		22		ns
25	$\overline{RAS}$ pre-charge $\overline{CAS}$ active time	t_{RPC}	1.5x – 31		24		ns
26	$\overline{CAS}$ setup time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}*	0.5x – 2		17		ns
27	$\overline{RAS}$ pre-charge time (Self refresh)	t_{RPS}*2	4.0x – 18		130		ns
28	$\overline{CAS}$ hold time (Self refresh)	t_{CHS}*2	0		0		ns
29	Refresh setup time	t_{CFL}*	1.0x – 10		27		ns
30	Refresh hold time	t_{CFH}*	1.0x – 17		20		ns
31	Write command pulse width	t_{WP}	2.0x – 42		32		ns
32	Write command hold time	t_{WCH}	1.5x – 36		20		ns
33	$\overline{OE}$ access time1	t_{OAC1}		2.5x – 53		40	ns
	$\overline{OE}$ access time2	t_{OAC2}		2.0x – 43		31	ns
34	After $\overline{OE}$ input data hold time	t_{OFF2}	0		0		ns

AC measuring conditions

- Output level: High = 0.7 V, Low = 0.3 V, CL = 50 pF
- Input level: High = 0.9 V, Low = 0.1 V

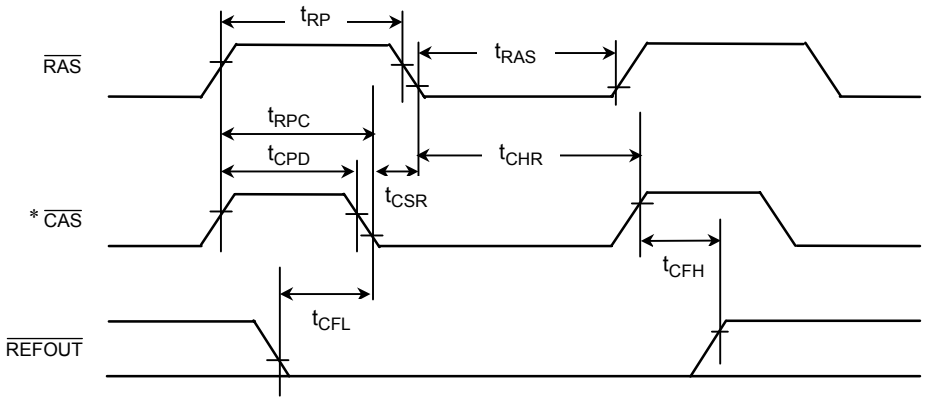
(7) DRAM read/write cycle



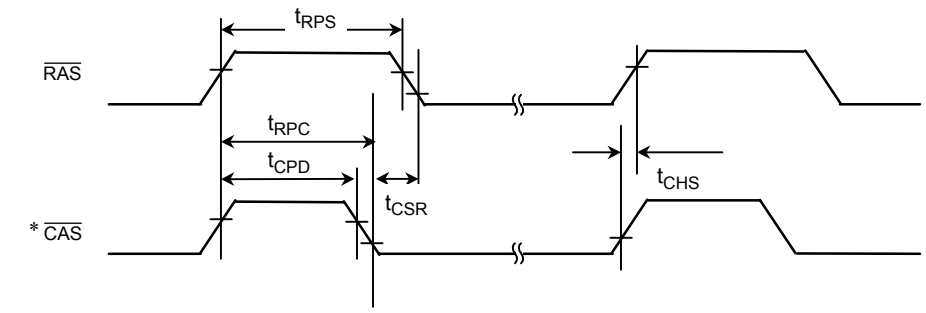
Note: CAS wave form in above figure, shows both of LCAS and UCAS.

(8) DRAM refresh cycle

$\overline{CAS}$ before $\overline{RAS}$ interval refresh cycle



$\overline{CAS}$ before $\overline{RAS}$ self refresh cycle



Note: $\overline{CAS}$ wave form in above figure, shows both of $\overline{LCAS}$ and $\overline{UCAS}$.

4.4 VLD Detect Characteristics

VLDVcc = Vcc, VLDGND = Vss

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
VREF current (Note 4)	IREF	3.6 V ≥ Vcc ≥ 2.7 V VREF = 1.5V		0.2	1	μA
Detect voltage accuracy (VLD0) (Note 1)	ADCTV0	3.6 V ≥ Vcc ≥ 2.7 V Vcc ≥ VLD0 ≥ VLDGND, VREF = 1.5 V (Note 2)	VLD0 × 0.98		VLD0 × 1.02	V
Not-detect voltage accuracy (VLD0) (Note1)	NADCTV0		VLD0 × 0.98		VLD0 × 1.02	V
VLD0 current (Note 3)	IVLD0			0.3	1	μA
Detect voltage accuracy (VLD1) (Note 1)	ADCTV1	3.6 V ≥ Vcc ≥ 2.7 V Vcc ≥ VLD0 ≥ VLDGND, VREF = 1.5 V (Note 2)	VLD0 × 0.98		VLD0 × 1.02	V
Not-detect voltage accuracy (VLD1) (Note 1)	NADCTV1		VLD0 × 0.98		VLD0 × 1.02	V
VLD1 current (Note 3)	IVLD1			0.3	1	μA
Detect voltage accuracy (VLD2) (Note 1)	ADCTV2	3.6 V ≥ Vcc ≥ 2.7 V Vcc ≥ VLD0 ≥ VLDGND, VREF = 1.5 V (Note 2)	VLD0 × 0.98		VLD0 × 1.02	V
Not-detect voltage accuracy (VLD2) (Note1)	NADCTV2		VLD0 × 0.98		VLD0 × 1.02	V
VLD2 current (Note 3)	IVLD2			0.3	1	μA

Note 1: “Detect voltage accuracy” means accuracy of voltage down, “Not-detect voltage accuracy” means accuracy of voltage rise-up.

Note 2: It is prohibit that setting over the Vcc voltage. (Example: Vcc = 2.7 V, Detect Voltage = 2.9 V)

Note 3: It shows highest detect voltage setting by each channel

Note 4: In case detecting voltage only for VLD2 (Vcc = VLD2), the setting “Detecting voltage = 2.6V” is possible.

Note 5: XT (Low-frequency oscillator) operate by Vcc and Vss swing

4.5 Serial Channel Timing (I/O internal mode)

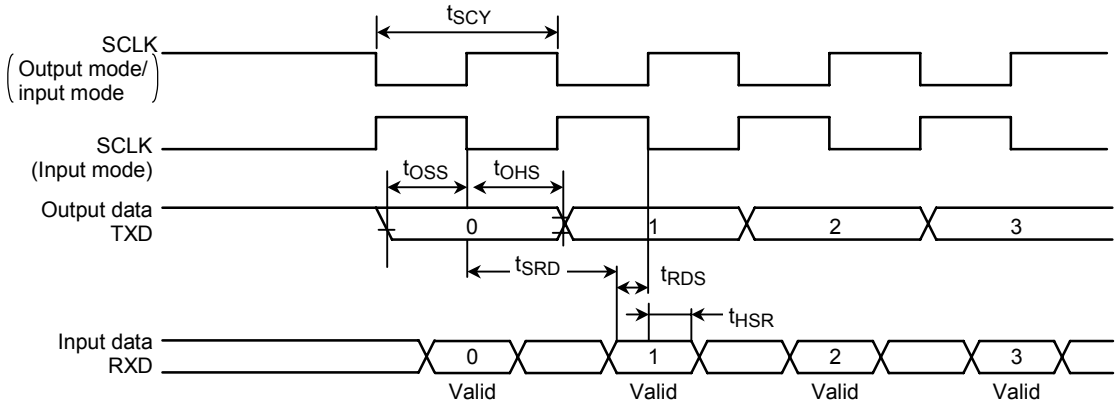
(1) SCLK input mode

Parameter	Symbol	Variable		27 MHz		10 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK period	T_{SCY}	16X		0.59		1.6		μs
Output data → SCLK Rising/falling edge*	T_{OSS}	$t_{SCY}/2 - 4X - 110$ (Vcc = 3 V ± 10%)		334		290		ns
		$t_{SCY}/2 - 4X - 180$ (Vcc = 2 V ± 10%)		–		220		ns
SCLK rising/falling edge* → Output data hold	T_{OHS}	$t_{SCY}/2 + 2X + 0$		370		1000		ns
SCLK rising/falling edge* → Input data hold	T_{HSR}	3X + 10		121		310		ns
SCLK rising/falling edge* → Valid data input	T_{SRD}		$t_{SCY} - 0$		592		1600	ns
Valid data input → SCLK rising/falling edge*	T_{RDS}	0		0		0		ns

(2) SCLK output mode

Parameter	Symbol	Variable		10 MHz		27 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK period (Programmable)	T_{SCY}	16X	8192X	1.6	819	0.59	303	μs
Output data →SCLK rising edge	T_{OSS}	$t_{SCY}/2 - 40$		760		256		ns
SCLK rising edge → Output data hold	T_{OHS}	$t_{SCY}/2 - 40$		760		256		ns
SCLK rising edge → Input data hold	T_{HSR}	0		0		0		ns
SCLK rising edge → Valid data input	T_{SRD}		$t_{SCY}/2 - 1X - 180$		1320		375	ns
Valid data input → SCLK rising/falling edge*	T_{RDS}	1X + 180		280		217		ns

Note: SCLK rinsing/falling edge: The rising edge is used in SCLK rising mode.
The falling edge is used in SCLK falling mode.
Value of 27 MHz and 10 MHz in above table, are that one on t_{SCY} = 16X case



4.6 Interrupt, Capture

(1) $\overline{NMI}$, INT0 to INT3 interrupts

Parameter	Symbol	Variable		10 MHz		27 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{NMI}$, INT0 to INT3 low level width	t_{INTAL}	4X + 40		440		188		ns
$\overline{NMI}$, INT0 to INT3 high level width	t_{INTAH}	4X + 40		440		188		ns

4.7 SCOUT Pin AC Characteristics

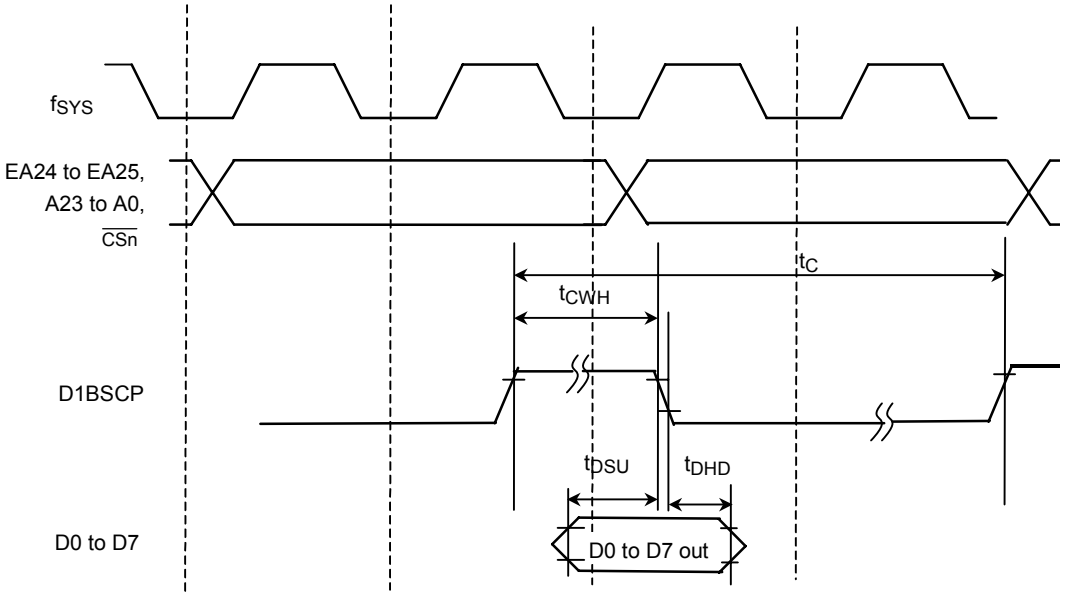
Parameter	Symbol	Variable		10 MHz		27 MHz		Condition	Unit
		Min	Max	Min	Max	Min	Max		
Low level width	t_{SCL}	0.5T − 10		40		8		Vcc ≥ 2.7 V	ns
		0.5T − 30		20		−		Vcc < 2.7 V	
High level width	t_{SCH}	0.5T − 10		40		8		Vcc ≥ 2.7 V	ns
		0.5T − 30		20		−		Vcc < 2.7 V	

Note: T = period of SCOUT

Measuring conditions

- Output level: High = 0.7 V, Low = 0.3 V, CL = 10 pF

4.8 LCD Controller (SR mode)



Read Bus Width	Type	Write Mode	Set Up Time (t_{DSU})	Hold Time (t_{DHD})	Clock High Width (t_{CWH})	Cycle (tc)	State/Cycle
Byte	A	Byte	0.5x – α	1.0x – β	1.5x – γ	4.0x	4.0x
		Nibble	0.5x – α	1.0x – β	1.0x – γ	2.0x	6.0x
		Bit	0.5x – α	1.0x – β	1.0x – γ	2.0x	18.0x
	B	Byte	1.0x – α	0.5x – β	2.0x – γ	4.0x	4.0x
		Nibble	1.0x – α	0.5x – β	1.0x – γ	2.0x	6.0x
		Bit	1.0x – α	0.5x – β	1.0x – γ	2.0x	18.0x
	C	Byte	1.0x – α	2.5x – β	1.5x – γ	6.0x	6.0x
		Nibble	1.0x – α	1.5x – β	2.5x – γ	5.0x	10.0x
		Bit	1.0x – α	1.0x – β	1.0x – γ	2.0x	20.0x
Word	A	Byte	0.5x – α	1.0x – β	1.0x – γ	2.0x	6.0x
		Nibble	0.5x – α	1.0x – β	1.0x – γ	2.0x	10.0x
		Bit	No support. Please use byte read mode.				
	B	Byte	1.0x – α	0.5x – β	1.0x – γ	2.0x	6.0x
		Nibble	1.0x – α	0.5x – β	1.0x – γ	2.0x	10.0x
		Bit	No support. Please use byte read mode				
	C	Byte	1.0x – α	1.5x – β	1.5x – γ	3.0x	8.0x
		Nibble	1.0x – α	1.5x – β	2.5x – γ	5.0x	20.0x
		Bit	No support. Please use byte read mode.				

* Value of alpha, beta and gamma are showed next page.

No.	Parameter	Symbol	Variable		27 MHz		10 MHz		Condition	Unit
			Min	Max	Min	Max	Min	Max		
1	D1BSCP rising-up → Data set up time	t_{DSU}	0.50x – 8		10		42		3.6 V ≥ Vcc ≥ 2.7 V	ns
			0.50x – 20		–		30		Vcc = 2.0 V ± 10%	
			1.00x – 8		29		92		3.6 V ≥ Vcc ≥ 2.7 V	
			1.00x – 20		–		80		Vcc = 2.0 V ± 10%	
2	D1BSCP falling down → Data hold time	t_{DHD}	0.50x – 8		10		42		3.6 V ≥ Vcc ≥ 2.7 V	
			0.50x – 20		–		30		Vcc = 2.0 V ± 10%	
			1.00x – 8		32		92		3.6 V ≥ Vcc ≥ 2.7 V	
			1.00x – 20		–		80		Vcc = 2.0 V ± 10%	
			1.50x – 8		50		142		3.6 V ≥ Vcc ≥ 2.7 V	
			1.50x – 20		–		130		Vcc = 2.0 V ± 10%	
			2.50x – 8		87		242		3.6 V ≥ Vcc ≥ 2.7 V	
			2.50x – 20		–		230		Vcc = 2.0 V ± 10%	
3	D1BSCP → High width	t_{CWH}	1.00x – 5		32		95		3.6 V ≥ Vcc ≥ 2.7 V	
			1.00x – 15		–		85		Vcc = 2.0 V ± 10%	
			1.50x – 5		50		145		3.6 V ≥ Vcc ≥ 2.7 V	
			1.50x – 15		–		135		Vcc = 2.0 V ± 10%	
			2.00x – 5		69		195		3.6 V ≥ Vcc ≥ 2.7 V	
			2.00x – 15		–		185		Vcc = 2.0 V ± 10%	
			2.50x – 5		87		245		3.6 V ≥ Vcc ≥ 2.7 V	
			2.50x – 15		–		235		Vcc = 2.0 V ± 10%	
4	D1BSCP → Clock cycle	t_C	2.00x		74		200		3.6 V ≥ Vcc ≥ 2.7 V	
			2.00x		–		200		Vcc = 2.0 V ± 10%	
			3.00x		111		300		3.6 V ≥ Vcc ≥ 2.7 V	
			3.00x		–		300		Vcc = 2.0 V ± 10%	
			4.00x		148		400		3.6 V ≥ Vcc ≥ 2.7 V	
			4.00x		–		400		Vcc = 2.0 V ± 10%	
			5.00x		185		500		3.6 V ≥ Vcc ≥ 2.7 V	
			5.00x		–		500		Vcc = 2.0 V ± 10%	
			6.00x		222		600		3.6 V ≥ Vcc ≥ 2.7 V	
			6.00x		–		600		Vcc = 2.0 V ± 10%	

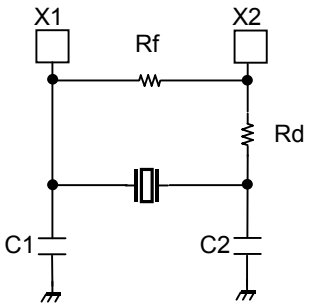
Note: The reading characteristics of display data from the memory which does not define above table, is same as 4.3 “AC Characteristics”.

4.9 Recommended Crystal Oscillation Circuit

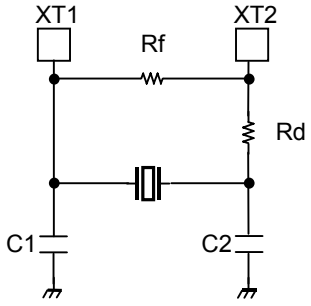
TMP91C016 is evaluated by below oscillator vender. When selecting external parts, make use of this information.

Note: Total loads value of oscillator is sum of external loads (C1 and C2) and floating loads of actual assemble board. There is a possibility of miss-operating using C1 and C2 value in below table. When designing board, it should design minimum length pattern around oscillator. And we recommend that oscillator evaluation try on your actual using board.

(1) Connection example



High-frequency oscillator



Low-frequency oscillator

(2) TMP91C016 recommended ceramic oscillator: Murata Manufacturing. Co., Ltd. (JAPAN)

Circuit parameter recommended

MCU	Oscillation Frequency [MHZ]	Item of Oscillator	Parameter of Elements				Running Condition	
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]	Voltage of Power [V]	Tc [°C]
TMP91C016	2.00	CSTLS2M00G56-B0	(47)	(47)	Open	0	1.8 to 2.2	−40 to +85
	2.50	CSTLS2M50G56-B0	(47)	(47)	Open	0		
	10.00	CSTLS10M0G53-B0	(15)	(15)	Open	0		
	12.50	CSALA12M5T55093-B0	30	30	Open	0		
		CSTLA12M5T55093-B0	(30)	(30)	Open	0		

MCU	Oscillation Frequency [MHZ]	Item of Oscillator	Parameter of Elements				Running Condition	
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]	Voltage of Power [V]	Tc [°C]
TMP91C016	4.00	CSTLS4M00G56-B0	(47)	(47)	Open	0	2.7 to 3.6	−40 to +85
	6.750	CSTLS6M75G56-B0	(47)	(47)	Open	0		
	12.50	CSALA12M5T55-B0	30	30	Open	0		
		CSTLA12M5T55-B0	(30)	(30)	Open	0		
	20.00	CSALS20M0X53-B0	5	5	Open	0		
		CSTLS20M0X51-B0	(5)	(5)	Open	0		
	27.00	CSALS27M0X51-B0	Open	Open	10K	0		
	32.00	CSALA32M0X51-B0	3	3	Open	0		

- The valves enclosed blackest in C1 and C2 columns apply to condenser built-in type.
- The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change.
  For up-to-date information, please refer to the following URL:
  http://www.murata.co.jp/search/index.html