CMOS 8-BIT MICROCONTROLLERS
TMP91C640N/TMP91C641N
TMP91C640F /TMP91C641F

1. OUTLINE AND CHARACTERISTICS

The TMP91C640 is a high-speed advanced 8-bit micro controller applicable to a variety of equipment.

With its 8-bit CPU, ROM, RAM, A/D converter, multi-function timer/event counter and general-purpose serial interface integrated into a single CMOS chip, the TMP91C640 allows the expansion of external memories for programs (up to 48K byte) and data (1M byte). The TMP91C641 is the same as the TMP91C640 but without the ROM.

The TMP91C640N/641N is a 64-pin shrink DIP product. (SDIP64-P-750)

The TMP91C640F/641F is a 64-pin flat package product. (QFP64-P-1420A)

The characteristics of the TMP91C640 include:

(1) Powerful instructions
163 basic instructions, including
Multiplication, division, 16-bit arithmetic operations, bit manipulation instructions
(2) Minimum instruction executing time: 320 ns (at 12.5 MHz oscillation frequency)
(3) Internal ROM: 16K byte (The TMP91C641 does not have a built-in ROM.)
(4) Internal RAM: 512 byte
(5) Memory expansion
Program memory: 64K byte
Data memory: 1M byte
(6) 8-bit A/D converter (6 channels)
(7) General-purpose serial interface (1 channel)
Asynchronous mode, I/O interface mode
(8) Multi-function 16-bit timer/event counter (1 channel)
(9) 8-bit timers (4 channels)
(10) Stepping motor control port (2 channels)
(11) Input/Output ports (54 pins)
(12) Interrupt function: 10 internal interrupts and 4 external interrupts
(13) Micro Direct Memory Access (μDMA) function (11 channels)
(14) Watchdog timer
(15) Standby function (4 HALT modes)

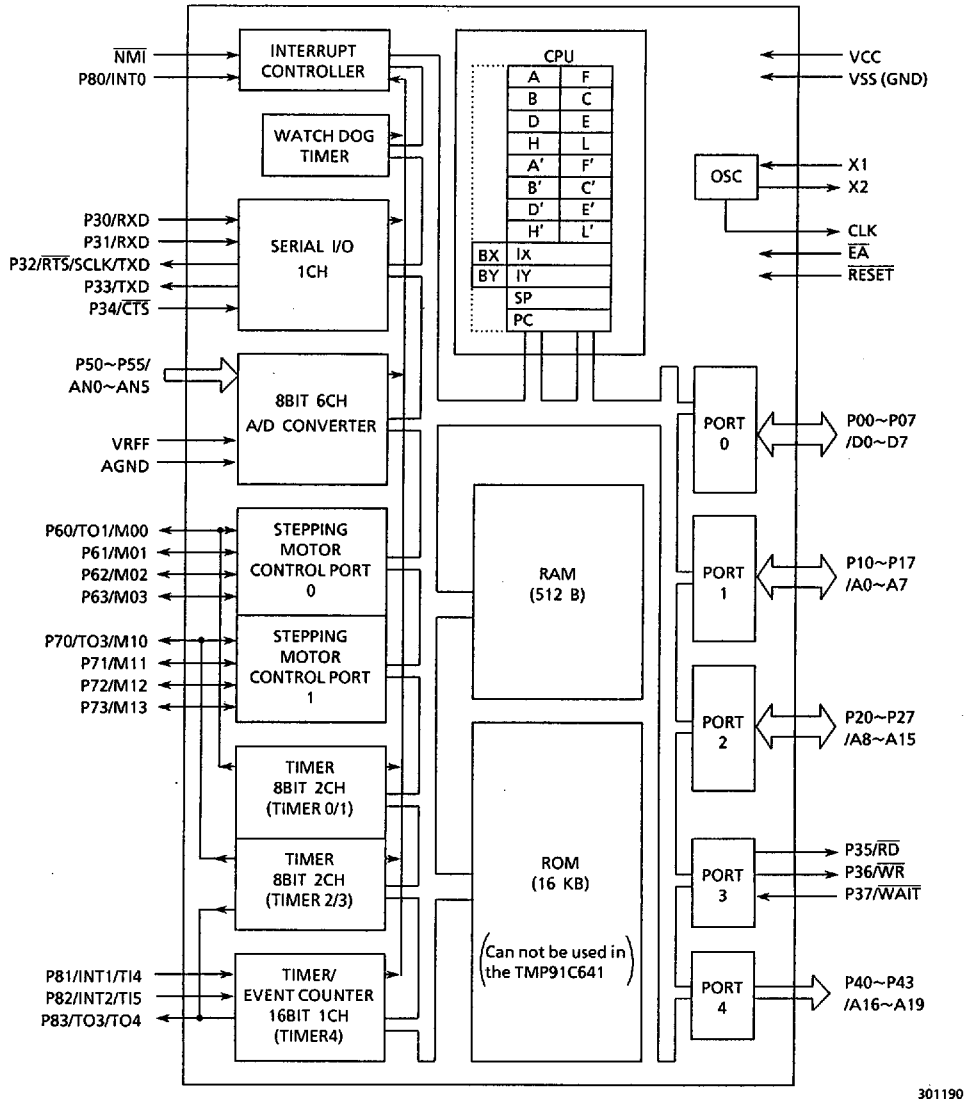

Figure 1 TMP91C640 Block Diagram

2. PIN ASSIGNMENT AND FUNCTIONS

The assignment of input/output pins, their names and functions are described below.

2.1 Pin Assignment

Figure 2.1-(1) shows pin assignment of the TMP91C640N/641N.

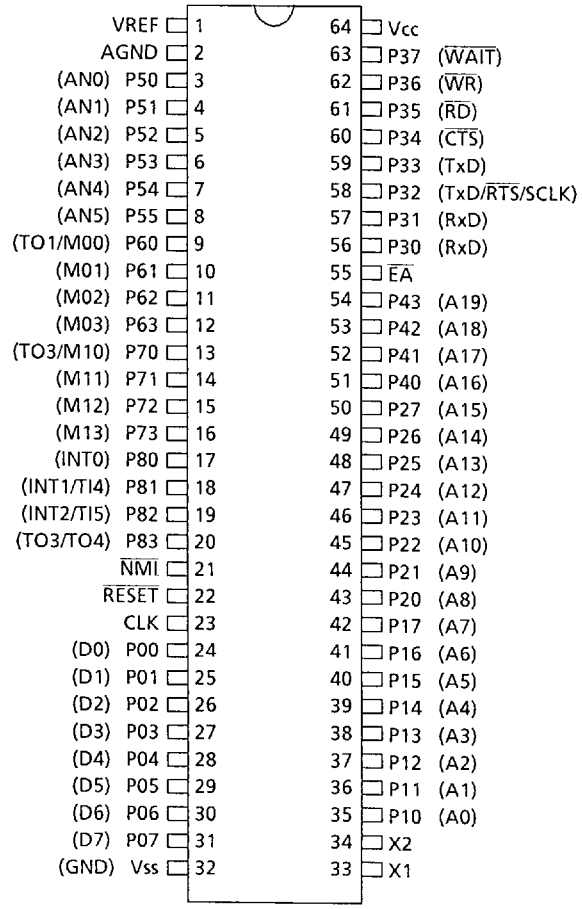

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Figure 2.1-(1) Pin Assignment (Shrink Dual Inline Package)

Figure 2.1-(2) shows pin assignment of the TMP91C640F/641F.

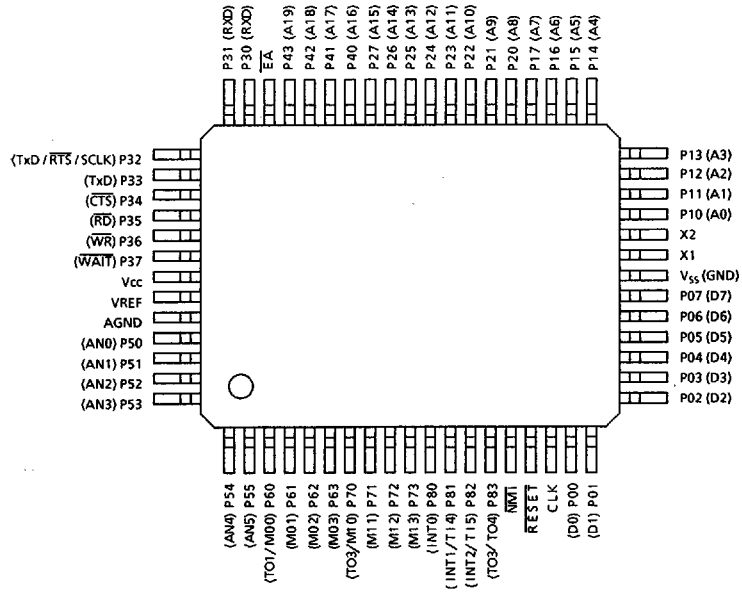

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Figure 2.1- (2) Pin Assignment (Flat Package)

2.2 Pin Names and Functions

The names of input/output pins and their functions are summarized in Table 2.2.

Table 2.2 Pin Names and Functions (1/2)

Pin Name	No. of pins	I/O 3 states	Function
P00~P07	8	I/O	Port 0: 8-bit I/O port that allows selection of input/output on byte basis
/D0~D7		3 states	Data bus: Also functions as 8-bit bidirectional data bus for external memory
P10~P17	8	I/O	Port 1: 8-bit I/O port that allows selection on byte basis
/A0~A7		Output	Address bus: The lower 8 bits address bus for external memory
P20~P27	8	I/O	Port 2: 8-bit I/O port that allows selection on bit basis
/A8~A15		Output	Address bus: The upper 8 bits address bus for external memory
P30	1	Input	Port 30: 1-bit input port
/RxD			Receiver Serial Data
P31	1	Input	Port 31: 1-bit input port
/RxD			Receiver Serial Data
P32	1	Output	Port 32: 1-bit output port
/TxD			Transmitter serial Data
/$\overline{RTS}$			Request to send serial data
/SCLK			Serial clock output
P33	1	Output	Port 33: 1-bit output port
/TxD			Transmitter Serial Data
P34	1	Input	Port 34: 1-bit input port
/$\overline{CTS}$			Clear to send Serial data
P35	1	Output	Port 35: 1-bit output port
/$\overline{RD}$			Read: Generates strobe signal for reading external memory
P36	1	Output	Port 36: 1-bit output port
/$\overline{WR}$			Write: Generates strobe signal for writing into external memory
P37	1	Input	Port 37: 1-bit input port
/$\overline{WAIT}$			Wait: Input pin for connecting slow speed memory or peripheral LSI
P40~P43	4	Output	Port 4: 4-bit output port that allows selection of Port/Address Bus on bit basis
/A16~A19			Address bus: Also functions as address bus for external memory (4 bits of bank address)
P50~P55	6	Input	Port 5: 6-bit input port
/AN0~AN5			Analog input: 6 analog inputs to A/D converter
VREF	1		Input of reference voltage to A/D converter

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Table 2.2 Pin Names and Functions (2/2)

Pin Name	No. of pins	I/O 3 states	Function
AGND	1		Ground pin for A/D converter
P60~P63 /M00~M03 /TO1	4	I/O	Port 6: 4-bit I/O port that allows I/O selection on bit basis
		Output	Stepping motor control port 0
		Output	Timer output 1: Output of Timer 0 or 1
P70~P73 /M10~M13 /TO3	4	I/O	Port 7: 4-bit I/O port that allows I/O selection on bit basis
		Output	Stepping motor control port 1
		Output	Timer output 3: Output of Timer 2 or 3
P80 /INT0	1	Input	Port 80: 1-bit input port
			Interrupt request pin 0: interrupt request pin (Level/rising edge is programmable)
P81 /INT1 /TI4	1	Input	Port 81: 1-bit input port
			Interrupt request pin 1: interrupt request pin (Rising/falling edge is programmable)
			Timer input 4: Counter/capture trigger signal for Timer 4
P82 /INT2 /TI5	1	Input	Port 82: 1-bit input port
			Interrupt request pin 2: rising edge interrupt request pin
			Timer input 5: capture trigger signal for Timer 4
P83 /TO3 /TO4	1	Output	Port 83: 1-bit output port
			Timer output 3/4: Output of Timer 2, 3 or 4
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Falling edge interrupt request pin
CLK	1	Output	Clock output: Generates clock pulse at 1/4 frequency of clock oscillation. It is Pulled up internally during resetting.
$\overline{EA}$	1	Input	External access: Connects with Vcc pin in the TMP91C640 using internal ROM, and with GND pin in the TMP91C641 with no internal ROM.
$\overline{RESET}$	1	Input	Reset : Initializes the TMP91C640/641. (Built-in pull-up resister)
X1/X2	2	Input/ Output	Pin for quartz crystal or ceramic resonator
Vcc	1		Power supply (+ 5V)
Vss (GND)	1		Ground (0V)

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3. OPERATION

The following explains the TMP91C640 functions and basic operations. The CPU functions and internal I/O functions of the TMP91C640 are the same as the TMP90C840A.

Refer to the "TMP90C840A" section concering functions which are not explained the following.

3.1 CPU

The TMP91C640 has a internal high-performance 8-bit CPU.

Refer to the "TLCS-90 CPU" section concering CPU operation.

3.2 Memory Map

The TMP91C640 supports a program memory of up to 64K bytes and a data memory of maximum 1M bytes.

The program memory may be assigned to the address space from 00000H to 0FFFFH, while the data memory can be allocated to any address from 00000H to FFFFFH.

(1) Internal ROM

The TMP91C640 internally contains an 16K-byte ROM. The address space from 0000H to 3FFFH is provided to the ROM. The CPU starts executing a program from 0000H by resetting.

The addresses 0010H to 007FH in this internal ROM area are used for the entry area for the interrupt processing.

The TMP91C641 does not have a built-in ROM; therefore, the address space 0000H ~3FFFH is used as external memory space.

(2) Internal RAM

The TMP91C640 also contains a 512 byte RAM, which is allocated to the address space from FDC0H to FFBFH. The CPU allows the access to a certain RAM area (FF00H to FFBFH, 192 bytes) by a short operation code (opcode) in a "direct addressing mode".

The addresses from FF10H to FF7FH in this RAM area can be used as parameter area for micro DMA processing (and for any other purposes when the micro DMA function is not used).

(3) Internal I/O

The TMP91C640 provides a 48-byte address space as an internal I/O area, whose addresses range from FFC0H to FFEFH. This I/O area can be accessed by the CPU using a short opcode in the "direct addressing mode".

Figure 3.1 (1) is a memory map indicating the areas accessible by the CPU in the respective addressing mode.

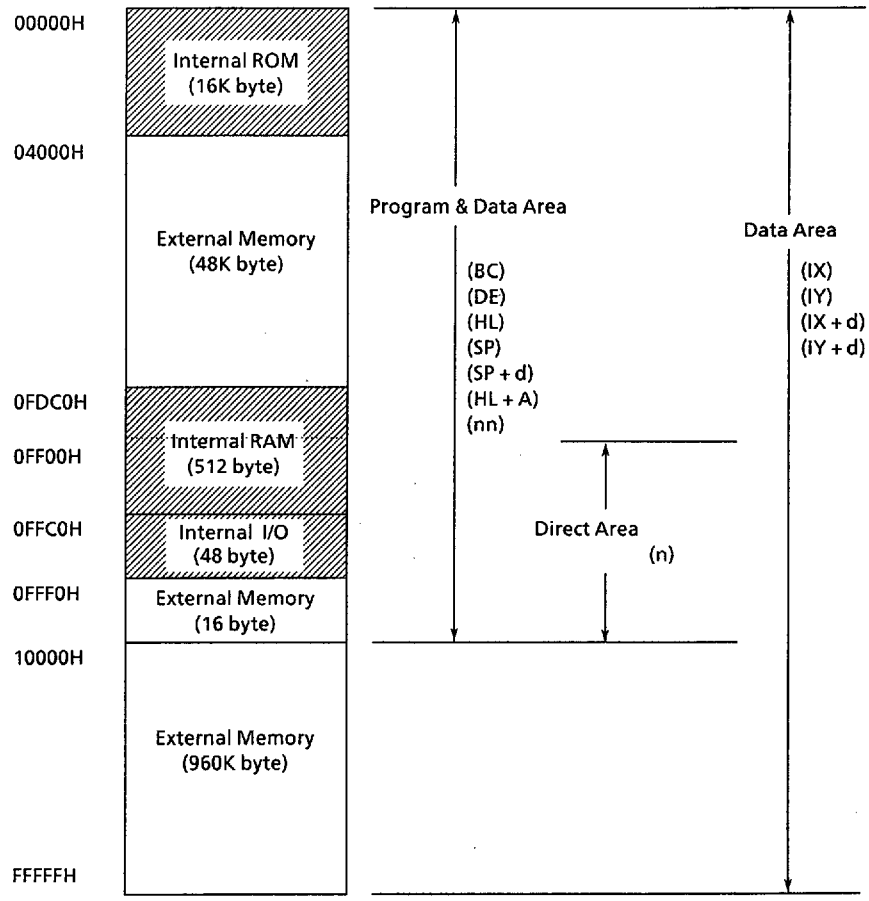

Figure 3.1 (1) Memory Map

4. ELECTRICAL CHARACTERISTICS

TMP91C640N/TMP91C640F/TMP91C641N/TMP91C641F

4.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Supply voltage	− 0.5 ~ + 7	V
V_{IN}	Input voltage	− 0.5 ~ Vcc + 0.5	V
P_D	Power dissipation (Ta = 85°C)	F 500	mW
		N 600	
T_{SOLDER}	Soldering temperature (10 s)	260	℃
T_{STG}	Storage temperature	− 65 ~ 150	℃
T_{OPR}	Operating temperature	− 40 ~ 85	℃

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4.2 DC Characteristics

Vcc = 5V ± 10% TA = − 40~85°C (1~10MHz)
TA = − 20~70°C (10~12.5MHz)
Typical Values are for TA = 25°C V_{CC} = 5V.

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (P0)	− 0.3	0.2Vcc − 0.1	V	
V_{IL1}	P1, P2, P3, P4, P5, P6, P7, P8	− 0.3	0.3Vcc	V	
V_{IL2}	$\overline{RESET}$, INT0 (P80), $\overline{NMI}$	− 0.3	0.25Vcc	V	
V_{IL3}	$\overline{EA}$	− 0.3	0.3	V	
V_{IL4}	X1	− 0.3	0.2Vcc	V	
V_{IH}	Input High Voltage (P0)	0.2Vcc + 1.1	Vcc + 0.3	V	
V_{IH1}	P1, P2, P3, P4, P5, P6, P7, P8	0.7Vcc	Vcc + 0.3	V	
V_{IH2}	$\overline{RESET}$, INT0 (P80), $\overline{NMI}$	0.75Vcc	Vcc + 0.3	V	
V_{IH3}	$\overline{EA}$	Vcc − 0.3	Vcc + 0.3	V	
V_{IH4}	X1	0.8Vcc	Vcc + 0.3	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 1.6mA
V_{OH} V_{OH1} V_{OH2}	Output High Voltage	2.4 0.75Vcc 0.9Vcc		V V V	I_{OH} = − 400μA I_{OH} = − 100μA I_{OH} = − 20μA
I_{DAR}	Darlington Drive Current (8 I/O pins) (Note)	− 1.0	− 3.5	mA	V_{EXT} = 1.5V R_{EXT} = 1.1 kΩ
I_{LI}	Input Leakage Current	0.02 (Typ)	± 5	μA	0.0 ≦ Vin ≦ Vcc
I_{LO}	Output Leakage Current	0.05 (Typ)	± 10	μA	0.2 ≦ Vin ≦ Vcc − 0.2
I_{CC}	Operating Current (RUN) Idle 1 Idle 2	20 (Typ) 1.5 (Typ) 9 (Typ)	40 5 15	mA mA mA	tosc = 10MHz (25%Up @12.5MHz)
	STOP (TA = − 40~85°C) STOP (TA = 0~50°C)	0.2 (Typ)	50 10	μA μA	0.2 ≦ Vin ≦ Vcc − 0.2
V_{STOP}	Power Down Voltage (@STOP)	2 RAM BACK UP	6	V	V_{IL2} = 0.2Vcc, V_{IH2} = 0.8Vcc
R_{RST}	$\overline{RESET}$ Pull Up Registor	50	150	kΩ	
CIO	Pin Capacitance		10	pF	testfreq = 1MHz
V_{TH}	Schmitt width $\overline{RESET}$, $\overline{NMI}$, INT0	0.4	1.0 (Typ)	V	

Note : I_{DAR} is guaranteed for a total of up to 8 optional ports. 040789

4.3 AC Characteristics

Vcc = 5V ± 10% TA = −40~85°C (1~10MHz)
CL = 50pF TA = −20~70°C (10~12.5MHz)

Symbol	Parameter	Variable		10MHz Clock		12.5MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{OSC}	OSC. Period = x	80	1000	100		80		ns
t_{CYC}	CLK Period	4x	4x	400		320		ns
t_{WL}	CLK Low width	2x − 40		160		120		ns
t_{WH}	CLK High width	2x − 40		160		120		ns
t_{AC}	Address Setup to $\overline{RD}$, $\overline{WR}$	x − 45		55		35		ns
t_{RR}	$\overline{RD}$ Low width	2.5x − 40		210		160		ns
t_{CA}	Address Hold Time After $\overline{RD}$, $\overline{WR}$	0.5x − 30		20		10		ns
t_{AD}	Address to Valid Data In		3.5x − 95		255		185	ns
t_{RD}	$\overline{RD}$ to Valid Data In		2.5x − 80		170		120	ns
t_{HR}	Input Data Hold After $\overline{RD}$	0		0		0		ns
t_{WW}	$\overline{WR}$ Low width	2.5x − 40		210		160		ns
t_{DW}	Data Setup to $\overline{WR}$	2x − 50		150		110		ns
t_{WD}	Data Hold After $\overline{WR}$	30	90	30	90	30	90	ns
t_{CWA}	$\overline{RD}$, $\overline{WR}$ to Valid $\overline{WAIT}$		1.5x − 100		50		20	ns
t_{AWA}	Address to Vaild $\overline{WAIT}$		2.5x − 130		120		70	ns
t_{WAS}	$\overline{WAIT}$ Setup to CLK	70		70		70		ns
t_{WAH}	$\overline{WAIT}$ Hold After CLK	0		0		0		ns
t_{RV}	$\overline{RD}$, $\overline{WR}$ Recovery Time	1.5x − 35		115		85		ns
t_{CPW}	CLK to Port Data Output		x + 200		300		280	ns
t_{PRC}	Port Data Setup to CLK	200		200		200		ns
t_{CPR}	Port Data Hold After CLK	100		100		100		ns
t_{CHCL}	$\overline{RD}$ / $\overline{WR}$ Hold After CLK	x − 60		40		20		ns
t_{CLC}	$\overline{RD}$ / $\overline{WR}$ Setup to CLK	1.5x − 50		100		70		ns
t_{CLHA}	Address Hold After CLK	1.5x − 80		70		40		ns
t_{ACL}	Address Setup to CLK	2.5x − 80		170		120		ns
t_{CLD}	Data Setup to CLK	x − 50		50		30		ns

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- AC output level High 2.2V/Low 0.8V
- AC input level High 2.4V/Low 0.45V (D0 − D7)
  High 0.8Vcc/Low 0.2Vcc (excluding D0 − D7)

4.4 A/D Conversion Characteristics

Vcc = 5V ± 10% TA = −40~85°C (1~10MHz)
TA = −20~70°C (10~12.5MHz)

Symbol	Parameter	Min	Typ	Max	Unit
V_{REF}	Analog reference voltage	Vcc − 1.5	Vcc	Vcc	V
A_{GND}	Analog reference voltage	V_{SS}	V_{SS}	Vss	
V_{AIN}	Allowable analog input voltage	V_{SS}		Vcc	
I_{REF}	Supply current for analog reference voltge		0.5	1.0	mA
Error	Total error (TA = 25°C, $V_{CC} = V_{REF} = 5.0V$)		1.0		LSB
	Total error			2.5	

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4.5 Zero- Cross Characteristics

Vcc = 5V ± 10% TA = −40~85°C (1~10MHz)
TA = −20~70°C (10~12.5MHz)

Symbol	Parameter	Condition	Min	Max	Unit
Vzx	Zero- cross detection input	AC coupling C = 0.1μF	1	1.8	VAC p − p
Azx	Zero- cross accuracy	50/60Hz sine wave		135	mV
Fzx	Zero- cross detection input frequency		0.04	1	kHz

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4.6 Serial Channel Timing – I/O Interface Mode

Vcc = 5V ± 10% TA = −40~85°C (1~10MHz)
CL = 50pF TA = −20~70°C (10~12.5MHz)

Symbol	Parameter	Variable		10MHz Clock		12.5MHz Clock		Units
		Min	Max	Min	Max	Min	Max	
t_{SCY}	Serial Port Clock Cycle Time	8x		800		640		ns
t_{OSS}	Output Data Setup SCLK Rising Edge	6x − 150		450		330		ns
t_{OHS}	Output Data Hold After SCLK Rising Edge	2x − 120		80		40		ns
t_{HSR}	Input Data Hold After SCLK Rising Edge	0		0		0		ns
t_{SRD}	SCLK Rising Edge to Input DATA Valid		6x − 150		450		330	ns

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4.7 16-bit Event Counter

Vcc = 5V ± 10% TA = −40~85°C (1~10MHz)
TA = −20~70°C (10~12.5MHz)

Symbol	Parameter	Variable		10MHz Clock		12.5MHz Clock		Units
		Min	Max	Min	Max	Min	Max	
t_{VCK}	TI4 clock cycle	8x + 100		900		740		ns
t_{VCKL}	TI4 Low clock pulse width	4x + 40		440		360		ns
t_{VCKH}	TI4 High clock pulse width	4x + 40		440		360		ns

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4.8 Interrupt Operation

Vcc = 5V ± 10% TA = −40~85℃ (1~10MHz)
TA = −20~70℃ (10~12.5MHz)

Symbol	Parameter	Variable		10MHz Clock		12.5MHz Clock		Units
		Min	Max	Min	Max	Min	Max	
t_{INTAL}	$\overline{NMI}$, INT0 Low level pulse width (⊓)	4x		400		320		ns
t_{INTAH}	$\overline{NMI}$, INT0 High level pulse width (⊔)	4x		400		320		ns
t_{INTBL}	INT1, INT2 Low level pulse width (⊓)	8x + 100		900		740		ns
t_{INTBH}	INT1, INT2 High level pulse width (⊔)	8x + 100		900		740		ns

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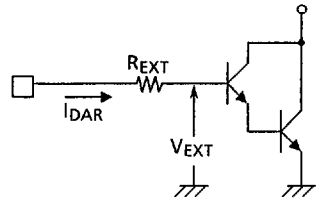
(Reference) Definition of I_{DAR}



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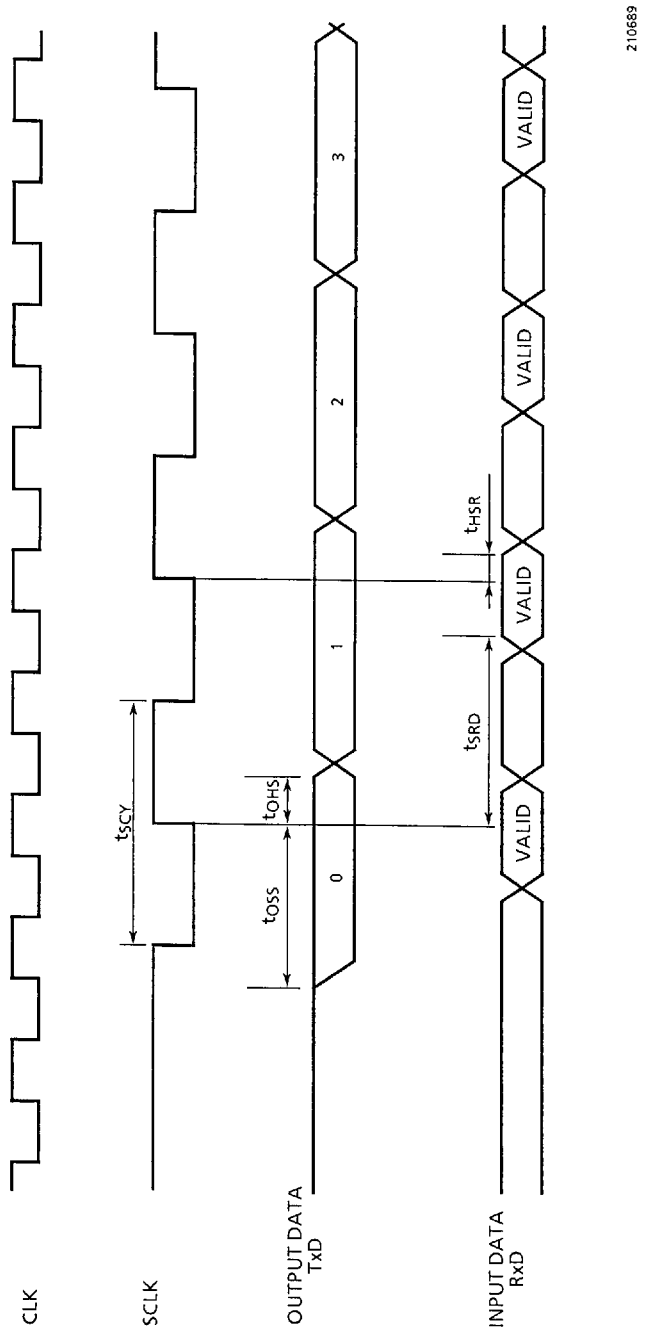
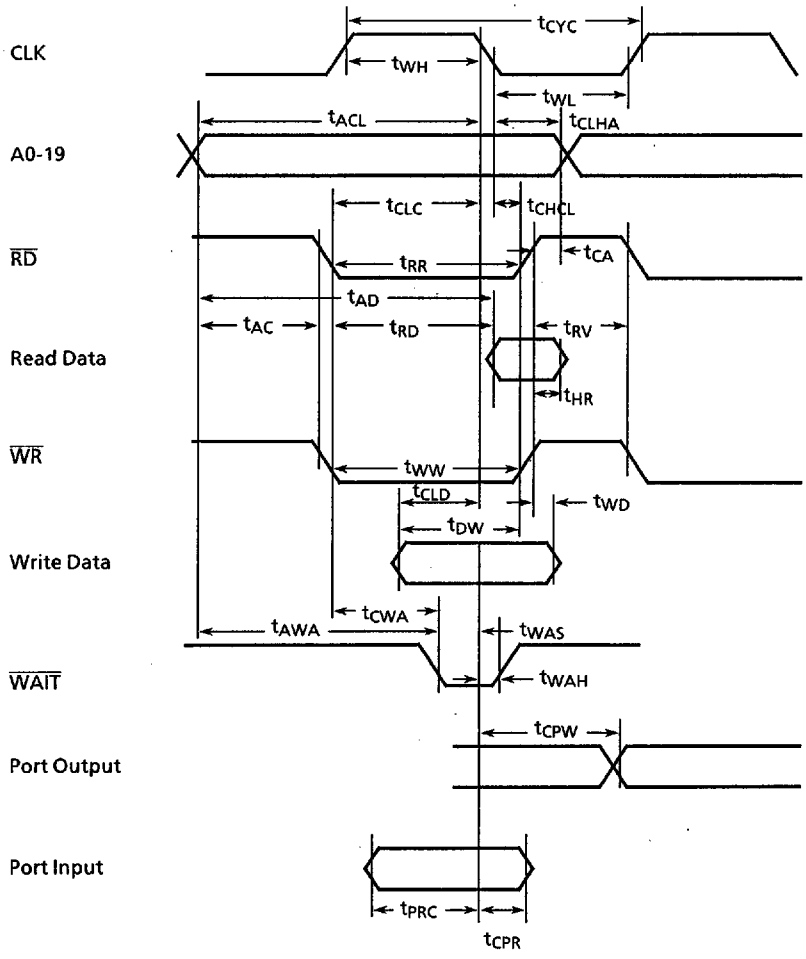
4.9 I/O Interface Mode Timing Chart



TMP91C640 I/O Interface Mode Timing Waveforms

4.10 Timing Chart



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