TOSHIBA

TOSHIBA Original CMOS 8-Bit Microcontroller

# TLCS-900/L1 Series

## TMP91CW12

TOSHIBA CORPORATION

Semiconductor Company

CMOS 16-Bit Microcontroller

# TMP91CW12F

## 1. Outline and Features

TMP91CW12 is a high-speed 16-bit microcontroller designed for the control of various mid-to-large scale equipment.

TMP91CW12F comes in a 100-pin flat package.

Listed below are the features.

(1) High-speed 16-bit CPU (900/L1 CPU)
- Instruction mnemonics are upward-compatible with TLCS-90/900
- 16 Mbytes of linear address space
- General-purpose registers and register banks
- 16-bit multiplication and division instructions; bit transfer and arithmetic instructions
- Micro DMA: Four-channels (1.0$\mu$s/2 bytes at 16MHz)

(2) Minimum instruction execution time : 250ns (at 16MHz)

(3) Built-in RAM: 4 Kbytes
Built-in ROM: 128 Kbytes

(4) External memory expansion
- Expandable up to 16 Mbytes (Shared program/data area)
- Can simultaneously support 8-/16-bit width external data bus
  ··· Dynamic data bus sizing

(5) 8-bit timers: 8 channels

(6) 16-bit timer/event counter: 2 channels



(7) General-purpose serial interface: 2 channels
- UART/Synchronous mode: 2 channels
- IrDA Ver.1.0 (115.2 kbps) mode selectable: 1 channel

(8) Serial bus interface: 1 channel
- $I^2C$ bus mode/clock synchronous mode selectable

(9) 10-bit AD converter: 8 channels

(10) Watchdog timer

(11) Timer for real-time clock (RTC)

(12) Chip select/wait controller: 4 blocks

(13) Interrupts: 45 interrupts
- 9 CPU interrupts: Software interrupt instruction and illegal instruction
- 26 internal interrupts: ] Seven selectable priority levels
- 10 external interrupts: ]

(14) Input/output ports: 81 pins

(15) Standby mode
- Three HALT modes: Programmable-IDLE2, IDLE1, STOP

(16) Triple clock controller
- Clock doubler (DFM) circuit is inside
- Clock gear function: Selectable a high-frequency clock fc/1 to fc/16
- RTC (fs = 32.768 kHz)

(17) Operating voltage
- $V_{CC}$ = 2.7 to 5.5 V (fc max = 16 MHz)
- $V_{CC}$ = 4.5 to 5.5 V (fc max = 25 MHz)

(18) Package
- 100-pin QFP: P-LQFP100-1414-0.50C

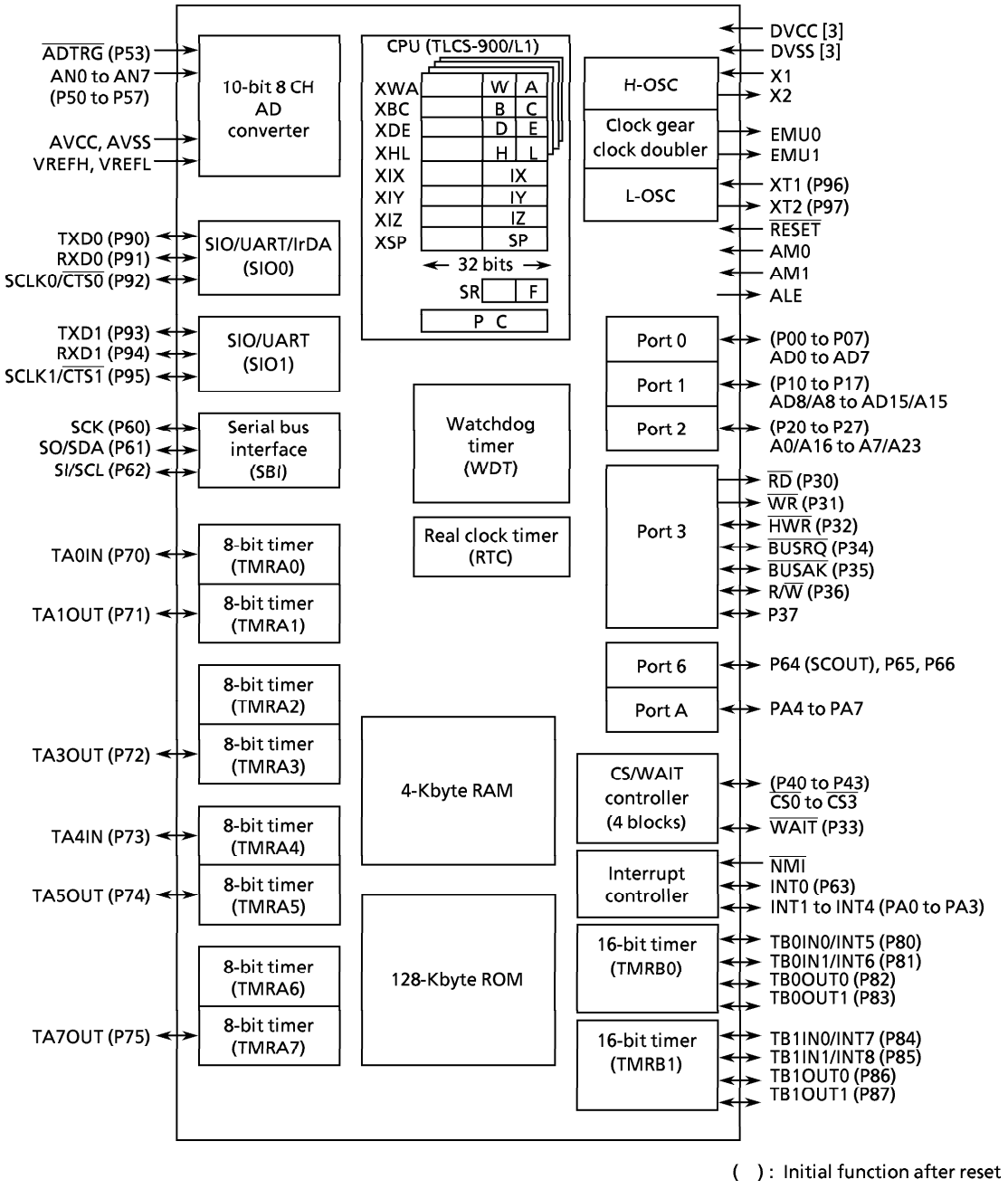



Figure 1.1 TMP91CW12 Block Diagram

## 2. Pin Assignment and Pin Functions

This section shows the TMP91CW12F pin assignment, and the names and an outline of the functions of the input/output pins.

### 2.1 Pin Assignment Diagram

Figure 2.1.1 is a pin assignment diagram for TMP91CW12F.

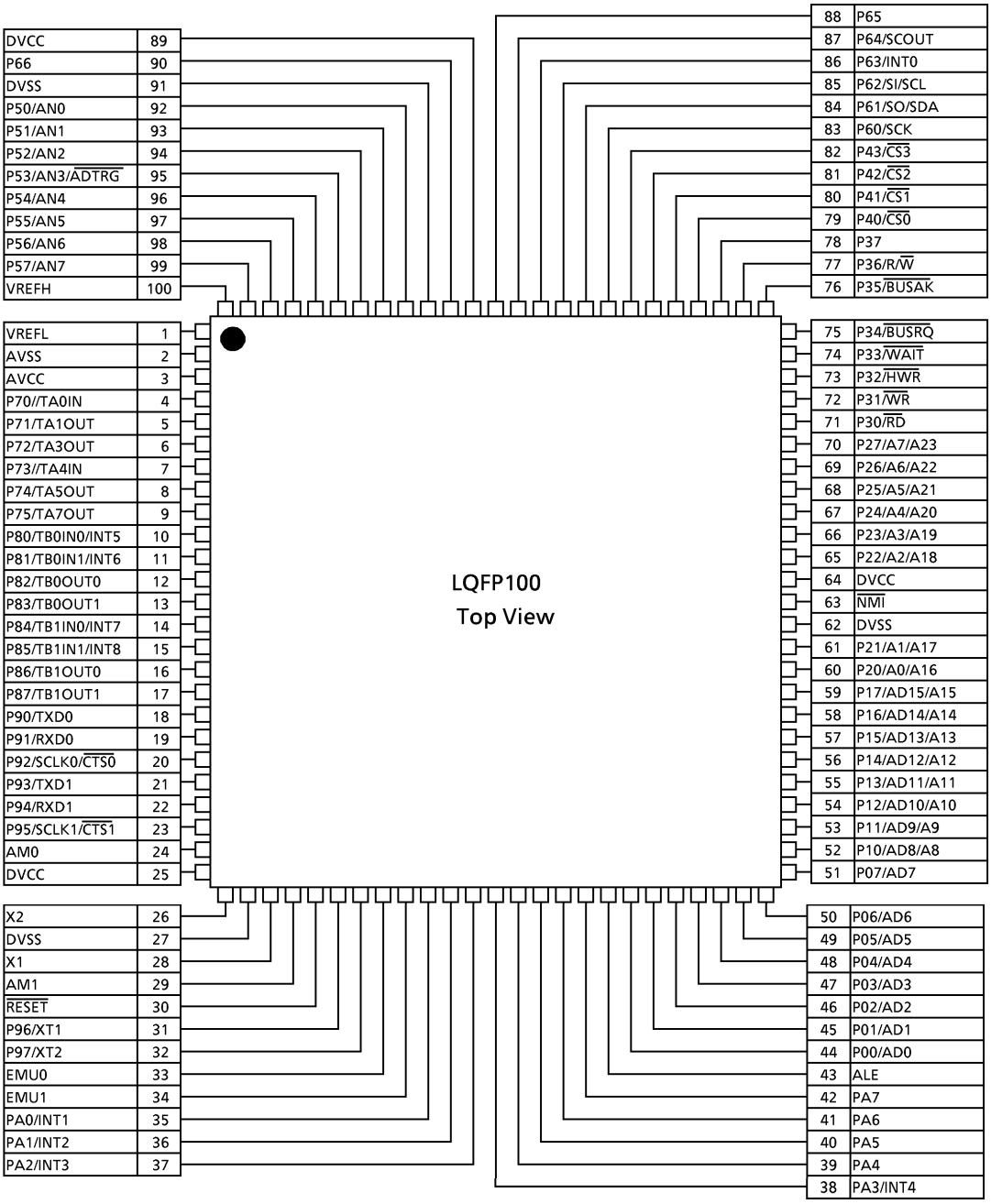



Figure 2.1.1 Pin Assignment Diagram (100-pin LQFP)

## 2.2 Pin Names and Functions

The names of the input/output pins and their functions are described below.
Table 2.2.1 Pin Names and Functions.

Table 2.2.1 Pin Names and Functions (1/4)

| Pin Name | Number of Pins | I/O | Functions |
|---|---|---|---|
| P00 to P07<br>AD0 to AD7 | 8 | I/O<br>Tri-state | Port 0: I/O port that allows I/O to be selected at the bit level<br>Address and data (Lower): Bits 0 to 7 for address and data bus |
| P10 to P17<br>AD8 to AD15<br>A8 to A15 | 8 | I/O<br>Tri-state<br>Output | Port 1: I/O port that allows I/O to be selected at the bit level<br>Address and data (Upper): Bits 8 to 15 for address and data bus<br>Address: Bits 8 to 15 for address bus |
| P20 to P27<br>A0 to A7<br>A16 to A23 | 8 | I/O<br>Output<br>Output | Port 2: I/O port that allows to be selected at the bit level<br>Address: Bits 0 to 7 for address bus<br>Address: Bits 16 to 23 for address bus |
| P30<br>$\overline{RD}$ | 1 | Output<br>Output | Port 30: Output port<br>Read: Strobe signal for reading external memory |
| P31<br>$\overline{WR}$ | 1 | Output<br>Output | Port 31: Output port<br>Write: Strobe signal for writing data on pins AD0 to 7 |
| P32<br>$\overline{HWR}$ | 1 | I/O<br>Output | Port 32: I/O port (with pull-up resistor)<br>High write: Strobe signal for writing data on pins AD8 to 15 |
| P33<br>$\overline{WAIT}$ | 1 | I/O<br>Input | Port 33: I/O port (with pull-up resistor)<br>Wait: Pin used to request CPU bus wait ((1 + N) WAIT mode) |
| P34<br>$\overline{BUSRQ}$ | 1 | I/O<br>Input | Port 34: I/O port (with pull-up resistor)<br>Bus request: Signal used to request bus release. |
| P35<br>$\overline{BUSAK}$ | 1 | I/O<br>Output | Port 35: I/O port (with pull-up resistor)<br>Bus acknowledge: Signal used to acknowledge bus release. |
| P36<br>R/$\overline{W}$ | 1 | I/O<br>Output | Port 36: I/O port (with pull-up resistor)<br>Read/write: 1 represents read or dummy cycle; 0 represents write cycle. |
| P37 | 1 | I/O | Port 37: I/O port (with pull-up resistor) |
| P40<br>$\overline{CS0}$ | 1 | I/O<br>Output | Port 40: I/O port (with pull-up resistor)<br>Chip select 0: Outputs 0 when address is within specified address area. |
| P41<br>$\overline{CS1}$ | 1 | I/O<br>Output | Port 41: I/O port (with pull-up resistor)<br>Chip select 1: Outputs 0 if address is within specified address area. |
| P42<br>$\overline{CS2}$ | 1 | I/O<br>Output | Port 42: I/O port (with pull-up resistor)<br>Chip select 2: Outputs 0 if address is within specified address area. |
| P43<br>$\overline{CS3}$ | 1 | I/O<br>Output | Port 43: I/O port (with pull-up resistor)<br>Chip select 3: Outputs 0 if address is within specified address area. |
| P50 to P57<br>AN0 to AN7<br>$\overline{ADTRG}$ | 8 | Input<br>Input<br>Input | Port 5: Pin used to input port<br>Analog input: Pin used to input to AD converter<br>AD trigger: Signal used to request AD start. |

Note: This device's built-in memory or built-in I/O cannot be accessed by an external DMA controller, using the $\overline{BUSRQ}$ and $\overline{BUSAK}$ signals.

Table 2.2.1 Pin Names and Functions (2/4)

| Pin Name | Number of Pins | I/O | Functions |
|---|---|---|---|
| P60<br>SCK | 1 | I/O<br>I/O | Port 60: I/O port<br>Serial bus interface clock at SIO mode. |
| P61<br>SO<br>SDA | 1 | I/O<br>Output<br>I/O | Port 61: I/O port<br>Serial bus interface output data at SIO mode.<br>Serial bus interface data at $I^2C$ bus mode. |
| P62<br>SI<br>SCL | 1 | I/O<br>Input<br>I/O | Port 62: I/O port<br>Serial bus interface input data at SIO mode.<br>Serial bus interface clock at $I^2C$ bus mode. |
| P63<br>INT0 | 1 | I/O<br>Input | Port 63: I/O port<br>Interrupt request pin 0: Interrupt request pin with programmable level/rising edge/falling edge |
| P64<br>SCOUT | 1 | I/O<br>Output | Port 64: I/O port<br>System clock output: Output $f_{FPH}$ or fs clock |
| P65 | 1 | I/O | Port 65: I/O port |
| P66 | 1 | I/O | Port 66: I/O port |
| P70<br>TA0IN | 1 | I/O<br>Input | Port 70: I/O port<br>Timer A0 input |
| P71<br>TA1OUT | 1 | I/O<br>Output | Port 71: I/O port<br>Timer A1 output |
| P72<br>TA3OUT | 1 | I/O<br>Output | Port 72: I/O port<br>Timer A3 output |
| P73<br>TA4IN | 1 | I/O<br>Input | Port 73: I/O port<br>Timer A4 input |
| P74<br>TA5OUT | 1 | I/O<br>Output | Port 74: I/O port<br>Timer A5 output |
| P75<br>TA7OUT | 1 | I/O<br>Output | Port 75: I/O port<br>Timer A7 output |
| P80<br>TB0IN0<br><br>INT5 | 1 | I/O<br>Input<br><br>Input | Port 80: I/O port<br>Timer B0 input 0<br>Interrupt request pin 5: Interrupt request pin with programmable rising edge/falling edge |
| P81<br>TB0IN1<br>INT6 | 1 | I/O<br>Input<br>Input | Port 81: I/O port<br>Timer B0 input 1<br>Interrupt request pin 6: Interrupt request pin with rising edge |
| P82<br>TB0OUT0 | 1 | I/O<br>Output | Port 82: I/O port<br>Timer B0 output 0 |
| P83<br>TB0OUT1 | 1 | I/O<br>Output | Port 83: I/O port<br>Timer B0 output 1 |

Table 2.2.1 Pin Names and Functions (3/4)

| Pin Name | Number of Pins | I/O | Functions |
|---|---|---|---|
| P84<br>TB1IN0<br>INT7 | 1 | I/O<br>Input<br>Input | Port 84: I/O port<br>Timer B1 input 0<br>Interrupt request pin 7: Interrupt request pin with programmable rising edge/falling edge |
| P85<br>TB1IN1<br>INT8 | 1 | I/O<br>Input<br>Input | Port 85: I/O port<br>Timer B1 input 1<br>Interrupt request pin 8: Interrupt request pin with rising edge |
| P86<br>TB1OUT0 | 1 | I/O<br>Output | Port 86: I/O port<br>Timer B1 output 0 |
| P87<br>TB1OUT1 | 1 | I/O<br>Output | Port 87: I/O port<br>Timer B1 output 1 |
| P90<br>TXD0 | 1 | I/O<br>Output | Port 90: I/O port<br>Serial send data 0 |
| P91<br>RXD0 | 1 | I/O<br>Input | Port 91: I/O port<br>Serial receive data 0 |
| P92<br>SCLK0<br>$\overline{CTS0}$ | 1 | I/O<br>I/O<br>Input | Port 92: I/O port<br>Serial clock I/O 0<br>Serial data send enable 0 (Clear to Send) |
| P93<br>TXD1 | 1 | I/O<br>Output | Port 93: I/O port<br>Serial send data 1 |
| P94<br>RXD1 | 1 | I/O<br>Input | Port 94: I/O port (with pull-up resistor)<br>Serial receive data 1 |
| P95<br>SCLK1<br>$\overline{CTS1}$ | 1 | I/O<br>I/O<br>Input | Port 95: I/O port (with pull-up resistor)<br>Serial clock I/O 1<br>Serial data send enable 1 (Clear to Send) |
| P96<br>XT1 | 1 | I/O<br>Input | Port 96: I/O port (Open Drain Output)<br>Low-frequency oscillator connecting pin |
| P97<br>XT2 | 1 | I/O<br>Output | Port 97: I/O port (Open Drain Output)<br>Low-frequency oscillator connecting pin |
| PA0 to PA3<br>INT1 to INT4 | 4 | I/O<br>Input | Port A0 to A3: I/O port<br>Interrupt request pin 1 to 4: Interrupt request pin with programmable rising edge/falling edge |
| PA4 to PA7 | 4 | I/O | Port A4 to A7: I/O port |
| ALE | 1 | Output | Address latch enable (Can be disabled for reducing noise.). |
| $\overline{NMI}$ | 1 | Input | Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge or both edges. |
| AM0/AM1 | 2 | Input | Address mode: The Vcc pin should be connected. |
| EMU0/EMU1 | 2 | Output | Test pin: Open pins. |
| $\overline{RESET}$ | 1 | Input | Reset: Initializes TMP91CW12. (with pull-up resistor) |

Table 2.2.1 Pin Names and Functions (4/4)

| Pin Name | Number of Pins | I/O | Functions |
|---|---|---|---|
| VREFH | 1 | Input | Pin for reference voltage input to AD converter (H) |
| VREFL | 1 | Input | Pin for reference voltage input to AD converter (L) |
| X1/X2 | 2 | I/O | High-frequency oscillator connecting pin |
| AVCC | 1 | | Power supply pin for AD converter |
| AVSS | 1 | | GND pin for AD converter (0 V) |
| DVCC | 3 | | Power supply pin<br>(All VCC pins should be connected with the power supply pin.) |
| DVSS | 3 | | GND pin (0 V) (All VSS pins should be connected with GND (0 V).) |

Note: All pins that have built-in pull-up resistors (other than the $\overline{\text{RESET}}$ pin) can be disconnected from the built-in pull-up resistor by software.

## 3. Operation

The following describes block by block the functions and basic operation of TMP91CW12.
Notes and restrictions for each block are outlined in 7. "Points to Note and Restrictions" at the end of this manual.

### 3.1 CPU

TMP91CW12 incorporates a high-performance 16-bit CPU (900/L1 CPU). For CPU operation, see the "TLCS-900/L1 CPU".
The following describes the unique functions of the CPU used in TMP91CW12; these functions are not covered in the TLCS-900/L1 CPU section.

#### 3.1.1 Reset

When resetting the TMP91CW12 microcontroller, ensure that the power supply voltage is within the operating voltage range, and that the internal high-frequency oscillator has stabilized. Then set the $\overline{\text{RESET}}$ input to low level at least for 10 system clocks (80 $\mu$s at 4 MHz).
Thus, when turn on the switch, be set to the power supply voltage is within the operating voltage range, and that the internal high-frequency oscillator has stabilized. Then hold the $\overline{\text{RESET}}$ input to low level at least for 10 system clocks.
Clock gear is initialized 1/16 mode by reset operation. It means that the system clock mode $f_{SYS}$ is set to fc/32 (= fc/16 × 1/2).
When the reset is accepted, the CPU:

- Sets as follows the program counter (PC) in accordance with the reset vector stored at address FFFF00H - FFFF02H:
  PC (7:0) ← Value at FFFF00H address
  PC (15:8) ← Value at FFFF01H address
  PC (23:16) ← Value at FFFF02H address
- Sets the stack pointer (XSP) to 100H.
- Sets bits <IFF2:0> of the status register (SR) to 111 (Sets the interrupt level mask register to level 7).
- Sets the <MAX> bit of the status register to 1 (MAX mode).
  (Note: As this product does not support a MIN mode, don't write 0 to <MAX>.)
- Clears bits <RFP2:0> of the status register to 000 (Sets the register bank to 0).

When reset is released, the CPU starts executing instructions in accordance with the program counter settings. CPU internal registers not mentioned above do not change when the reset is released.
When the reset is accepted, the CPU sets internal I/O, ports, and other pins as follows.

- Initializes the internal I/O registers.
- Sets the port pins, including the pins that also act as internal I/O, to general-purpose input or output port mode.
- Sets the ALE pin to High-Z.
  Figure 3.1.1 is a reset timing of the TMP91CW12.

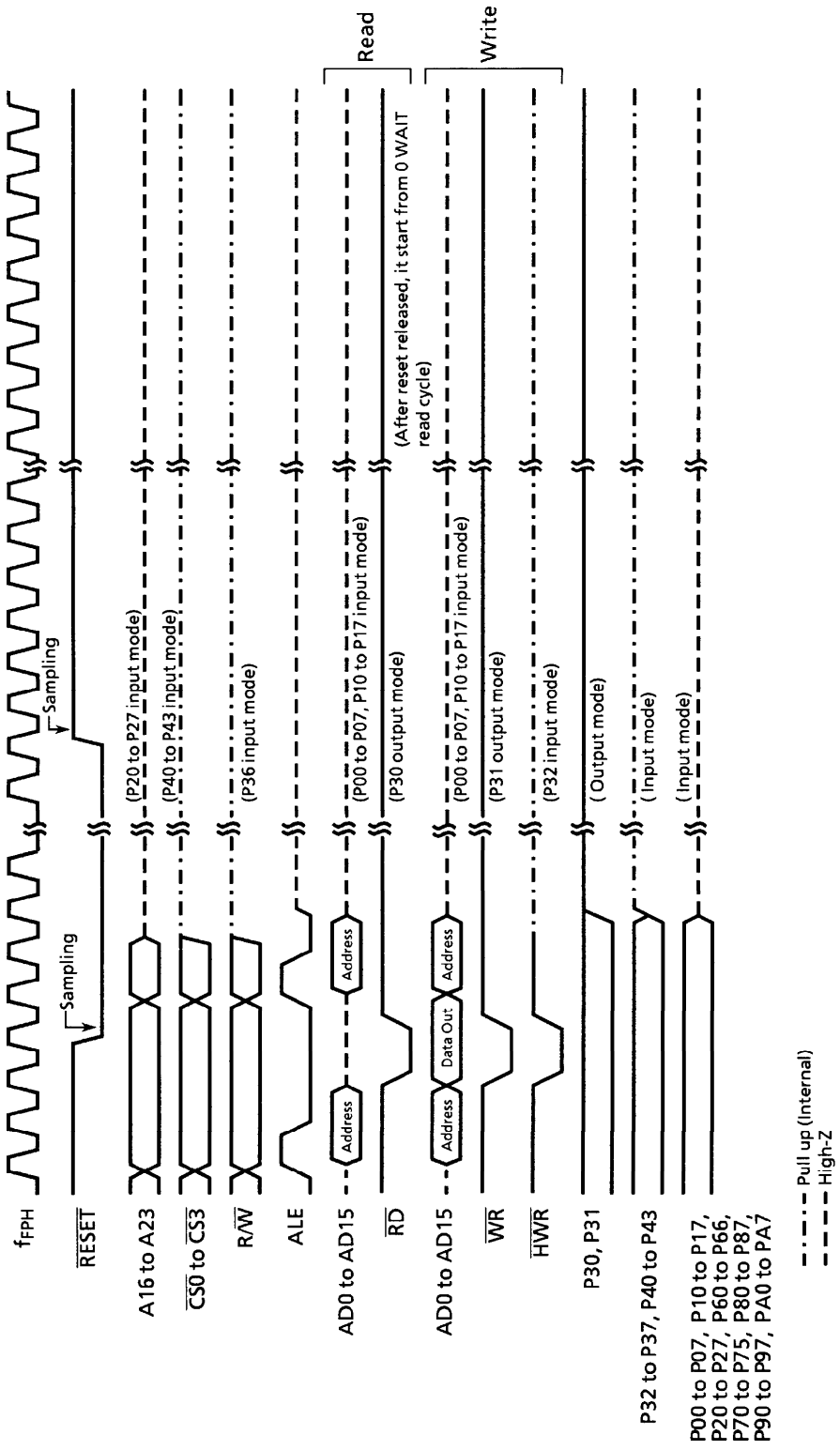



Figure 3.1.1 TMP91CW12 Reset Timing Example

### 3.2 Memory Map

Figure 3.2.1 is a memory map of the TMP91CW12.

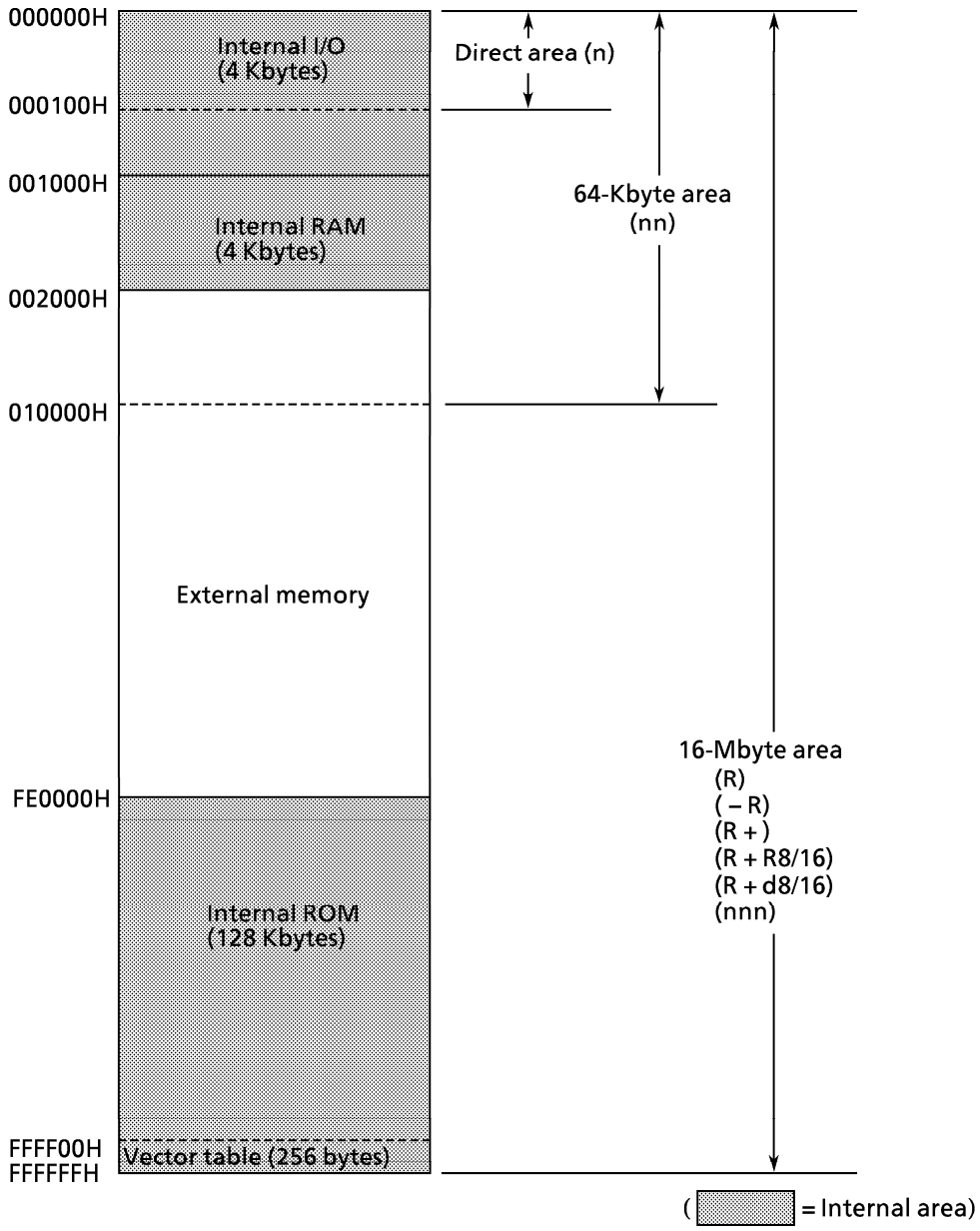



Figure 3.2.1 Memory Map

## 4. Electrical Characteristics

### 4.1 Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Power supply voltage | Vcc | – 0.5 to 6.5 | V |
| Input voltage | $V_{IN}$ | – 0.5 to Vcc + 0.5 | |
| Output current | $I_{OL}$ | 2 | mA |
| Output current | $I_{OH}$ | – 2 | |
| Output current (Total) | $\Sigma I_{OL}$ | 80 | |
| Output current (Total) | $\Sigma I_{OH}$ | – 80 | |
| Power dissipation (Ta = 85 °C) | $P_D$ | 600 | mW |
| Soldering temperature (10 s) | $T_{SOLDER}$ | 260 | °C |
| Storage temperature | $T_{STG}$ | – 65 to 150 | |
| Operating temperature | $T_{OPR}$ | – 40 to 85 | |

Note: The maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no maximum rating value will ever be exceeded.

### 4.2 DC Characteristics (1/2)

| Parameter | | Symbol | Condition | | Min | Typ. (Note) | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Power supply voltage (AVcc = DVcc) (AVss = DVss = 0 V) | | Vcc | fc = 2 to 16 MHz | fs = 30 to 34 kHz | 2.7 | | 5.5 | V |
| | | | fc = 4 to 25 MHz | | 4.5 | | | |
| Input low voltage | P00 to P17 (AD0 to AD15) | $V_{IL}$ | Vcc < 4.5 V | | – 0.3 | | 0.6 | V |
| | | | Vcc ≧ 4.5 V | | | | 0.8 | |
| | P20 to PA7 (except P63) | $V_{IL1}$ | Vcc = 2.7 to 5.5 V | | | | 0.3Vcc | |
| | $\overline{RESET}$, $\overline{NMI}$, P63 (INT0) | $V_{IL2}$ | | | | | 0.25Vcc | |
| | AM0, AM1 | $V_{IL3}$ | | | | | 0.3 | |
| | X1 | $V_{IL4}$ | | | | | 0.2Vcc | |
| Input high voltage | P00 to P17 (AD0 to AD15) | $V_{IH}$ | Vcc<4.5 V | | 2.0 | | Vcc + 0.3 | |
| | | | Vcc≧4.5 V | | 2.2 | | | |
| | P20 to PA7 (except P63) | $V_{IH1}$ | Vcc = 2.7 to 5.5 V | | 0.7Vcc | | | |
| | $\overline{RESET}$, $\overline{NMI}$, P63 (INT0) | $V_{IH2}$ | | | 0.75Vcc | | | |
| | AM0, AM1 | $V_{IH3}$ | | | Vcc – 0.3 | | | |
| | X1 | $V_{IH4}$ | | | 0.8Vcc | | | |
| Output low voltage | | $V_{OL}$ | $I_{OL}$ = 1.6 mA (Vcc = 2.7 to 5.5 V) | | | | 0.45 | V |
| Output high voltage | | $V_{OH}$ | $I_{OH}$ = – 400 μA (Vcc = 3.0 V ± 10%) | | 2.4 | | | |
| | | | $I_{OH}$ = – 400 μA (Vcc = 5.0V ± 10%) | | 4.2 | | | |

Note: Typical values are for Ta = 25°C and $V_{CC}$ = 3.0 V unless otherwise noted.

### 4.2 DC Characteristics (2/2)

| Parameter | Symbol | Condition | | Min | Typ. (Note1) | Max | Unit |
|---|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | $0.0 \leqq V_{IN} \leqq Vcc$ | | | 0.02 | ± 5 | μA |
| Output leakage current | $I_{LO}$ | $0.2 \leqq V_{IN} \leqq Vcc - 0.2$ | | | 0.05 | ± 10 | |
| Power down voltage (at STOP, RAM backup) | $V_{STOP}$ | $V_{IL2} = 0.2$ Vcc, $V_{IH2} = 0.8$ Vcc | | 2.0 | | 6.0 | V |
| $\overline{RESET}$ pull-up resistor | $R_{RST}$ | Vcc = 3 V ± 10% | | 100 | | 400 | kΩ |
| | | Vcc = 5 V ± 10% | | 50 | | 230 | |
| Pin capacitance | $C_{IO}$ | fc = 1 MHz | | | | 10 | pF |
| Schmitt width $\overline{RESET}$, $\overline{NMI}$, INT0 | $V_{TH}$ | | | 0.4 | 1.0 | | V |
| Programmable pull-up resistor | $R_{KH}$ | Vcc = 3 V ± 10% | | 100 | | 400 | kΩ |
| | | Vcc = 5 V ± 10% | | 50 | | 230 | |
| NORMAL (Note 2) | Icc | Vcc = 3 V ± 10% fc = 16 MHz | | | 6.7 | 10.0 | mA |
| IDLE2 | | | | | 2.4 | 4.0 | |
| IDLE1 | | | | | 0.8 | 1.6 | |
| NORMAL (Note 2) | | Vcc = 5 V ± 10% fc = 25 MHz (Typ. : Vcc = 5.0 V) | | | 20.5 | 35.0 | |
| IDLE2 | | | | | 8.6 | 13.0 | |
| IDLE1 | | | | | 3.5 | 7.0 | |
| SLOW (Note 2) | | Vcc = 3 V ± 10% fs = 32.768 kHz | | | 16.0 | 35.0 | μA |
| IDLE2 | | | | | 5.4 | 12.0 | |
| IDLE1 | | | | | 3.0 | 8.0 | |
| STOP | | Ta ≦ 50°C | Vcc = 2.7 to 5.5 V | | | 10 | |
| | | Ta ≦ 70°C | | | 0.2 | 20 | |
| | | Ta ≦ 85°C | | | | 50 | |

Note 1: Typical values are for Ta = 25°C and $V_{CC}$ = 3.0 V unless otherwise noted.

Note 2: $I_{CC}$ measurement condition (NORMAL, SLOW):
All functions are operational; output pins are open and input pins are fixed.

### 4.3 AC Characteristics

(1) Vcc = 3.0 V ± 10 %

| No. | Parameter | Symbol | Variable | | 16 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| 1 | $f_{FPH}$ period ( = x) | $t_{FPH}$ | 62.5 | 31250 | 62.5 | | ns |
| 2 | A0 to A15 valid → ALE fall | $t_{AL}$ | 0.5x – 26 | | 5 | | ns |
| 3 | ALE fall → A0 to A15 hold | $t_{LA}$ | 0.5x – 26 | | 5 | | ns |
| 4 | ALE high width | $t_{LL}$ | x – 52 | | 10 | | ns |
| 5 | ALE fall → $\overline{RD}$/$\overline{WR}$ fall | $t_{LC}$ | 0.5x – 28 | | 3 | | ns |
| 6 | $\overline{RD}$ rise → ALE rise | $t_{CLR}$ | 0.5x – 26 | | 5 | | |
| 7 | $\overline{WR}$ rise → ALE rise | $t_{CLW}$ | x – 26 | | 36 | | ns |
| 8 | A0 to A15 valid → $\overline{RD}$/$\overline{WR}$ fall | $t_{ACL}$ | x – 41 | | 21 | | ns |
| 9 | A0 to A23 valid → $\overline{RD}$/$\overline{WR}$ fall | $t_{ACH}$ | 1.5x – 50 | | 43 | | ns |
| 10 | $\overline{RD}$ rise→ A0 to A23 hold | $t_{CAR}$ | 0.5x – 31 | | 0 | | |
| 11 | $\overline{WR}$ rise→ A0 to A23 hold | $t_{CAW}$ | x – 31 | | 31 | | ns |
| 12 | A0 to A15 valid→ D0 to D15 input | $t_{ADL}$ | | 3.0x – 87 | | 100 | ns |
| 13 | A0 to A23 valid→ D0 to D15 input | $t_{ADH}$ | | 3.5x – 98 | | 120 | ns |
| 14 | $\overline{RD}$ fall → D0 to D15 input | $t_{RD}$ | | 2.0x – 75 | | 50 | ns |
| 15 | $\overline{RD}$ low width | $t_{RR}$ | 2.0x – 40 | | 85 | | ns |
| 16 | $\overline{RD}$ rise → D0 to D15 hold | $t_{HR}$ | 0 | | 0 | | ns |
| 17 | $\overline{RD}$ rise → A0 to A15 output | $t_{RAE}$ | x – 25 | | 37 | | ns |
| 18 | $\overline{WR}$ low width | $t_{WW}$ | 1.5x – 55 | | 39 | | ns |
| 19 | D0 to D15 valid → $\overline{WR}$ rise | $t_{DW}$ | 2.0x – 78 | | 15 | | ns |
| 20 | $\overline{WR}$ rise →D0 to D15 hold | $t_{WD}$ | x – 49 | | 13 | | ns |
| 21 | A0 to A23 valid → $\overline{WAIT}$ input $\left(^{(1+N)\ WAIT}_{mode}\right)$ | $t_{AWH}$ | | 3.5x – 118 | | 100 | ns |
| 22 | A0 to A15 valid → $\overline{WAIT}$ input $\left(^{(1+N)\ WAIT}_{mode}\right)$ | $t_{AWL}$ | | 3.0x – 117 | | 70 | ns |
| 23 | $\overline{RD}$/$\overline{WR}$ fall →$\overline{WAIT}$ hold $\left(^{(1+N)\ WAIT}_{mode}\right)$ | $t_{CW}$ | 2.0x + 0 | | 125 | | ns |
| 24 | A0 to A23 valid → Port input | $t_{APH}$ | | 3.5x – 168 | | 50 | ns |
| 25 | A0 to A23 valid → Port hold | $t_{APH2}$ | 3.5x | | 218 | | ns |
| 26 | A0 to A23 valid → Port valid | $t_{AP}$ | | 3.5x + 100 | | 319 | ns |

AC measuring conditions

- Output level: High 0.7 Vcc/Low 0.3 Vcc , CL = 50 pF
- Input level: High 0.9 Vcc/Low 0.1 Vcc

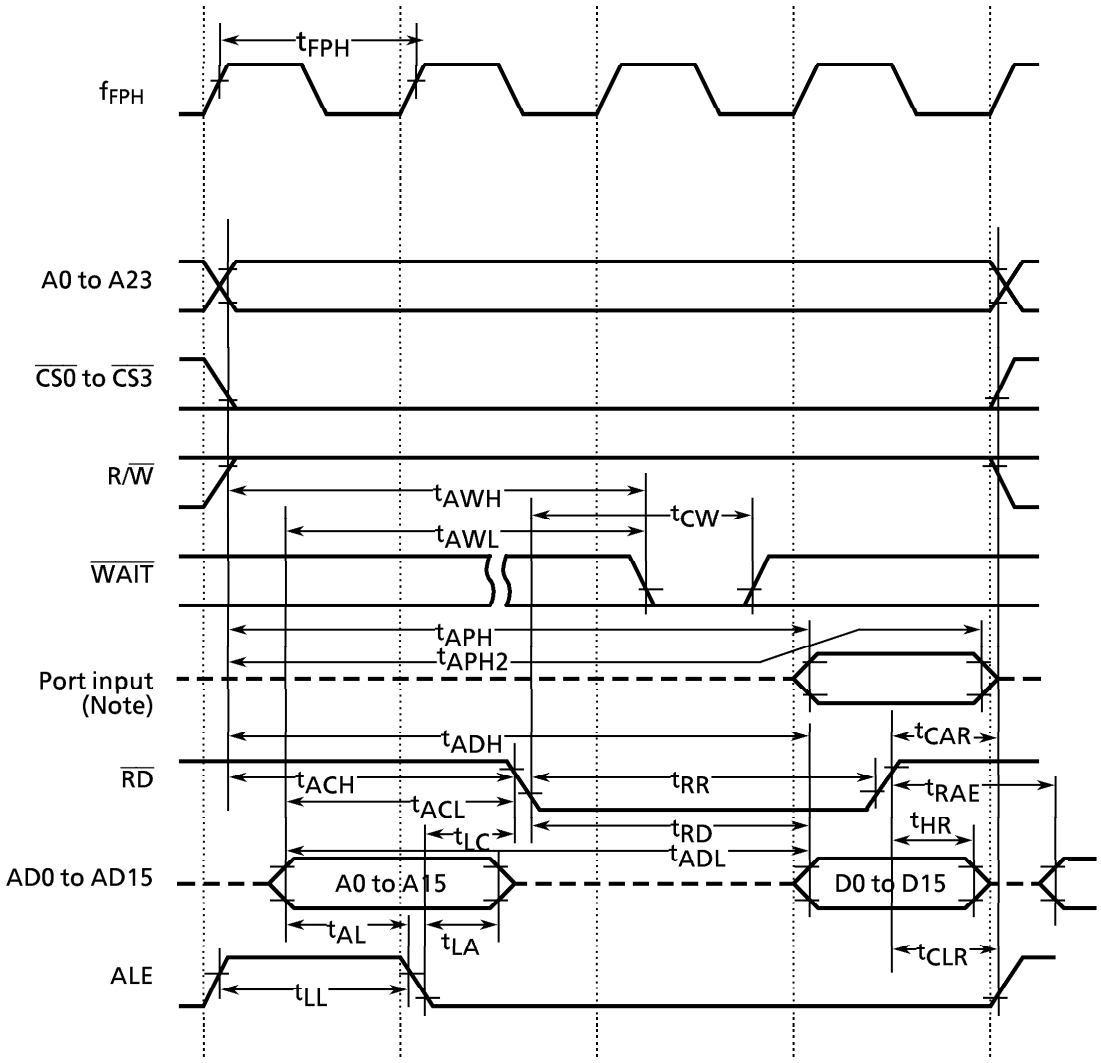
(2) Vcc = 5.0 V ± 10 %

| No. | Parameter | Symbol | Variable | | 25 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| 1 | $f_{FPH}$ period ( = x) | $t_{FPH}$ | 40 | 31250 | 40 | | ns |
| 2 | A0 to A15 valid → ALE fall | $t_{AL}$ | 0.5x – 15 | | 5 | | ns |
| 3 | ALE fall → A0 to A15 hold | $t_{LA}$ | 0.5x – 15 | | 5 | | ns |
| 4 | ALE high width | $t_{LL}$ | x – 20 | | 20 | | ns |
| 5 | ALE fall → $\overline{RD}/\overline{WR}$ fall | $t_{LC}$ | 0.5x – 20 | | 0 | | ns |
| 6 | $\overline{RD}$ rise → ALE rise | $t_{CLR}$ | 0.5x – 15 | | 5 | | |
| 7 | $\overline{WR}$ rise → ALE rise | $t_{CLW}$ | x – 15 | | 25 | | ns |
| 8 | A0 to A15 valid → $\overline{RD}/\overline{WR}$ fall | $t_{ACL}$ | x – 25 | | 15 | | ns |
| 9 | A0 to A23 valid → $\overline{RD}/\overline{WR}$ fall | $t_{ACH}$ | 1.5x – 50 | | 10 | | ns |
| 10 | $\overline{RD}$ rise→ A0 to A23 hold | $t_{CAR}$ | 0.5x – 20 | | 0 | | |
| 11 | $\overline{WR}$ rise→ A0 to A23 hold | $t_{CAW}$ | x – 20 | | 20 | | ns |
| 12 | A0 to A15 valid→ D0 to D15 input | $t_{ADL}$ | | 3.0x – 45 | | 75 | ns |
| 13 | A0 to A23 valid→ D0 to D15 input | $t_{ADH}$ | | 3.5x – 35 | | 105 | ns |
| 14 | $\overline{RD}$ fall → D0 to D15 input | $t_{RD}$ | | 2.0x – 40 | | 40 | ns |
| 15 | $\overline{RD}$ low width | $t_{RR}$ | 2.0x – 20 | | 60 | | ns |
| 16 | $\overline{RD}$ rise → D0 to D15 hold | $t_{HR}$ | 0 | | 0 | | ns |
| 17 | $\overline{RD}$ rise → A0 to A15 output | $t_{RAE}$ | x – 15 | | 25 | | ns |
| 18 | $\overline{WR}$ low width | $t_{WW}$ | 1.5x – 20 | | 40 | | ns |
| 19 | D0 to D15 valid → $\overline{WR}$ rise | $t_{DW}$ | 1.5x – 50 | | 10 | | ns |
| 20 | $\overline{WR}$ rise →D0 to D15 hold | $t_{WD}$ | x – 15 | | 25 | | ns |
| 21 | A0 to A23 valid → $\overline{WAIT}$ input $\left(\begin{smallmatrix}(1+N)\text{ WAIT}\\ \text{mode}\end{smallmatrix}\right)$ | $t_{AWH}$ | | 3.5x – 90 | | 50 | ns |
| 22 | A0 to A15 valid → $\overline{WAIT}$ input $\left(\begin{smallmatrix}(1+N)\text{ WAIT}\\ \text{mode}\end{smallmatrix}\right)$ | $t_{AWL}$ | | 3.0x – 80 | | 40 | ns |
| 23 | $\overline{RD}/\overline{WR}$ fall →$\overline{WAIT}$ hold $\left(\begin{smallmatrix}(1+N)\text{ WAIT}\\ \text{mode}\end{smallmatrix}\right)$ | $t_{CW}$ | 2.0x + 0 | | 80 | | ns |
| 24 | A0 to A23 valid → Port input | $t_{APH}$ | | 3.5x – 120 | | 20 | ns |
| 25 | A0 to A23 valid → Port hold | $t_{APH2}$ | 3.5x | | 140 | | ns |
| 26 | A0 to A23 valid → Port valid | $t_{AP}$ | | 3.5x + 100 | | 319 | ns |

AC measuring conditions

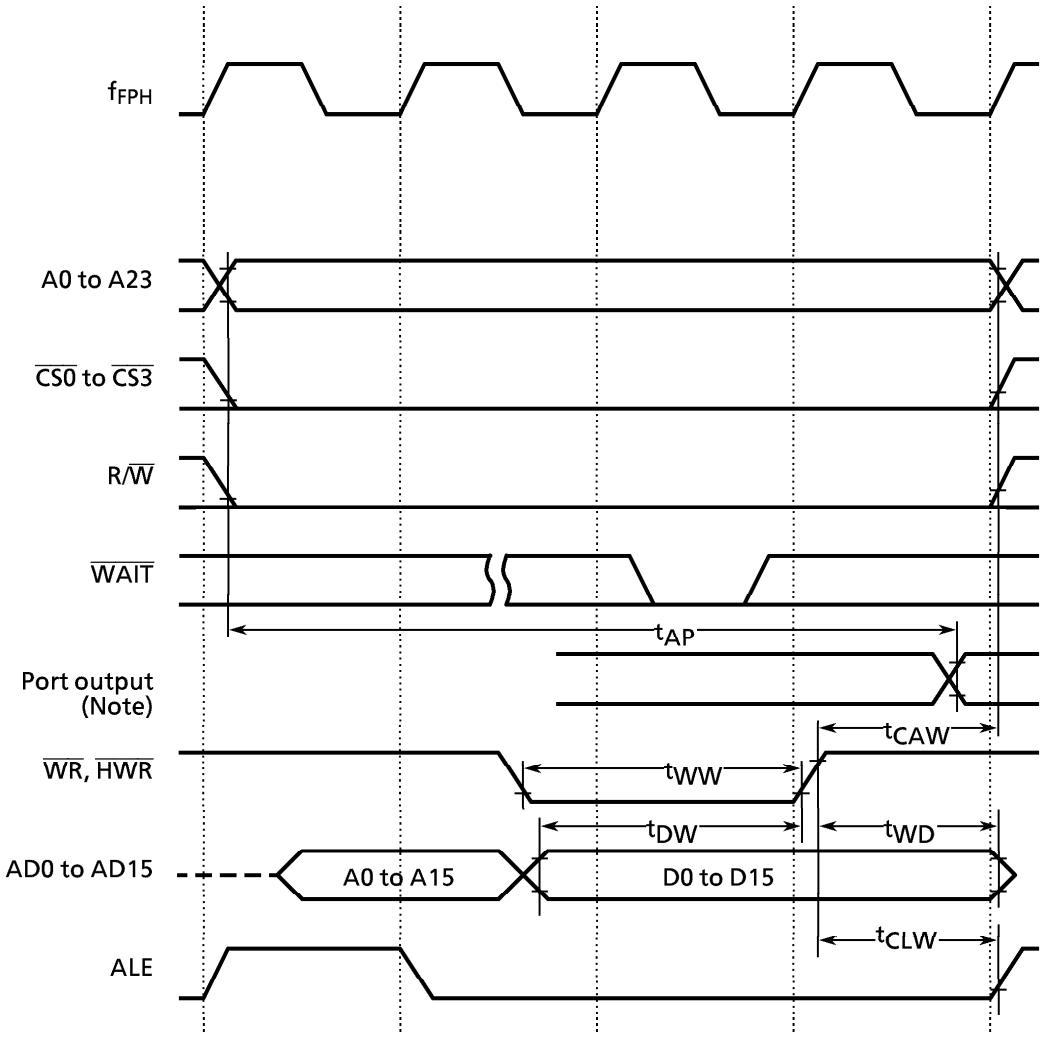
- Output level: High 2.2 V/Low 0.8 V, CL = 50 pF
- Input level: High 2.4 V/Low 0.45 V (AD0 to AD15)
  High 0.8 Vcc/Low 0.2 Vcc (except AD0 to AD15)

(1) Read cycle




Note: Since the CPU accesses the internal area to read data from a port, the control signals of external pins such as $\overline{RD}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

(2) Write cycle




Note: Since the CPU accesses the internal area to write data to a port, the control signals of external pins such as $\overline{WR}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

### 4.4 AD Conversion Characteristics

$AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$

| Parameter | Symbol | Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Analog reference voltage (+) | VREFH | $V_{CC}$ = 3 V ± 10% | $V_{CC}$ – 0.2 V | $V_{CC}$ | $V_{CC}$ | V |
| | | $V_{CC}$ = 5 V ± 10% | $V_{CC}$ – 1.5 V | $V_{CC}$ | $V_{CC}$ | |
| Analog reference voltage (–) | VREFL | $V_{CC}$ = 3 V ± 10% | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.2 V | |
| | | $V_{CC}$ = 5 V ± 10% | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.2 V | |
| Analog input voltage range | VAIN | | VREFL | | VREFH | |
| Analog current for analog reference voltage <VREFON> = 1 | IREF (VREFL = 0 V) | $V_{CC}$ = 3 V ± 10% | | 0.85 | 1.20 | mA |
| | | $V_{CC}$ = 5 V ± 10% | | 1.44 | 2.00 | |
| <VREFON> = 0 | | $V_{CC}$ = 2.7 to 5.5 V | | 0.02 | 5.0 | μA |
| Error (not including quantizing errors) | – | $V_{CC}$ = 3 V ± 10% | | ± 1.0 | ± 4.0 | LSB |
| | | $V_{CC}$ = 5 V ± 10% | | ± 1.0 | ± 4.0 | |

Note 1: 1LSB = (VREFH – VREFL)/1024 [V]
Note 2: The operation above is guaranteed for $f_{FPH} \geqq 4$ MHz.
Note 3: The value $I_{CC}$ includes the current which flows through the AVCC pin.

### 4.5 Serial Channel Timing (I/O internal mode)

(1) SCLK input mode

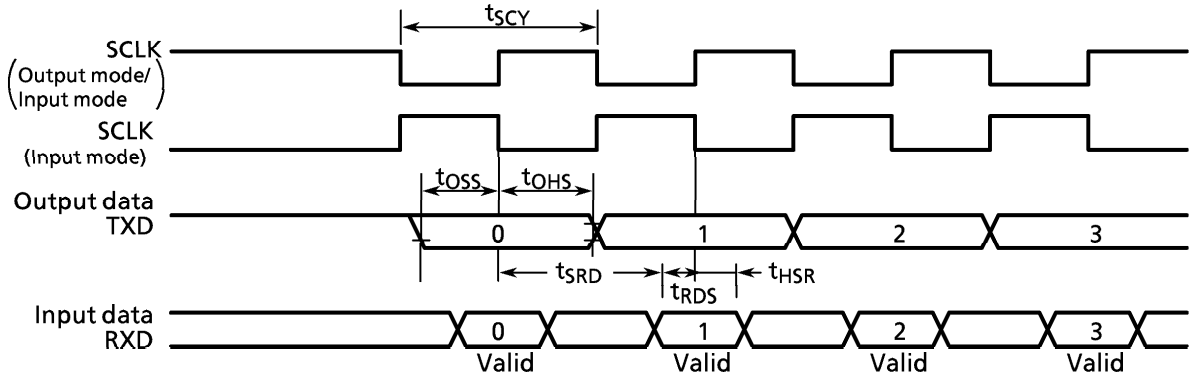
| Parameter | Symbol | Variable | | 25 MHz | | 16 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| SCLK period | $t_{SCY}$ | 16X | | 0.64 | | 1.0 | | μs |
| Output data → SCLK rising/falling edge* | $t_{OSS}$ | $t_{SCY}/2 - 4X - 85$ ($V_{CC}$ = 5 V ± 10%) | | 75 | | 165 | | ns |
| | | $t_{SCY}/2 - 4X - 130$ ($V_{CC}$ = 3 V ± 10%) | | — | | 120 | | |
| SCLK rising/falling edge* → Output data hold | $t_{OHS}$ | $t_{SCY}/2 + 2X + 0$ | | 400 | | 625 | | ns |
| SCLK rising/falling edge* → Input data hold | $t_{HSR}$ | 3X + 10 | | 130 | | 198 | | ns |
| SCLK rising/falling edge* → Valid data input | $t_{SRD}$ | | $t_{SCY} - 0$ | | 640 | | 1000 | ns |
| Valid data input → SCLK rising/falling edge* | $t_{RDS}$ | 0 | | 0 | | 0 | | ns |

* ) SCLK rising/falling edge: The rising edge is used in SCLK rising mode.
The falling edge is used in SCLK falling mode.

Note: 25 MHz and 16 MHz values are calculated from $t_{SCY} = 16 \times$ Case.

(2) SCLK Output Mode

| Parameter | Symbol | Variable | | 25 MHz | | 16 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| SCLK period (Programable) | $t_{SCY}$ | 16X | 8192X | 0.64 | 327 | 1.0 | 512 | μs |
| Output data → SCLK rising/falling edge | $t_{OSS}$ | $t_{SCY}/2 - 40$ | | 280 | | 460 | | ns |
| SCLK rising/falling edge → Output data hold | $t_{OHS}$ | $t_{SCY}/2 - 40$ | | 280 | | 460 | | ns |
| SCLK rising/falling edge → Input data hold | $t_{HSR}$ | 0 | | 0 | | 0 | | ns |
| SCLK rising/falling edge → Valid data input | $t_{SRD}$ | | $t_{SCY} - 1X - 90$ | | 510 | | 847 | ns |
| Valid data input → SCLK rising/falling edge | $t_{RDS}$ | 1X + 90 | | 130 | | 153 | | ns |



### 4.6 Event Counter (TA0IN, TA4IN, TB0IN0, TB0IN1, TB1IN0, TB1IN1)

| Parameter | Symbol | Variable | | 25 MHz | | 16 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Clock period | $t_{VCK}$ | 8X + 100 | | 420 | | 600 | | ns |
| Clock low level width | $t_{VCKL}$ | 4X + 40 | | 200 | | 290 | | ns |
| Clock high level width | $t_{VCKH}$ | 4X + 40 | | 200 | | 290 | | ns |

### 4.7 Interrupt, Capture

(1) $\overline{NMI}$, INT0 to INT4 interrupts

| Parameter | Symbol | Variable | | 25 MHz | | 16 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $\overline{NMI}$, INT0 to INT4 low level width | $t_{INTAL}$ | 4X + 40 | | 200 | | 290 | | ns |
| $\overline{NMI}$, INT0 to INT4 high level width | $t_{INTAH}$ | 4X + 40 | | 200 | | 290 | | ns |

(2) INT5 to INT8 interrupt, capture

The INT5 to INT8 input width depends on the system clock select mode, prescaler clock mode.

| System Clock Selected <SYSCK> | Prescaler Clock Selected <PRCK1:0> | $t_{INTBL}$ (INT5 to INT8 low level width) | | $t_{INTBH}$ (INT5 to INT8 high level width) | | Unit |
|---|---|---|---|---|---|---|
| | | Variable | 25 MHz | Variable | 25 MHz | |
| | | Min | Min | Min | Min | |
| 0 (fc) | 00 ($f_{FPH}$) | 8X + 100 | 420 | 8X + 100 | 420 | ns |
| | 10 (fc/16) | 128Xc + 0.1 | 5.22 | 128Xc + 0.1 | 5.22 | μs |
| 1 (fs) | 00 ($f_{FPH}$) | 8X + 0.1 | 244.3 | 8X + 0.1 | 244.3 | |

Note: Xc = Period of clock fc

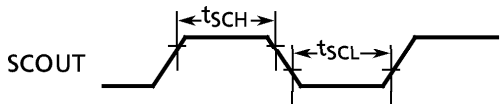
### 4.8 SCOUT pin AC characteristics

| Parameter | Symbol | Condition | Variable | | 25 MHz | | 16 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| Low level width | $t_{SCH}$ | $V_{CC}$ = 3 V ± 10% | 0.5T – 20 | | – | | 11 | | ns |
| | | $V_{CC}$ = 5 V ± 10% | 0.5T – 15 | | 5 | | 16 | | |
| High level width | $t_{SCL}$ | $V_{CC}$ = 3 V ± 10% | 0.5T – 20 | | – | | 11 | | ns |
| | | $V_{CC}$ = 5 V ± 10% | 0.5T – 15 | | 5 | | 16 | | |

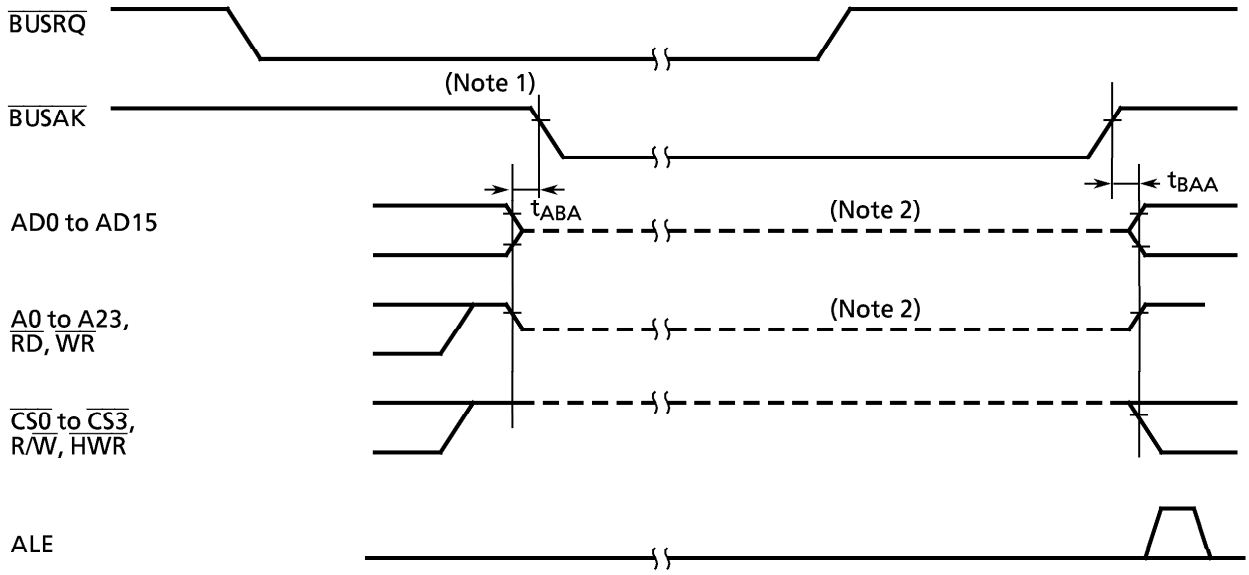
Note: T = Period of SCOUT

Measrement condition

- Output level: High 0.7 $V_{CC}$/low 0.3 $V_{CC}$, CL = 10 pF



### 4.9 Bus Request/Bus Acknowledge




| Parameter | Symbol | Variable | | 25 MHz | | 16 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Output buffer off to $\overline{\text{BUSAK}}$ low | $t_{ABA}$ | 0 | 80 | 0 | 80 | 0 | 80 | ns |
| $\overline{\text{BUSAK}}$ high to output buffer on | $t_{BAA}$ | 0 | 80 | 0 | 80 | 0 | 80 | ns |

Note 1: Even if the $\overline{\text{BUSRQ}}$ signal goes low, the bus will not be released while the $\overline{\text{WAIT}}$ signal is low. The bus will only be released when $\overline{\text{BUSRQ}}$ goes low while $\overline{\text{WAIT}}$ is high.

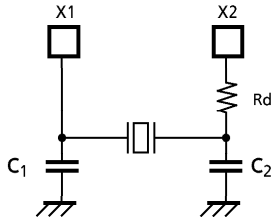
Note 2: This line shows only that the output buffer is in the off state.
It does not indicate that the signal level is fixed.
Just after the bus is released, the signal level set before the bus was released is maintained dynamically by the external capacitance. Therefore, to fix the signal level using an external resistor during bus release, careful design is necessary, as fixing of the level is delayed.
The internal programmable pull-up/pull-down resistor is switched between the active and non-active states by the internal signal.

### 4.10 Recommended Oscillation Circuit

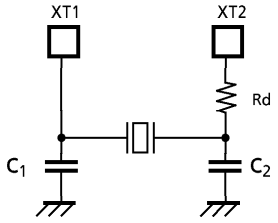
The TMP91CW12F/TMP91PW12F have been evaluated by the following resonator manufacturer. The evaluation results are shown below for your information.

Note: The load capacitance of the oscillation terminal is the sum of the load capacitances of C1 and C2 to be connected and the stray capacitance on the board. Even if the ratings of C1 and C2 are used, the load capacitance varies with each board and the oscillator may malfunction. Therefore, when designing a board, make the pattern around the oscillation circuit shortest. It is recommended that final evaluation of the resonator be performed on the board.

(1) Examples of resonator connection




High-frequency oscillator connection




Low-frequency oscillator connection

(2) Recommended ceramic resonators for the TMP91CW12F/PW12F: Murata Manufacturing Co., Ltd.

| Item | Oscillation Frequency | Recommended Resonator | Recommended Rating | | | VCC [V] | Remarks |
|---|---|---|---|---|---|---|---|
| | | | C1 [pF] | C2 [pF] | Rd [kΩ] | | |
| High-frequency oscillator | 2.0 | CSA2.00MG | 30 | 30 | 0 | 2.7 to 3.3 | – |
| | | CST2.00MG | (30) | (30) | | | |
| | 4.0 | CSA4.00MG | 30 | 30 | | 2.7 to 5.5 | |
| | | CST4.00MGW | (30) | (30) | | | |
| | 10.0 | CSA10.0MTZ | 30 | 30 | | 4.5 to 5.5 | |
| | | CST10.0MTW | (30) | (30) | | | |
| | | CSA10.0MTZ | 30 | 30 | | 2.7 to 3.3 | TMP91CW12F only |
| | | CST10.0MTW | (30) | (30) | | | |
| | | CSA10.0MTZ093 | 30 | 30 | | 2.7 to 3.3 | TMP91PW12F only |
| | | CST10.0MTW093 | (30) | (30) | | | |
| | 12.5 | CSA12.5MTZ | 30 | 30 | | 4.5 to 5.5 | – |
| | | CST12.5MTW | (30) | (30) | | | |
| | | CSA12.5MTZ | 30 | 30 | | 2.7 to 3.3 | TMP91CW12F only |
| | | CST12.5MTW | (30) | (30) | | | |
| | | CSA12.5MTZ093 | 30 | 30 | | 2.7 to 3.3 | TMP91PW12F only |
| | | CST12.5MTW093 | (30) | (30) | | | |
| | 16.0 | CSA16.00MXZ040 | 5 | 5 | | 4.5 to 5.5 | – |
| | | CST16.00MXW0C1 | (5) | (5) | | | |
| | | CSA16.00MXZ040 | Open | Open | | 2.7 to 3.3 | TMP91CW12F only |
| | | CSA16.00MXZ046 | Open | Open | | 2.7 to 3.3 | TMP91PW12F only |
| | 20.0 | CSA20.00MXZ040 | 3 | 3 | | 4.5 to 5.5 | – |
| | 25.0 | CSA25.00MXZ040 | Open | Open | | | |

- The values enclosed in brackets in the C1 and C2 columns apply to the condenser built-in type.
- Murata Manufacturing Co., Ltd. (JAPAN)
  The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL:
  http://www.murata.co.jp/search/index.html