CMOS 8-BIT MICROCONTROLLERS

TMP91P640E – 10 / TMP91P640N – 10 / TMP91P640F – 10

1. OUTLINE AND CHARACTERISTICS

The TMP91P640 is a system evalution LSI having a built in EPROM or One-Time PROM for TMP91C640 or TMP90C840A.

A programming and verification for the internal PROM is achieved by using a general EPROM programmer with an adapter socket.

The function of this device is exactly same as the TMP91C640 or TMP90C840A by programming to the internal PROM.

The different points between TMP91P640 and TMP90C840A are the memory size (ROM/RAM) and maximum operating frequency.

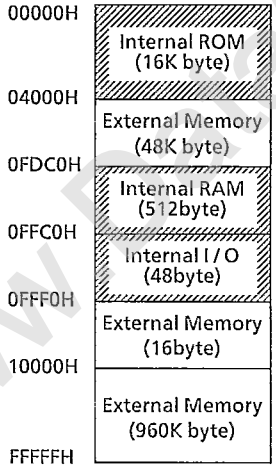
The operating frequency range of TMP91P640 is from 1MHz to 10MHz, against that of TMP91C640/TMP90C840A is from 1MHz to 12.5MHz.

The TMP91P640E-10 is in a CERDIP with window.

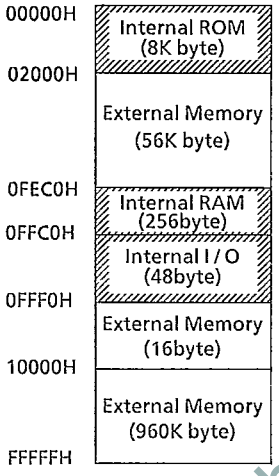
The TMP91P640N-10 is in a Shrink Dual Inline Package (SDIP64-P-750).

The TMP91P640F-10 is in a Quad Flat Package (QFP64-P-1420A).

The following are the memory map of TMP91C640 and TMP90C840A.



TMP91C640 Memory Map



TMP90C840A Memory Map

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PARTS NO.	ROM	RAM	PACKAGE	ADAPTER SOCKET NO.
TMP91P640E-10	EPROM 16384×8bit	512×8bit	64-SDIC with window	BM1115A
TMP91P640N-10	OTP 16384×8bit		64-SDIP	
TMP91P640F-10			64-FP	BM1116A

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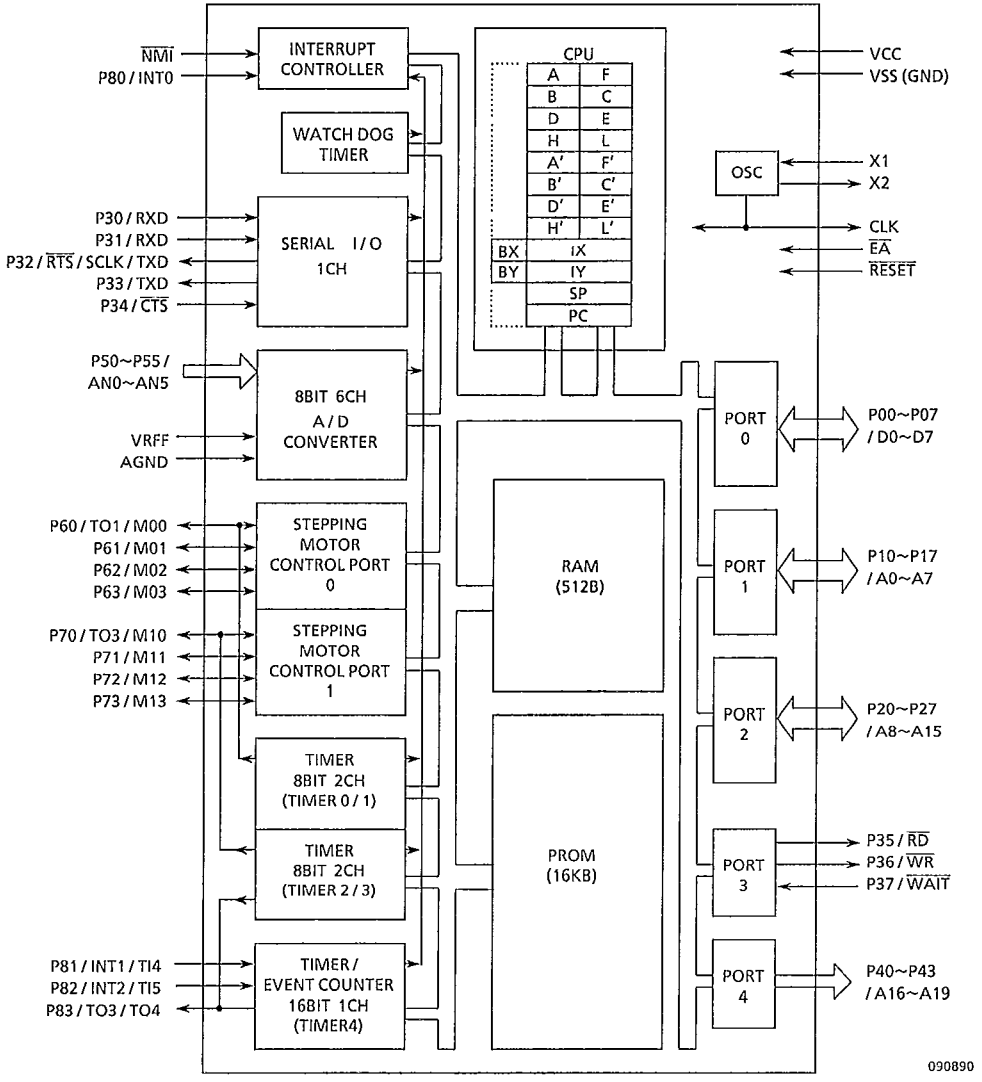

Figure 1 TMP91P640 Block Diagram

2. PIN ASSIGNMENT AND FUNCTIONS

2.1 Pin Assignment

Figure 2.1 (1) shows pin assignment of the TMP91P640E-10 / 640N-10.

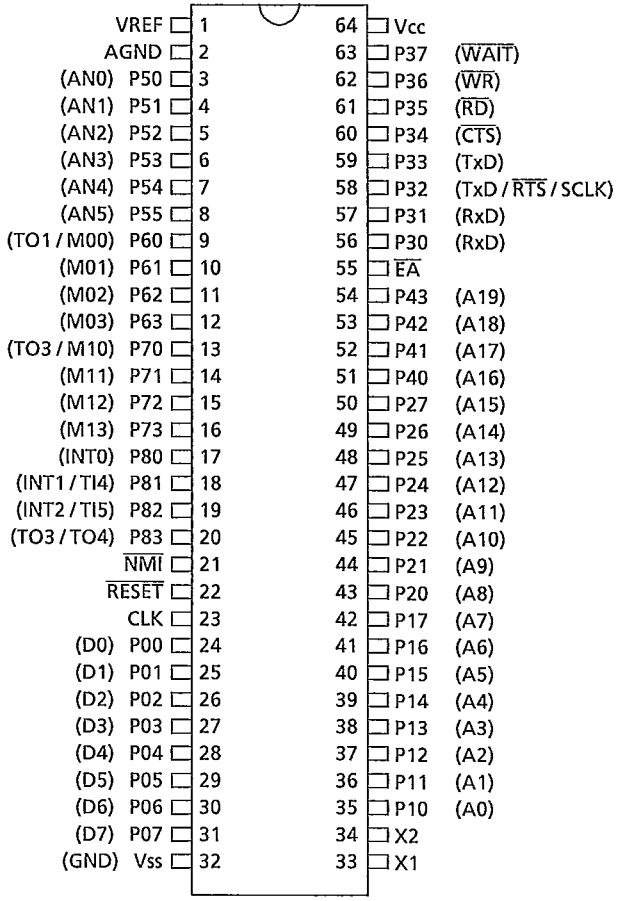

Figure 2.1 (1) Pin Assignment (64-SDIC / SDIP)

Figure 2.1 (2) shows pin assignment of the TMP91P640F-10.

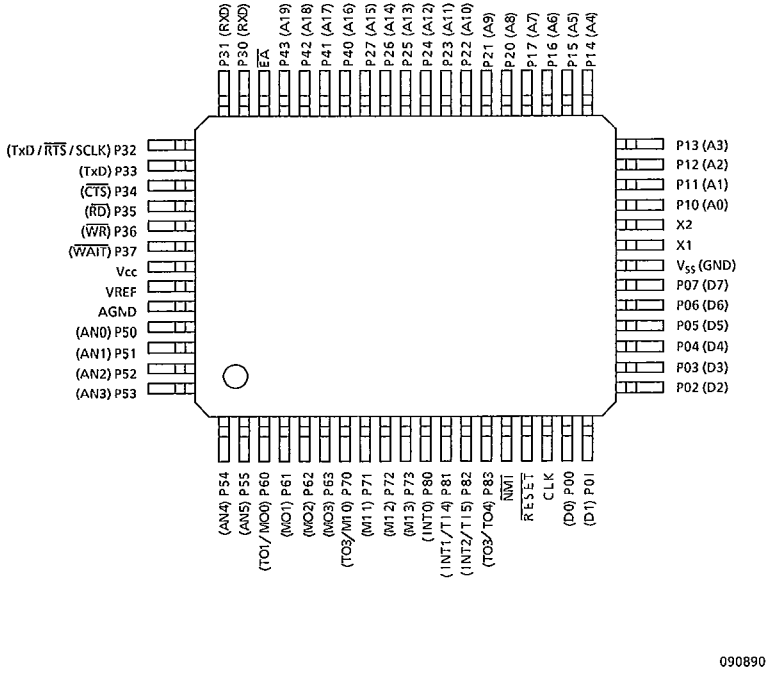

Figure 2.1 (2) Pin Assignment (64-FP)

2.2 Pin Names and Functions

The TMP91P640 has MCU mode and PROM mode.

(1) MCU Mode (The TMP91C640 and the TMP91P640 are pin compatiple)

Pin Names and Functions (1/2)

Pin Name	No. of pins	I/O 3 states	Function
P00~P07	8	I/O	Port 0: 8-bit I/O port that allows selection of input/output on byte basis
/D0~D7		3 states	Data bus: Also functions as 8-bit bidirectional data bus for external memory
P10~P17	8	I/O	Port 1: 8-bit I/O port that allows selection on byte basis
/A0~A7		Output	Address bus: The lower 8 bits address bus for external memory
P20~P27	8	I/O	Port 2: 8-bit I/O port that allows selection on bit basis
/A8~A15		Output	Address bus: The upper 8 bits address bus for external memory
P30	1	Input	Port 30: 1-bit input port
/RxD			Receiver Serial Data
P31	1	Input	Port 31: 1-bit input port
/RxD			Receiver Serial Data
P32	1	Output	Port 32: 1-bit output port
/TxD			Transmitter serial Data
/$\overline{RTS}$			Request to send serial data
/SCLK			Serial clock output
P33	1	Output	Port 33: 1-bit output port
/TxD			Transmitter Serial Data
P34	1	Input	Port 34: 1-bit input port
/$\overline{CTS}$			Clear to send Serial data
P35	1	Output	Port 35: 1-bit output port
/RD			Read: Generates strobe signal for reading external memory
P36	1	Output	Port 36: 1-bit output port
/$\overline{WR}$			Write: Generates strobe signal for writing into external memory
P37	1	Input	Port 37: 1-bit input port
/$\overline{WAIT}$			Wait: Input pin for connecting slow speed memory or peripheral LSI
P40~P43	4	Output	Port 4: 4-bit output port that allows selection of Port/Address Bus on bit basis
/A16~A19			Address bus: Also functions as address bus for external memory (4 bits of bank address)
P50~P55	6	Input	Port 5: 6-bit input port
/AN0~AN5			Analog input: 6 analog inputs to A/D converter

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Pin Names and Functions (2/2)

Pin Name	No. of pins	I/O 3 states	Function
VREF	1		Input of reference voltage to A/D converter
AGND	1		Ground pin for A/D converter
P60~P63	4	I/O	Port 6: 4-bit I/O port that allows I/O selection on bit basis
/M00~M03		Output	Stepping motor control port 0
/TO1		Output	Timer output 1: Output of Timer 0 or 1
P70~P73	4	I/O	Port 7: 4-bit I/O port that allows I/O selection on bit basis
/M10~M13		Output	Stepping motor control port 1
/TO3		Output	Timer output 3: Output of Timer 2 or 3
P80	1	Input	Port 80: 1-bit input port
/INT0			Interrupt request pin 0: interrupt request pin (Level/rising edge is programmable)
P81	1	Input	Port 81: 1-bit input port
/INT1			Interrupt request pin 1: interrupt request pin (Rising/falling edge is programmable)
/TI4			Timer input 4: Counter/capture trigger signal for Timer 4
P82	1	Input	Port 82: 1-bit input port
/INT2			Interrupt request pin 2: rising edge interrupt request pin
/TI5			Timer input 5: capture trigger signal for Timer 4
P83	1	Output	Port 83: 1-bit output port
/TO3/TO4			Timer output 3/4: Output of Timer 2, 3 or 4
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Falling edge interrupt request pin
CLK	1	Output	Clock output: Generates clock pulse at 1/4 frequency of clock oscillation. It is Pulled up internally during resetting.
$\overline{EA}$	1	Input	External access: Connects with Vcc pin in the TMP90C840A using internal ROM, and with GND pin in the TMP90C841A with no internal ROM.
$\overline{RESET}$	1	Input	Reset : Initializes the LSI. (Built in pull-up resister)
X1/X2	2	Input/ Output	Pin for quartz crystal or ceramic resonator
Vcc	1		Power supply (+ 5V)
Vss (GND)	1		Ground (0V)

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(2) PROM Mode

Table 2.1

Pin Function Name	No. of pins	I/O	Function	Pin Name (MCU mode)
A7~A0	8	Input	Address Input	P17~P10
A13~A8	6	Input		P25~P20
A14	2	Input	Befixed to "L" level.	P26
A15				P27
D7~D0	8	I/O	Data Input/Output	P07~P00
$\overline{OE}$	1	Input	Output Enable Input	P35
$\overline{CE}$	1	Input	Chip Enable Input	P36
VPP	1	Power Supply	12.5V / 5V (Programming Power Supply)	$\overline{EA}$
VCC	1	Power Supply	5V	VCC
VSS	1	Power Supply	0V	VSS

Pin Name	No. of pins	I/O	Pin Setting
P30, P31	2	Input	Be fixed to "L" level.
P32, P33	2	Output	Open
P34, P37	2	Input	Be fixed to "L" level.
P43~P40	4	Output	Open
P55~P50 P63~P60 P73~P70 P82~P80	6 4 4 3	Input	Be fixed to "L" level.
P83	1	Output	Open
VREF	1		Be fixed to "L" level.
AGND	1		Be fixed to "L" level.
$\overline{RESET}$	1	Input	Be fixed to "L" level.
CLK	1	Input	Be fixed to "L" level.
$\overline{NMI}$	1	Input	Be fixed to "H" level.
X1	1	Input	Resonator connection pin
X2	1	Output	

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3. OPERATION

The TMP91P640 is the EPROM/OTP version of the TMP91C640 that is replaced an internal ROM from Mask ROM to EPROM. Packaging of TMP91P640 selects whether it is EPROM version or OTP version. It is called EPROM version which is housed in CERDIP with window and is called OTP version which is housed in Plastic Package.

The function of TMP91P640 is exactly same as that of TMP90C840A except the internal ROM/RAM size.

Refer to the TMP90C840A except the functions which are not described this section.

The following is an explanation of the hardware configuration and operation in relation to the TMP91P640.

The TMP91P640 has an MCU mode and a PROM mode.

3.1 MCU Mode

(1) Mode Setting and Function

The MCU mode is set by opening the CLK pin (Output status).

In the MCU mode, the operation is same as that of TMP91C640.

(2) Memory Map

The memory map is same as that of TMP91C640.

Figure 3.1 shows the memory map of TMP91P640, and the accessing area by the respective addressing mode.

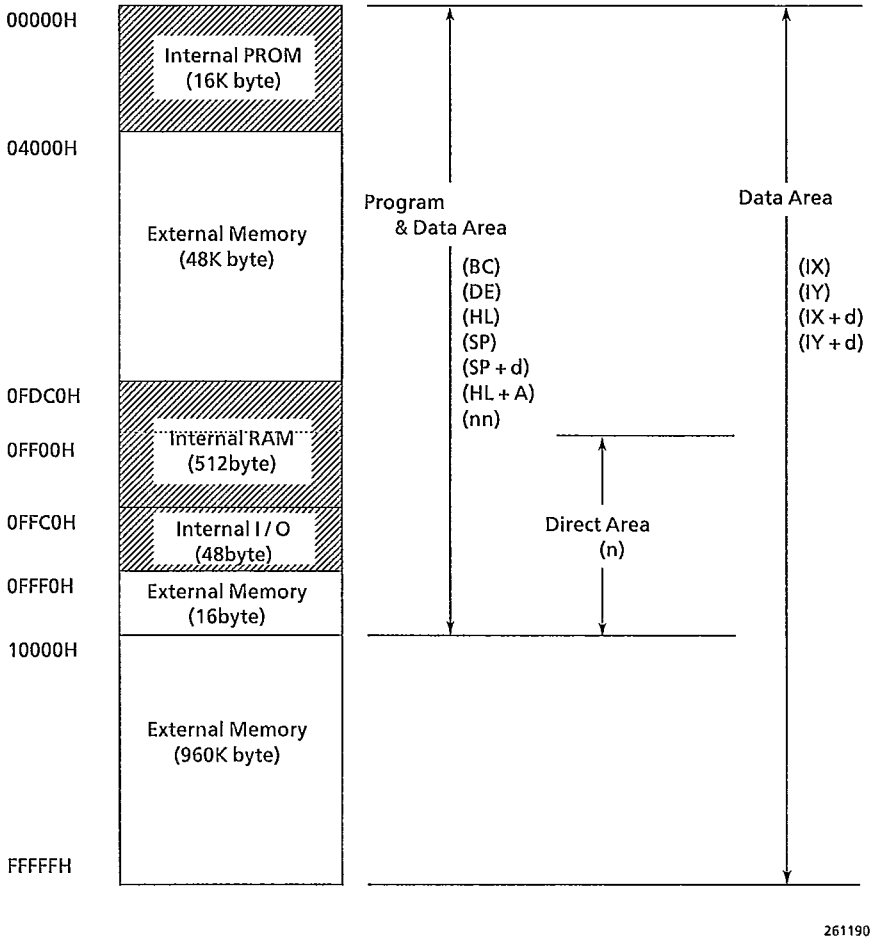


Figure 3.1 TMP91P640 Memory Map

3.2 PROM Mode

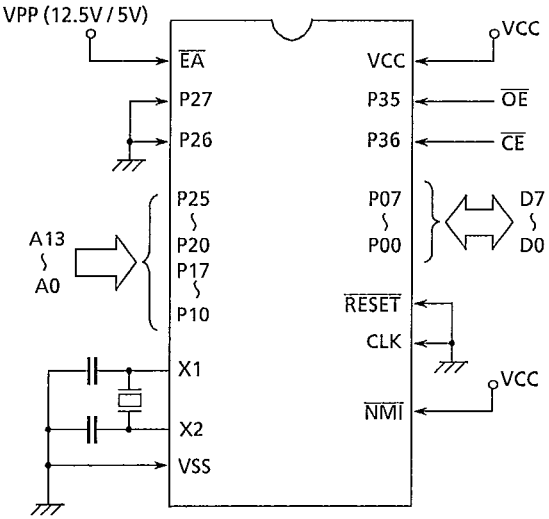
(1) Mode Setting and Function

PROM mode is set by setting the $\overline{\text{RESET}}$ and CLK pins to the "L" level.

The programming and verification for the internal PROM is achieved by using a general EPROM programmer with the adaptor socket. The device selection (ROM Type) should be "27256" with following conditions.

size : 256Kbit (32K×8bit) VPP : 12.5V TPW : 1msec

Figure 3.2 shows the setting of pins in PROM mode.



For other pins, refer to the section on pin functions (Figure 2.1).

※ Use the 10MHz resonator in case of programming and verification by a general EPROM programmer.

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Figure 3.2 PROM Mode Pin Setting

(2) Programming Flow Chart

The programming mode is set by applying 12.5V (programming voltage) to the VPP pin when the following pins are set as follows,

Vcc : 6.0V
$\overline{\text{RESET}}$: "L" level
CLK : "L" level

* These conditions can be obtained by using adaptor socket.

After the addres and data have been fixed, a data on the Data Bus is programmed when the $\overline{\text{CE}}$ pin is set to "Low" (1ms plus is required).

General programming procedure of an EPROM programmer is as follows,

- Write a data to a specified address for 1ms.
- Verify the data. If the read-out data does not match the expected data, another writing is performed until the correct data is written (Max. 25 times).

After the correct data is written, an additional writting is performed by using three times longer programming pulse width (1ms×programming times), or using three times

more programming pulse number. Then, verify the data and increment the address.

The verification for all data is done under the condition of Vpp=Vcc=5V after all data were witten.

Figure 3.3 shows the programming flow chart.

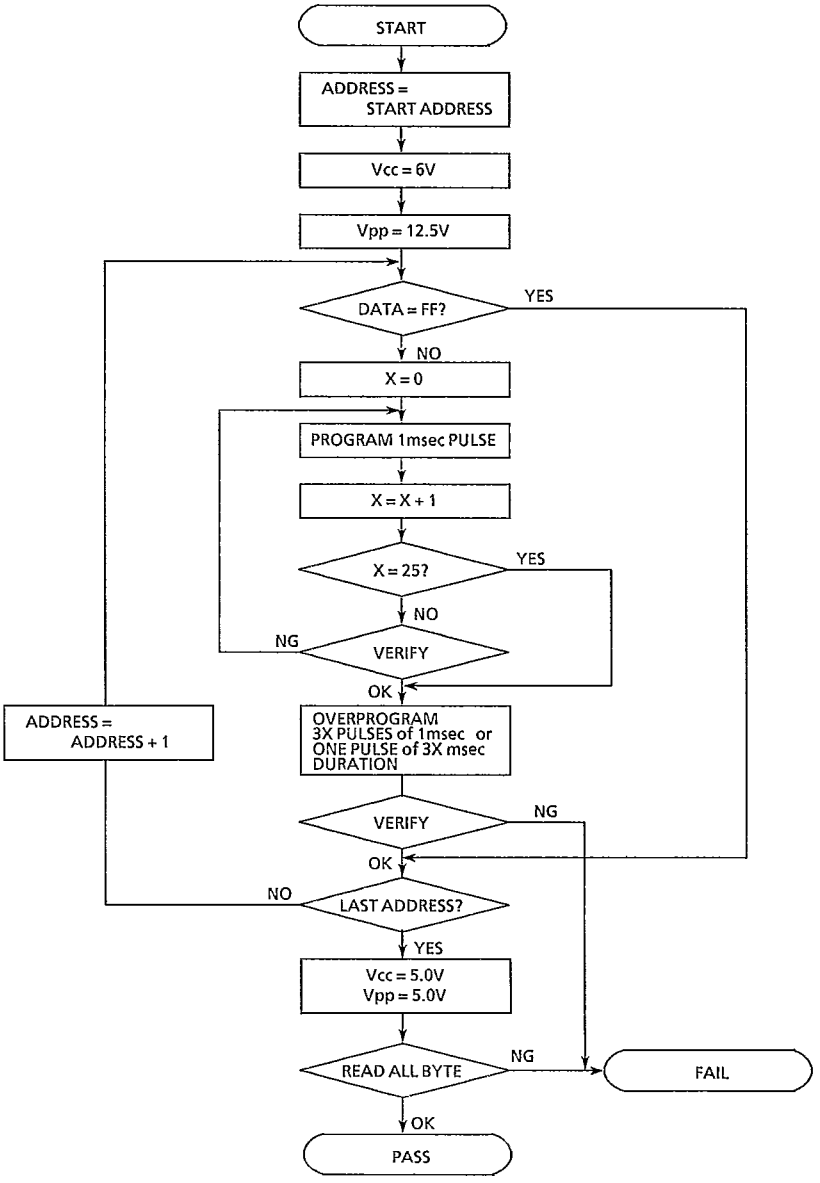

Figure 3.3 Flow Chart

4. ELECTRICAL CHARACTERISTICS

TMP91P640E-10/TMP91P640N-10/TMP91P640F-10

4.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Supply voltage	−0.5 ~ +7	V
V_{IN}	Input voltage	−0.5 ~ Vcc + 0.5	V
P_D	Power dissipation (Ta = 85°C)	F 500 N 600	mW
T_{SOLDER}	Soldering temperature (10Sec)	260	°C
T_{STG}	Storage temperature	−65 ~ 150	°C
T_{OPR}	Operating temperature	−40 ~ 85	°C

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4.2 DC Characteristics

Vcc = 5V ± 10% TA = −40~85°C (1~10MHz)
Typical Values are for TA = 25°C and Vcc = 5V.

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (P0)	−0.3	0.2Vcc − 0.1	V	
V_{IL1}	P1, P2, P3, P4, P5, P6, P7, P8	−0.3	0.3Vcc	V	
V_{IL2}	$\overline{RESET}$, INT0 (P80), $\overline{NMI}$	−0.3	0.25Vcc	V	
V_{IL3}	$\overline{EA}$	−0.3	0.3	V	
V_{IL4}	X1	−0.3	0.2Vcc	V	
V_{IH}	Input High Voltage (P0)	0.2Vcc + 1.1	Vcc + 0.3	V	
V_{IH1}	P1, P2, P3, P4, P5, P6, P7, P8	0.7Vcc	Vcc + 0.3	V	
V_{IH2}	$\overline{RESET}$, INT0 (P80), $\overline{NMI}$	0.75Vcc	Vcc + 0.3	V	
V_{IH3}	$\overline{EA}$	Vcc − 0.3	Vcc + 0.3	V	
V_{IH4}	X1	0.8Vcc	Vcc + 0.3	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 1.6mA
V_{OH} V_{OH1} V_{OH2}	Output High Voltage	2.4 0.75Vcc 0.9Vcc		V V V	I_{OH} = −400μA I_{OH} = −100μA I_{OH} = −20μA
I_{DAR}	Darlington Drive Current (8 I/O pins)	−1.0	−3.5	mA	V_{EXT} = 1.5V R_{EXT} = 1.1 kΩ
I_{LI}	Input Leakage Current	0.02 (Typ)	±5	μA	0.0 ≦ Vin ≦ Vcc
I_{LO}	Output Leakage Current	0.05 (Typ)	±10	μA	0.2 ≦ Vin ≦ Vcc − 0.2
I_{CC}	Operating Current (RUN) Idle 1 Idle 2	20 (Typ) 1.5 (Typ) 9 (Typ)	40 5 15	mA mA mA	fosc = 10MHz
	STOP (TA = −40~85°C) STOP (TA = 0~50°C)	0.2 (Typ)	50 10	μA μA	0.2 ≦ Vin ≦ Vcc − 0.2
V_{STOP}	Power Down Voltage (@STOP)	2 RAM BACK UP	6	V	V_{IL2} = 0.2Vcc, V_{IH2} = 0.8Vcc
R_{RST}	$\overline{RESET}$ Pull Up Registor	50	150	KΩ	
CIO	Pin Capacitance		10	pF	testfreq = 1MHz
V_{TH}	Schmitt width $\overline{RESET}$, $\overline{NMI}$, INT0	0.4	1.0 (Typ)	V	

Note : I_{DAR} is guaranteed for a total of up to 8 optional ports.

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4.3 AC Characteristics

Vcc = 5V ± 10% TA = −40 ~ 85°C (1 ~ 10MHz)
CL = 50pF

Symbol	Parameter	Variable		10MHz Clock		Units
		Min	Max	Min	Max	
t_{OSC}	OSC. Period = x	100	1000	100		ns
t_{CYC}	CLK Period	4x	4x	400		ns
t_{WL}	CLK Low width	2x − 40		160		ns
t_{WH}	CLK High width	2x − 40		160		ns
t_{AC}	Address Setup to $\overline{RD}$, $\overline{WR}$	x − 45		55		ns
t_{RR}	$\overline{RD}$ Low width	2.5x − 40		210		ns
t_{CA} *	Address Hold Time After $\overline{RD}$, $\overline{WR}$	0.5x − 40		10		ns
t_{AD}	Address to Valid Data In		3.5x − 95		255	ns
t_{RD}	$\overline{RD}$ to Valid Data In		2.5x − 80		170	ns
t_{HR}	Input Data Hold After $\overline{RD}$	0		0		ns
t_{WW}	$\overline{WR}$ Low width	2.5x − 40		210		ns
t_{DW}	Data Setup to $\overline{WR}$	2x − 50		150		ns
t_{WD}	Data Hold After $\overline{WR}$	30	90	30	90	ns
t_{CWA}	$\overline{RD}$, $\overline{WR}$ to Valid $\overline{WAIT}$		1.5x − 100		50	ns
t_{AWA}	Address to Vaild $\overline{WAIT}$		2.5x − 130		120	ns
t_{WAS}	$\overline{WAIT}$ Setup to CLK	70		70		ns
t_{WAH}	$\overline{WAIT}$ Hold After CLK	0		0		ns
t_{RV}	$\overline{RD}$/$\overline{WR}$ Recovery Time	1.5x − 35		115		ns
t_{CPW}	CLK to Port Data Output		x + 200		300	ns
t_{PRC}	Port Data Setup to CLK	200		200		ns
t_{CPR}	Port Data Hold After CLK	100		100		ns
t_{CHCL}	$\overline{RD}$/$\overline{WR}$ Hold After CLK	x − 60		40		ns
t_{CLC}	$\overline{RD}$/$\overline{WR}$ Setup to CLK	1.5x − 50		100		ns
t_{CLHA}	Address Hold After CLK	1.5x − 80		70		ns
t_{ACL}	Address Setup to CLK	2.5x − 80		170		ns
t_{CLD}	Data Setup to CLK	x − 50		50		ns

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- AC output level High 2.2V/Low 0.8V
- AC input level High 2.4V/Low 0.45V (D0 − D7)
  High 0.8Vcc/Low 0.2Vcc (excluding D0 − D7)

* t_{CA} spec is different from other parts of TLCS-90.

4.4 A/D Conversion Characteristics

Vcc = 5V ± 10% TA = −40~85℃ (1~10MHz)

Symbol	Parameter	Min	Typ	Max	Unit
V_{REF}	Analog reference voltage	Vcc − 1.5	Vcc	Vcc	V
A_{GND}	Analog reference voltage	V_{SS}	V_{SS}	Vss	
V_{AIN}	Allowable analog input voltage	V_{SS}		Vcc	
I_{REF}	Supply current for analog reference voltge		0.5	1.0	mA
Error	Total error (TA = 25℃, Vcc = VREF = 5.0V)			1.5	LSB
	Total error			3.0	

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4.5 Zero- Cross Characteristics

Vcc = 5V ± 10% TA = −40~85℃ (1~10MHz)

Symbol	Parameter	Condition	Min	Max	Unit
Vzx	Zero- cross detection input	AC coupling C = 0.1μF	1	1.8	VAC p − p
Azx	Zero- cross accuracy	50/60Hz sine wave		135	mV
Fzx	Zero- cross detection input frequency		0.04	1	KHz

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4.6 Serial Channel Timing – I/O Interface Mode

Vcc = 5V ± 10% TA = −40~85℃ (1~10MHz)
CL = 50pF

Symbol	Parameter	Variable		10MHz Clock		Unit
		Min	Max	Min	Max	
t_{SCY}	Serial Port Clock Cycle Time	8x		800		ns
t_{OSS}	Output Data Setup SCLK Rising Edge	6x − 150		450		ns
t_{OHS}	Output Data Hold After SCLK Rising Edge	2x − 120		80		ns
t_{HSR}	Input Data Hold After SCLK Rising Edge	0		0		ns
t_{SRD}	SCLK Rising Edge to Input DATA Valid		6x − 150		450	ns

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4.7 16-bit Event Counter

Vcc = 5V ± 10% TA = −40~85℃ (1~10MHZ)

Symbol	Parameter	Variable		10MHz Clock		Units
		Min	Max	Min	Max	
t_{VCK}	TI4 clock cycle	8x + 100		900		ns
t_{VCKL}	TI4 Low clock pulse width	4x + 40		440		ns
t_{VCKH}	TI4 High clock pulse width	4x + 40		440		ns

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4.8 Interrupt Operation

Vcc = 5V ± 10% TA = −40~85℃ (1~10MHZ)

Symbol	Parameter	Variable		10MHz Clock		Units
		Min	Max	Min	Max	
t_{INTAL}	$\overline{NMI}$, INT0 Effective pulse width (⊓)	4x		400		ns
t_{INTAH}	$\overline{NMI}$, INT0 Effective pulse width (⊔)	4x		400		ns
t_{INTBL}	INT1, INT2 Effective pulse width (⊓)	8x + 100		900		ns
t_{INTBH}	INT1, INT2 Effective pulse width (⊔)	8x + 100		900		ns

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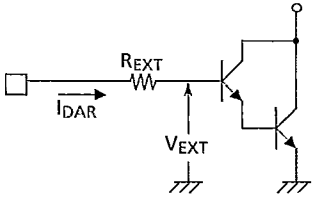
(Reference) Definition of I_{DAR}



4.9 Read Operation (PROM Mode)

DC Characteristic, AC Characteristic

TA = −40~85°C Vcc = 5V ± 10%

Symbol	Parameter	Condition	Min	Max	Unit
V_{PP}	V_{PP} Read Voltage	–	4.5	5.5	V
V_{IH1}	Input High Voltage (A0~A15, $\overline{CE}$, $\overline{OE}$)	–	0.7 × V_{CC}	V_{CC} + 0.3	V
V_{IL1}	Input Low Voltage (A0~A15, $\overline{CE}$, $\overline{OE}$)	–	−0.3	0.3 × V_{CC}	V
t_{ACC}	Address to Output Delay	C_L = 50pF	–	2.25TCYC + α	ns

TCYC = 400ns (10MHz Clock)
α = 200ns

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4.10 Programming Operation (PROM Mode)

DC Characteristic, AC Characteristic

TA = 25 ± 5°C Vcc = 6V ± 0.25V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PP}	Programing Voltage	–	12.25	12.50	12.75	V
V_{IH}	Input High Voltage (D0~D7)	–	0.2V_{CC} + 1.1		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage (D0~D7)	–	−0.3		0.2V_{CC}-0.1	V
V_{IH1}	Input High Voltage (A0~A15, $\overline{CE}$, $\overline{OE}$)	–	0.7V_{CC}		V_{CC} + 0.3	V
V_{IL1}	Input Low Voltage (A0~A15, $\overline{CE}$, $\overline{OE}$)	–	−0.3		0.3V_{CC}	V
I_{CC}	V_{CC} Supply Current	f_{OSC} = 10MHz	–		50	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = 13.00V	–		50	mA
t_{PW}	$\overline{CE}$ Programming Pulse Width	C_L = 50pF	0.95	1.00	1.05	ms

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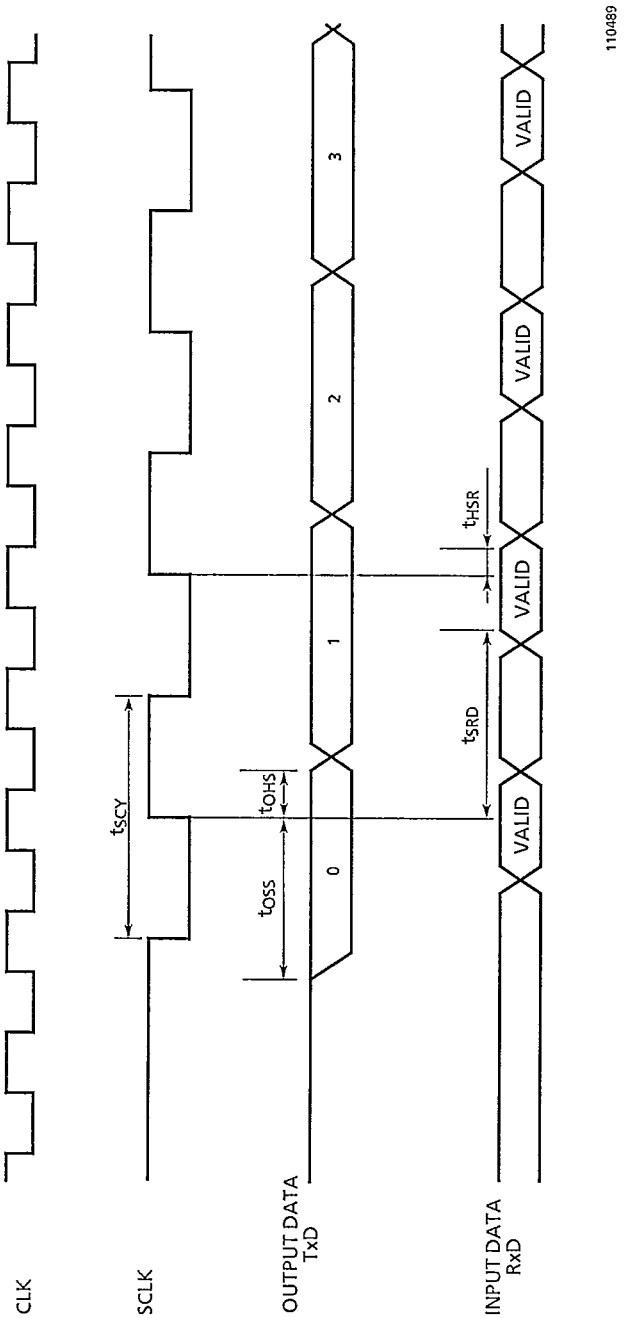
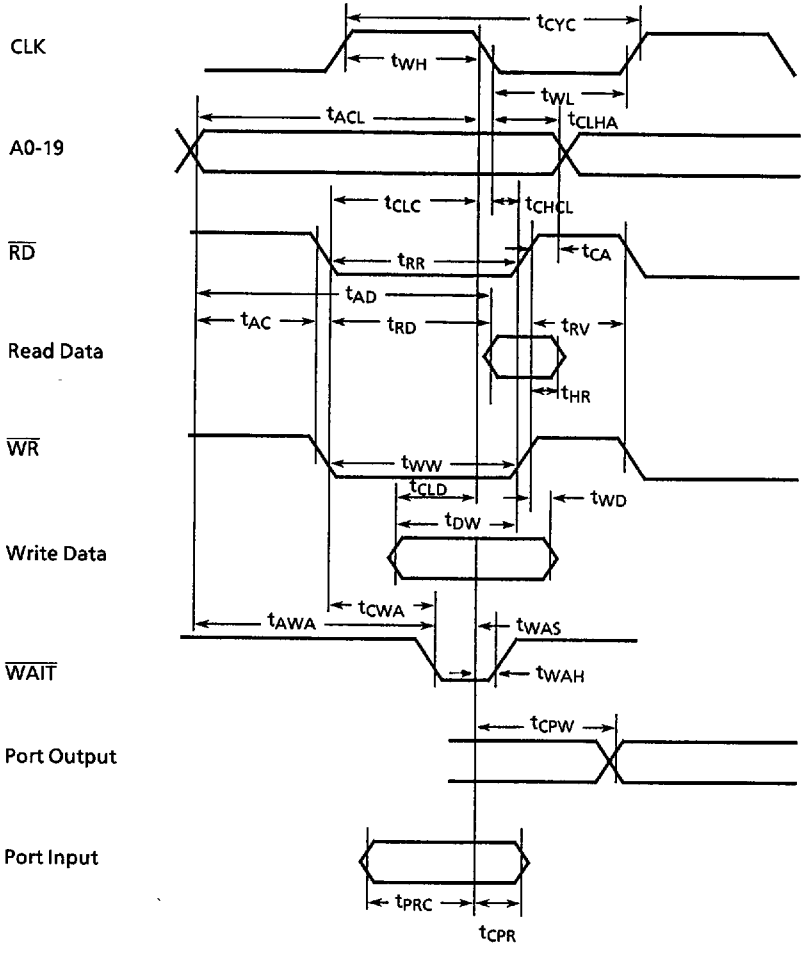
4.11 I/O Interface Mode Timing Chart



4.12 Timing Chart



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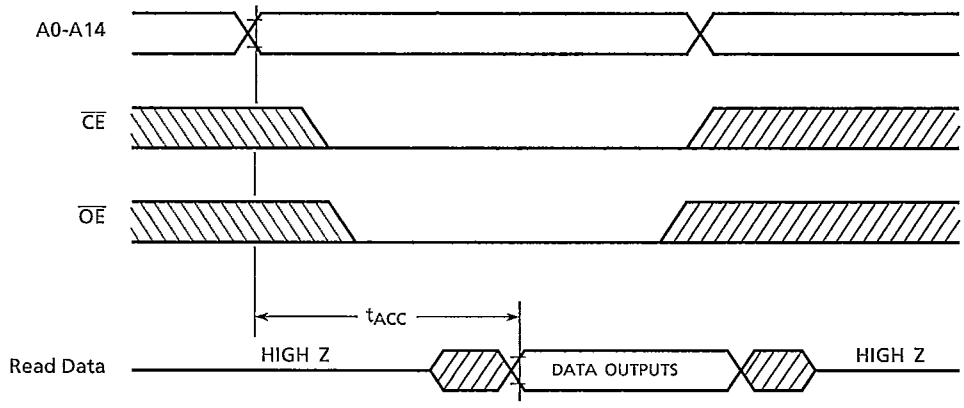
4.13 Read Operation Timing Chart (PROM Mode)



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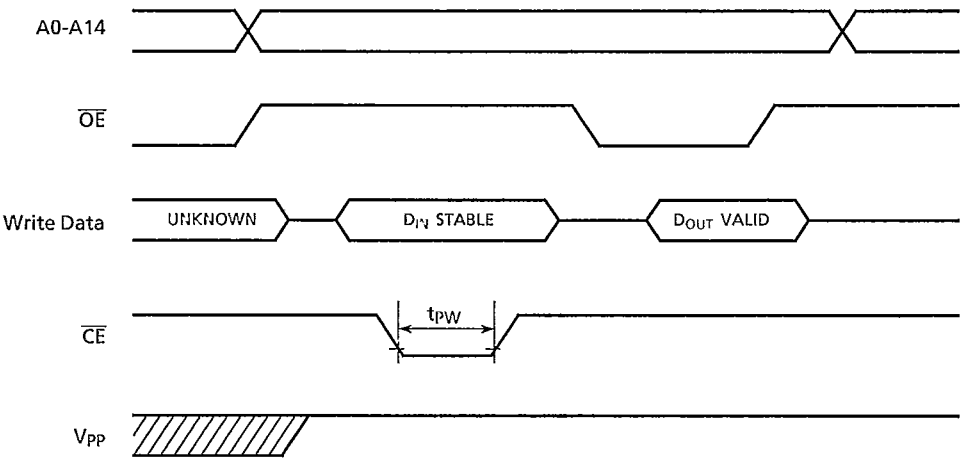
4.14 Programming Operation Timing Chart (PROM Mode)



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(2) The channel clock, bit clock and data format for data outputs SDO0~2 are selected by LROS0~2, BCOS02 and SOFMT0~1 of control register 2 (CNT-R2).
Table 2 (a), (b), and (c) show setting modes for data outputs SDO0-2.

Table 2. (a) Setting Modes for Data Output SDO0

CONTROL REGISTER					FORMATS FOR DATA OUTPUT SDO0				
CNT-R2				CNT-R1	DATA	BIT CLOCK		CHANNEL CLOCK	DATA FORMAT
LROS0	BCOS0	SOFMT0	LROS2	EBCS					
0	0	0	*	0	16bit	32fs (FS32 terminal) Internally generated		LR terminal Internally generated	MSB first
0	1	0	*	0	24bit	64fs (FS64 terminal) Internally generated		LR terminal Internally generated	MSB first, effective data after the change point of LRCK
*	0	0	*	1	16bit	32fs (FS32 terminal) 1/2 of EBCI0 (64fs)		ELRO terminal Internally generated	MSB first
*	1	1	0	0	24bit	64fs (FS64 terminal) Internally generated		LR terminal (※1) Internally generated	MSB first, effective data after the change point of LRCK (8 clock shift output)
1	*	0	*	0	16bit	32fs	EBCO terminal Externally input	ELRO terminal Externally input	MSB first
					24bit	48fs			MSB first, effective data after the change point of LRCK
						64fs			
1	*	1	1	0	16bit	48fs	EBCO terminal Externally input	ELRO terminal Externally input	MSB first, effective data after the change point of LRCK (8 clock shift output)
					24bit	64fs			

* : Don't care
(※1) Clock output from LR terminal is input to ELRO terminal.

Table 2. (b) Setting Modes for Data Output SDO1

CONTROL REGISTER					FORMATS FOR DATA OUTPUT SDO1				
CNT-R2				CNT-R1	DATA	BIT CLOCK		CHANNEL CLOCK	DATA FORMAT
LROS1	BCOS1	SOFMT1	LROS2	EBCS					
0	0	0	*	0	16bit	32fs (FS32 terminal) Internally generated		LR terminal Internally generated	MSB first
0	1	0	*	0	24bit	64fs (FS64 terminal) Internally generated		LR terminal Internally generated	MSB first, effective data after the change point of LRCK
*	0	0	*	1	16bit	32fs (FS32 terminal) 1/2 of EBCI0 (64fs)		ELRO terminal Internally generated	MSB first
*	1	1	0	0	24bit	64fs (FS64 terminal) Internally generated		LR terminal (※1) Internally generated	MSB first, effective data after the change point of LRCK (8 clock shift output)
1	*	0	*	0	16bit	32fs	EBCO terminal Externally input	ELRO terminal Externally input	MSB first
					24bit	48fs			MSB first, effective data after the change point of LRCK
						64fs			
1	*	1	1	0	16bit	48fs	EBCO terminal Externally input	ELRO terminal Externally input	MSB first, effective data after the change point of LRCK (8 clock shift output)
					24bit	64fs			

Table 2. (c) Setting Modes for Data Output SDO2

CONTROL REGISTER				FORMATS FOR DATA OUTPUT SDO2				
CNT-R2			CNT-R1	DATA	BIT CLOCK		CHANNEL CLOCK	DATA FORMAT
LROS2	BCOS2	LROS2	EBCS					
0	0	*	0	16bit	32fs (FS32 terminal) Internally generated		LR terminal Internally generated	MSB first
0	1	*	0	24bit	64fs (FS64 terminal) Internally generated		LR terminal Internally generated	MSB first, effective data after the changepoint of LRCK
*	0	*	1	16bit	32fs (FS32 terminal) 1/2 of EBCI0 (64fs)		ELRO terminal Internally generated	MSB first
*	1	0	0	24bit	64fs (FS64 terminal) Internally generated		LR terminal (※1) Internally generated	MSB first, effective data after the change point of LRCK (8 clock shift output)
1	*	*	0	16bit	32fs	EBCO terminal Externally input	ELRO terminal Externally input	MSB first
				24bit	48fs			MSB first, effective data after the change point of LRCK
					64fs			
1	*	1	0	16bit	48fs	EBCO terminal Externally input	ELRO terminal Externally input	MSB first, effective data after the change point of LRCK (8 clock shift output)
				24bit	64fs			

* : Don't care

(※1) Clock output from LR terminal is input to ELRO terminal.

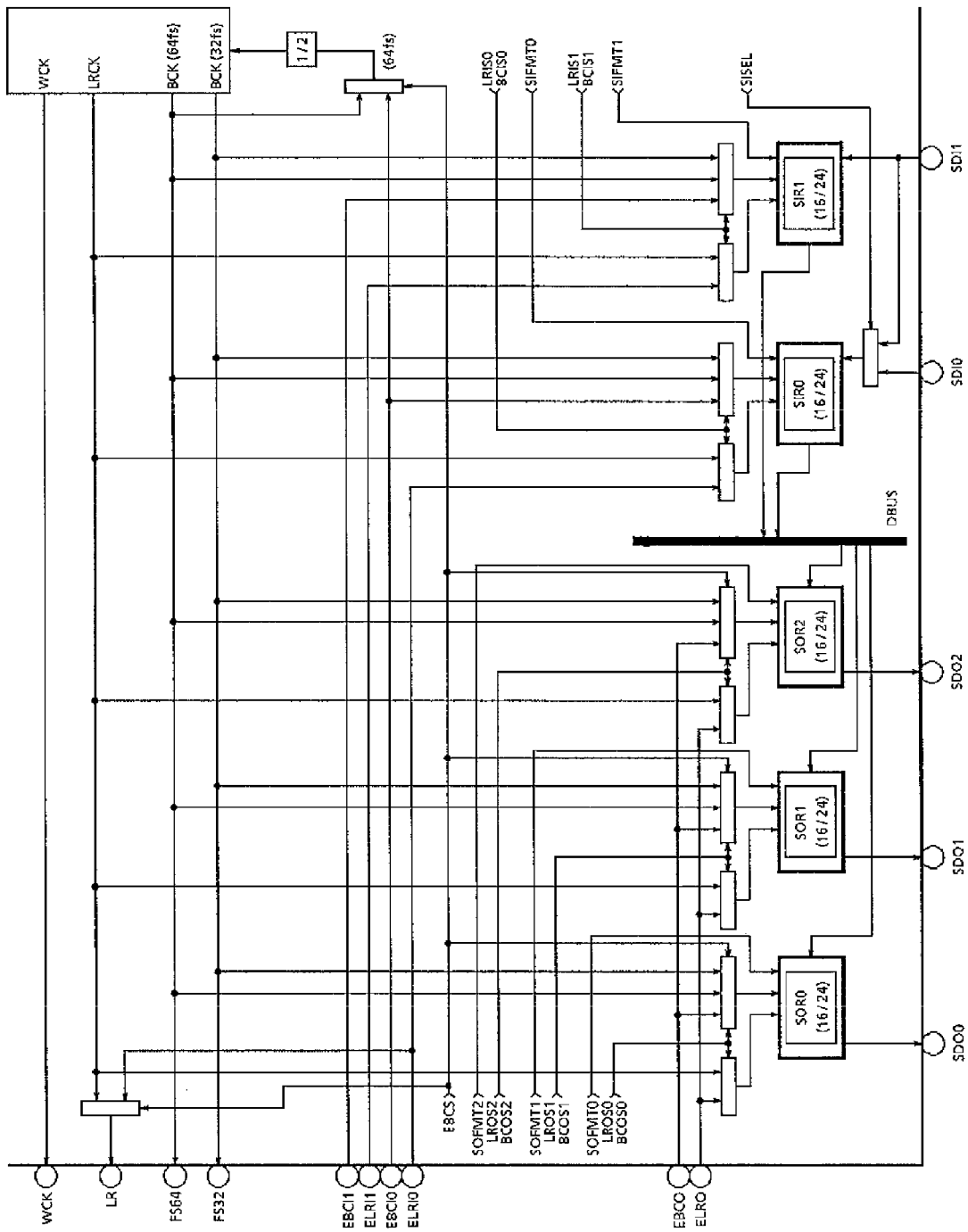

Fig.5 Data Input/Output Clock Selector

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