CMOS 8-BIT MICROCONTROLLERS

TMP91C642AN / TMP91C642AF

1. OUTLINE AND CHARACTERISTICS

The TMP91C642A is an advanced-function and highly integrated 8-bit microcontroller which is developed for use with software servos.

In addition to I/O ports and other basic components, the TMP91C642A has high-speed high-precision signal measuring circuit, PWM dedicated output, and high-precision timing pulse circuit that simplify control of VCR systems and servo motors.

The TMP91C642AN is a 64-pin shrink DIP product. (SDIP64-P-750)

The TMP91C642AF is a 64-pin flat package product. (QFP64-P-1420A)

The characteristics of the TMP91C642A include :

(1) Efficient instructions

163 basic instructions
Instructions for multiplication, division, 16-bit arithmetic operations, bit manipulation

(2) Minimum execution time : 400 ns (at 10 MHz oscillation frequency)

(3) Internal ROM : 16 K bytes

(4) Internal RAM : 320 bytes

(5) 18-bit time base counter

(6) Servo input control pins : drum FG / PG, Capstan FG, P-CTL, and EXT

(7) VISS / VASS detection

- P-CTL Duty discriminator
- 16-bit VASS data latch

(8) Composite sync (C-sync) input

- Vertical sync signal (V-sync) separation
- Odd-even field discriminator
- 60 / 50 Field discriminator

(9) 24-bit time base counter capture with 8-step FIFO

(10) 32-bit timing pulse generator with 8-step FIFO
(16-bit comparate data × 2, 16-bit timing output × 2, maximum 20-bit output simultaneously)

(11) Servo control output pins (drum motor, capstan motor, current limitter control)

12-bit PWM output (2 channels)
8-bit PWM output (1 channel)

(12) 8-bit timer / counter (4 channels)

- 1 channel for reloadable timer with up / down mode
- Readable counter data (writable for one channel)

(13) General-purpose synchronized serial interface (2 channels)

(14) High-precision 8-bit A/D converter (8 + 4 channels)

(15) Input / Output ports : 54 pins

(16) Interrupt function : 10 internal interrupts and 3 external interrupts

(17) Micro Direct Memory Access (DMA) function (10 channels)

(18) Watchdog timer

(19) Standby function (2 HALT mode)

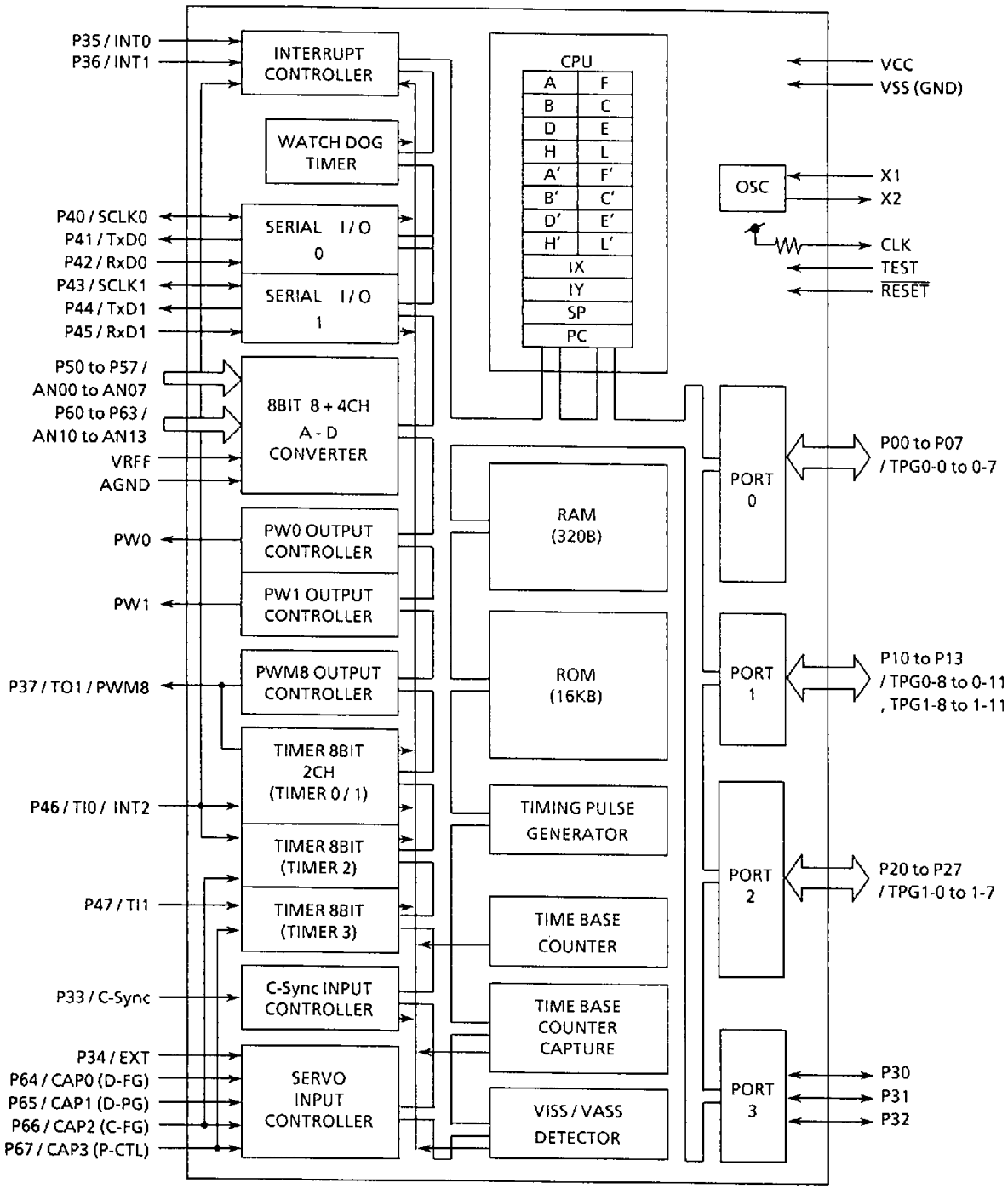


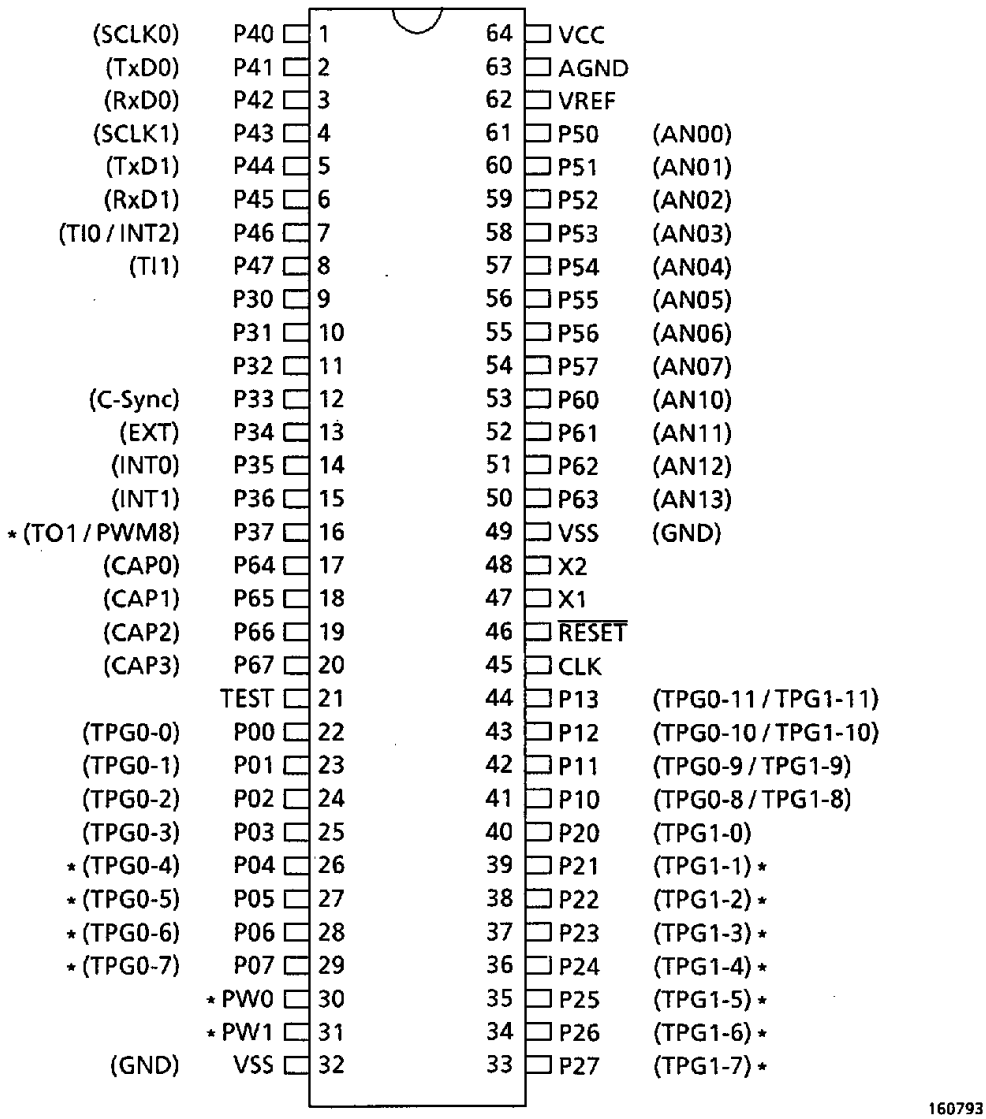
Figure 1 TMP91C642A Block Diagram

2. PIN ASSIGNMENT AND FUNCTIONS

The assignment of input/output pins, their names and functions are as shown below.

2.1 Pin Assignment

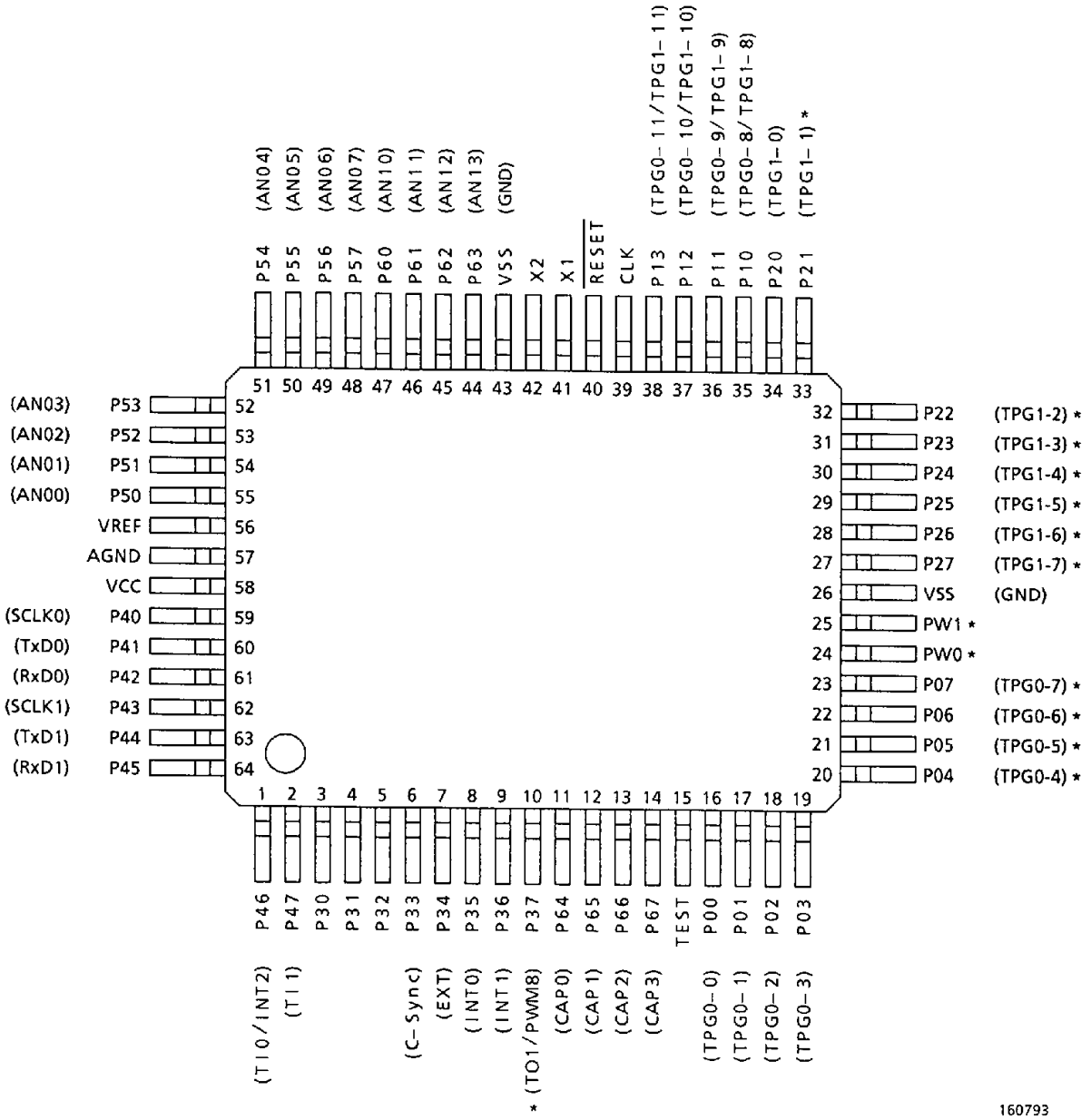
Figure 2.1 (1) shows pin assignment of the TMP91C642AN.



*) open drain pin

Figure 2.1 (1) Pin Assignment (shrink DIP)

Figure 2.1 (2) shows pin assignment of the TMP91C642AF.



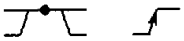
*) open drain pin

Figure 2.1 (2) Pin Assignment (flat package)

2.2 Pin Names and Functions

The name of input / output pins and their functions are summarized in Table 2.2.

Table 2.2 Pin Names and Functions (1/3)

Pin name	Number of pins	I/O or 3-state	Function
P00 / TPG0-0 to P07 / TPG0-7	8	I/O, 3-state* (P04 to P07 are open drain output pins.)	Port 0 : 8-bit I/O port. I/O specifiable in units of bytes.
			Timing pulse generator (TPG) output: Can also be used as TPG0-0 to TPG0-7 output pins. *P00 only can be set to 3-state by internal signals to TPG0-15.
P10/TPG0-8 /TPG1-8 to P13 /TPG0-11 / TPG1-11	4	I/O, 3-state*	Port 1 : 4-bit I/O port. I/O specifiable in units of bits.
			Timing pulse generator (TPG) output: Can also be used as TPG0-8 to TPG0-11/TPG1-8 to TPG1-11 output pins. *P10 only can be set to 3-state by internal signals to TPG0-14/TPG1-14.
P20 / TPG1-0 to P27 / TPG1-7	8	I/O, 3-state* (P21 to P27 are open drain output pins.)	Port 2 : 8-bit I/O port. I/O specifiable in units of bits.
			Timing pulse generator (TPG) output: Can also be used as TPG1-0 to TPG1-7 output pins. *P20 only can be set to 3-state by internal signals to TPG1-15.
P30 to P32	3	I/O	Port 3 : 3-bit I/O port. I/O specifiable in units of bits.
P33 / C-Sync	1	I/O	Port 3 : 1-bit I/O port. I/O specifiable.
			Composite sync input
P34 / EXT	1	I/O	Port 3 : 1-bit I/O port. I/O specifiable.
			Servo signal trigger input
P35 / INT0	1	Input	Port 3 : 1-bit input port.
			Interrupt request pin 0 : Level and rising edge are programmable. 
P36 / INT1	1	Input	Port 3 : 1-bit input port.
			Interrupt request pin 1 : at rising edge. 
P37 / PWM8 / TO1	1	Open drain output	Port 3 : 1-bit output port.
			Motor control output : PWM8 output
			Timers 0 and 1 output : timer 0 and 1 output.

(Note) * : Only 1 put can be set to the 3-state.

Table 2.2 Pin Names and Functions (2/3)

Pin name	Pin name	I/O or 3-state	Function
P40 / SCLK0, P43 / SCLK1	2	I/O	Port 4 : 2-bit I/O port. I/O specifiable in units of bits.
			Serial clock I/O 0 and 1
P41 / TxD0, P44 / TxD1	2	I/O	Port 4 : 2-bit I/O port. I/O specifiable in units of bits.
			Serial send data 0 and 1
P42 / RxD0, P45 / RxD1	2	I/O	Port 4 : 2-bit I/O port. I/O specifiable in units of bits.
			Serial receive data 0 and 1
P46 / TI0 / INT2	1	I/O	Port 4 : 1-bit I/O port. I/O specifiable.
			Timer 0/timer 2 count input
			Interrupt request pin 2 : at rising edge
P47 / TI1	1	I/O	Port 4 : 1-bit I/O port. I/O specifiable.
			Timer 3 count input
P50 / AN00 to P57 / AN07	8	Input	Port 5 : 8-bit input port. I/O specifiable.
			Analog input 0 : 8 analog inputs to A/D converter
P60 / AN10 to P63 / AN13	4	I/O	Port 6 : 4-bit I/O port. I/O specifiable in units of bits.
			Analog input 1 : 4 analog inputs to A/D converter
P64 / CAP0 to P67 / CAP3	4	Input	Port 6 : 4-bit input port.
			Servo signal trigger input
PW0	1	Open drain output	Motor control output : PWM0 output
PW1	1	Open drain output	Motor control output : PWM1 output
VREF	1	–	A/D converter reference voltage input
AGND	1	–	Grauond pin for A/D converter
CLK	1	–	Pulled up internally (Do not connect an external circuit.)

Table 2.2 Pin Names and Functions (3/3)

Pin name	Number of pins	I/O or 3-state	Function
TEST	1	–	Test pin (normally pulled up)
$\overline{\text{RESET}}$	1	Input	Reset : Initializes the TMP91C642A. (Built-in pull-up registor)
X_1 / X_2	2	I/O	Crystal oscillator connector pin
VSS (GND)	2	–	GND pin (0 V)
VCC	1	–	Power supply pin (+ 5 V)

3. OPERATION

This chapter covers the functions and basic operations of the TMP91C642A by blocks.

3.1 CPU

TMP91C642A includes a high-performance 8-bit CPU. For the function of the CPU, see the previous chapter "TLCS-90 CPU".

This chapter explains exclusively the functions of the CPU of TMP91C642A which are not discribed in the chapter "TLCS-90 CPU".

3.1.1 Reset

Figure 3.1 shows the basic timing of reset.

To reset the TMP91C642A, the power supply voltage must be within the operating voltage and oscillation by the internal oscillator must be stable. Also, the $\overline{\text{RESET}}$ input must be maintained at level 0 for at least 10 system clocks (10 states : 2 μs at 10 MHz clock oscillation).

When a reset is accepted, all I/O ports (port 0, port 1, port 3 (P30 to P34), port 4, and port 6 (P60 to P63) are set to input (high impedance). Output dedicated port *CLK is set to "1" and P37 (PWM8) to high impedance. The other output dedicated ports (PW0 and PW1) are set to "0". The input dedicated ports remain the same.

The CPU registers do not change. The program counter (PC) and interrupt enable flag IFF are cleared to "0". Register A becomes indeterminate.

When a reset is cleared, the CPU starts execution from address 0000H.

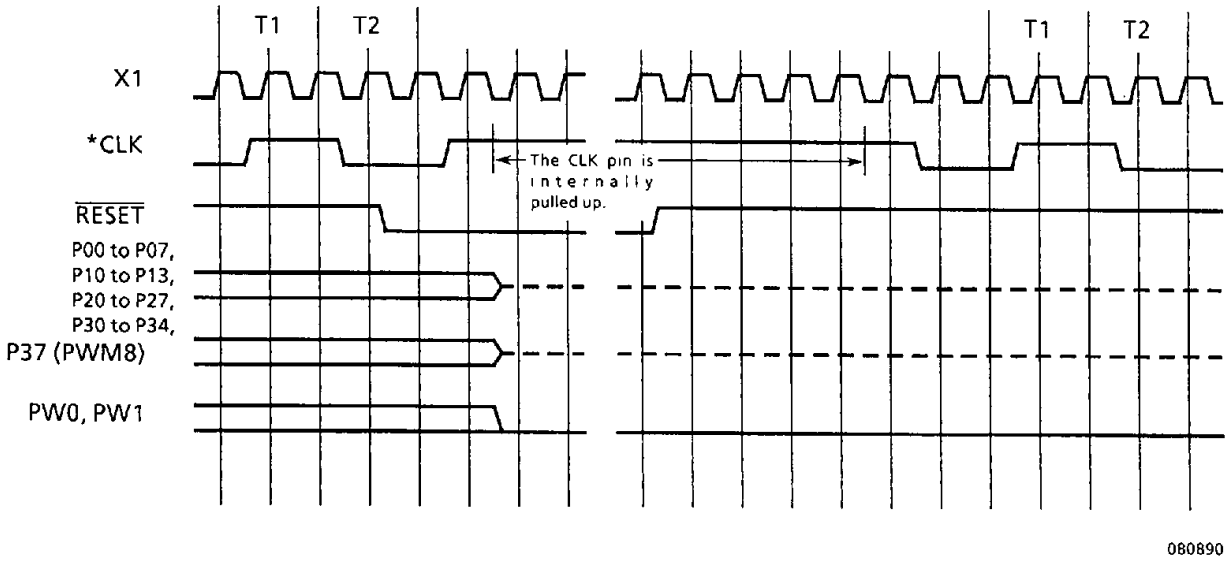


Figure 3.1 Reset Timing

(Note) * With the TMP91C642A, CLK is always internally pulled up to "1".

3.1.2 Exchange Flag (EXF)

The EXF register is inverted by execution of data exchange instruction EXX, which exchanges data between the main and the auxiliary registers. The TMP91C642A allocates the EXF register to bit 1 at address FFE6H in memory.

The EXF register is not initialized by the reset operation.

Watchdog Timer Mode Register

WDMOD (FFE6H)

	7	6	5	4	3	2	1	0
bit Symbol		FTBC2	FTBC1	WDTE	FTPG	HALT	EXF	DRVE
Read/Write		R/W	R/W	R/W	R/W	R/W	R	R/W
Value after reset		0	0	1	0	0	Underfined	0
Function		1: TBC15 to 18 interrupt flag	1: TBC11 to 14 interrupt flag	1: WDT Enable	1: TPG0-13 interrupt flag	HALT mode 0: RUN mode 1: STOP mode	Inverted by execution of EXX instruction.	1: Drives pin in STOP mode.

3.2 Memory Map

(1) Internal ROM

The TMP91C642A integrates a 16K-byte ROM. The ROM is allocated to the address space from 0000H to 3FFFH. After reset, the CPU starts execution of the program from address 0000H.

Addresses 0010H to 007FH in the ROM are used as the interrupt entry area by the interrupt processing.

(2) Internal RAM

The TMP91C642A integrates a 320-byte RAM. The RAM is allocated to the address space from FE80H to FFBFH. The CPU can access part of the RAM (FF00H to FFBFH, 192-byte area) using direct addressing mode with short instruction codes.

Addresses FF10H to FF7FH in the RAM are used as the micro-DMA parameter area. (Note that when the DMA is not in use, the area can be freely used.)

(3) Internal I/O

The TMP91C642A uses 64-byte address space as an internal I/O area. The area is allocated to the address area from FFC0H to FFFFH. This I/O area can be accessed by the CPU using a short opcode in the "direct addressing mode".

Figure 3.2 shows the memory map and the CPU addressing mode access ranges.

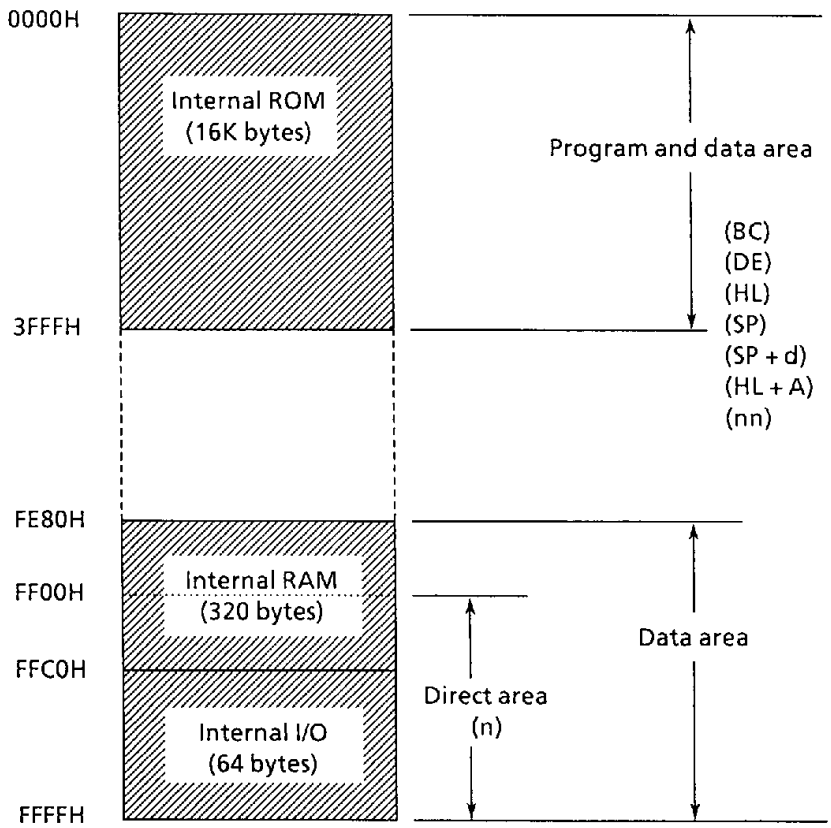


Figure 3.2 Memory Map

3.3 Interrupt Functions

The TMP91C642A supports general-interrupt processing mode used to respond to internal and external interrupt requests and micro DMA processing mode used for automatic data transfer by the CPU.

After a reset is cleared, all interrupt requests are set to general-purpose interrupt processing mode. By using the DMA enable register described later, interrupt requests can be set to micro DMA processing mode.

Figure 3.3. (1) shows the interrupt response flow.

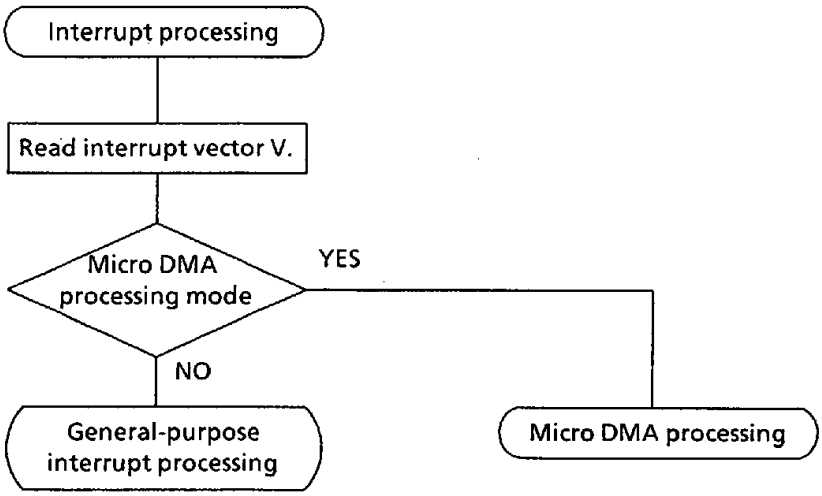


Figure 3.3 (1) Interrupt Response Flow

When an interrupt request is generated, the interrupt source notifies the CPU using the internal interrupt controller. The CPU starts the interrupt processing if the non-maskable or maskable interrupt request is enabled (interrupt enable flag (IFF in register F) = "1"). If the request is non-maskable and interrupt is disabled (IFF = "0"), the CPU ignores the request. (The CPU samples interrupt requests at the falling edge of the *CLK signal.)

Accepting the interrupt, to determine the interrupt source, the CPU reads the interrupt vector from the internal interrupt controller.

Then, the CPU checks whether the interrupt requests general-purpose or micro DMA interrupt processing and starts processing accordingly.

The CPU reads an interrupt vector during internal operation cycle, the bus cycle results in dummy cycle.

(Note) * With the TMP91C642A, CLK is always internally pulled up to 1.

3.3.1 General-purpose Interrupt Processing

Figure 3.3 (2) shows the flow of general-purpose interrupt processing.

The CPU first saves contents of the PC and register AF (contains the IFF indicating the interrupt status just before the interrupt generation), then resets interrupt enable flag IFF to "0" (interrupt disable mode). The CPU copies contents V of the interrupt vector to the PC and jumps to the interrupt processing program.

The overhead from accepting an interrupt to jumping to the interrupt processing program is 20 states.

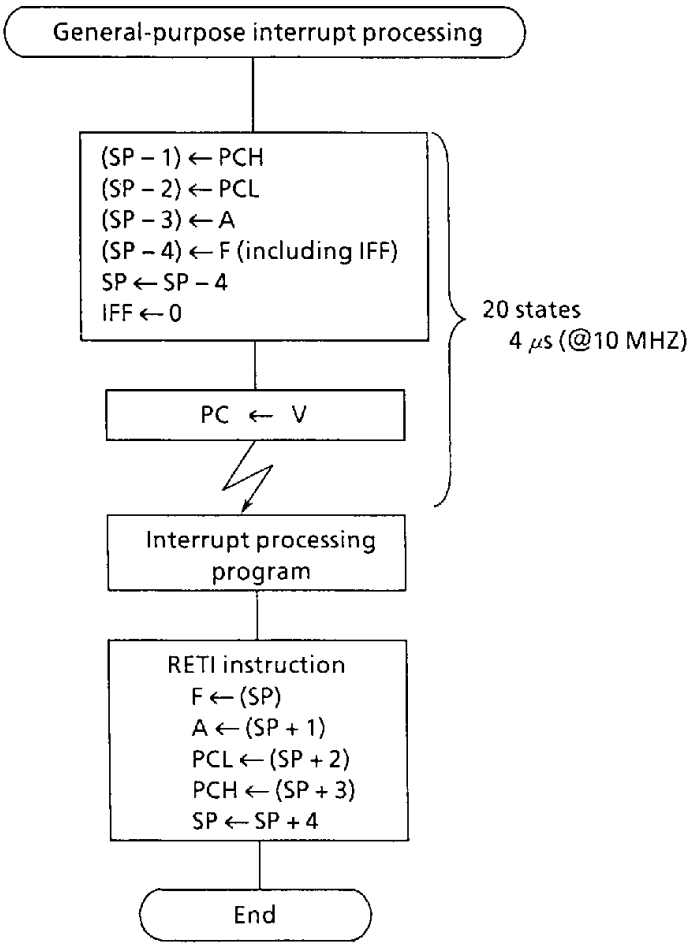


Figure 3.3 (2) General-Purpose Processing Flow

The interrupt processing program ends with the RETI instruction for both non-maskable and maskable interrupts.

Executing the RETI instruction restores the contents of the PC and register AF from the stack. (The status returns to that of the interrupt enable flag just before the interrupt generation.)

When the CPU reads the interrupt vector, the interrupt source acknowledges that the CPU accepts the interrupt and clears the interrupt request.

Non-maskable interrupts cannot be disabled by program. On the other hand, maskable interrupts can be enabled/disabled by program. Bit 5 in register F is the interrupt enable flag (IFF). The CPU can select interrupt enable / disable by setting IFF to "1" using the EI (enable interrupt) instruction; reset to "0" using the DI (disable interrupt). IFF is reset by a reset or acceptance of an interrupt including non-maskable interrupt.

Interrupts are enabled after the instruction subsequent to the EI instruction.

Table 3.3 (1) shows interrupt sources.

Table 3.3 (1) Interrupt Sources

Priority	Type	Interrupt source	Vector value /8	Vector value V	General-purpose interrupt processing start address	Micro DMA processing parameter start address
1	Non-	SWI instruction		10H	0010H	—
2	maskable	INTWD (watchdog timer)		20H	0020H	—
3		INT0 (External input 0)	05H	28H	0028H	FF28H
4		INTCAP (Capture interrupt)※1	06H	30H	0030H	FF30H
5		INTAD (A/D converter)※2	07H	38H	0038H	FF38H
6		INTSIO (Serial I / O)※3	08H	40H	0040H	※4
7		INTT0 (Timer 0)	09H	48H	0048H	FF48H
8	Maskable	INTT1 (Timer 1)	0AH	50H	0050H	FF50H
9		INTT2 (Timer 2)	0BH	58H	0058H	FF58H
10		INTT3 (Timer 3)	0CH	60H	0060H	FF60H
11		INTTB (Divider)	0DH	68H	0068H	FF68H
12		INT1 (External input 1)	0EH	70H	0070H	FF70H
13		INTVA (VASS) ※5	0FH	78H	0078H	FF78H
13		INT2 (External input 2) ※5	0FH	78H	0078H	FF78H

(Note) ※1) C-FG, D-FG, D-PG, P-CTL, EXT, VP (C-Sync) / TPFIFO
※2) INTAD cannot be used.
※3) SIO_1 / SIO_2
※4) INTSIO cannot use micro DMA processing.
※5) INTVA or INT2 is selected according to INT2 interrupt select register INTEH<INT2S>.

"Priority" in table 3.3 (1) shows the priority of interrupt sources to be acknowledged by the CPU when multiple interrupt requests are generated simultaneously.

For example, when interrupts with priorities 3 and 4 are generated simultaneously, the CPU accepts the interrupt with priority 3 first. After processing of the interrupt with priority 3 is ended by the RETI instruction, the interrupt with priority 4 is accepted. However, a lower priority interrupt can be acknowledged immediately by executing an EI instruction in a program that processes a higher priority interrupt.

The internal interrupt controller only determines priorities of interrupt sources to be acknowledged by the CPU when multiple interrupt requests are generated. It does not compare the priority of the currently-processed interrupt and that of the interrupt being requested.

To enable other interrupts during interrupt processing, set the interrupt enable flag of the interrupt source to be enabled and perform the EI instruction.

3.3.2 Micro DMA processing

Figure 3.3 (3) shows the flow of the micro DMA processing. The CPU loads the parameters (transfer source, destination addresses and transfer mode) necessary for data transfer between memories from the address modified by the interrupt vector, transfers data between memories according to the parameters, then saves the updated parameters back. The CPU decrements the number of transfers. If the value is other than 0, the micro DMA processing ends. If the value is 0, the general-purpose processing is performed.

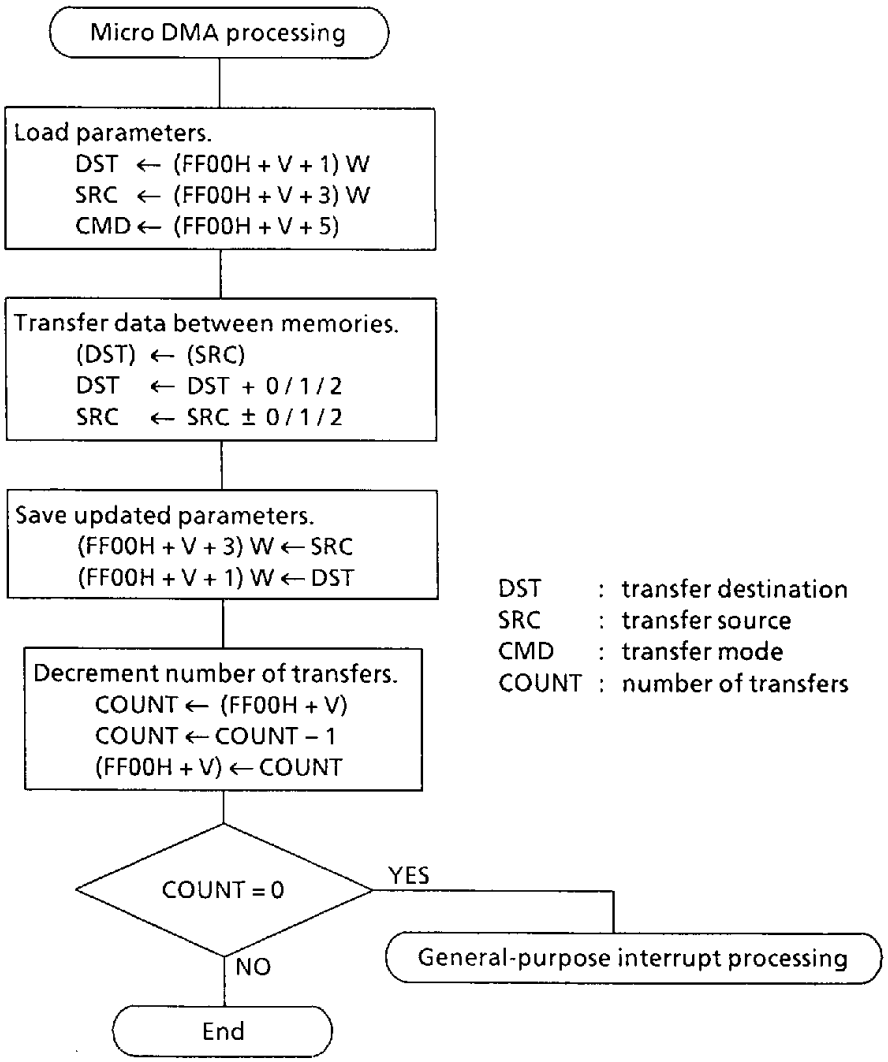


Figure 3.3 (3) Micro DMA Processing Flow

Most of the interrupt processing consists of simple data transfer. The previous processing depends on software. On the other hand, the micro DMA processing only uses hardware to improve interrupt processing speed. The CPU registers are not influenced by the micro DMA processing.

Figure 3.3 (4) shows the functions of parameters used by the micro DMA processing.

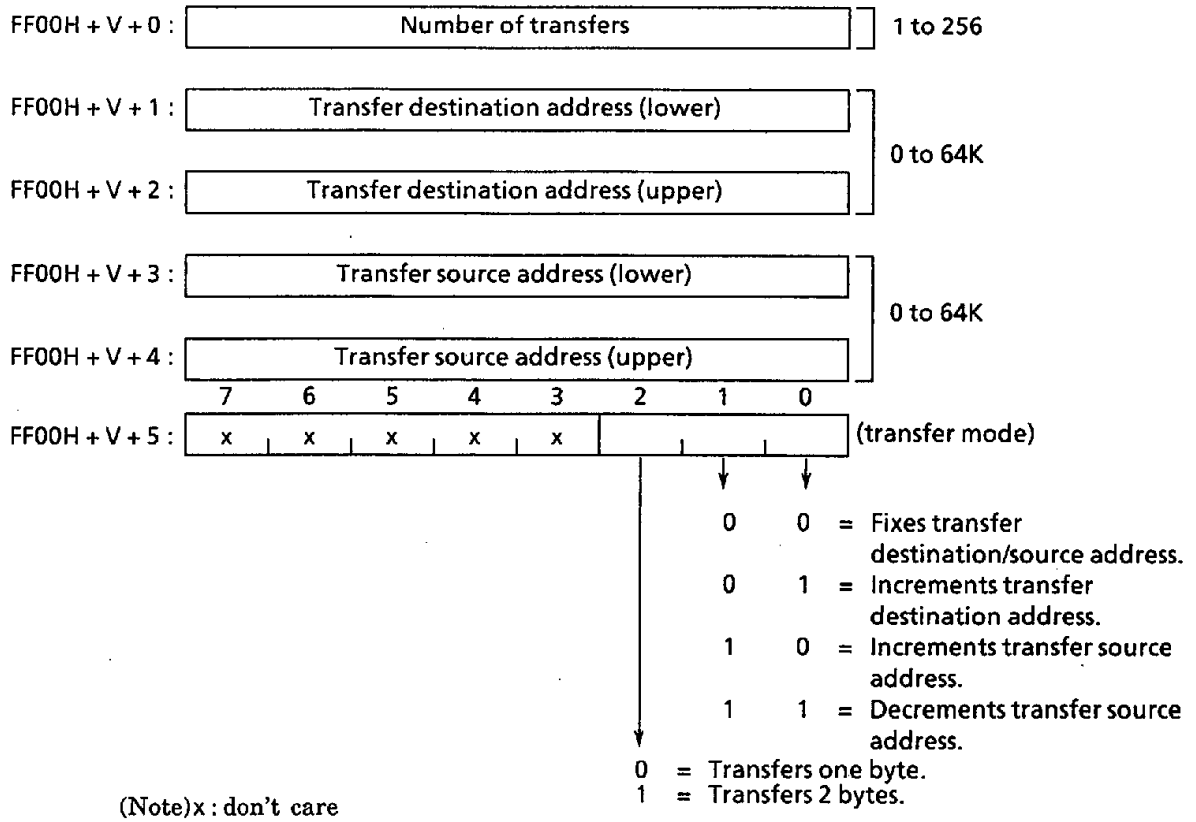


Figure 3.3 (4) Micro DMA Parameters

The micro DMA parameters are allocated to the internal RAM. (See Table 3.3 (1), Interrupt Sources.) Each micro DMA processing parameter start address is determined by "FF00H + interrupt vector value". A parameter uses 6 bytes starting from the start address. When the micro DMA processing mode is not in use, the area can be freely used as user memory.

A parameter consists of the number of transfers, transfer source address, and transfer mode. Specify the number of data transfers to be accepted by the micro DMA processing as the number of transfers. The micro DMA processing transfers 1 or 2 bytes of data at a time. When the value of the number of transfers is 00H, the number of transfers is 256. Specify the transfer destination and source addresses in two data bytes. The micro DMA processing can use the address area from 0000H to FFFFH.

Specify in bits 0 and 1 transfer mode for updating the transfer destination or source address. Specify in bit 2 the transfer data length, as 1 or 2 bytes.

Table 3.3 (2) shows transfer modes and transfer destination and source address increment / decrement.

Table 3.3 (2) Micro DMA Address Increment/Decrement

Transfer mode	Function	Transfer destination address	Transfer source address
000	1-byte transfer, Fixes transfer destination and source addresses.	0	0
001	1-byte transfer, Increments transfer destination address.	+1	0
010	1-byte transfer, Increments transfer source address.	0	+1
011	1-byte transfer, Decrements transfer source address.	0	−1
100	2-byte transfer, Fixes transfer destination and source addresses.	0	0
101	2-byte transfer, Increments transfer destination address.	+2	0
110	2-byte transfer, Increments transfer source address.	0	+2
111	2-byte transfer, Decrements transfer source address.	0	−2

In 2-byte transfer mode, data are transferred as follows:

(transfer destination address) ← (transfer source address)
(transfer destination address + 1) ← (transfer source address + 1)

In a mode where the transfer source address is decremented, data are transferred as above, but the address is updated as shown in Table 3.3.(2).

The micro DMA updates addresses taking I/O transfer into consideration. Therefore, either transfer destination or transfer source address is fixed.

The execution time (the number of transfers is other than 0 due to decrement) of the micro DMA processing is 46 states (9.2 μs at 10 MHz oscillation frequency) regardless of 1-byte or 2-byte mode.

Figure 3.3 (5) shows the flow of overall interrupt processing.

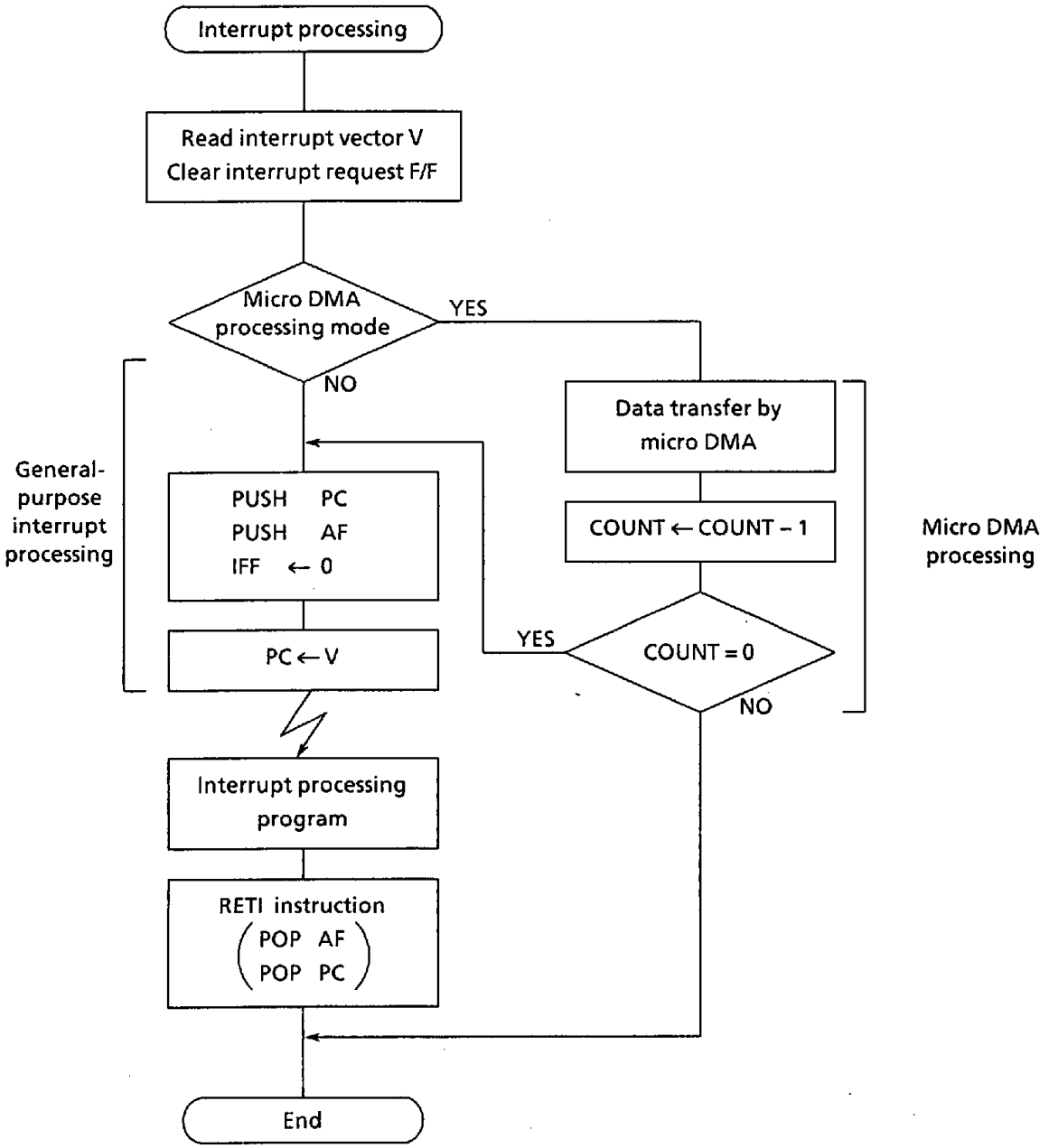


Figure 3.3 (5) Interrupt Processing Flow

3.3.3 Interrupt Controller

Figure 3.3 (7) outlines the interrupt circuit. The left half of the figure shows the interrupt controller. The right half shows the CPU interrupt request signal circuit and halt release circuit (for halt, see 3.4 Standby Function).

The interrupt controller has an interrupt flip / flop, interrupt enable register, and micro DMA enable flag for each channel (total of 12 channels). The interrupt request flip / flop is used to latch an interrupt request. The interrupt request flip / flop is reset to "0" at reset, when the CPU accepts an interrupt and reads the vector, or when the instruction used to clear the interrupt request of the channel (writes vector value / 8) to address FFEDH in memory) is performed. For example, when executing the following:

LD (FFEDH) , 30H / 8

the interrupt request flip / flop of channel INTCAP whose vector value is 30H is reset to "0". (To clear the flip / flop, even if the interrupt request flag is assigned to FFECH, write to FFEDH.)

The status of the interrupt flip / flop can be determined by reading address FFECH or FFEDH in memory. "0" indicates no interrupt request; "1" indicates an interrupt request. Figure 3.3 (6) shows the bit configuration of the interrupt request flip / flop.

Interrupt Request Flags (L)

IRFL (FFECH)

	7	6	5	4	3	2	1	0
bit Symbol		IRF0	IRFCAP	IRFAD			SIO1F	SIO0F
Read/Write		R					R	R
Value after reset		0	0	0			0	0
Function		Interrupt Request Flag 1: Interrupt being requested					1: SIO1 Request	1: SIO0 Request

Serial channel 0, 1 request flag
*INTAD request flag
INTCAP request flag
INT0 request flag

0	no interrupt
1	interrupt

Interrupt Request Flags (H)

IRFH (FFEDH)

Prohibit read-modify-write.

	7	6	5	4	3	2	1	0
bit Symbol	IRFSIO	IRFT0	IRFT1	IRFT2	IRFT3	IRFTB	IRF1	IRF2VA
Read/Write	R (Only IRF Clear code can be used to write)							
Value after reset	0	0	0	0	0	0	0	0
Function	1: Interrupt being requested (IRF is cleared to "0" by writting IRF clear code.)							

INTVA / INT2 request flag
INT1 request flag
INTTB request flag
INTT3 request flag
INTT2 request flag
INTT1 request flag
INTT0 request flag
INTSIO request flag

0	no interrupt
1	interrupt

(Note) Writing vector value / 8 to address FFEDH in memory clears the specified interrupt request flip/flop.

* INTAD cannot be used.

Figure 3.3 (6) Interrupt Request Flip / Flop

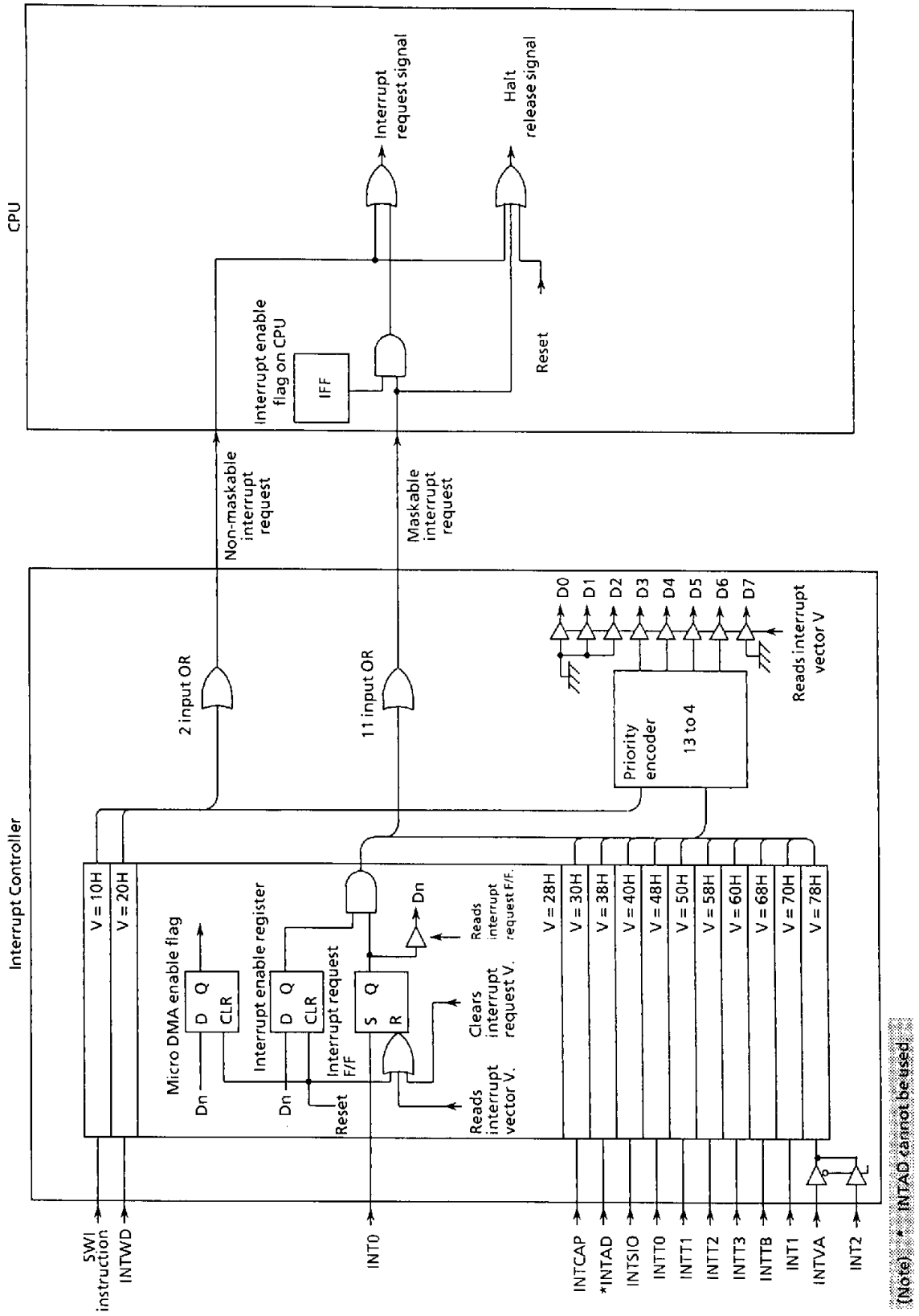


Figure 3.3 (7) Interrupt Circuit

The interrupt enable register for each interrupt request channel is assigned to address FFE9H or FFEAH in memory. Setting the flag to "1" enables an interrupt to the channel. Reset resets the flag to "0".

Clear an interrupt request flag when interrupts are disabled.

The micro DMA enable flag for each interrupt request channel is assigned to address FFEAH or FFEBH in memory. Setting the flag to "1" sets the mode to micro DMA processing mode for interrupts to the channel. Reset resets the flag to "0" (that is general-purpose interrupt processing mode).

Figure 3.3 (8) shows the bit configuration of interrupt enable registers and micro DMA enable flags.

INT2, which is an interrupt by external input 2, and INTVA, which is an interrupt by the VASS flag, share the same interrupt request channel. After reset, INTVA is input to the interrupt controller. When using INT2, set INTVA / INT2 select bit (<INT2S> : bit 3 at FFEAH in memory) to "1".

External interrupt functions are as listed below :

Interrupt	Shared pin	Mode	Setting
INT0	P35	level	P3CR<P35M> = 0
		rising edge	P3CR<P35M> = 1
INT1	P36	rising edge	———
INT2	P46	rising edge	———

For the pulse width of the external interrupt function, see 4.7, Interrupt Operation.

Note that the following 4 items are exceptional circuits.

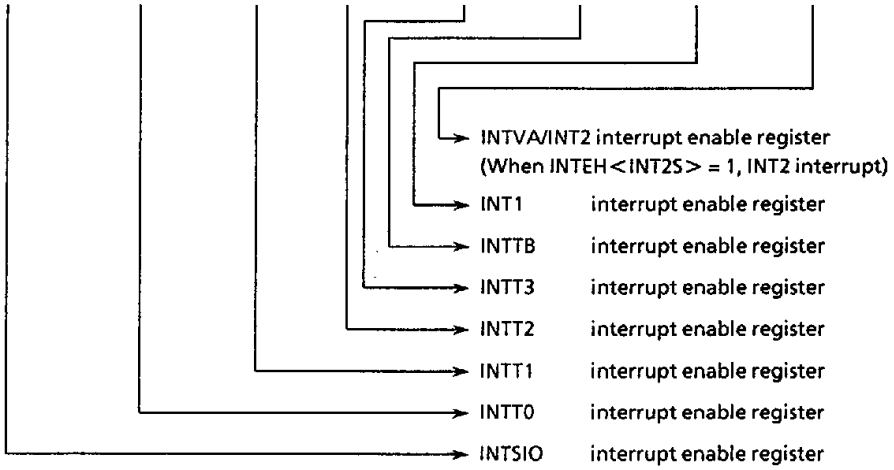
INT0 level mode	The interrupt request flip / flop function is cancelled because an interrupt is not edge-type. A peripheral interrupt request passes through the flip / flop S input and becomes Q output. When the mode is changed from edge to level, the previous interrupt request flag is automatically cleared.
	After changing INT0 from "0" to "1", when the CPU enters the interrupt response sequence, INT0 must be maintained at "1" until the second bus cycle of the interrupt response sequence is complete. To use INT0 level mode for releasing HALT, INT0 must be changed from "0" to "1" and be maintained at "1" until halt is released. (Make sure that it is not set to "0" due to noise.)
	When the mode is changed from level to edge, an interrupt request flag accepted in level mode is not cleared. Clear the interrupt request flag in the following sequence.
	DI
	LD (0FFC7H), 20H ; Changes from level to edge.
	LD (0FFEDH), 05H ; Clears interrupt request flag.
	EI

INTCAP	The interrupt request flip / flop is cleared depending on the source: source from the capture circuit or source from TPG. When an interrupt is generated by the capture circuit, the interrupt request flip/flop is cleared by reading all the data from capture FIFO status CAPFST. The flip / flop can also be cleared by writing "1" to SVCFREG<CARFS>. When an interrupt request is generated from TPG, the interrupt request flip/flop is cleared by writing data to FIFO of TPG.
INTSIO	The interrupt request flip / flop is cleared by reset or by reading data from the receive data buffer of the serial channel. It cannot be cleared by instructions. Reading IRFL clears the interrupt request flag (IRFSIO) and the channel information (SIO1F, SIO0F).
INTVA / INT2	When an interrupt source is cleared (INTAD↔INTT2), the previous interrupt request flag is automatically cleared.

Interrupt Enable Registers (L)

INTEL (FFE9H)

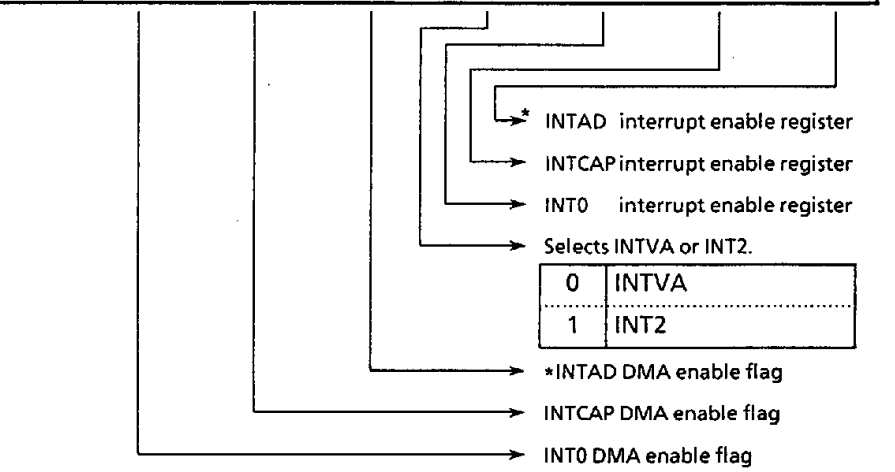
	7	6	5	4	3	2	1	0
bit Symbol	ENISIO	ENITO	ENIT1	ENIT2	ENIT3	ENITB	ENI1	ENI2VA
Read/Write	R/W							
Value after reset	0	0	0	0	0	0	0	0
Function	1 : Enable					0 : Disable		



Interrupt Enable Registers (H) and Micro DMA Enable Flags (L)

INTEH [DMAEL] (FFEAH)

	7	6	5	4	3	2	1	0
bit Symbol	(Note) Always write "0".	DE0	DECAP	DEAD	INT2S	ENI0	ENICAP	ENIAD
Read/Write		R/W			R/W			
Value after reset		0	0	0	0	0	0	0
Function		1: Enable 0: Disable			0 : INTVA 1 : INT2	1: Enable 0: Disable		



0	INTVA
1	INT2

(NOTE) * : INTAD cannot be used.

Figure 3.3 (8) - 1 Interrupt / Micro DMA Enable Flags

Micro DMA Enable Flags (H)

DMAEH (FFEBH)

	7	6	5	4	3	2	1	0
bit Symbol	(Note) Always write "0".	DET0	DET1	DET2	DET3	DETB	DE1	DE2VA
Read/Write		R/W						
Value after reset		0	0	0	0	0	0	0
Function		1: Enable				0: Disable		

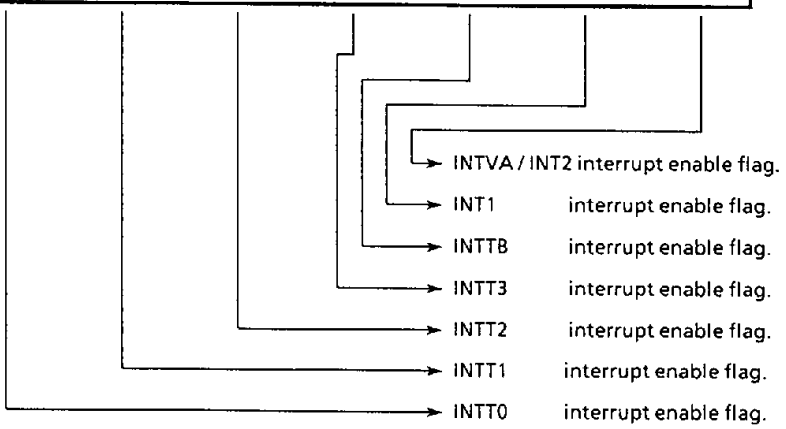


Figure 3.3 (8) - 2 Interrupt / Micro DMA Enable Flags

3.4 Standby Function

Executing the HALT instruction sets the TMP91C642A to RUN or STOP mode according to the halt mode setting register (bit 2 at address FFE6H in memory). Features of these modes are as follows:

(1) RUN : Only suspends the CPU. Power consumption remains the same.

(2) STOP : Suspends all internal circuits including the internal oscillator. Power consumption is greatly reduced.

The above halt states are released by an interrupt request or reset*. Table 3.4 (2) lists halt release sources. If interrupts are enabled (EI) by the CPU for non-maskable or maskable interrupts, an interrupt is accepted and interrupt processing starts. If interrupts are disabled (DI) by the CPU for maskable interrupts, execution resumes from the instruction subsequent to the HALT instruction; the interrupt request flag remains "1".

If interrupts are disabled (DI) and an interrupt request is generated before execution of the HALT instruction and latched by the interrupt request flag, HALT is released immediately after execution of the HALT instruction (does not enter HALT state.) Therefore, to enter HALT state, clear the interrupt request flag or disable the interrupt enable flag (IFF) before executing the HALT instruction.

Example) Enters stop mode when interrupts are disabled (DI) and releases halt by INT0.
(Internal I/O just use timer 0.)

```
DI                          ;  Disables interrupts.
SET     2,(INTEH)           ;  Enables INT0 for releasing halt.
RES     6,(INTEL)           ;  Disables timer 0 interrupts.
LD      (WDMOD), 04H        ;  STOP mode
HALT                        ;  HALT

Program to be executed
after releasing HALT.
```

* When halt is released by reset, the states (including those of the internal RAM) before halt state was entered can be maintained. However, if the HALT instruction is executed within the internal RAM, the contents of the RAM may not be maintained. In this case, we recommend releasing the halt state using INT0.

Watchdog Timer Mode Register

WDMOD (FFE6H)

	7	6	5	4	3	2	1	0
bit Symbol		FTBC2	FTBC1	WDTE	FTPG	HALT	EXF	DRVE
Read/Write		R/W	R/W	R/W	R/W	R/W	R	R/W
Value after reset		0	0	1	0	0	Undefined	0
Function		1: TBC15 to 18 interrupt flag	1: TBC11 to 14 interrupt flag	1: WDT Enable	1: TPG0-13 interrupt flag	HALT mode 0: RUN mode 1: STOP mode	Inverted by execution of EXX instruction	1: Drives pin in STOP mode.

See 3.6, Time Base Counter and 3.7, Watchdog Timer.

I/O pin control in STOP mode

0	I/O off
1	State before HALT

See 3.4.2, STOP mode.

Exchange flag
See 3.1.2, Registers.

HALT mode setting

0	RUN mode
1	STOP mode

Figure 3.4 (1) HALT Mode Setting Register

3.4.1 RUN Mode

Figure 3.4 (2) shows the timing for releasing halt state by an interrupt in RUN mode.

In RUN mode, the internal MCU system clock does not stop after the HALT instruction is executed. The CPU stops only execution of instructions. Therefore, the CPU repeats dummy cycles until the halt state is released. Interrupt requests are sampled at the falling edge of the CLK* signal in halt state.

(Note) The watchdog timer is also in operation.

* With the TMP91C642A, CLK is always internally pulled up to "1".

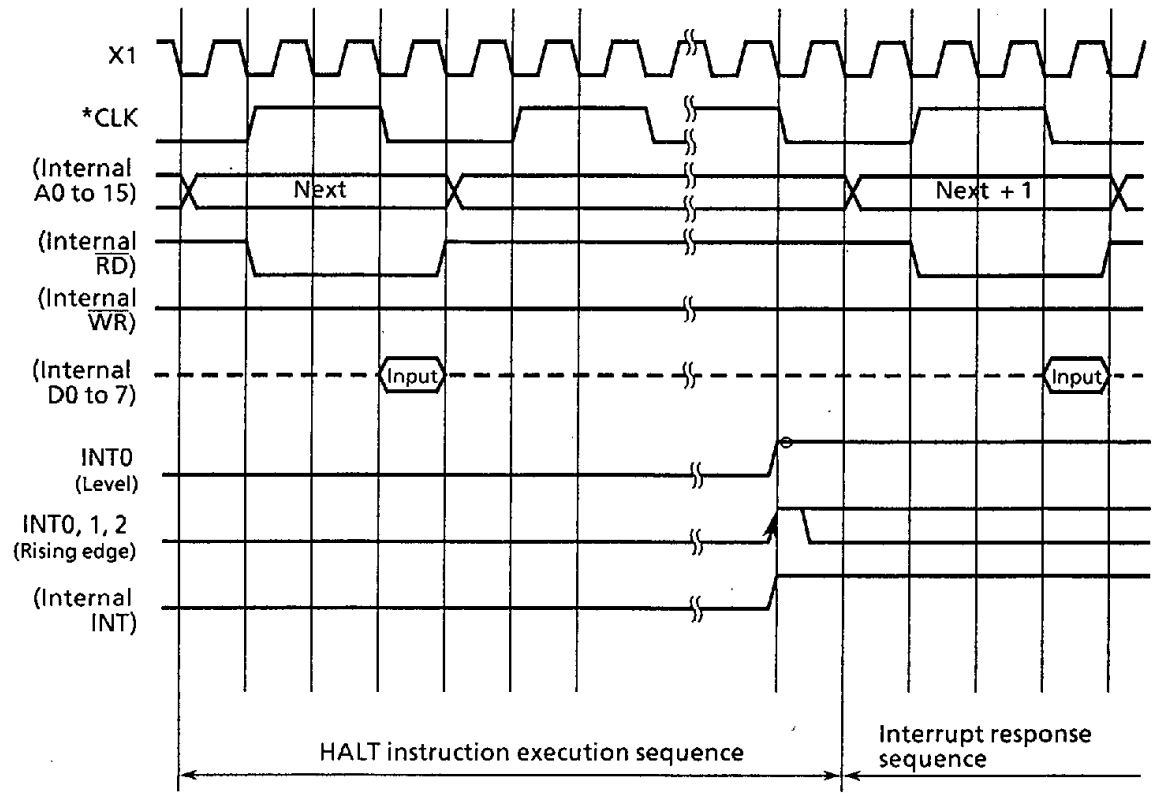


Figure 3.4 (2) Timing for Releasing Halt State by Interrupt in RUN Mode

3.4.2 STOP Mode

Figure 3.4 (3) shows the timing for releasing halt state by an interrupt in STOP mode.

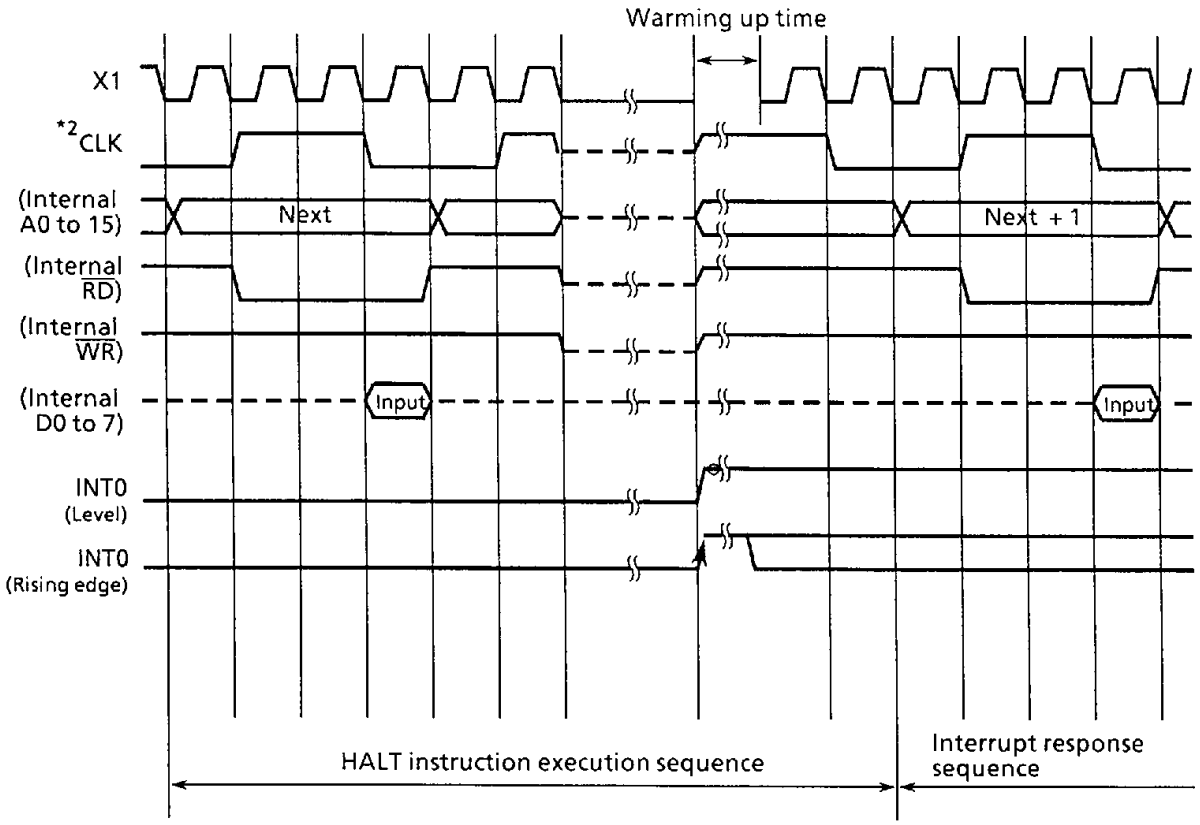
In STOP mode, all internal circuits including the internal oscillator.

In STOP mode, almost all pins are disconnected from the MCU and set to high impedance. Table 3.4 (1) lists the pin states in STOP mode.

If the WDMOD<DRVE> (drive enable: bit 0 at FFE6H in memory) in the internal I/O register is set to "1", pin functions remain unchanged. The register is reset to "0" by reset.

When the CPU accepts an interrupt request, the internal oscillator restarts. To obtain stabilized oscillation, the system clock starts outputting after the time set by the warming up counter (*1).

(Note) *1 Warming up takes a maximum of 2^{20}/fc seconds.



(Note) *2 With the TMP91C642A, CLK is always internally pulled up to "1".

Figure 3.4 (3) Timing Chart for Releasing HALT State by Interrupt in STOP Mode

Inputting a 0-level voltage to the CPU $\overline{\text{RESET}}$ pin also restarts the internal oscillator. However, for quick response at power on, the warming up counter does not operate. As a result, the unstabilized clock immediately after restart of the internal oscillator may cause incorrect operation. The voltage input at 0-level must be maintained for sufficient time when releasing halt state by reset in STOP mode.

To release STOP mode in INT0 level mode, INT0 must be maintained at "1" until the second bus cycle of the interrupt response sequence is complete.

Table 3.4 (1) Pin States in STOP Mode

Pin name	Input/Output	State	
		<DRVE> = 0	<DRVE> = 1
P0	Input mode	——	——
	Output mode	Output	Output
P1	Input mode	——	Input
	Output mode	——	Output
P2	Input mode	——	Input
	Output mode	——	Output
P30 to P32	Input mode	——	Input
	Output mode	——	Output
P33, P34	Input mode	——	Input
	Output mode	——	Output
P35 (INT0)	Input pin	Input	Input
P36 (INT1)	Input pin	——	Input
P37	Output pin	——	Output
P4	Input mode	——	Input
	Output mode	——	Output
P5	Input pin	——	Input
P60 to P63	Input mode	——	Input
	Output mode	——	Output
P64 to P67	Input pin	——	Input
PW0, PW1	Output pin	Output	Output
CLK	Output pin	* ——	"1"
$\overline{\text{RESET}}$	Input pin	Input	Input
X1	Input pin	——	——
X2	Output pin	"1"	"1"

—— : Input is invalid for input mode or input pin; high impedance for output mode or output pin.

Input : Input enabled.

Input : Input gate is in operation. To prevent input pin from floating, fix input voltage to "0" or "1".

Output : Output state.

(Note)* With the TMP91C642A, CLK is always internally pulled up to "1".

Table 3.4 (2) I/O Operations in Halt State and Halt Release

Halt mode			RUN	STOP
WDMOD<HALT>			0	1
Operation block	CPU		Halt	
	I/Oport		※ Maintains state	See Table 3.4 (1)
	Time vase counter		Operation	Halt
	Watchdog timer			
	VISS / VASS detection circuit			
	C-Sync input processing circuit			
	Capture circuit			
	Timing pulse generator			
	PWM circuit			
	8-bit timer			
	Serial inter-face			
	A/D converter			
	Interrupt controller			
Halt release source	Interrupt	INTWD	○	—
		INT0	○	○
		INTCAP	○	—
		*INTAD	○	—
		INTSIO	○	—
		INTT0	○	—
		INTT1	○	—
		INTT2	○	—
		INTT3	○	—
		INTTB	○	—
		INT1	○	—
		INTVA (VASS)	○	—
		INT2	○	—
	Reset		○	○

(Note)* : INTAD cannot be used.

○ : Can be used for releasing halt state.

— : Cannot be used for releasing halt state.

※ .... Maintains state at execution of halt instruction.

3.5 Function of Ports

The TMP91C642A supports a total of 54-pin I/O ports. Port pins function not only as general-purpose I/O ports but also as I/O ports for internal CPU or internal I/O. Table 3.5 shows port pin functions.

Table 3.5 Function of Ports

Port name	Pin name	Number of pins	Input / output	Unit	State after reset	Pin name for internal function
Port 0	P00 to P07	8	I/O	Byte	Input	TPG0-0 to TPG0-7
Port 1	P10 to P13	4	I/O	Bit	Input	TPG0-8 / 1-8 to TPG0-11 / 1-11
Port 2	P20 to P27	8	I/O	Bit	Input	TPG1-0 to TPG1-7
Port 3	P30 to P32	3	I/O	Bit	Input	—
	P33	1	I/O	Bit	Input	C – Sync
	P34	1	I/O	Bit	Input	EXT
	P35	1	Input	—	Input	INT0
	P36	1	Input	—	Input	INT1
	P37	1	Output	—	Output	PWM8 / TO1
Port 4	P40	1	I/O	Bit	Input	SCLK0
	P41	1	I/O	Bit	Input	TxD0
	P42	1	I/O	Bit	Input	RxD0
	P43	1	I/O	Bit	Input	SCLK1
	P44	1	I/O	Bit	Input	TxD1
	P45	1	I/O	Bit	Input	RxD1
	P46	1	I/O	Bit	Input	INT2 / TI0
	P47	1	I/O	Bit	Input	TI1
Port 5	P50 to P57	8	Input	—	Input	AN00 to AN07
Port 6	P60 to P63	4	I/O	Bit	Input	AN10 to AN13
	P64 to P67	4	Input	—	Input	CAP0 to CAP3

Reset sets port pins to general-purpose I/O ports. Port pins which can be programmed as input or output are set to input ports. To use port pins for internal functions, make settings by program.

3.5.1 Port 0 (P00 to P07)

Port 0 is an 8-bit general-purpose I/O port P0 (address FFC0H in memory) to which I/O can be specified in units of bytes. To specify I/O, use control register P0CR<P0C> (bit 0 at address FFC1H in memory). Output to P00 can also be controlled by signals (TPG0-15) from the timing pulse generator and control register P0CR<P0S> (bit 1 at address FFC1H in memory).

Reset resets all bits in the control register and the output latch register to "0" and to input mode.

In addition to its general-purpose I/O port function, port 0 (TPG0-0 to TPG0-7) is used for output by the timing pulse generator (TPG).

To use port 0 as a general-purpose I/O port, write "0" to the bit which is also used as a port in TPG output data register TPO0DAR0. To use port 0 for TPG output, write "0" to the port 0 data register P0.

Do not use the bit modify instruction with the port 0 register.

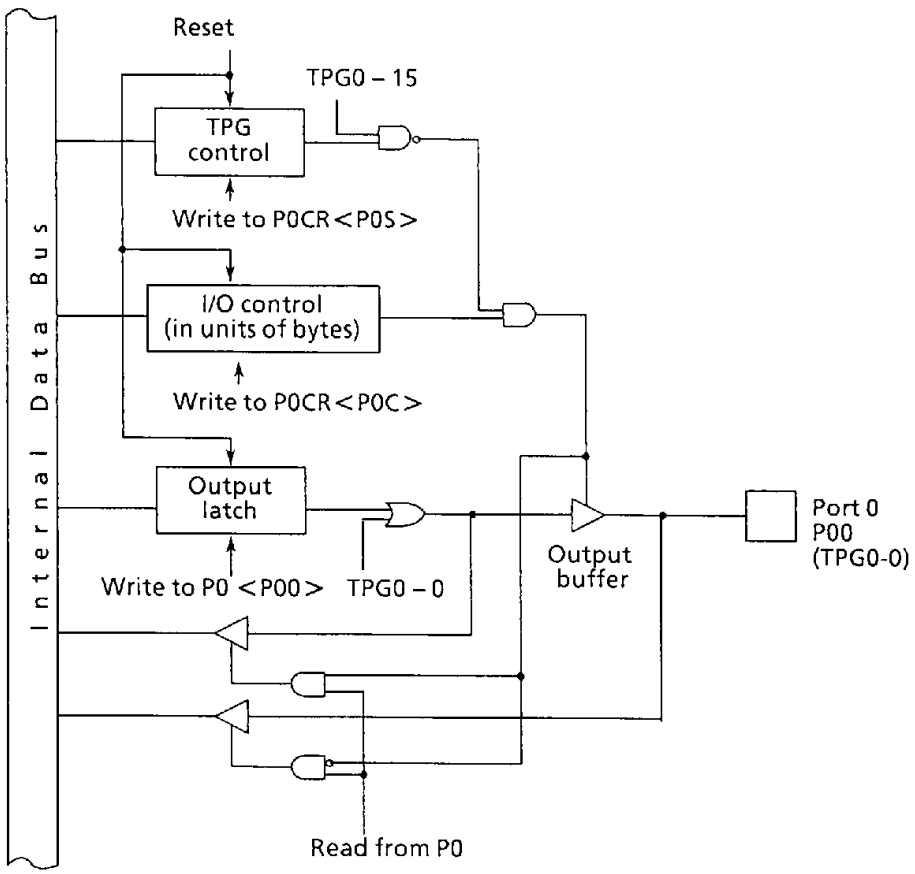
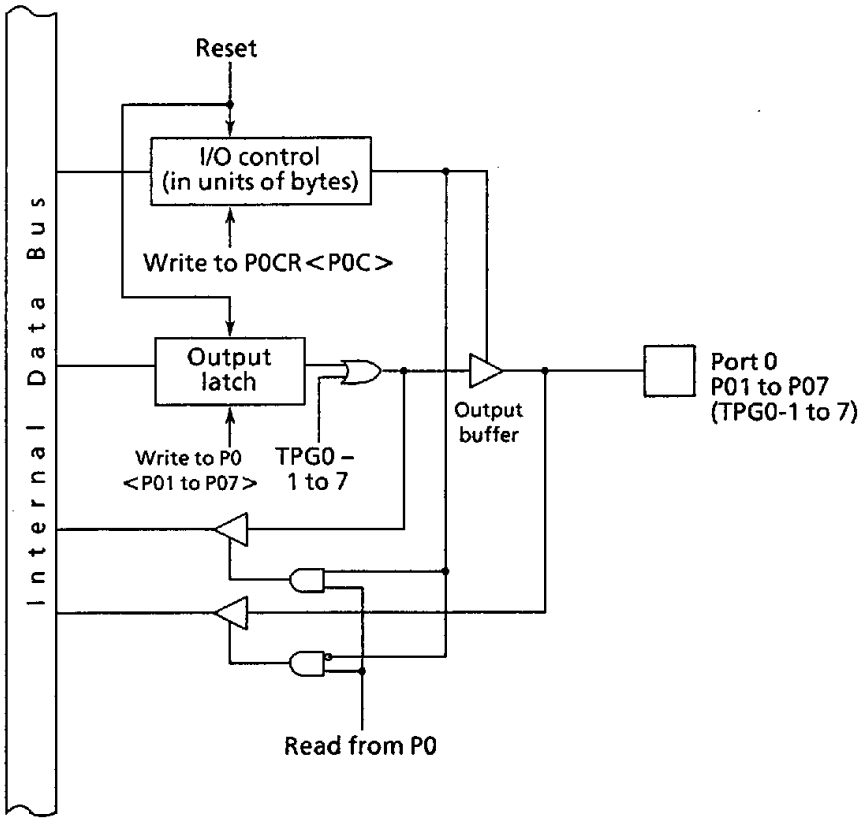


Figure 3.5 (1)-1 Port 0 (P00)



(Note) P04 to P07 outputs are open drain.

Figure 3.5 (1)-2 Port 0 (P01 to P07)

Port 0 Register

P0 (FFC0H)

Prohibit read-modify-write.

	7	6	5	4	3	2	1	0
bit Symbol	P07	P06	P05	P04	P03	P02	P01	P00
Read/Write	R/W							
Value after reset	Input mode							
Function	Also used for TPG output (TPG0-0 to TPG0-7). / 3-state output only for P00.							

Port 0 Control Register

P0CR (FFC1H)

Prohibit read-modify-write.

	7	6	5	4	3	2	1	0
bit Symbol						P2S	P0S	P0C
Read/Write						W	W	W
Value after reset						0	0	0
Function						Output of P20 3-state (TPG1-15 control) 0: Disable 1: Enable	Output of P00 3-state (TPG0-15 control) 0: Disable 1: Enable	P0 control 0: In 1: Out

See 3.5.3, Port 2.

Sets port 0 input/output.

0	Input
1	Output

Controls output to P00 by TPG0-15.

0	Disable
1	Enable

P00 states according to <P0C> and <P0S> of Port 0 control register and TPG0-15

<P0C>	<P0S>	TPG0 – 15	P00 state
0	–	–	Input
1	0	0	Output
	0	1	
	1	0	
	1	1	High impedance

※ (Note)
When P0CR<P0C> is "0", P00 is set to input mode regardless of the value of <P0S> or TPG0-15.
When both P0CR<P0C> and <P0S> are set to "1" and TPG0-15 is set to "1", P00 is set to high impedance regardless of the value of P0 <P00>.

Figure 3.5 (2) Port 0 Related Registers

3.5.2 Port 1 (P10 to P13)

Port 1 is a 4-bit general-purpose I/O port (address FFC2H in memory) to which I/O can be specified in units of bits. To specify I/O, use control register P1CR<P10C, P11C, P12C, and P13C> (bits 0 to 3 at address FFC3H in memory). Output to P10 can also be controlled by signals (TPG0-14 / TPG1-14) from the timing pulse generator.

Reset resets all bits in the control register and the output latch register to "0" and to input mode.

In addition to its general-purpose I/O port function, port 1 is also used for output (TPG0-8 / TPG1-8 / TPG0-11 / TPG1-11) by the timing pulse generator (TPG).

To use port 1 as a general-purpose I/O port, write "0" to the bit which is also used as a port in TPG output data registers TPO0DAR1 <TPO08 to 0B> and TPO1DAR1 <TPO18 to 1B>. To use port 1 for TPG output, write "0" to the port 1 data register. When using the TPG output function, specify I/O in units of 4 bits.

Do not use the bit modify instruction with the port 1 register.

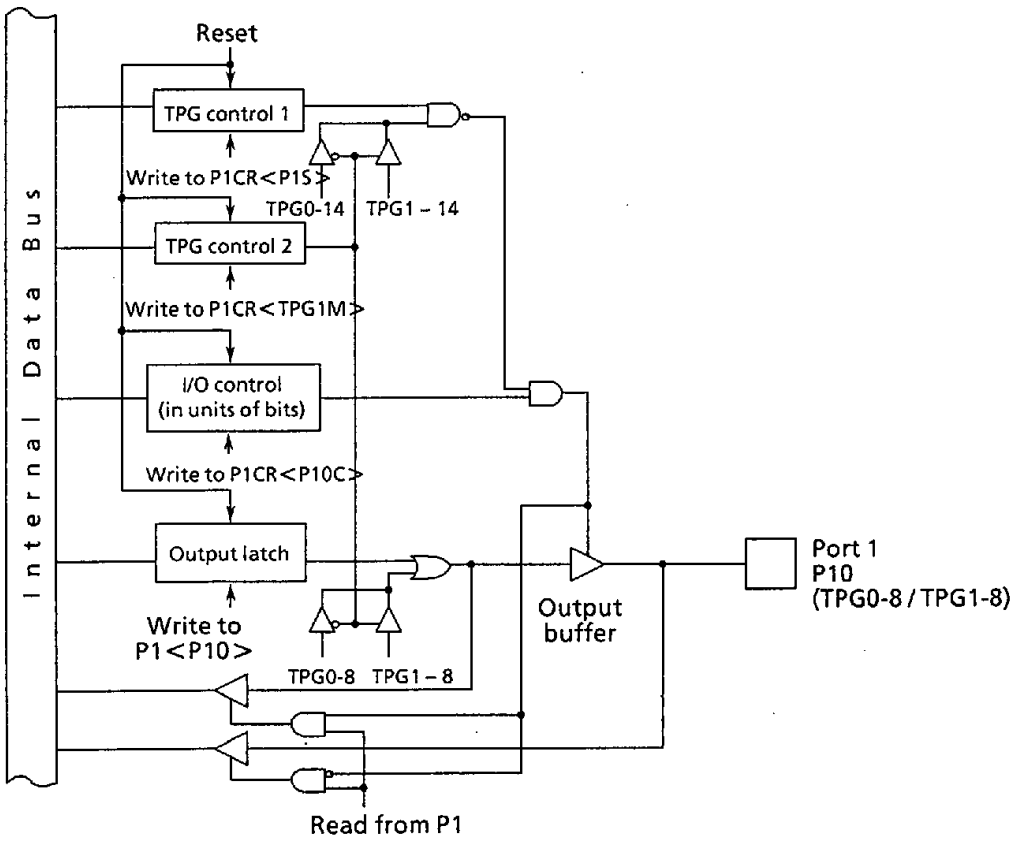


Figure 3.5 (3) - 1 Port 1 (P10)

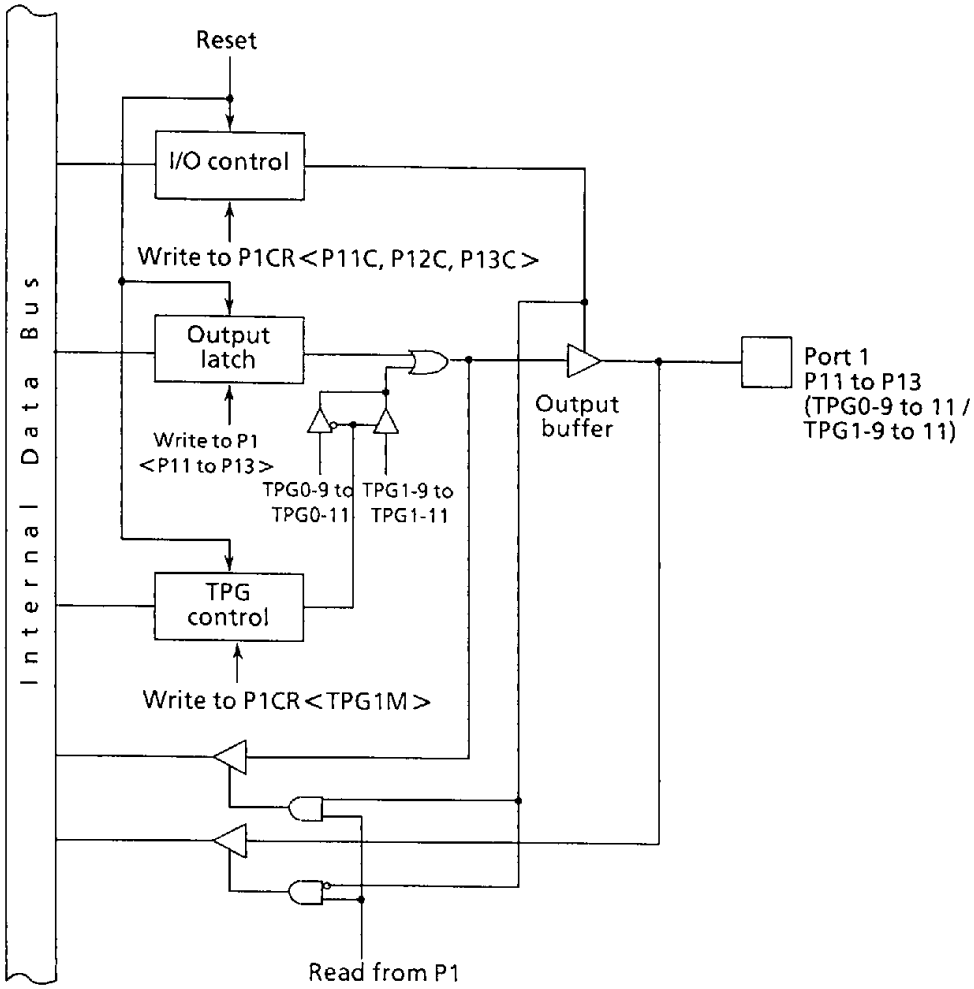


Figure 3.5 (3)-2 Port 1 (P11 to P13)

Port 1 Register

P1 (FFC2H)

Prohibit read-modify-write.

	7	6	5	4	3	2	1	0
bit Symbol					P13	P12	P11	P10
Read/Write					R/W			
Value after reset					Input mode			
Function					Also used for TPG output (TPG0-8 to 0-11 / TPG1-8 to 1-11). / 3-state output only for P10.			

Port 1 Control Register

P1CR (FFC3H)

Prohibit read-modify-write.

	7	6	5	4	3	2	1	0
bit Symbol		(Note) Always write "0".	TPG1M	P1S	P13C	P12C	P11C	P10C
Read/Write			W	W	W			
Value after reset			0	0	0			
Function			TPG output control 0 : TPG0 1 : TPG1	Output of P10 3-state (TPG 0-14 / TPG1-14 control) 0 : Disable 1 : Enable	0 : In 1 : Out (Specifies I/O in units of bits)			

Sets port 1 input / output.

0	Input
1	Output

Controls output to P10 by TPG0-14 / TPG1-14.

0	Disable
1	Enable

Sets port 1 to TPG0 / TPG1.

0	TPG0
1	TPG1

P10 states according to <P10C> and <P1S> of Port 1 control register and TPG0- 14 / TPG1-14

<P10C>	<P1S>	TPG0 – 14/TPG1 – 14	P10 state
0	–	–	Input
1	0	0	Output
	0	1	
	1	0	
	1	1	High impedance

※ (Note)
When P1CR<P10C> is "0", P10 is set to input mode regardless of the value of <P1S> or TPG0-14/TPG1-14.
When both P1CR<P10C> and <P1S> are set to "1" and TPG0-14/TPG1-14 is set to "1", P10 is set to high impedance regardless of the value of P1<P10>.

Figure 3.5 (4) Port 1 Related Registers

3.5.3 Port 2 (P20 to P27)

Port 2 is a 4-bit general-purpose I/O port (address FFC4H in memory) to which I/O can be specified in units of bits. To specify I/O, use control register P2CR (address FFC5H in memory). Output to P20 can also be controlled by signals (TPG1-15) from the timing pulse generator.

Reset resets all bits in the control register and the output latch register to "0" and to input mode.

In addition to its general-purpose I/O port function, port 2 is also used for output (TPG1-0 to TPG1-7) by the timing pulse generator (TPG).

To use port 2 as a general-purpose I/O port, write "0" to the bit which is also used as a port in TPG output data register TPO1DAR0. To use port 2 for TPG output, write "0" to the port 2 data register P2. When using the TPG output function, specify I/O in units of bytes.

Do not use the bit modify instruction with the port 2 register.

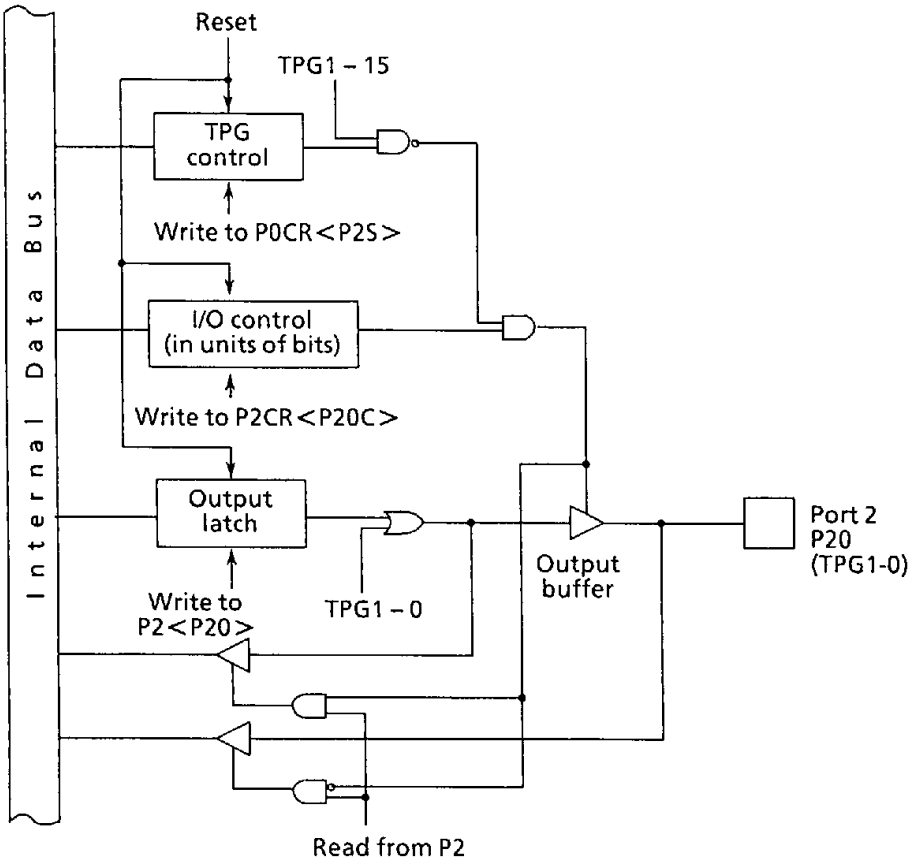
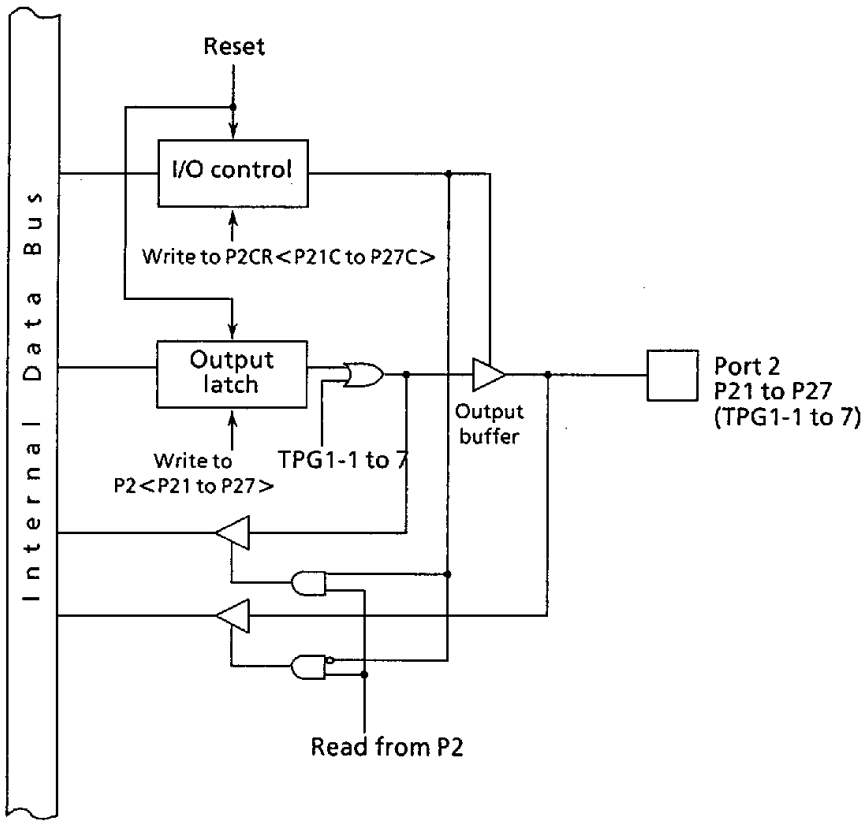


Figure 3.5 (5)-1 Port 2 (P20)



(Note) P21 to P27 outputs are open drain.

Figure 3.5 (5)-2 Port 2 (P21 to P27)

Port 2 Register

P2 (FFC4H)

Prohibit read-modify-write.

	7	6	5	4	3	2	1	0
bit Symbol	P27	P26	P25	P24	P23	P22	P21	P20
Read/Write	R/W							
Value after reset	Input mode							
Function	Also used for TPG output (TPG1-0 to TPG1-7). / 3-state output only for P20.							

Port 2 Control Register

P2CR (FFC5H)

Prohibit read-modify-write.

	7	6	5	4	3	2	1	0
bit Symbol	P27C	P26C	P25C	P24C	P23C	P22C	P21C	P20C
Read/Write	W							
Value after reset	0							
Function	0 : In					1 : Out (Specifies I/O in units of bits.)		

Sets port 2 input / output.

0	Input
1	Output

Port 0 Control Register

P0CR (FFC1H)

Prohibit read-modify-write.

	7	6	5	4	3	2	1	0
bit Symbol						P2S	P0S	P0C
Read/Write						W	W	W
Value after reset						0	0	0
Function						Output of P20 3-state (TPG1-15 control) 0: Disable 1: Enable	Output of P00 3-state (TPG0-15 control) 0: Disable 1: Enable	P0 control 0: In 1: Out

See 3.5.1, Port 0.

Controls output to P20 by TPG1-15.

0	Disable
1	Enable

P20 states according to <P20C> and <P2S> of Port 0/2 control register and TPG1-15

<P20C>	<P2S>	TPG0 – 15	P20 state
0	–	–	Input
1	0	0	Output
	0	1	
	1	0	
	1	1	High impedance

※ (Note)

When P2CR<P20C> is "0", P20 is set to input mode regardless of the value of <P2S> or TPG1-15.

When both P2CR<P20C> and P0CR<P2S> are set to "1" and TPG1-15 is set to "1", P20 is set to high impedance regardless of the value of P2<P20>.

Figure 3.5 (6) Port 2 Related Registers

3.5.4 Port 3 (P30 to P37)

Port 3 (address FFC6H in memory) consists of a 5-bit general-purpose I/O port to which I/O can be specified in units of bits, and a 3-bit general-purpose I/O port to which input or output is fixed.

To specify I/O for P30 to P34, use control register P3CR (bits 0 to 4 at address FFC7H in memory).

Reset resets all bits in the control register and the output latch register to "0"; I/O port (P30 to P32) and input-fixed port (P33 and P34) to input mode; output-fixed port (P37) to PWM8 output.

P33 / C-Sync is also used for input from the C-Sync input processing circuit. P34 / EXT is also used for servo signal trigger input. P35 and P36 are also used as interrupt control pins (INT0 and INT1).

After reset, servo input function is enabled. P33 can be used for C-Sync input; P34, for EXT input.

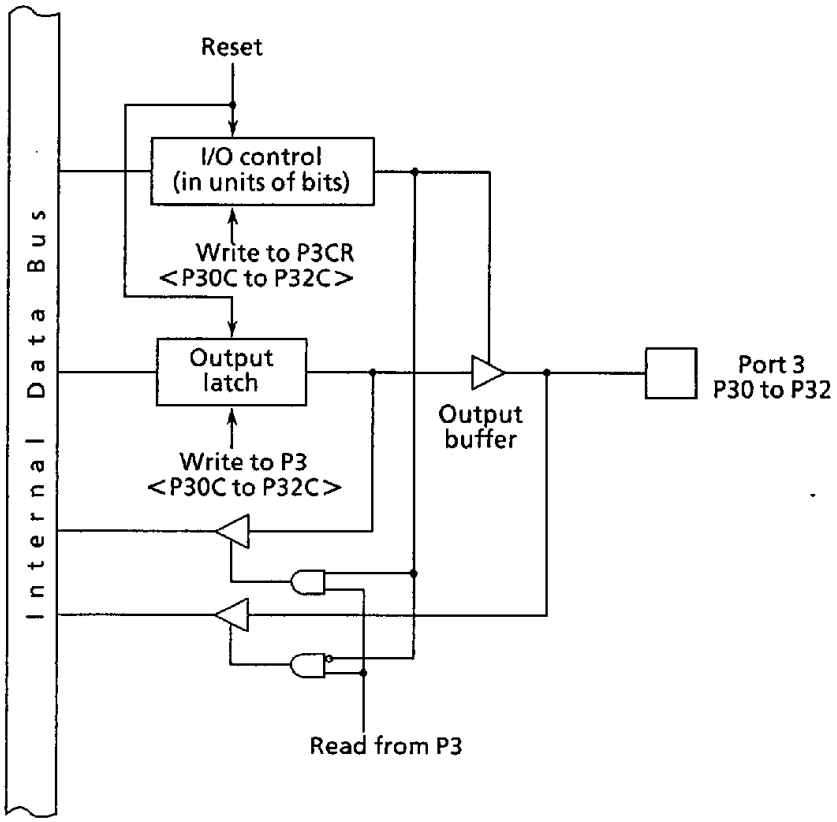


Figure 3.5 (7)-1 Port 3 (P30 to P32)

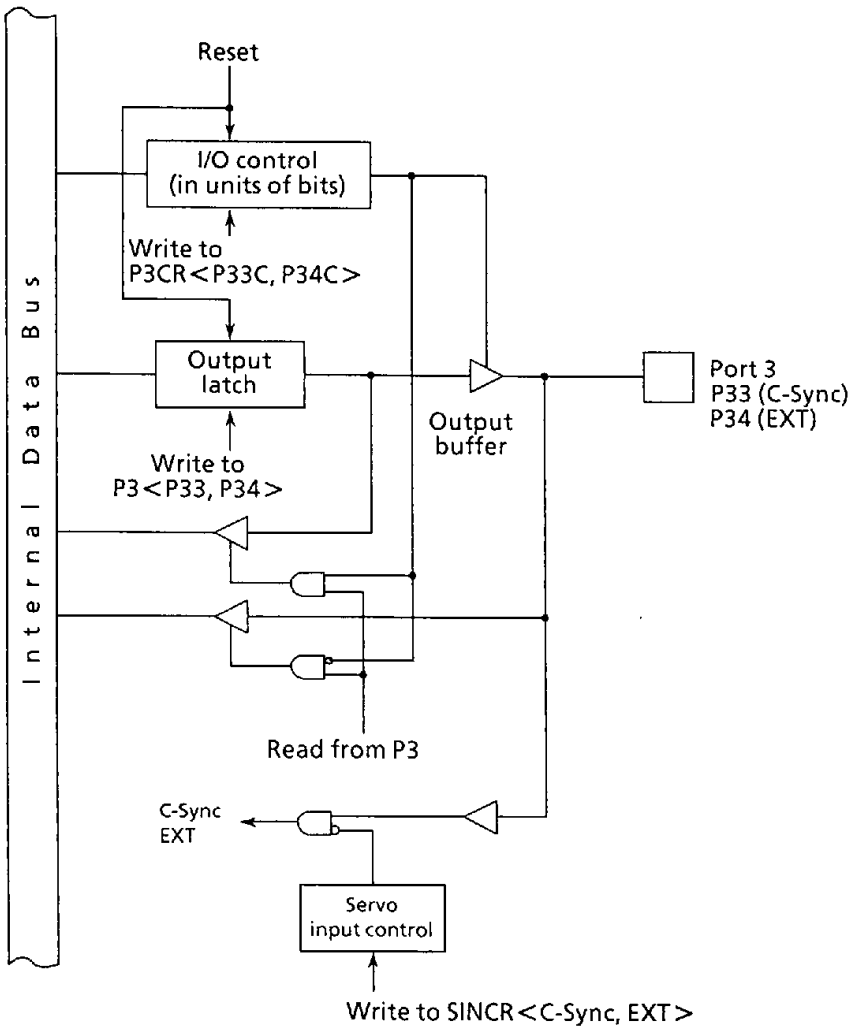


Figure 3.5 (7)-2 Port 3 (P33 and P34)

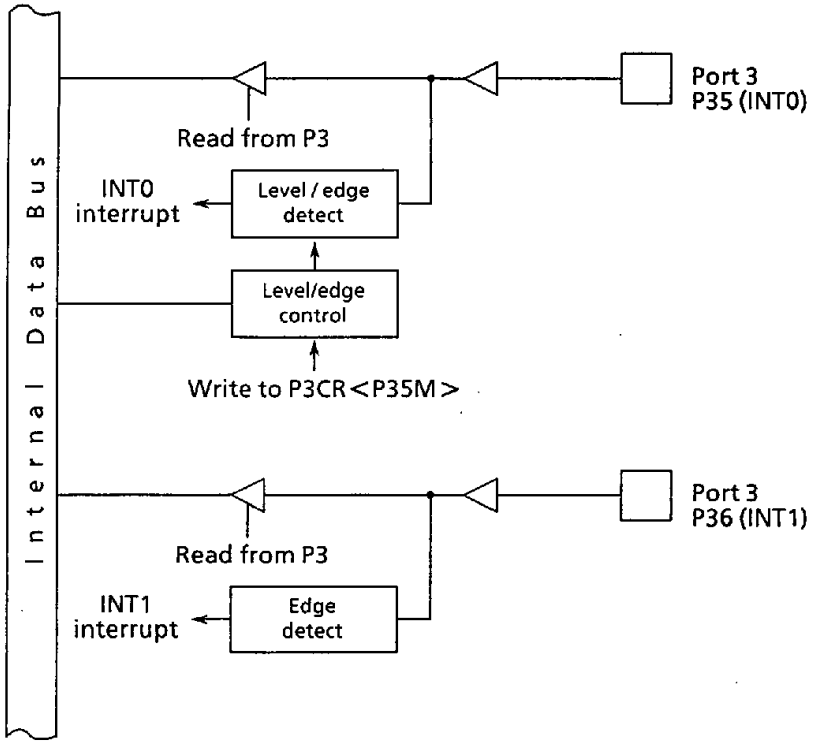
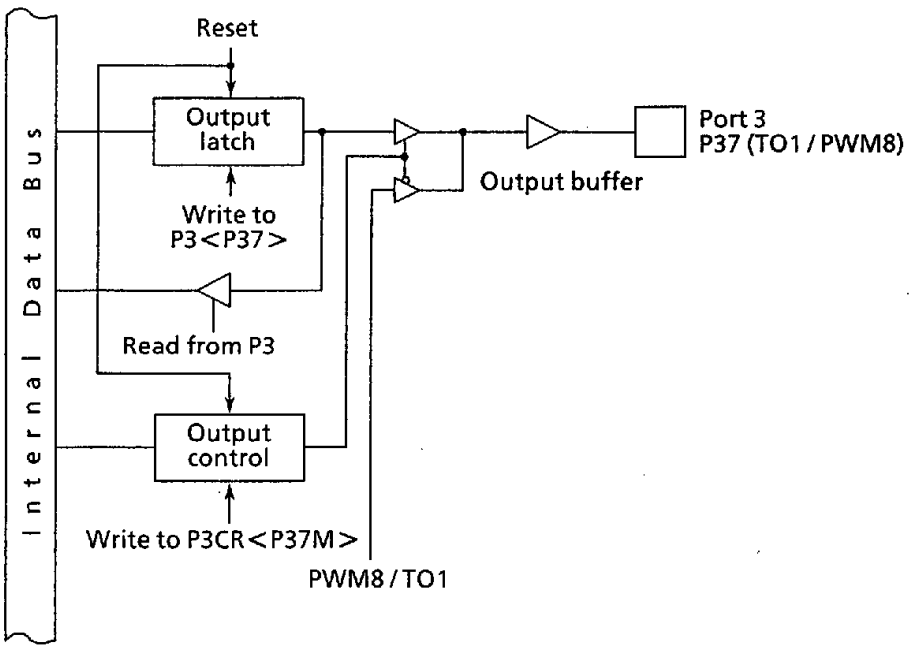


Figure 3.5 (7)-3 Port 3 (P35 and P36)



(Note) P37 output is open drain.

Figure 3.5 (7)-4 Port 3 (P37)

Port 3 Register

P3 (FFC6H)

	7	6	5	4	3	2	1	0
bit Symbol	P37	P36	P35	P34	P33	P32	P31	P30
Read/Write	R/W (Note)	R		R/W				
Value after reset	PWM8 output	Input only		Input mode				
Function	Also used for PWM8 and TO1.	Also used for INT1.	Also used for INT0.	Also used for EXT.	Also used for C-Sync.			

(Note) <P37> data can be read from the port output latch.
The port function is output only.

Port 3 Control Register

P3CR (FFC7H)

	7	6	5	4	3	2	1	0
bit Symbol		P37M	P35M	P34C	P33C	P32C	P31C	P30C
Read/Write		R/W	R/W	R/W				
Value after reset		0	0	0				
Function		P37 function control 0 : PWM8/TO1 1 : Port	INT0 control 0 : level 1 : ↑ edge	0 : In 1 : Out (Specifies I/O in units of bits.)				

Sets port 3 input / output

0	Input
1	Output

Controls INT0

0	Interrupt detected at high level
1	Interrupt detected at rising edge

P37 function control

0	PWM8 / TO1
1	P37

(Note) To select PWM8 or TO1, use the TFFCR<TOSEL> (FFD9H).

TFFCR <TOSEL> \ <P37M>	0	1
0	PWM8	Output to P37
1	TO1	

Servo Input Control Register

SINCR (FFCEH)

	7	6	5	4	3	2	1	0
bit Symbol			C-Sync	EXT	P-CTL	C-FG	D-PG	D-FG
Read/Write			R/W	R/W	R/W	R/W	R/W	R/W
Value after reset			0	0	0	0	0	0
Function			Servo Input Signal 0 : Enable 1 : Disable					

Figure 3.5 (8) Port 3 Related Registers

3.5.5 Port 4 (P40 to P47)

Port 4 an 8-bit general-purpose I/O port P4 (address FFC8H in memory) to which I/O can be specified in units of bits. To specify I/O, use control register P4CR (address FFC9H in memory).

Reset resets all bits in the control register and the output latch register to "0" and to input mode.

In addition to its general-purpose I/O port function, other port 4 functions are: serial channel (SIO0, SIO1) input/output (SCLK0, 1 / TxD0,1 / RxD0,1), and interrupt and timer (INT2 / TI0, TI1) input.

To use port 4 for serial channel, set the I/O pin settings using port 4 mode control register P4MR (address FFCAH in memory).

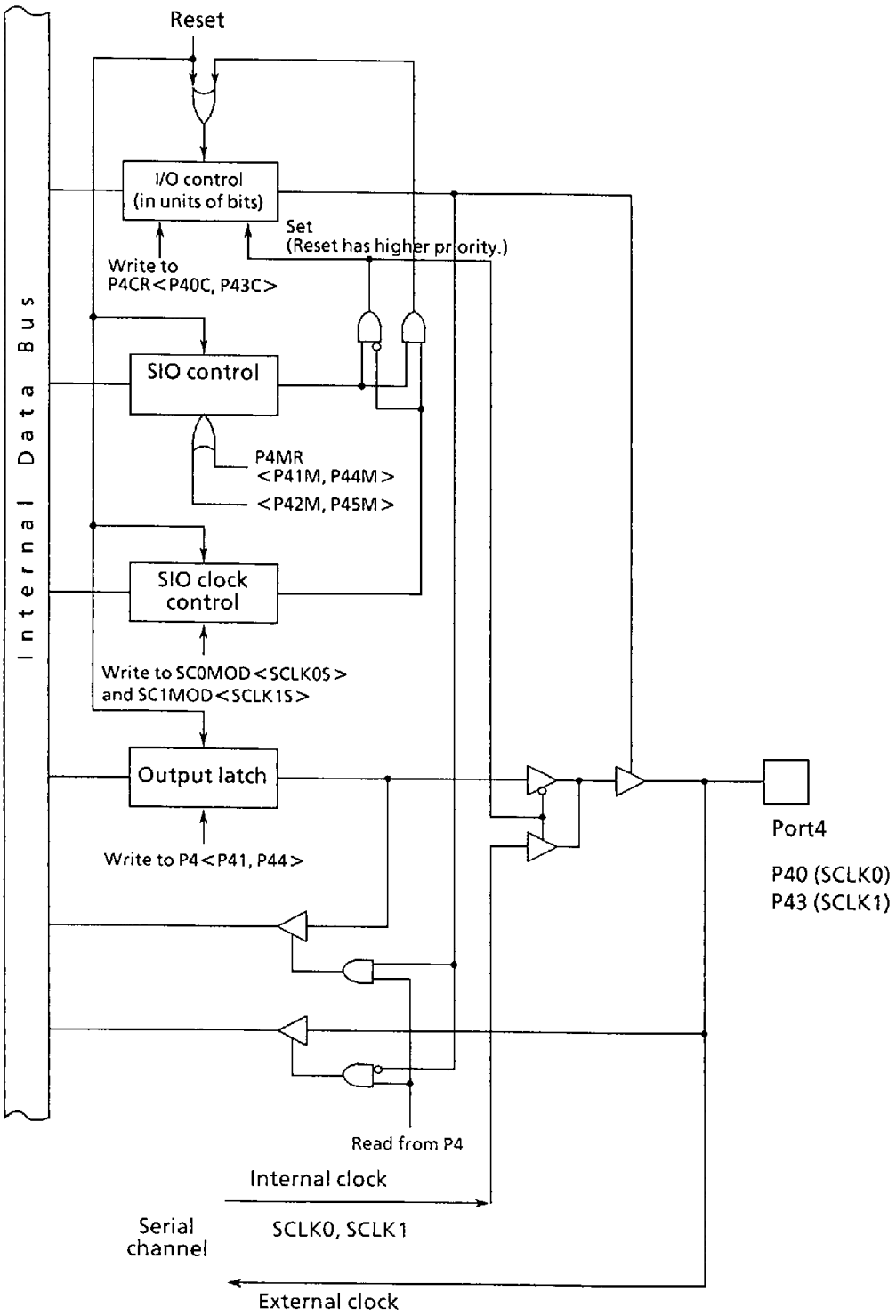


Figure 3.5 (9) - 1 Port 4 (P40 and P43)

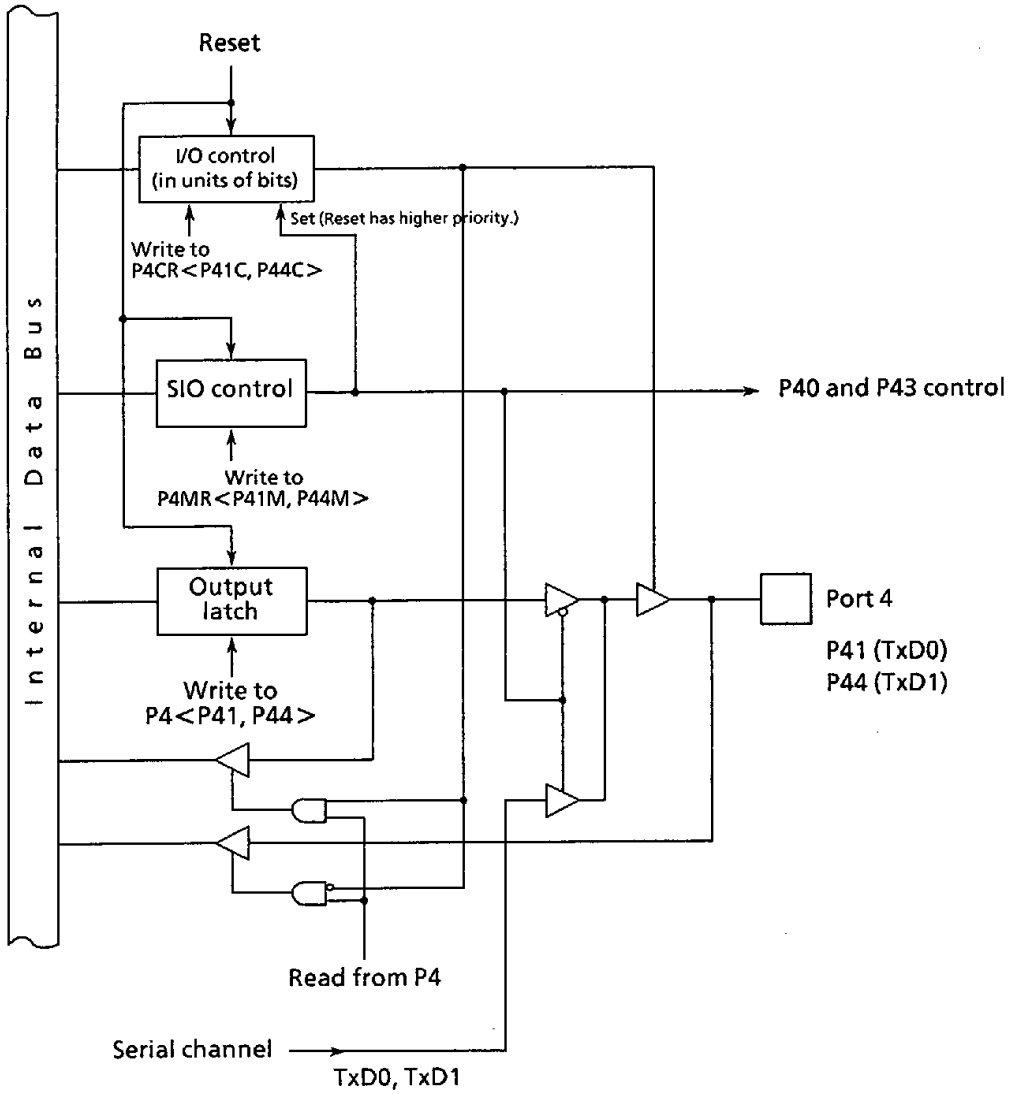


Figure 3.5 (9) - 2 Port 4 (P41 and P44)

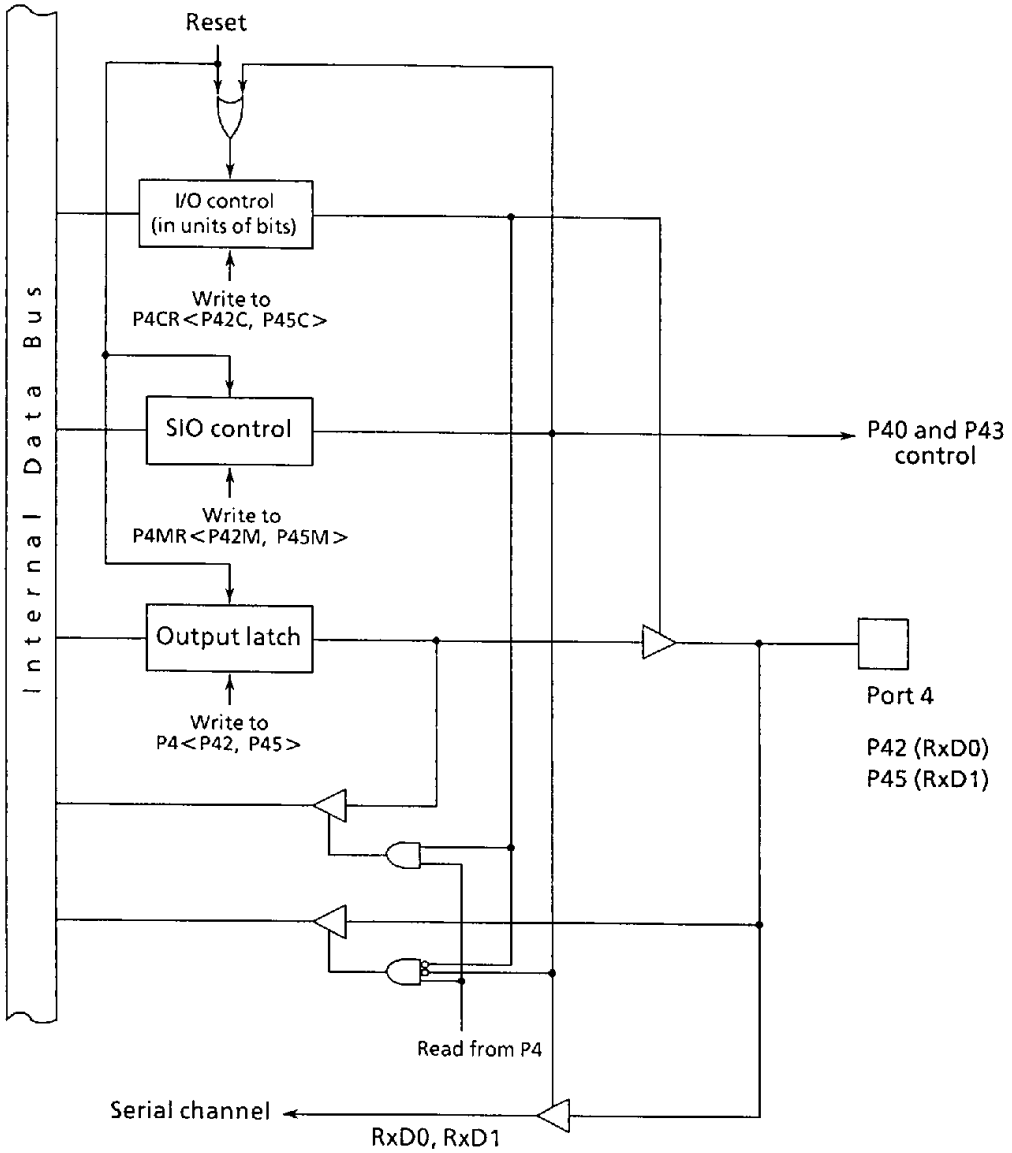


Figure 3.5 (9) - 3 Port 4 (P42 and P45)

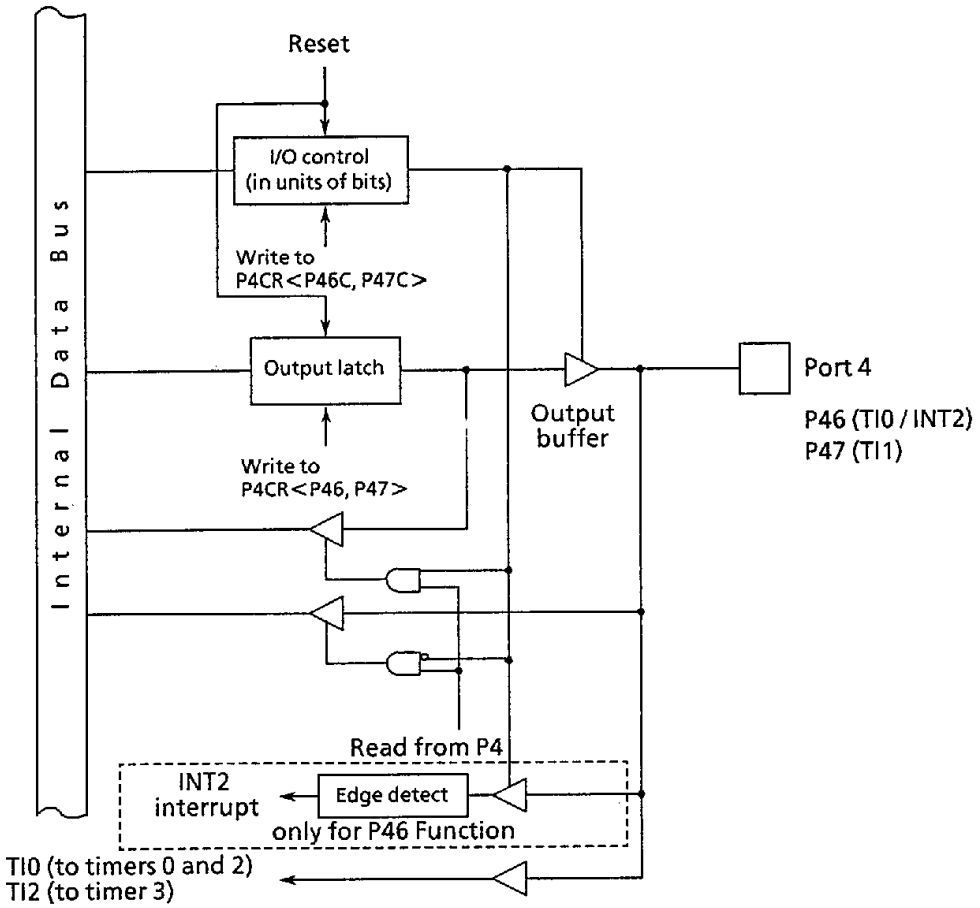


Figure 3.5 (9) - 4 Port 4 (P46 and P47)

Port 4 Register

P4 (FFC8H)

	7	6	5	4	3	2	1	0
bit Symbol	P47	P46	P45	P44	P43	P42	P41	P40
Read/Write	R/W							
Value after reset	Input mode							
Function	Also used for TI1.	Also used for TI0 and INT2.	Also used for RxD1.	Also used for TxD1.	Also used for SCLK1.	Also used for RxD0.	Also used for TxD0.	Also used for SCLK0.

Port 4 Control Register

P4CR (FFC9H)

	7	6	5	4	3	2	1	0
bit Symbol	P47C	P46C	P45C	P44C	P43C	P42C	P41C	P40C
Read/Write	R/W							
Value after reset	0							
Function	0 : In				1 : Out	(Specifies I/O in units of bits.)		

→ Sets port 4 input / output

0	Input
1	Output

Port 4 Mode Control Register

P4MR (FFCAH)

	7	6	5	4	3	2	1	0
bit Symbol					P45M	P44M	P42M	P41M
Read/Write					R/W	R/W	R/W	R/W
Value after reset					0	0	0	0
Function					SIO1 receive Control 0: Port 1: RxD1	SIO1 send Control 0: Port 1: TxD1	SIO1 receive Control 0: Port 1: RxD0	SIO1 send Control 0: Port 1: TxD0

→ Sets P40, P41/SCLK0, TxD0 function

0	P40, P41
1	SCLK0, TxD0

→ Sets P40, P42/SCLK0, RxD0 function

0	P40, P42
1	SCLK0, RxD0

Sets P43, P45 / SCLK1, RxD1 function

0	P43, P45
1	SCLK1, RxD1

→ Sets P43, P44/SCLK1, TxD1 function

0	P43, P44
1	SCLK1, TxD1

Figure 3.5 (10) Port 4 Related Registers

3.5.6 Port 5 (P50 to P57)

Port 5 is an 8-bit input port (address FFCBH in memory) which is also used for analog input (AN00 to AN07).

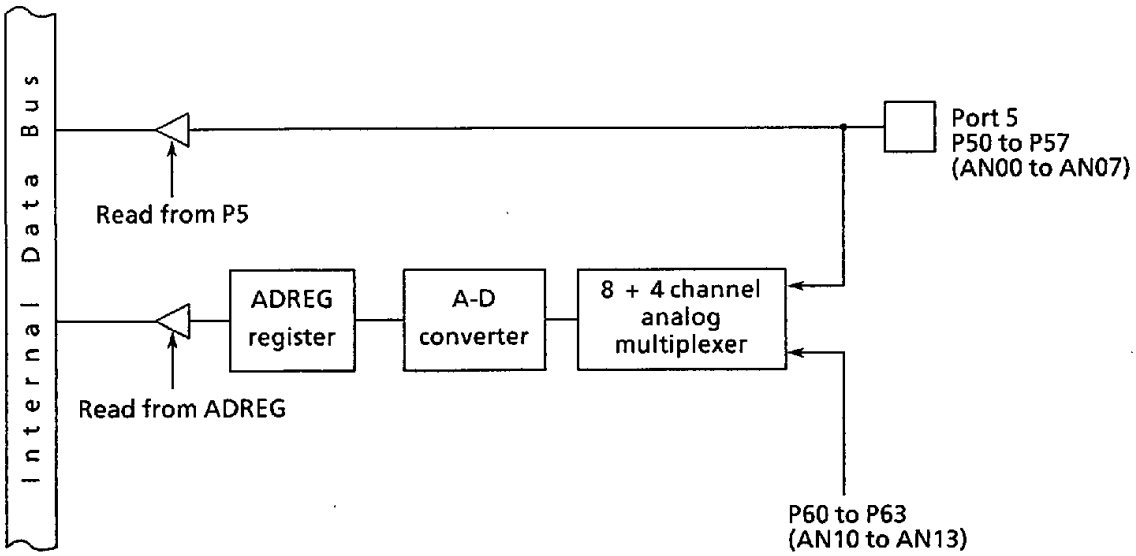


Figure 3.5 (11) Port 5

Port 5 Register

	7	6	5	4	3	2	1	0
bit Symbol	P57	P56	P55	P54	P53	P52	P51	P50
Read/Write	R							
Value after reset	Input only							
Function	Also used for analog input pin (AN00 to AN07)							

P5 (FFCBH)

Figure 3.5 (12) Port 5 Related Registers

3.5.7 Port 6 (P60 to P67)

Port 6 is a general-purpose I/O port consisting of 4 bits to which I/O can be specified in units of bits, and 4 bits to which input is fixed.

To specify I/O for the pins from P60 to P63, use control register P6CR<P60C, P61C, P62C, P63C> (bits 0 to 3 at address FFCDH in memory).

Reset resets all bits in the control register and the output latch register to "0" and to input mode.

In addition to its general-purpose I/O port function, port 6 is used for A/D input (AN10 to AN13) and servo signal trigger input (CAP0 to CAP3).

After reset, servo input function is enabled. P64 to P67 can be used for CAP0 to CAP3 input.

(Note) When using P60 to P63 for A/D input (P6CR<P6M> = 1), I/O port function cannot be used.

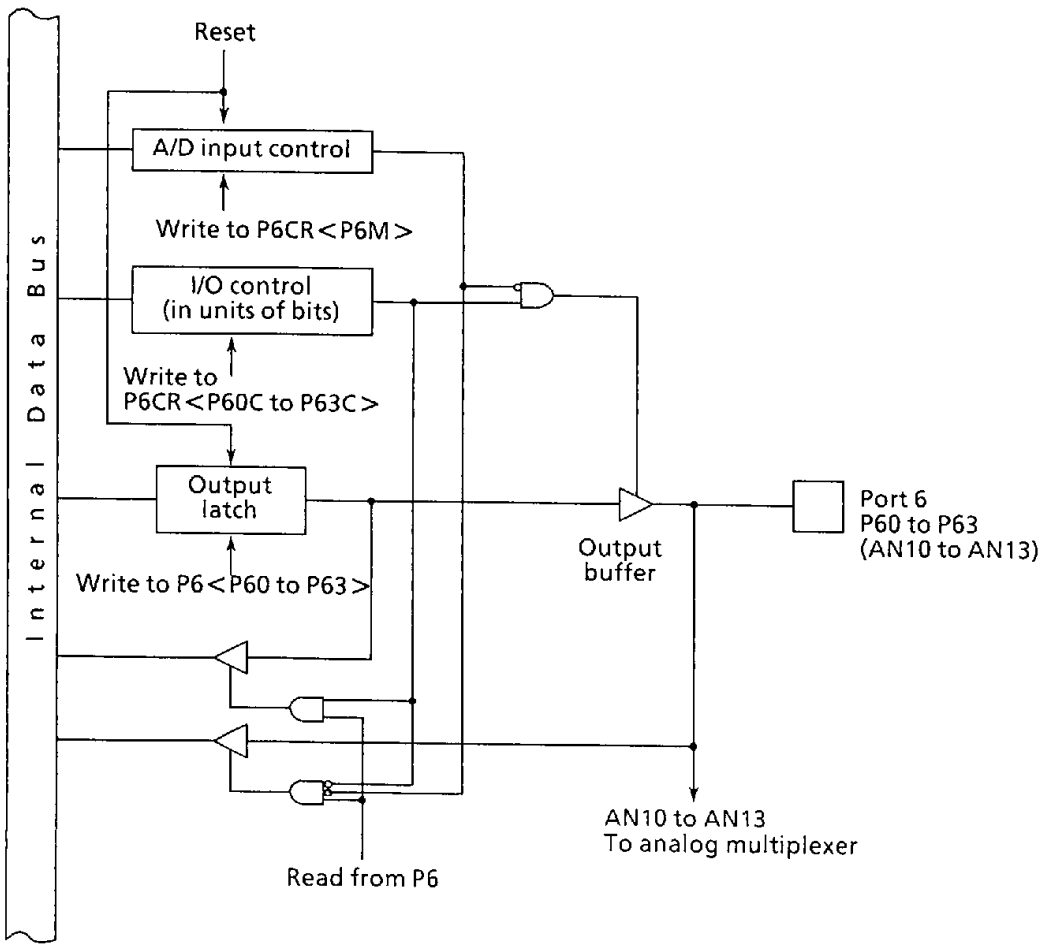


Figure 3.5 (13) -1 Port 6 (P60 to P63)

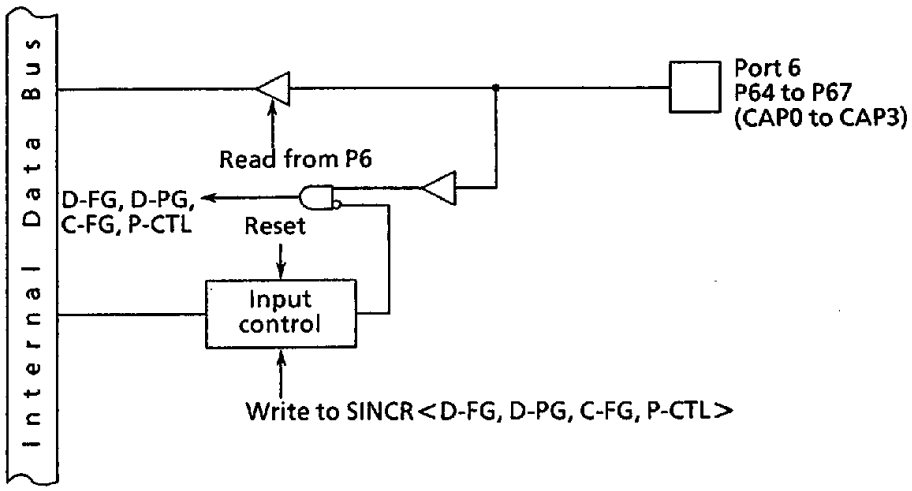


Figure 3.5 (13) -2 Port 6 (P64 to P67)

Port 6 Register

P6 (FFCCH)

	7	6	5	4	3	2	1	0
bit Symbol	P67	P66	P65	P64	P63	P62	P61	P60
Read/Write	R				R/W			
Value after reset	Input only				Input mode			
Function	Also used servo signal trigger input (CAP0 to CAP3)				Also used for analog input pin (AN10 to AN13)			

Port 6 Control Register

P6CR (FFCDH)

	7	6	5	4	3	2	1	0
bit Symbol		Note : Always write "0"		P6M	P63C	P62C	P61C	P60C
Read/Write				R/W	R/W			
Value after reset				0	0			
Function				A/D input control 0: Port 1: A/D input	0: In 1: Out (Specifies I/O in units of bits.)			

Sets port 6 (P60 to P63) input / output

0	Input
1	Output

Sets port 6 (P60 to P63) function

0	Port 6
1	A/D input (AN10 to AN13)

Servo Input Control Register

SINCR (FFCEH)

	7	6	5	4	3	2	1	0
bit Symbol			C-Sync	EXT	P-CTL	C-FG	D-PG	D-FG
Read/Write			R/W	R/W	R/W	R/W	R/W	R/W
Value after reset			0	0	0	0	0	0
Function			Servo Input Signal 0: Enable 1: Disable					

Figure 3.5 (14) Port 6 Related Registers

3.6 Time Base Counter (TBC)

The TMP91C642A has an 18-bit time base counter which generates operation timing reference signals. The software servo is controlled by system time, which is based on the contents of the time base counter. A clock obtained by dividing the fundamental clock (fc) by two is input to the time base counter.

The time base counter outputs (TBC1 to TBC18) are used as reference signals for timers 0 to 3, 24-bit capture, timing pulse generator, 12-bit PWM, and watchdog timer. Figure 3.6 (1) is the block diagram of the time base counter.

3.6.1 Operation

The time base counter value can be cleared by time base counter operating mode register TBMOD<TBCCLR>. Setting <TBCCLR> = 1 zero-clears the counter value. During reset, <TBCCLR> is cleared to "0". Releasing reset starts the timer base counter from "0".

The time base counter has two interrupt sources. It can select an interrupt source according to control register TBMOD<INTS2,1>. Both interrupt generating circuits use control register TBMOD<INTTBC2,1> to select one of the four TBC output signals and generate an INTTB interrupt. These interrupts are output to TPG0-13, also used for output by the timing pulse generating circuit. Reading <FTBC2, 1><FTPG> of watchdog timer mode register WDMOD identifies the interrupt source.

When using an INTTB interrupt for the TBC, do not share the interrupt (TPG0-13) with the TPG. (If an INTTB interrupt is shared with TPG, interrupt timing may be incorrect.)

Figure 3.6 (2) is the INTTB interrupt generation block diagram.

Table 3.6 lists time base counter outputs and cycles.

Table 3.6 Time Base Counter Outputs and Cycles

TBC Output signal	Cycle (μs)	TBC Output signal	Cycle (μs)	TBC Output signal	Cycle (μs)
TBC1 (2^2/fc)	0.4	TBC7 (2^8/fc)	25.6	TBC13 (2^{14}/fc)	1638.4
2 (2^3/fc)	0.8	8 (2^9/fc)	51.2	14 (2^{15}/fc)	3276.8
3 (2^4/fc)	1.6	9 (2^{10}/fc)	102.4	15 (2^{16}/fc)	6553.6
4 (2^5/fc)	3.2	10 (2^{11}/fc)	204.8	16 (2^{17}/fc)	13107.2
5 (2^6/fc)	6.4	11 (2^{12}/fc)	409.6	17 (2^{18}/fc)	26214.4
6 (2^7/fc)	12.8	12 (2^{13}/fc)	819.2	18 (2^{19}/fc)	52428.8

@ fc = 10 MHz

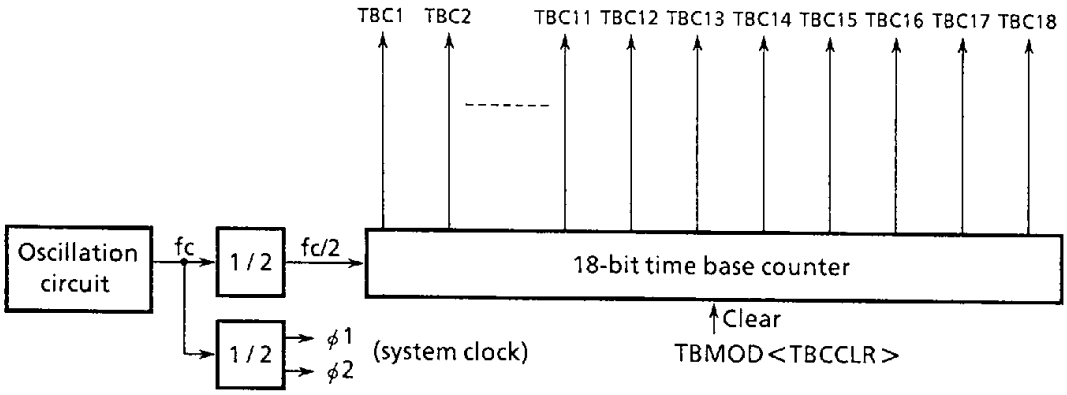


Figure 3.6 (1) Time Base Counter (TBC) Block Diagram

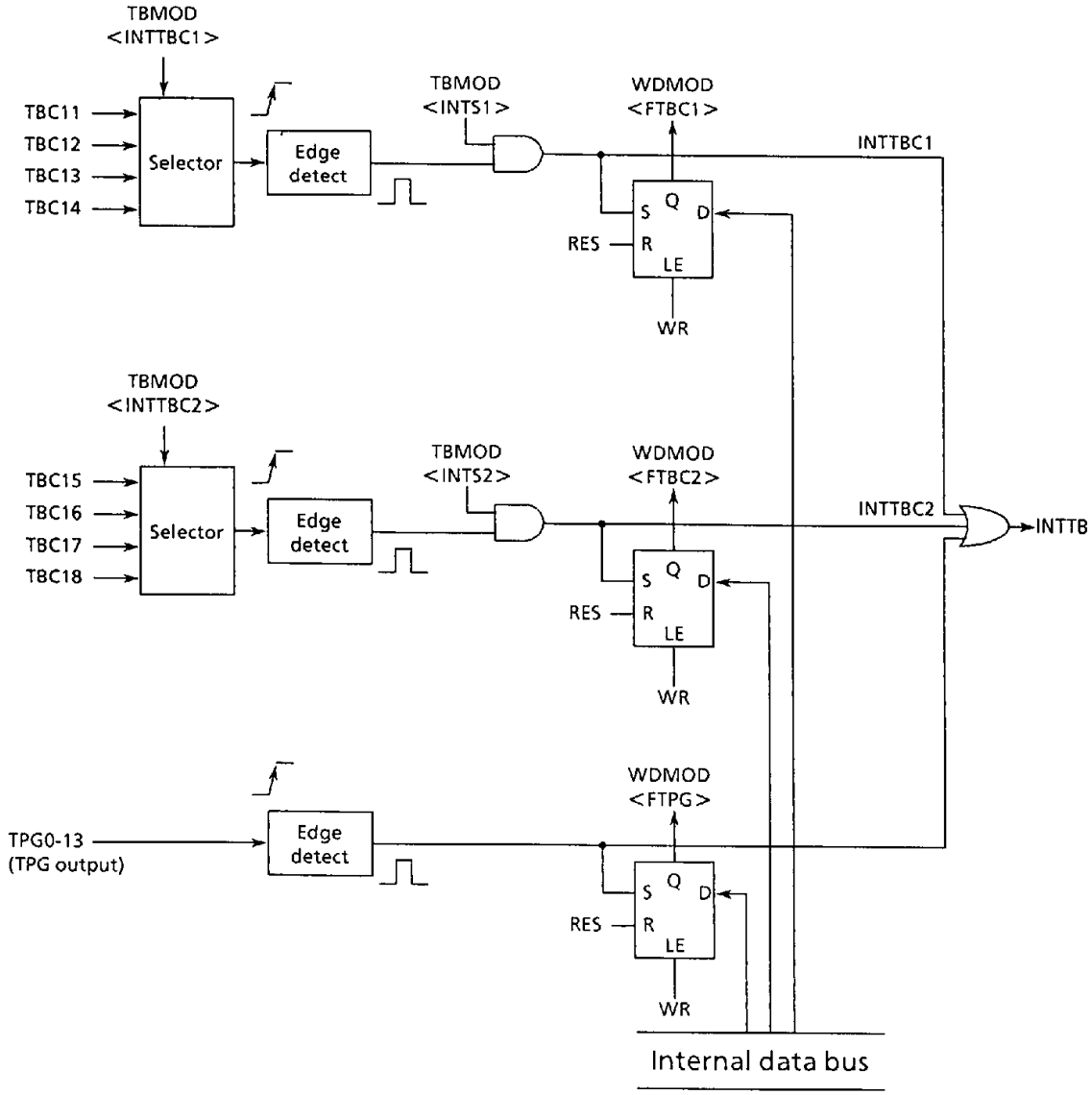


Figure 3.6 (2) INTTB Interrupt Generation Block Diagram

3.6.2 Control Registers

The time base counter is controlled by two control registers: TBMOD and WDMOD. Figure 3.6 (3) shows the TBC related register.

Time Base Counter Mode Control Register

		7	6	5	4	3	2	1	0
TBMOD (FFE8H)	bit Symbol		TBCCLR	INTS2	INTS1	INTTBC2		INTTBC2	
	Read/Write		R/W	R/W	R/W	R/W		R/W	
	Value after reset		0	0	0	0	0	0	0
	Function		TBC clear 0: – 1: Stop & Clear	TBC interrupt enable register 00: Disable 01: INT TBC1 10: INT TBC2 11: INT TBC1 & INT TBC2		TBC interrupt source select 2 00: TBC15 01: TBC16 10: TBC17 11: TBC18		TBC interrupt source select 1 00: TBC11 01: TBC12 10: TBC13 11: TBC14	

Time base counter interrupt source select 1

00	TBC11
01	TBC12
10	TBC13
11	TBC14

Time base counter interrupt source select 2

00	TBC15
01	TBC16
10	TBC17
11	TBC18

Time base counter interrupt enable register

00	Interrupt disable
01	INTTBC1 enable
10	INTTBC2 enable
11	INTTBC1&INTTBC2

Time base counter clear

0	–
1	Stop & Clear

Figure 3.6 (3)-1 TBC Related Registers

Watchdog Timer Mode Register

WDMOD (FFE6H)

	7	6	5	4	3	2	1	0
bit Symbol		FTBC2	FTBC1	WDTE	FTPG	HALT	EXF	DRVE
Read/Write		R/W	R/W	R/W	R/W	R/W	R	R/W
Value after reset		0	0	1	0	0	Undefined	0
Function		1: TBC15 to 18 interrupt flag	1: TBC11 to 14 interrupt flag	1: WDT Enable	1: TPG0-13 interrupt flag	HALT mode 0: RUN mode 1: STOP mode	Inverted by execution of EXX instruction	1: Drives pin in STOP mode.

I/O Pin control in STOP mode

0	I/O off
1	State before HALT

(Note) See 3.4.2, STOP mode.

Inverted by execution of EXX instruction.

(Note) Undefined immediately after reset.

HALT mode setting

0	RUN mode
1	STOP mode

TPG0-13 interrupt generation check flag

0	—
1	Interrupt generated.

(Note) Write "0" after check.

Watchdog timer enable/disable control

0	Disable (Note)
1	Enable

(Note) To disable the watchdog timer, the disable code must also be written to WDCR as well as WDMOD.

(TBC11 to TBC14) interrupt generation check flag

0	—
1	Interrupt generated.

(Note) Write "0" after check.

(TBC15 to TBC18) interrupt generation check flag

0	—
1	Interrupt generated.

(Note) Write "0" after check.

Figure 3.6 (3) - 2 TBC Related Registers

3.7 Watchdog Timer (Malfunction Detection Timer)

When the CPU starts misoperation (that is, malfunction) due to noise or some other cause, the watchdog timer (WDT) detects looping and brings the CPU back to normal operation. The malfunction is detected, a non-maskable interrupt is generated and the CPU is notified of malfunction.

3.7.1 Configuration

Figure 3.7 (1) is the block diagram of the watchdog timer.

The watchdog timer consists of a 5-step binary counter which uses TBC18 as an input clock, a flip / flop for watchdog timer output enable / disable, and control registers.

The watchdog timer generates an INTWD interrupt after a minimum detection time of 2^{22}/fc. The binary counter of the watchdog timer is zero-cleared before an INTWD interrupt generated by software (instruction). If the CPU misoperates due to noise or other cause and an instruction to clear the binary counter is not executed, the binary counter overflows and an INTWD interrupt is generated. Then the CPU detects the misoperation; normal operation can be resumed using a program to deal with malfunction.

The watchdog timer resumes operation immediately after reset is released.

The watchdog timer is stopped only in STOP mode. After STOP mode is released, the watchdog timer resumes operation after the warming up time.

The watchdog timer operates in RUN mode (the other HALT mode). It can be disabled before entering RUN mode.

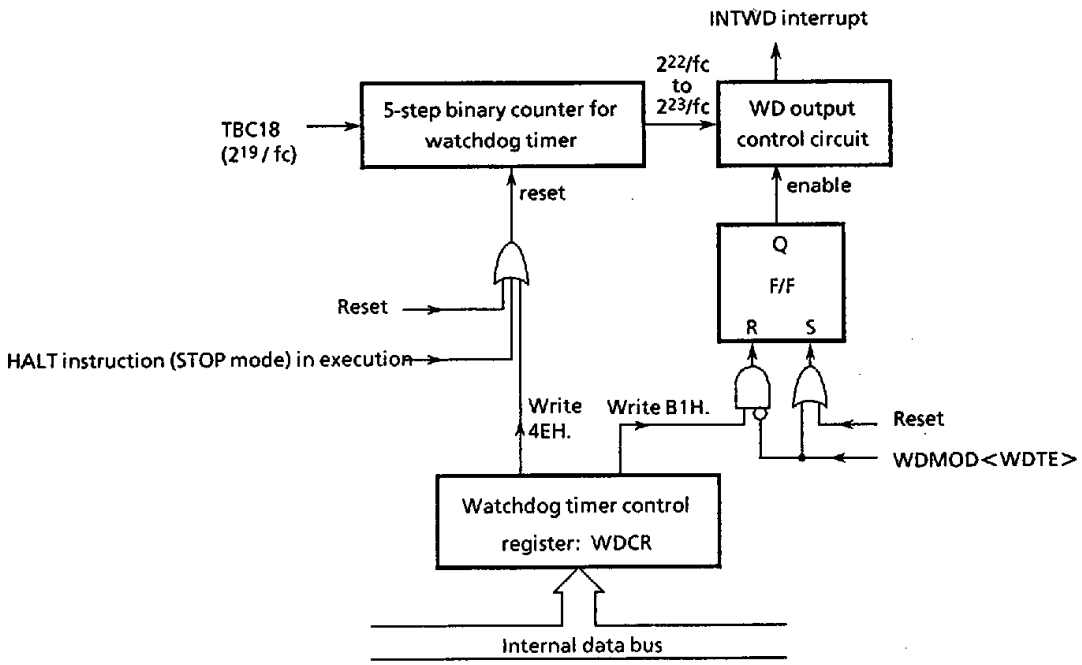


Figure 3.7 (1) Watchdog Timer Block Diagram

3.7.2 Operation

(1) Watchdog timer enable/disable control (WDMOD <WDTE>)

The watchdog timer is enabled because it is initialized <WDTE> = 1 by reset.

To disable the watchdog timer, WDTE must be zero-cleared and the disable code (B1H) must be written to watchdog timer control register WDCR.

To enable the watchdog timer, set <WDTE> to "1".

(2) Watchdog timer control register (WDCR)

Used to control disabling the watchdog timer and clearing the 5-step binary counter.

① Watchdog timer disable control

Writing "0" to WDMOD<WDTE>, then writing the disable code (B1H) to WDCR disables the watchdog timer.

Setting example:

```
WDMOD ← x x x 0 x x x x    Zero-clears <WDTE>.
WDCR  ← 1 0 1 1 0 0 0 1    Writes the disable code (B1H).
```

② Clear control of watchdog timer binary counter

Writing the clear code (4EH) to WDCR clears the binary counter and performs re-count.

During reset or halt execution after setting the mode to STOP mode, the clear signal is input and the watchdog timer is reset.

Setting example:

Clear control by writing clear code

```
WDCR  ← 0 1 0 0 1 1 1 0    Writes the clear code (4EH).
```

Clear control by HALT mode

```
WDMOD ← - - - - - - 1 x x  Sets to STOP mode.
Executes HALT instruction.  Sets to HALT mode.
```

3.7.3 Control Register

The watchdog timer (WDT) is controlled by two control registers: WDMOD and WDCR. Figure 3.7 (2) shows the WDT related register.

Watchdog Timer Mode Register

WDMOD (FFE6H)

	7	6	5	4	3	2	1	0
bit Symbol		FTBC2	FTBC1	WDTE	FTPG	HALT	EXF	DRVE
Read/Write		R/W	R/W	R/W	R/W	R/W	R	R/W
Value after reset		0	0	1	0	0	Undefined	0
Function		1: TBC15 to 18 interrupt flag	1: TBC11 to 14 interrupt flag	1: WDT Enable	1: TPG0-13 interrupt flag	HALT mode 0: RUN mode 1: STOP mode	Inverted by execution of EXX instruction.	1: Drives pin in STOP mode.

See 3.6, Time Base Counter

See 3.1, CPU / 3.4, Standby function

Watchdog timer enable / disable control

0	Disable (Note)
1	Enable

(Note) To disable the watchdog timer, the disable code must also be written to WDCR as well as WDMOD.

Watchdog Timer Control Register

WDCR (FFE7H)

	7	6	5	4	3	2	1	0
bit Symbol								
Read/Write	W							
Value after reset	—							
Function	B1H : WDT Disable Code 4EH : WDT Clear Code							

Watchdog Timer disable and clear

B1H	Disable code
4EH	Clear code
Other than above	—

Figure 3.7 (2) Watchdog Timer Related Registers

3.8 Servo Input Circuit

TMP91C642A incorporates the following servo input dedicated circuits and signal processing circuits to efficiently perform servo operation by software.

- D-FG / D-PG input processing circuit
- C-FG programmable divider
- C-FG mask counter
- P-CTL programmable divider
- VISS / VASS detector (explained in 3.9, VISS / VASS detector.)
- C-Sync input processing circuit (explained in 3.10, C-Sync Input Circuit.)

3.8.1 D-FG / D-PG Input Circuit / P64 (CAP0) · P65 (CAP1)

There are three commonly-used methods (2PG, 2PG / FG, and 1PG / FG) of generating frequencies and pulses for VCR servo control using a drum. The D-FG / D-PG input circuit incorporates a detect-edge selector and a 3-bit programmable divider for processing the D-FG input signal used to synchronize the D-FG input with the D-PG input signal.

0V-5V logical-level signals are obtained by amplifying and shaping, using the sense amp of the external circuit, the small signals from the frequency generator (FG) and pulse generator (PG) on the drum motor. These logical-level signals are used as the D-FG / D-PG input signals.

Edge detection of D-FG / D-PG is controlled by servo input control register SSINCR1<DFGPO, DPGPO> (bits 5 and 1 at address FFEEH in memory). The 3-bit programmable divider can set the frequency division ratio from 1 to 1/8 in the D-FG frequency divider control register, PCDFCR<DFGPR2 to 0> (bits 7 to 5 at address FFF1H in memory).

The frequency dividing counter is reset when a D-PG edge detect pulse is generated with SSINCR1<DPFG>=1. In the 1PG / FG method, this operation is used to divide the D-FG signal.

Table 3.8 (1) lists settings of the D-FG frequency divider control register and D-FG signal frequency division ratios.

Table 3.8 (1) Settings of D-FG Frequency Divider Control Register and D-FG Signal Frequency Division Ratios

PCDFCR<DFGPR2 to 0>			D-FG input signal frequency division ratio
2	1	0	
0	0	0	1
0	0	1	1/2
0	1	0	1/3
0	1	1	1/4
1	0	0	1/5
1	0	1	1/6
1	1	0	1/7
1	1	1	1/8

The D-FG / D-PG input signal is enabled/disabled using servo input control register SINCR<D-FG, D-PG>. The D-FG/D-PG input pins can be simultaneously used as input ports (P64, P65).

Reading SSINCR1<DPGIN> checks the D-PG input signal. Writing "1" to SVCFREG<DPGFRS> clears SSINCR1<DPGIN>.

The following explains using examples with TMP91C642A the three commonly-used methods of VCR servo control with FG · PG generation using a drum.

(1) 2PG Method

Generates two PG pulses per one rotating of the drum and uses these pulses to generate the head switching (D-FF) signal. At this time, to correct inaccuracies of the PG magnet and rotating head positioning, adjusts them by varying their delay times. TMP91C642A captures TBC time data at the PG pulse timing and detects them as phase data. The value determined by adding the pre-defined delay data to the detected phase data is set to the TPG comparator register and a D-FF signal is generated. The D-AFC (drum motor-auto frequency controller) detects both edges of the signal.

With this method, a D-FF signal is generated at the PG pulse timing for reference. The D-FF signal can be generated in sync with the PG pulse timing even if the PG timing is delayed.

The 2PG method controls the speed of rotation using the PG pulse, with the output of the PWM circuit.

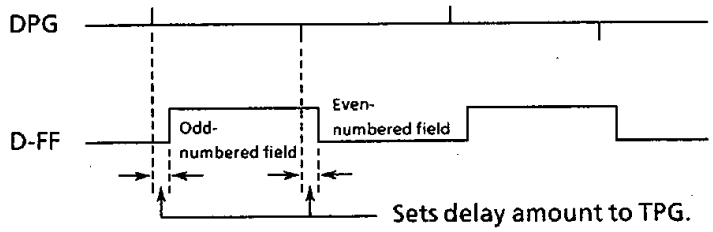


Figure 3.8 (1) D-FF Signal Generation Using 2PG Method

(2) 2PG / FG Method

The 2PG / FG method is the 2PG method with a D-AFC dedicated FG added to improve the performance of the AFC. The PG pulse is processed the same way as the 2PG method.

(3) 1PG/FG Method

Generates a one-edge head switching (D-FF) signal from FG. The one-edge pulse is generated on the assumption that the 180° division of FG is accurate. The advantage of this method is that the PG pulse is adjusted only once. The PG pulse only indicates which FG pulse corresponds to the phase of the drum head.

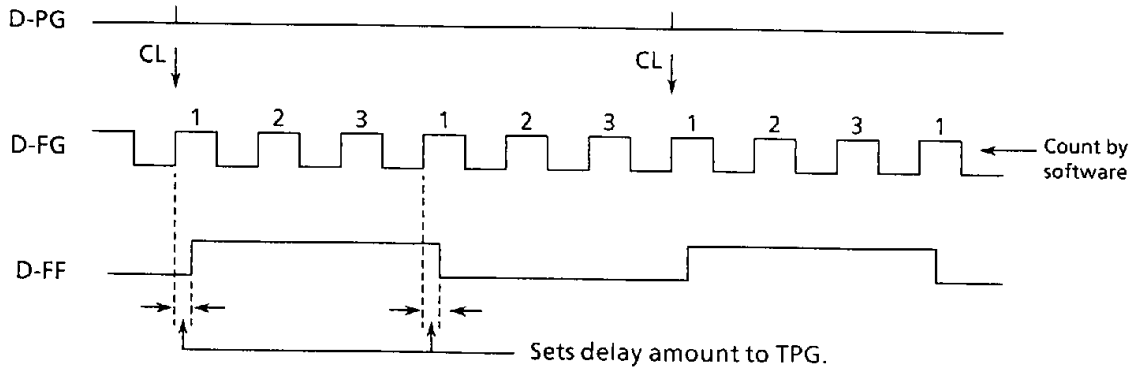


Figure 3.8 (2) Generation of D-FF Signal Using 1PG / FG Method

3.8.2 C-FG Input Circuit / P66 (CAP2)

To enable capstan motor variable-speed playback (special playback), the C-FG input circuit incorporates a 1/2 divider or doubler, used to change C-FG circuit sampling rate, and a 5-bit programmable divider. To prevent the CPU from losing control due to frequent interrupts during motor malfunction, the C-FG circuit incorporates a 4-bit mask counter.

0 to 5V logical-level signals are obtained by amplifying and shaping, using the sense amp of the external circuit, the small signals from the frequency generator (FG) obtained from the capstan motor. These logical-level signals are used as the C-FG input signals.

The input C-FG signal can be used as the input clock for timer 2 without change, thus enabling events to be counted.

Input pulses are enabled/disabled using servo input control register SINCR<C-FG> (bit 2 at address FFCEH in memory). The C-FG input circuit can be simultaneously used as an input port (P66).

(1) C-FG signal sampling rate selector

The C-FG signal sampling rate selector is used to select input signal sampling rates from 1/2, 1, and 2. The selector is controlled by servo input control register SSINCR1<CFWPR, CFWEG> (bits 4 and 3 at address FFEEH in memory).

(2) C-FG Programmable Frequency Divider

This divider consists of a 5-bit counter. A ratio of 1 to 32 is set to the C-FG frequency divider control register, PCFSCR<CFGPR4 to 0> (bits 4 to 0 at address FFF2H in memory).

Table 3.8 (2) lists settings of the C-FG frequency divider control register and C-FG frequency division ratios.

Table 3.8 (2) Settings of C-FG Frequency Divider Control Register and C-FG Frequency Division Ratios

PCFSCR <CFGPR4 to 0>					C-FG input signal frequency division ratio	PCFSCR <CFGPR4 to 0>					C-FG input signal frequency division ratio
4	3	2	1	0		4	3	2	1	0	
0	0	0	0	0	1	1	0	0	0	0	1/17
0	0	0	0	1	1/2	1	0	0	0	1	1/18
0	0	0	1	0	1/3	1	0	0	1	0	1/19
0	0	0	1	1	1/4	1	0	0	1	1	1/20
0	0	1	0	0	1/5	1	0	1	0	0	1/21
0	0	1	0	1	1/6	1	0	1	0	1	1/22
0	0	1	1	0	1/7	1	0	1	1	0	1/23
0	0	1	1	1	1/8	1	0	1	1	1	1/24
0	1	0	0	0	1/9	1	1	0	0	0	1/25
0	1	0	0	1	1/10	1	1	0	0	1	1/26
0	1	0	1	0	1/11	1	1	0	1	0	1/27
0	1	0	1	1	1/12	1	1	0	1	1	1/28
0	1	1	0	0	1/13	1	1	1	0	0	1/29
0	1	1	0	1	1/14	1	1	1	0	1	1/30
0	1	1	1	0	1/15	1	1	1	1	0	1/31
0	1	1	1	1	1/16	1	1	1	1	1	1/32

(3) C-FG Mask Counter

The C-FG mask counter is used to mask C-FG signals generated within the time specified by software and to prevent interrupts from being generated in less than the mask time.

The C-FG mask counter is a 4-bit counter. The counter uses internal signal TBC8 (2^9/fc) as input. The mask time is set in the C-FG mask time control register PCFCR1<CFMSK3 to 0> (upper 4 bits at address FFF0H in memory). Up to 768 μs (@fc=10 MHz) can be masked.

If the C-FG signal is input during masking, the malfunction detect flag, SSINCR2<CFGMCP> (bit 0 at address FFFFH in memory) is set to "1". Writing "1" to SVCFREG<CFGFRS> clears SSINCR2<CFGMCP>.

Table 3.8 (3) lists settings of the mask time control register and mask times.

Table 3.8 (3) Settings of C-FG Input Mask Time

PCFCR1 <CFMSK3 to 0> 3	2	1	0	n	C-FG input mask time (μs) @fc = 10 MHz
0	0	0	0	0	–
0	0	0	1	1	51.2
0	0	1	0	2	102.4
0	0	1	1	3	153.6
0	1	0	0	4	204.8
0	1	0	1	5	256.0
0	1	1	0	6	307.2
0	1	1	1	7	358.4
1	0	0	0	8	409.6
1	0	0	1	9	460.8
1	0	1	0	10	512.0
1	0	1	1	11	563.2
1	1	0	0	12	614.4
1	1	0	1	13	665.6
1	1	1	0	14	716.8
1	1	1	1	15	768.0

Mask Time

$= TBC8 \times n$

$= (1/(fc/2)) \times 2^8 \times n$ (s)

3.8.3 P-CTL Input Circuit / P67 (CAP3)

The P-CTL input circuit consists of an edge detect selector and a 5-bit programmable divider.

0 V-5 V logical-level signals obtained by amplifying and shaping, using the sense amp of the external circuit, signals recorded on the VCR tape which are extracted at playback by the control head. These logical-level signals are used as the P-CTL input signals.

Edge detect is selected using control register CSYNCR<PCTPO> (bit 5 at address FFEFH in memory). The control signals recorded on VCR tape consist of binary 1s and 0s. When switching the P-CTL edge, note that depending on the level of the P-CTL input, the number 1s of may not be counted correctly.

A frequency division ratio of 1 to 32 is set in the 5-bit programmable divider using the P-CTL frequency divider control register PCDFCR<PCTPR4 to 0> (bits 4 to 0 at address FFF1H in memory). (For how to make the setting, see Table 3.8 (2), Settings of C-FG Frequency Divider Control Register and C-FG Frequency Division Ratios.)

The input signal is enabled/disabled using servo input control register SINCR<P-CTL>. The P-CTL input circuit can be simultaneously used as an input port (P67).

First, the polarity of the input P-CTL signal is controlled according to CSYNCR<PCTPO>, then supplied to the timer 3 input clock and the VISS/VASS detector (see 3.9, VISS / VASS Detector).

<PCTPO> is a register used to select the rising/falling edge of the input signal. Switching the P-CTL input edge detect facilitates reading of P-CTL data at video forward/reverse.

3.8.4 C-Sync Input Circuit / P33

The C-Sync input circuit is used to input the composite sync signal (C-Sync) of the TV or VCR to the C-Sync input processing circuit (see 3.10, C-Sync Input Processing Circuit).

As the C-Sync input signals, 0 to 5V logical-level signals obtained by amplifying and shaping C-Sync signals, using the sense amp of the external circuit, are used.

Input signals are enabled/disabled using servo input control register SINCR<C-Sync>. (After reset, <C-Sync> = "0" and the C-Sync input circuit is enabled.)

3.8.5 EXT Input Circuit / P34

The EXT input circuit is a servo input circuit with an edge detect selector.

Edge detect is selected by servo input control register SSINCR1<EXTPO>.

Input signals are enabled/disabled using servo input control register SINCR<EXT>.

Edge-selected input signals are OR-ed with software capture, SVCFREG<CASFWR>, and shared. (After reset, <EXT> = "0" and the EXT input circuit is enabled.)

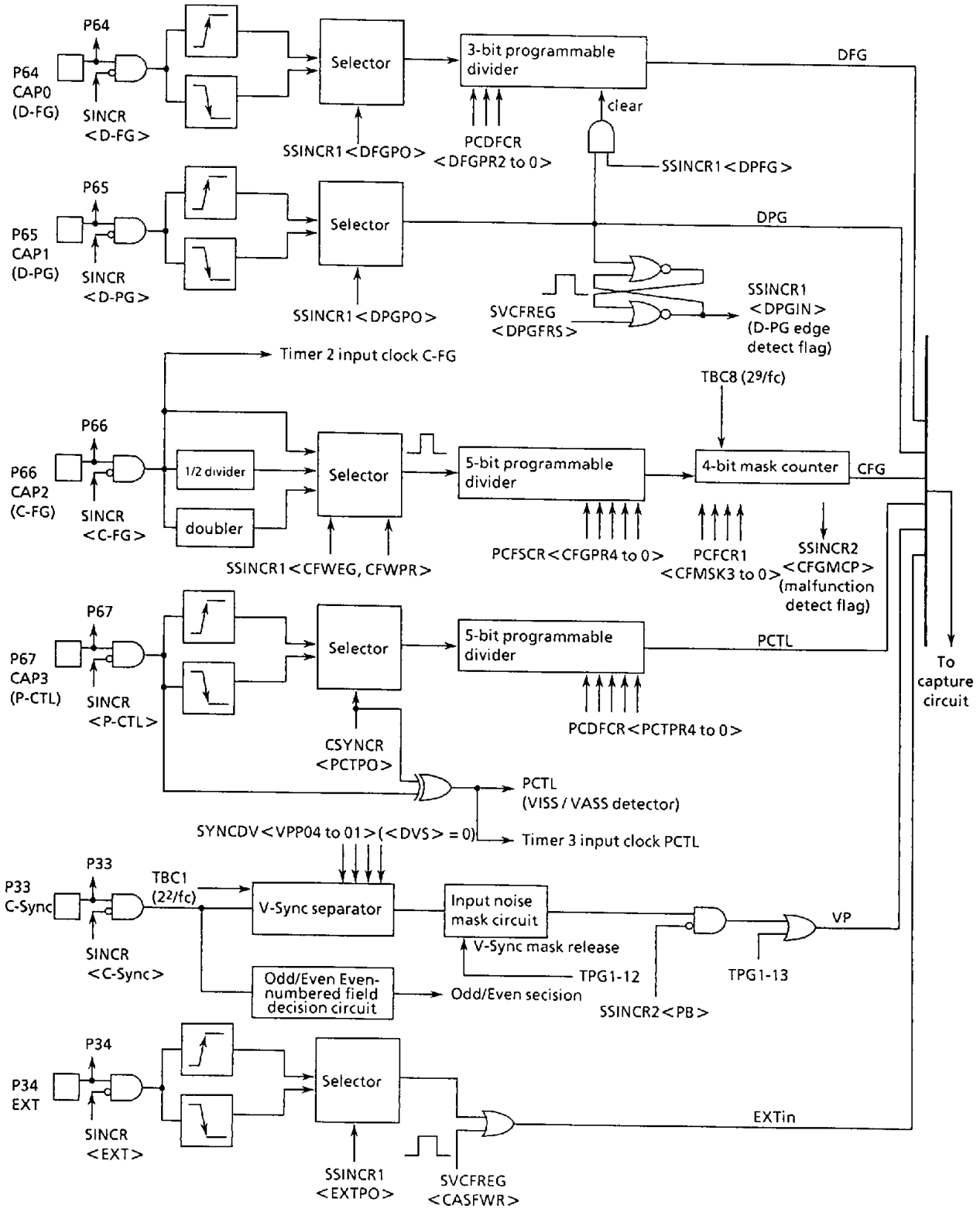


Figure 3.8 (3) Servo Input Block Diagram

3.8.6 Control Registers

Figure 3.8 (4) shows the servo input related register.

Servo Input Control Register

SINCR (FFCEH)

	7	6	5	4	3	2	1	0
bit Symbol			C-Sync	EXT	P-CTL	C-FG	D-PG	D-FG
Read/Write			R/W	R/W	R/W	R/W	R/W	R/W
Value after reset			0	0	0	0	0	0
Function			Servo Input Signal 0: Enable 1: Disable					

→ Servo input control

0	Enable
1	Disable

Figure 3.8 (4)-1 Servo Input Circuit Related Registers

Servo Input Control Register 1

SSINCR1 (FFEEH)

Prohibit read-modify-write.

	7	6	5	4	3	2	1	0
bit Symbol		EXTPO	DFGPO	CFWPR	CFWEG	DPFG	DPGPO	DPGIN
Read/Write		W	W	W	W	W	W	R
Value after reset		0	0	0	0	0	0	0
Function		EXT Edge Detection 0: ↑ 1: ↓	DFG Edge Detection 0: ↑ 1: ↓	CFG frequency division selector 0: 1 1: 1/2	CFG Edge Detection 0: ↑ ↓ 1: ↑	DFG/DPG sync register 0: Disable 1: Enable	DPG Edge Detection 0: ↑ 1: ↓	DPG Edge Detect Flag 1: D-PG edge detect

D-PG edge detect flag

0	–
1	D-PG edge detect

(Note) Writing "1" clears SVCFREG<DPGFRS> (bit 2 at address FFFEH in memory) to 0.

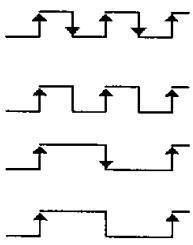
D-PG edge detect selector

0	Rising edge
1	Falling edge

DFG / DPG sync enable register

0	Disable
1	Resets D-FG counter at D-PG detect.

C-FG input sampling selector



00	Double (both edges at x1 frequency division)
01	x1 (rising edge at x1 frequency division)
10	x1 (both edges at 1/2 frequency division)
11	1/2 (rising edge at 1/2 frequency division)

D-FG edge detect selector

0	Rising edge
1	Falling edge

EXT edge detect selector

0	Rising edge
1	Falling edge

Figure 3.8 (4)-2 Servo Input Circuit Related Registers

C-FG Mask Time / VISS Discrimination Control Register

PCFCR1 (FFF0H)

Prohibit read-modify-write.

	7	6	5	4	3	2	1	0
bit Symbol	CFMSK3	CFMSK2	CFMSK1	CFMSK0	VISS3	VISS2	VISS1	VISS0
Read/Write	W				W			
Value after reset	0	0	0	0	0	0	0	0
Function	C-FG Mask Time Control				VISS discrimination control			

C-FG mask time control register
(Note) For settings, see Table 3.8 (3).

(Note) See 3.9, VISS / VASS Detector.

P-CTL / D-FG Control Register

PCDFCR (FFF1H)

Prohibit read-modify-write.

	7	6	5	4	3	2	1	0
bit Symbol	DFGPR2	DFGPR1	DFGPR0	PCTPR4	PCTPR3	PCTPR2	PCTPR1	PCTPR0
Read/Write	W			W				
Value after reset	0	0	0	0	0	0	0	0
Function	D-FG 3-bit prescaler control			P-CTL 5-bit prescaler control				

D-FG frequency divider control register
(Note) For settings, see Table 3.8 (1).

P-CTL frequency divider control register
(Note) For settings, see Table 3.8 (2).

P-CTL / C-FG Signal Register

PCFSCR (FFF2H)

Prohibit read-modify-write.

	7	6	5	4	3	2	1	0
bit Symbol	DVS	PCTLCK2	PCTLCK1	CFGPR4	CFGPR3	CFGPR2	CFGPR1	CFGPR0
Read/Write	W	W		W				
Value after reset	0	0	0	0	0	0	0	0
Function	SYNCDV Reg. Select 0: VPD. SYNC 1: FEP	PCTL Duty Detection Input Clock 00: TBC2 10: TBC6 01: TBC4 11: TBC8		C-FG 5bit Prescaler Control				

C-FG frequency divider control register
(Note) For settings, see Table 3.8 (2).

C-Sync control register select

0	VPP0/SYNP0 side (C-Sync input Control register)
1	FEP0 side (Odd / even discrimination control register)

(Note) See SYNCDV (address FFCFH in memory)

P-CTL duty measurement clock selector

00	TBC2 (2^3/fc)
01	TBC4 (2^5/fc)
10	TBC6 (2^7/fc)
11	TBC8 (2^9/fc)

Figure 3.8 (4)-3 Servo Input Circuit Related Register

Servo Input Control Register 2

SSINCR2 (FFFFH)

	7	6	5	4	3	2	1	0
bit Symbol					TP	DFMA	PB	CFGMCP
Read/Write					R/W	R/W	R/W	R
Value after reset					0	0	0	Undefind
Function					TPG0 / TPG1 Reg. Control 0: TPG0 1: TPG1	Control of input signal for 60/50 field discriminat ion 0: TPG0-1 (D-FF) 1: TPG1-13 (V-Sync (VP) embedd ed)	V-Sync detect or output control 0: Enable 1: Disable	CFG Malfunction Flag 0: – 1: Mal-function detect

C-FG malfunction detect flag

0	—
1	Malfunction

Even if the <CFGMCP> is reset, the data is not cleared. To clear the data, 1 must be written to the SVCFREG <CFGFRS>.

Vertical sync detect output control register

0	Enable
1	Disable

Control of input signal for 60/50 field discrimination

0	TPG0-1 (D-FF (head switching) signal)
1	TPG1-13 (V-Sync (VP) embedded)

TPG1 / TPG0 data control

0	TPG0
1	TPG1

Figure 3.8 (4)-4 Servo Input Circuit Related Registers

C-Sync Control Register

	7	6	5	4	3	2	1	0
CSYNCR (FFEFH) bit Symbol	CSYNCF	TPGF	PCTPO	OEDR	NPS	CTLDTY	VISSFL	VASSFL
Read/Write	R/W	R/W	W	R	R	R	R	R
Value after reset	0	0	0	0	0	0	0	0
Function	V-Sync Detection Flag 1: V-Sync	Pseudo V detect flag 1: Embedded	PCTL Signal Control 0: Forward 1: Reverse	Odd / Even discrimination result 0: Odd 1: Even	60 / 50 discrimination result 0: 60 1: 50	P-CTL Duty 0: ≦ 50 % 1: ≧ 50 %	VISS detect Flag 0: – 1: VISS data	VASS detect Flag 0: – 1: VASS data

Prohibit read-modify-write.

VASS detect flag

0	—
1	VASS data

VISS detect flag

0	—
1	VISS data

P-CTL duty discrimination result flag

0	Duty ≦ 50 %
1	Duty ≧ 50 %

60 / 50 discrimination result flag

0	60 field
1	50 field

Odd / even-numbered field discrimination result flag

0	Even-numbered field
1	Odd-numbered field

P-CTL signal control

0	Forward (rising edge)
1	Reverse (falling edge)

(Note) When switching the P-CTL edge, note that depending on the level of the P-CTL input, the number of 1s may not be counted correctly.

VP embedded signal generation flag

0	—
1	Embedded (TPG1-13)

VP signal generation flag

0	—
1	V – Sync

(Note) After <CSYNCF> and <TPGF> are read, they must be reset to "1". (reset)

Figure 3.8 (4)-5 Servo Input Circuit Related Registers

Servo Flag Control Register

SVCFREG (FFFEH)

	7	6	5	4	3	2	1	0
bit Symbol	VISFRS	VASFRS	TPFRS1	TPFRS0	CFGFRS	DPGFRS	CASFWR	CAFRS
Read/Write	R/W (Always "0" at read)							
Value after reset	0	0	0	0	0	0	0	0
Function	VISS Status Flag 0: – 1: Clear	VASS Status Flag 0: – 1: Clear	TPG1 FIFO Counter 0: – 1: Reset	TPG0 FIFO Counter 0: – 1: Reset	C-FG Malfunction Flag 0: – 1: Clear	D-PG Input Status Flag 0: – 1: Clear	Software Capture 0: – 1:Capture	Capture FIFO Counter 0: – 1: Reset

See 3.9, VISS / VASS Detector.

See 3.11, Capture Circuit.

D-PG input status flag clear

0	—
1	Clear

C-FG malfunction flag clear

0	—
1	Clear

TPG0 FIFO reset

0	—
1	Reset

TPG1 FIFO reset

0	—
1	Reset

(Note) After writing "1" to SVCFREG, set to "0". If read, "0" is always read.

Figure 3.8 (4)-6 Servo Input Circuit Related Registers

3.9 VISS / VASS Detector

The VISS / VASS detector enables the control coding method for the VHS system. The PCTL signal input from the P-CTL input circuit is used. The VISS / VASS detector consists of the duty discriminator, code detector, and 16-bit data register.

Figure 3.9 (1) shows the block diagram of the VISS / VASS detector.

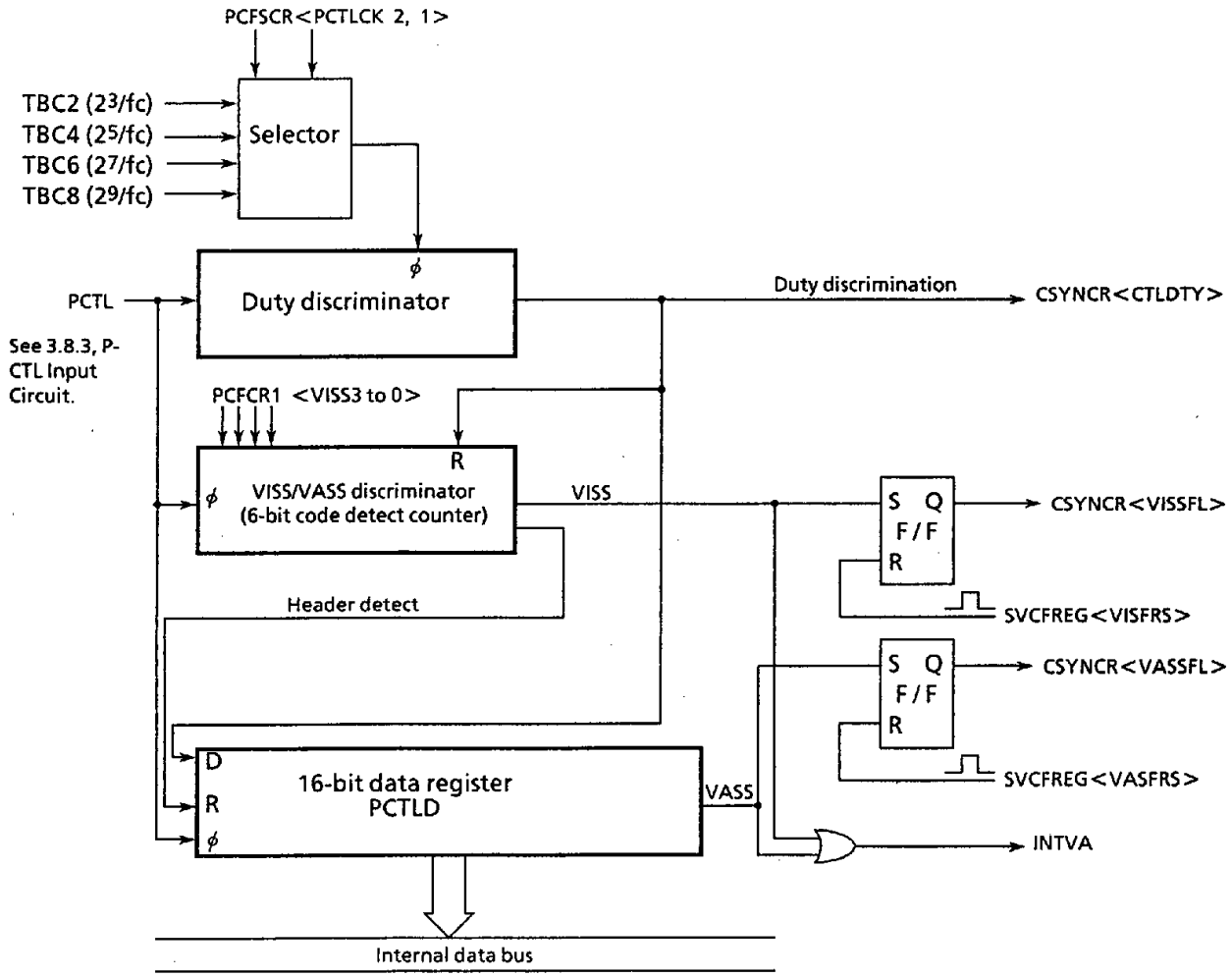


Figure 3.9 (1) Block Diagram of VISS / VASS Detector

3.9.1 Duty Discriminator

The duty discriminator consists of an up counter, a latch counter used to latch the upper 9 bits from the 10-bit up counter, a 9-bit comparator used to detect matches between the lower 9-bit data and the latch data, and the R-S flip / flop used to hold the match data.

Figure 3.9 (2) is a block diagram of the duty discriminator.

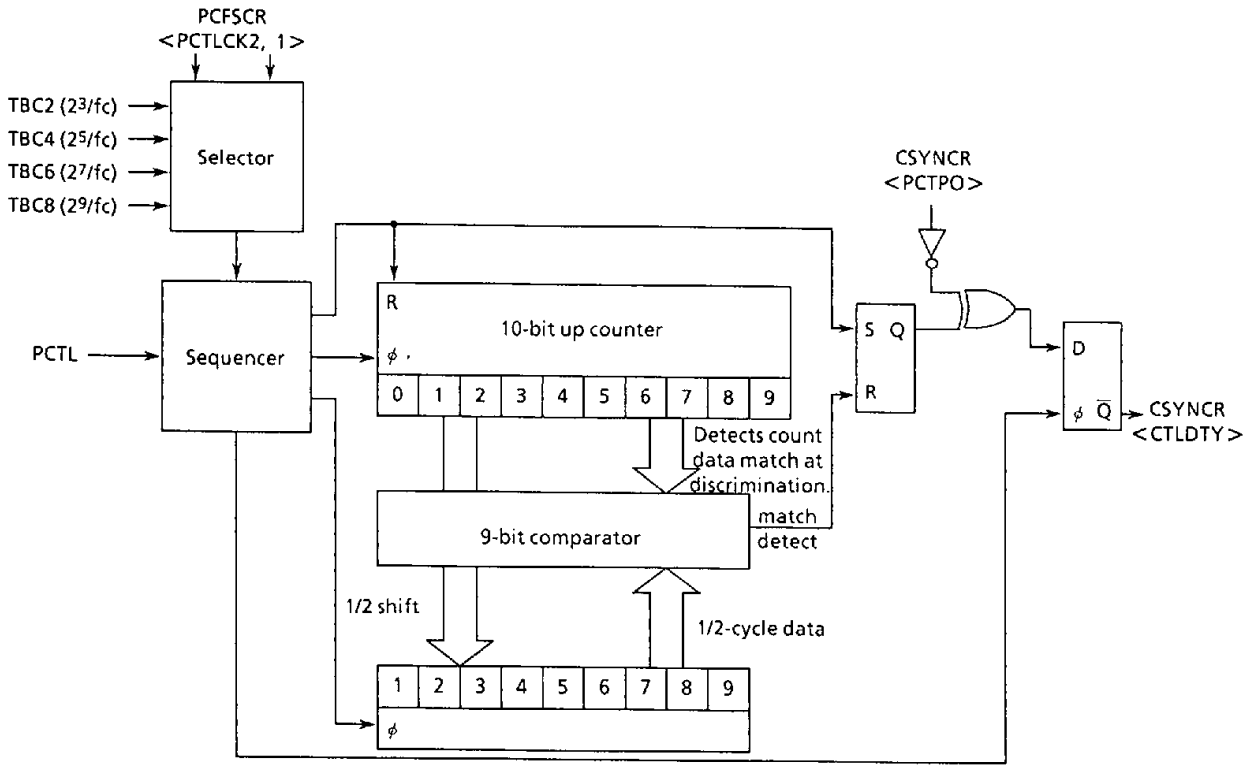


Figure 3.9 (2) Block Diagram of Duty Discriminator

The duty discriminator measures P-CTL signals input from the P-CTL input circuit and detects the duty width.

The VISS / VASS standards specify when the P-CTL signal duty is 60 %±5 %, pulse is "0"; when it is 27.5 %±2.5 %, pulse is "1". The duty discriminator discriminates the duty using these two ratios.

The duty discriminator discriminates the duty after measuring the P-CTL signal cycle, by discriminating the 1/2-cycle data of the measured cycle using the data of the next P-CTL signal cycle measured during high level. The 1/2 data of the P-CTL signal cycle can be obtained by shifting the measured cycle data 1 bit lower. At this time, the duty discrimination threshold value is 50%. The 9-bit comparator detects a match between the 1/2-cycle data of the previous cycle and the measured data and resets the R-S flip/flop using the detected data. The output data from the R-S flip / flop are sampled at the falling edge of the P-CTL input signal and the duty discrimination result is obtained.

Figure 3.9 (3) is the timing chart for duty discrimination.

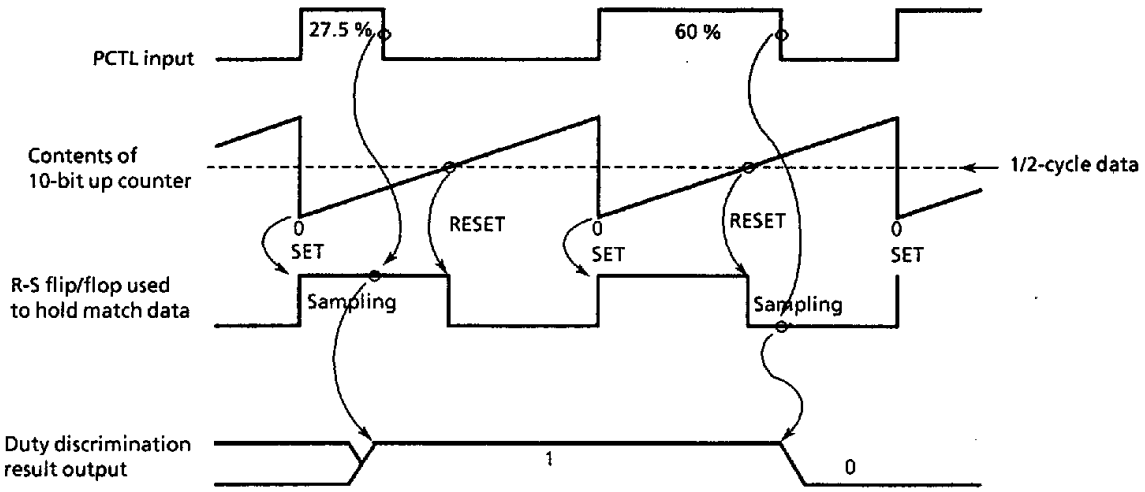


Figure 3.9 (3) Duty Discrimination Timing Chart

The duty discrimination result is saved to the duty discrimination flag register, CSYNCR<CTLDTY>. Referencing this register at the P-CTL edge detect timing (INTCAP interrupt generation) reads the duty discrimination result. The duty discrimination result must be read within the P-CTL input signal cycle (NTSC=30 Hz, PAL=25 Hz).

The duty discriminator supports a 10-bit up counter which enables the selection of one of four counter input clocks so that both VCR systems (NTSC and PAL) can be used. A counter input clock (TBC2, 4, 6, or 8) can be selected by the PCTL C-FG control register, PCFSCR<PCTLCK2,1>. The maximum frequency of the P-CTL input signal is 9 kHz (300 times standard playback mode) in FF/REW mode for NTSC; the minimum frequency is 25 Hz in standard playback mode for PAL. The duty discriminator can discriminate the duty of P-CTL signals input from 19.1 to 25 kHz.

Table 3.9 (1) lists P-CTL input cycles in relation to the duty discriminator input clocks and multipliers by NTSC and PAL.

Table 3.9 (1)

Input clock	PCFSCR <PCTLCK2, 1>	Frequency range (Hz)	Multipliers by NTSC and PAL (time)	
			NTSC	PAL
TBC2	0 0	1.22k to 25 k	41 to 834	49 to 1000
TBC4	0 1	305 to 6.25 k	10 to 208	12 to 250
TBC6	1 0	76.3 to 1.56 k	2.5 to 52	3 to 62
TBC8	1 1	19.1 to 391	0.6 to 13	0.8 to 15

(@ fc = 10 MHz)

Do not use as the P-CTL input signal a signal whose cycle is shorter than the minimum frequency specified in PCFSCR<PCFSCR2,1> for the duty discriminator.

3.9.2 VISS / VASS Discriminator

The VISS/VASS discriminator discriminates the result obtained by the duty discriminator as VISS or VASS code. It consists of a 6-bit detect counter and a 16-bit shift register.

An INTVA interrupt generated by the VISS/VASS discriminator is shared with VISS and VASS. The interrupt is identified by referencing the VISS / VASS detect flag register, CSYNCR<VISSFL, VASSFL> using the interrupt processing routine. Writing "1" to SVCFREG<VISFRS, VASFRS> clears CSYNCR<VISSFL, VASSFL>.

(1) Index search code detect (VISS: VHS Index Search System)

The index search code can be obtained when the 6-bit detect counter detects that the duty detect result is 61 ± 3 consecutive bits set to "1". With TMP91C642A, allowing for reduction of detect time and prevention of misoperation, the detect count value can be set to 4 to 60 (must be a multiple of 4) by software using four bits in the VISS discriminator control register, PCFCR1<VISS3 to 0> (bits 3 to 0 at address FFF0H in memory).

The 4-bit count value set in the VISS discriminator control register is compared with the upper 4 bits in the 6-bit code detect counter. When the data match (index search code is detected), the VISS detect flag, CSYNCR<VISSFL> (bit 1 at address FFEFH in memory) is set and an interrupt (INTVA) is generated.

Table 3.9 (2) lists settings of the VISS code detect counts by the VISS discriminator control register.

Table 3.9 (2) Settings of VISS Code Detect Counts

PCFCR1 <VISS3 to 0>				VISS code detect count value
3	2	1	0	
0	0	0	0	None
0	0	0	1	4
0	0	1	0	8
0	0	1	1	12
0	1	0	0	16
0	1	0	1	20
0	1	1	0	24
0	1	1	1	28
1	0	0	0	32
1	0	0	1	36
1	0	1	0	40
1	0	1	1	44
1	1	0	0	48
1	1	0	1	52
1	1	1	0	56
1	1	1	1	60

Figure 3.9 (4) shows index search code specifications in the VHS system.

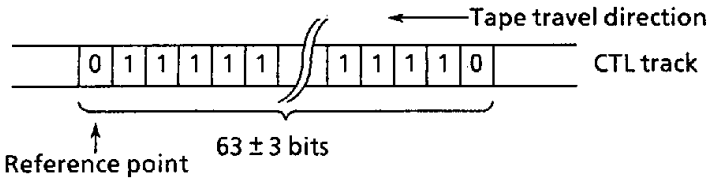


Figure 3.9 (4) Index Search Code Specifications in VHS System

According to the specifications for the index search code, both ends must be set to "0" and 61 ± 3 consecutive bits in between must be set to "1"; a total of 63 ± 3 bits must be set.

(2) Address code detect (VASS : VHS Address Search System)

Address code detect consists of header detect and address code detect.

To detect the header, the duty detect result is counted by the 6-bit detect counter. If the duty detect result starts with "0" followed by 9 consecutive bits set to "1", the header is detected.

To detect the address code, after acknowledging detection of the header, the 16 bits following the next "0" in the duty detect result are read into the 16-bit shift register as the address code. Then the VASS detect flag register, CSYNCR<VASSFL> is set, an INTVA interrupt is generated to inform the CPU of detection of the address code.

The CPU transfers the address code data in the 16-bit shift register to the RAM using the interrupt processing routine. One address code has four headers, thus four INTVA interrupts are generated. The fourth address data are insignificant; therefore, the data must be disabled by software. (If the same address data are detected at least twice, program so that the data are used as an address code.)

An INTVA interrupt is generated every 11 bits (header) + 16 bits (address data) = 27 bits. The frequency is 333 Hz in FF / REW mode (× 300 speed) in the fastest system, NTSC.

Figure 3.9 (5) shows address code specifications and VASS interrupt generation points in VHS.

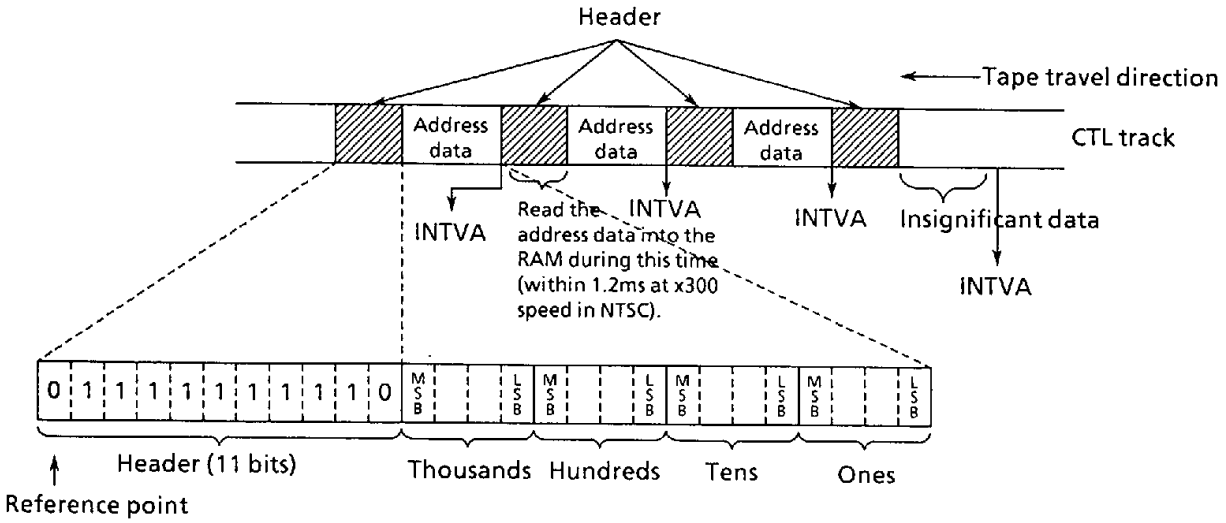
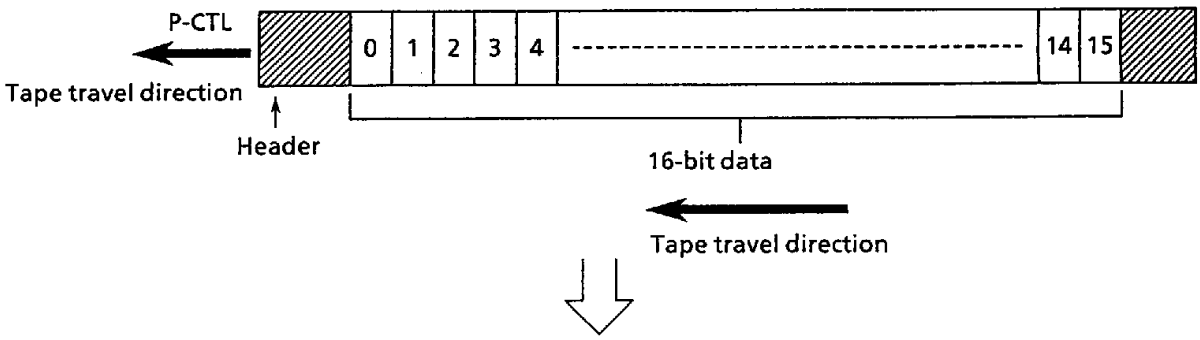


Figure 3.9 (5) Address Code Specifications and VASS Interrupt Generation Points in VHS

According to the specifications, write 4-bit BCD 4-digit data three times in between 11-bit headers.

Data are saved in the 16-bit shift register as shown below:

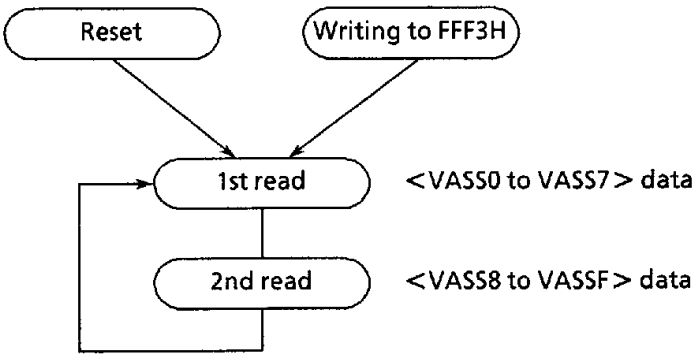


16-bit VASS data register PCTLD (address FFF3H in memory)

Register	VASS7	VASS6	VASS5	VASS4	VASS3	VASS2	VASS1	VASS0
Latch data	7	6	5	4	3	2	1	0

VASSF	VASSE	VASSD	VASSC	VASSB	VASSA	VASS9	VASS8
15	14	13	12	11	10	9	8

(Note) To read data from the 16-bit VASS data register, read from address FFF3H twice. Data read the first time are the values of <VASS0 to VASS7>. Data read the second time are the values of <VASS8 to VASSF>. If data are read again, the data read the first time are read again.
Note that the 16-bit load instruction cannot be used. Writing any data to address FFF3H specifies <VASS0 to VASS7>.



3.9.3 Control Registers

Figures 3.9 (6) show VISS / VASS detect circuit related registers.

P-CTL / C-FG Signal Control Register

		7	6	5	4	3	2	1	0
PCFSCR (FFF2H)	bit Symbol	DVS	PCTLCK2	PCTLCK1	CFGPR4	CFGPR3	CFGPR2	CFGPR1	CFGPR0
	Read/Write	W	W		W				
Prohibit read-modify-write.	Value after reset	0	0	0	0	0	0	0	0
	Function	SYNCDV Reg. Select 0: VPD, SYNC 1: FEP	PCTL Duty Detection Input Clock 00: TBC2 10: TBC6 01: TBC4 11: TBC8		C-FG Sbit Prescaler Control				

See 3.10, C-Sync Input Processing Circuit.

See 3.8, Servo Input Circuit.

PCTL duty measuring clock

00	TBC2 (2^3/fc)
01	TBC4 (2^5/fc)
10	TBC6 (2^7/fc)
11	TBC8 (2^9/fc)

Figure 3.9 (6)-1 VISS / VASS Detect Circuit Related Registers

C-FG Mask Time / VISS Discrimination Control Register

PCFCR1 (FFF0H)

Prohibit read-modify-write.

	7	6	5	4	3	2	1	0
bit Symbol	CFMSK3	CFMSK2	CFMSK1	CFMSK0	VISS3	VISS2	VISS1	VISS0
Read/Write	W				W			
Value after reset	0	0	0	0	0	0	0	0
Function	C-FG Mask Time Control				VISS discrimination control			

See 3.8, Servo Input Circuit.

VISS discriminator control register
(Note) For settings, see Table 3.9 (2).

16-bit VASS Data Register

PCTLD (FFF3H)

① ②

	7	6	5	4	3	2	1	0
bit Symbol	VASS7	VASS6	VASS5	VASS4	VASS3	VASS2	VASS1	VASS0
Read/Write	R							
Value after reset	0	0	0	0	0	0	0	0
Function	VASS Data Low Byte							

	7	6	5	4	3	2	1	0
bit Symbol	VASSF	VASSE	VASSD	VASSC	VASSB	VASSA	VASS9	VASS8
Read/Write	R							
Value after reset	0	0	0	0	0	0	0	0
Function	VASS Data High Byte							

Data read first time: values of <VASS0 to VASS7>
Data read second time: values of <VASS8 to VASSF>
Specification after reset: <VASS0 to VASS7>
Writing data to FFF3H specifies <VASS0 to VASS7>.

(Note) The 16-bit load instruction cannot be used.

Figure 3.9 (6)-2 VISS / VASS Detect Circuit Related Registers

C-Sync Control Register

CSYNCR (FFEFH)

Prohibit read-modify-write.

	7	6	5	4	3	2	1	0
bit Symbol	CSYNCF	TPGF	PCTPO	OEDR	NPS	CTLDTY	VISSFL	VASSFL
Read/Write	R/W	R/W	W	R	R	R	R	R
Value after reset	0	0	0	0	0	0	0	0
Function	V-Sync Detection Flag 1: V-Sync	Pseudo V Detect Flag 1: Embedded	PCTL Signal Control 0: Forward 1: Reverse	Odd/even discrimination result 0: Odd 1: Even	60/50 discrimination result 0: 60 1: 50	P-CTL Duty 0: ≦ 50 % 1: ≧ 50 %	VISS detect Flag 0: – 1: VISS data	VASS detect Flag 0: – 1: VASS data

See 3.8, Servo Input Circuit.
See 3.10, C-Sync Input Processing Circuit.

VASS detect flag

0	—
1	VASS data

VISS detect flag

0	—
1	VISS data

P-CTL duty discrimination result flag

0	Duty ≦ 50 %
1	Duty ≧ 50 %

Servo Flag Control Register

SVCFREG (FFFEH)

	7	6	5	4	3	2	1	0
bit Symbol	VISFRS	VASFRS	TPFRS1	TPFRS0	CFGFRS	DPGFRS	CASFWR	CAFRS
Read/Write	R/W (Always "0" at read)							
Value after reset	0	0	0	0	0	0	0	0
Function	VISS Status Flag 0: – 1: Clear	VASS Status Flag 0: – 1: Clear	TPG1 FIFO Counter 0: – 1: Reset	TPG0 FIFO Counter 0: – 1: Reset	C-FG Malfunction Flag 0: – 1: Clear	D-PG Input Status Flag 0: – 1: Clear	Software Capture 0: – 1: Capture	Capture FIFO Counter 0: – 1: Reset

See 3.8, Servo Input Circuit.
See 3.11, Capture Circuit.
See 3.12, Timing Pulse Generator.

VASS status flag clear

0	—
1	Clear

VISS status flag clear

0	—
1	Clear

(Note) After writing "1" to all the bits in SVCFREG, the bits are set to "0". Therefore, when reading, "0" is always read.

Figure 3.9 (6)-3 VISS / VASS Detect Circuit Related Registers

3.10 C-Sync (Composite Sync) Input Processing Circuit

The C-Sync input processing circuit consists of three functional blocks: a vertical sync (V-Sync) separator circuit, an odd/even field discriminator, and a 50 / 60 field discriminator.

0 V-5 V logical-level signals are obtained by amplifying and shaping, using the sense amp of the external circuit, the composite sync signals of TV and VCR video signals. These logical-level signals are used as the C-Sync input signal.

The V-Sync separator circuit is used to digitally separate the V-Sync signal from the C-Sync signal. The separated V-Sync signal is used as the reference signal for the servo during recording. To ensure stable operation when noise is mixed with the C-Sync signal in the weak electric field, a noise mask circuit is provided.

The odd/even field discriminator is used to discriminate between the odd and even fields of the C-Sync input signal. Using the discrimination result, the playback phase can be matched with the recording phase in units of frames (minimum units to display motion in TV broadcasting. NTSC uses 30 frames per second to display motion.)

The 60/50 field discriminator is used to measure the ratio of the frequencies of the V-Sync and H-Sync (horizontal sync) signals and discriminate whether the video signal type is NTSC or PAL.

(Note) High level input continuously to the C-Sync input port with the C-Sync input processing circuit enabled generates a VP interrupt (INTCAP). To avoid this, input either the C-Sync input signal or low level signal.

Figure 3.10 (1) is a block diagram of the C-Sync input processing circuit.

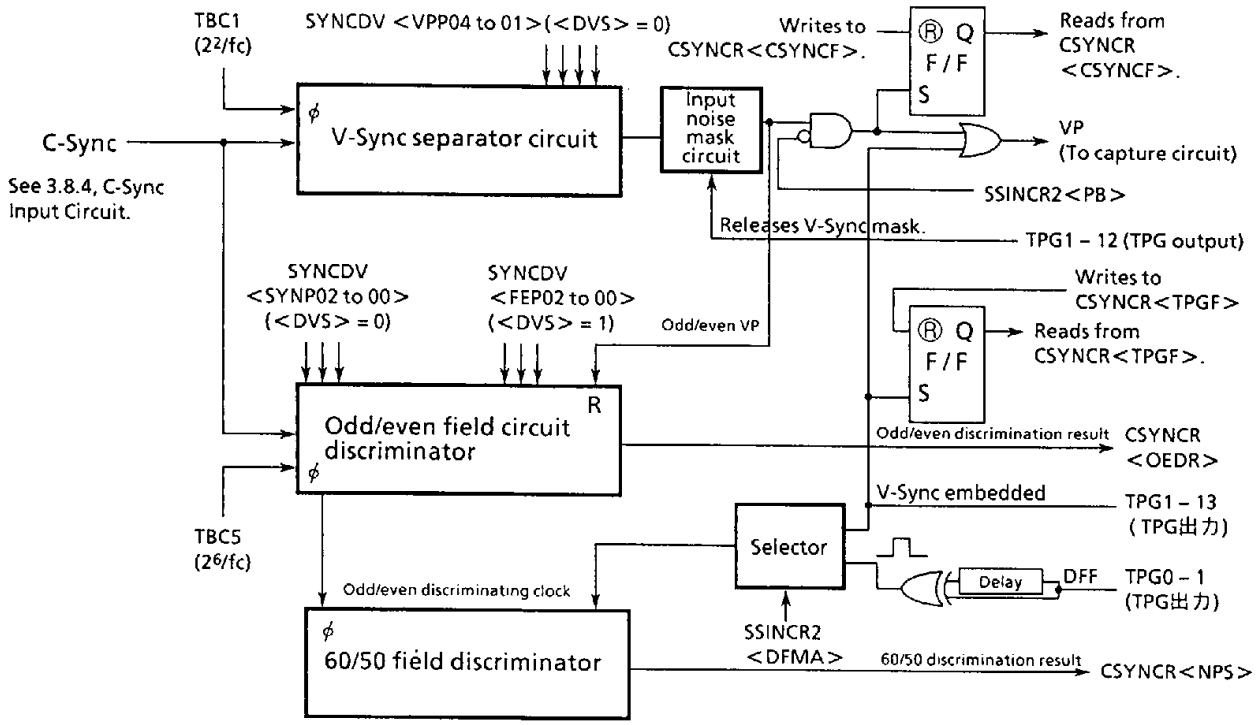


Figure 3.10 (1) Block Diagram of C-Sync Input Processing Circuit

3.10.1 V-Sync Separator Circuit

The V-Sync separator circuit is used to digitally separate the V-Sync signal (VP) from the C-Sync input signal.

The V-Sync separator circuit consists of a 7-bit up / down counter, a 4-bit C-Sync frequency divider control register, and a 4-bit comparator.

The 7-bit up / down counter uses TBC1(2^2/fc) as the input clock. The counter controls count direction (up or down) according to the input level of the C-Sync input signal. The counter is reset when a borrow is generated to the counter in down count mode. The reset input stops down counting.

The threshold value used to discriminate V-Sync signal is set in 4-bit C-Sync frequency divider control register, SYNCDV<VPP04 to 01>, (bits 3 to 0 at address FFCFH in memory, @ PCFSCR<DVS> = 0).

The 4-bit comparator generates a discrimination signal when the upper 4-bit count value of the 7-bit up/down counter exceeds the pre-set value (threshold value) of the 4-bit C-Sync frequency divider control register during up counting.

The discrimination signal output by the 4-bit comparator is output as VP via the input noise mask circuit controlled according to the TPG output (TPG1-12). To use VP, TPG output (TPG1-12) must be set to "1".

VP output by the V-Sync separator circuit is controlled according to the servo input control register, SSINCR2<PB>, (bit 1 at address FFFFH in memory). The register is set to output enable after reset is released.

VP output by the V-Sync separator circuit is used as the input signal for the capture circuit (see 3.11). Reading the C-Sync control register, CSYNCR<CSYNCF> (bit 7 at address FFEFH in memory), detects VP output generation. After the VP generation flag is read, it must be set to "1". The separated VP is used as a reference signal for the servo during recording.

Figure 3.10 (2) is a block diagram and Figure 3.10 (3) is the timing chart of VP discrimination.

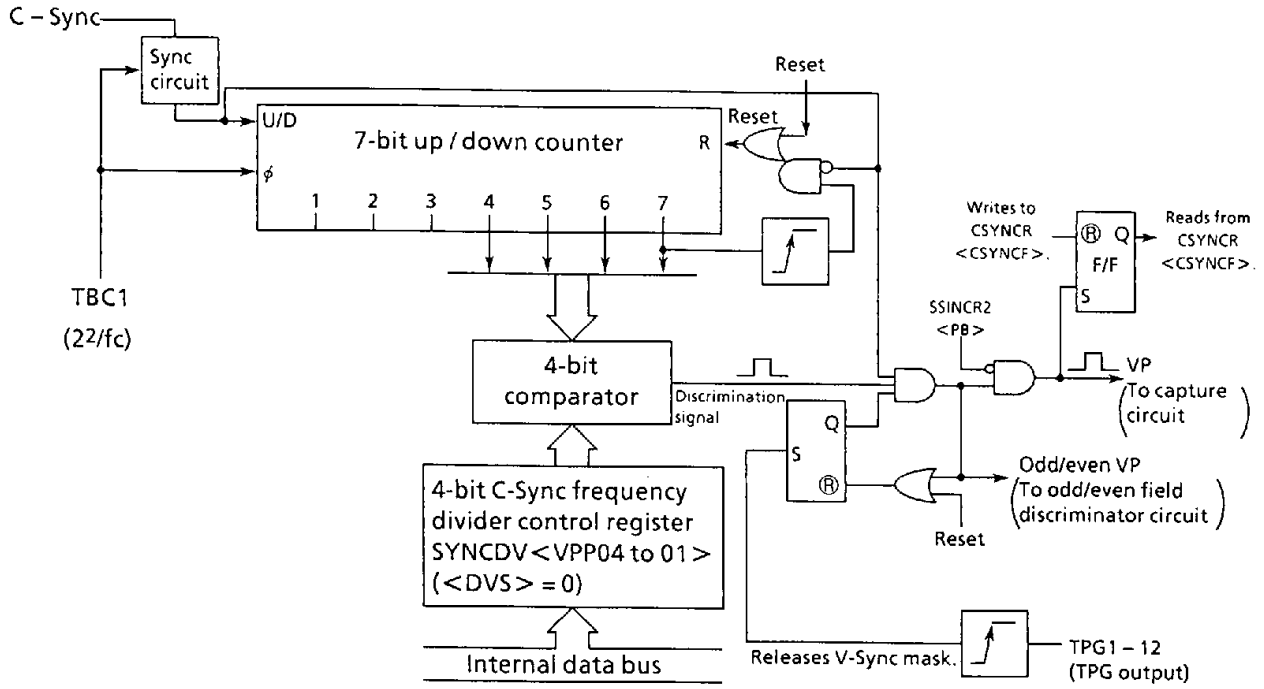


Figure 3.10 (2) V-Sync Separator Circuit

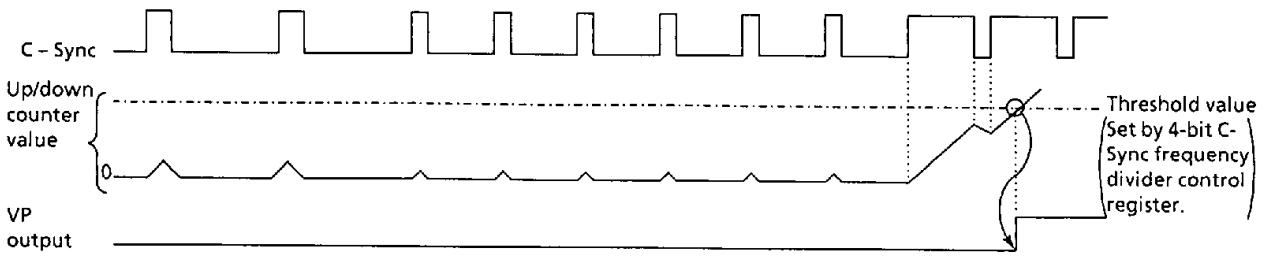


Figure 3.10 (3) VP Discrimination Timing Chart

Table 3.10 (1) lists settings of C-Sync frequency divider control register and total up count time until VP output generation.

Table 3.10 (1) VP Output Generating Time Setting

SYNCDV <VPP04 to 01> 04	03	02	01	n	VP output generating time (μs) @ 10 MHz	SYNCDV <VPP04 to 01> 04	03	02	01	n	VP output generating time (μs) @ 10 MHz
0	0	0	0	0	–	1	0	0	0	36	14.4
0	0	0	1	8	3.2	1	0	0	1	40	16.0
0	0	1	0	12	4.8	1	0	1	0	44	17.6
0	0	1	1	16	6.4	1	0	1	1	48	19.2
0	1	0	0	20	8.0	1	1	0	0	52	20.8
0	1	0	1	24	9.6	1	1	0	1	56	22.4
0	1	1	0	28	11.2	1	1	1	0	60	24.0
0	1	1	1	32	12.8	1	1	1	1	64	25.6

(Note) VP generating time means the total time of up-counting by the 7-bit up / down counter from reset to VP generation. When a reset is generated by down-counting, VP generating time means the total time of up-counting from the next up-counting.

3.10.2 Odd / Even Field Discriminator

The odd / even field discriminator is used to discriminate the odd and even fields of C-Sync input signal. By using the discrimination result, the playback phase can be matched with the recording phase in units of frames.

The odd/even field discriminator consists of a 3-bit counter used to mask the C-Sync signal for a fixed time, the mask control register, SYNCDV<SYNP02 to 00>, (bits 6 to 4 at address FFCFH in memory, @<DVS> = 0), and a 3-bit counter used to measure the fixed time from the V-Sync signal (odd/even VP), and register SYNCDV<FEP02 to 00> (bits 2 to 0 at address FFCFH in memory, @<DVS> = 1>.

Figure 3.10 (4) is a block diagram of the odd/even field discriminator.

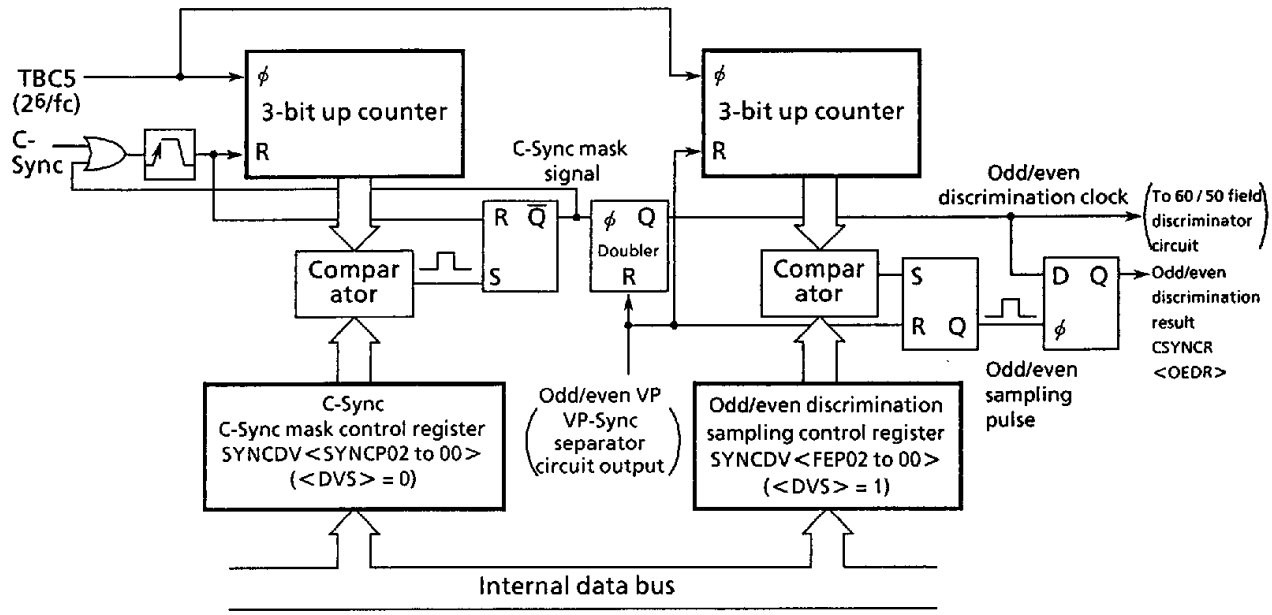


Figure 3.10 (4) Block Diagram of Odd/Even Field Discriminator

First, the odd / even field discriminator masks the C-Sync input signal for the time ($1/(2f_H)-1/f_H$; f_H is H-Sync frequency) set in the C-Sync mask control register, SYNCDV<SYNP02 to 00>. Then the discriminator generates an odd/even discriminating clock divided by 2.

To discriminate between odd and even fields, detects the signal level of the odd / even discriminating clock after the time set in the odd / even discrimination sampling control register, SYNCDV<FEP02 to 00>, elapses, starting from when VP falls (release of reset of 2-frequency divider).

The result of odd/even discrimination is confirmed by reading the C-Sync control register, CSYNCR<OEDR> (bit 4 at address FFEFH in memory).

Figure 3.10 (5) is the timing chart of odd/even field discrimination.

Table 3.10 (2) lists settings of the C-Sync mask control register and mask times. Table 3.10 (3) is the sample timing according to the odd/even discrimination sampling control register.

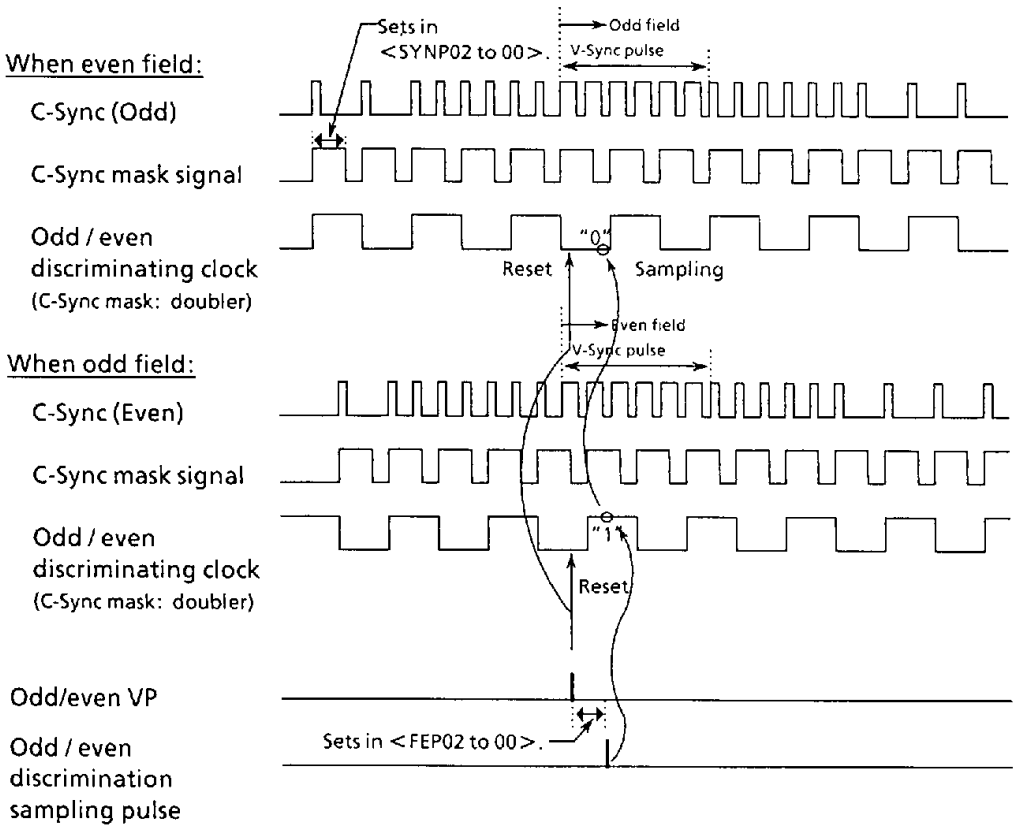


Figure 3.10 (5) Timing Chart of Even / Odd Field Discrimination

Table 3.10 (2) Setting of C-Sync Mask Control Register and Mask Time

SYNCDV <SYNP02 to 00> 02	01	00	n	Mask time (μs) @10 MHz
0	0	0	0	–
0	0	1	1	6.4
0	1	0	2	12.8
0	1	1	3	19.2
1	0	0	4	25.6
1	0	1	5	32.0
1	1	0	6	38.4
1	1	1	7	44.8

Mask Time = TBC5 × n (s)

Table 3.10 (3) Setting of Odd / Even Sampling Control Register and Odd / Even Discriminating Clock Sample Timing After Odd / Even VP Fall

SYNCDV <FEP02 to 00> 02	01	00	n	Sample timing (μs) @10 MHz
0	0	0	0	–
0	0	1	1	6.4
0	1	0	2	12.8
0	1	1	3	19.2
1	0	0	4	25.6
1	0	1	5	32.0
1	1	0	6	38.4
1	1	1	7	44.8

Sample Time = TBC5 × n (s)

3.10.3 60 / 50 Field Discriminator (NTSC/PAL discrimination)

The 60 / 50 field discriminator is used for recording/playback of different types of video signals (NTSC and PAL) using one VCR. Detecting the result of 60 / 50 field discrimination switches the system operating mode.

To discriminate between 60 and 50 fields, the discriminator counts the number of H-Sync signals within a V-Sync cycle.

Figure 3.10 (6) is a block diagram of the 60/50 field discriminator.

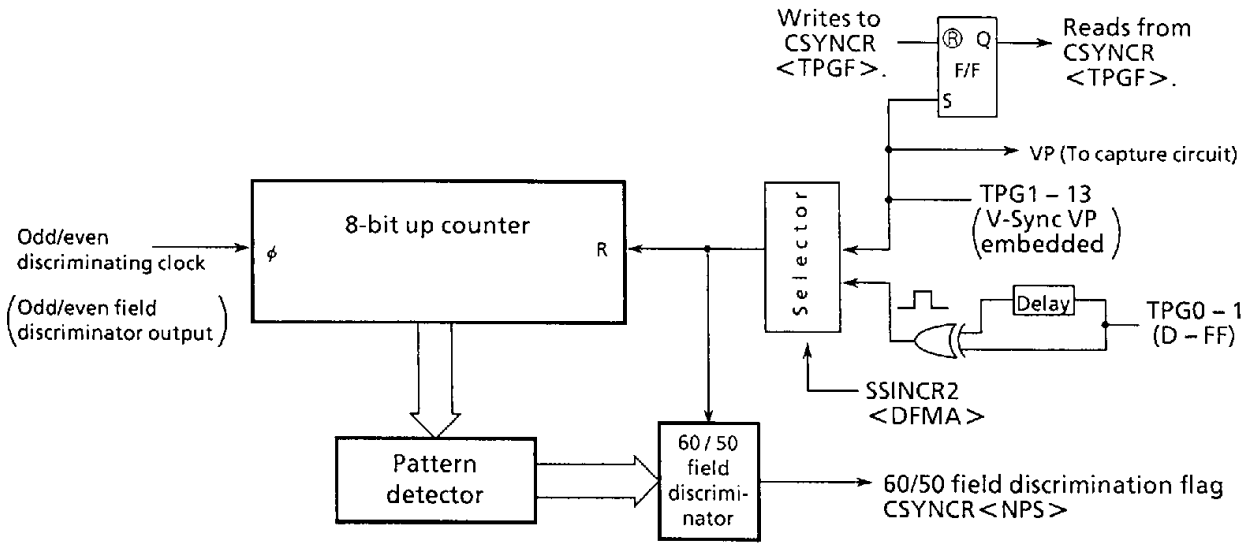


Figure 3.10 (6) Block Diagram of 60/50 Field Discriminator

The 60 / 50 field discriminator consists of an 8-bit up counter, a pattern detector, and a 60 / 50 discriminator.

An odd / even discriminating clock generated by the odd / even field discriminator is input to the 8-bit up counter. The counter value is reset by either the reset signal of TPG0-1 (D-FF) or TPG1-13 (VP embedded), using the servo input control register, SSINCR2<DFMA> (bit 2 at address FFFFH in memory). When discriminating between 60 and 50 fields, one counter reset is needed for one V-Sync cycle.

The pattern detector is used to detect and output the number of H-Sync signals per V-Sync cycle counted by the 8-bit up counter.

The 60/50 field discriminator detects the output detected by the pattern detector and sets the result in the C-Sync control register, CSYNCR<NPS> (bit 3 at address FFEFH in memory). If the quality of the C-Sync input signal is poor, output by the 60 / 50 discriminator may not be stable. In such a case, make sure that the state of 60 / 50 discriminator output is stable by software before processing.

Table 3.10 (4) lists V-Sync and H-Sync frequencies and H / V-Sync frequency ratios in NTSC and PAL.

Table 3.10 (4) V-Sync / H-Sync Frequencies and Their Ratios

	V-Sync frequency (Hz)	H-Sync frequency (Hz)	H/V-Sync frequency ratio
60 field type (NTSC)	59.94	15.734 k	262.5
50 field type (PAL)	50.00	15.625 k	312.5

The threshold value of 60 / 50 field discrimination is within the frequency ratio range of 262.5 to 312.5 listed in Table 3.10 (4).

If the quality of the C-Sync input signal is poor, instead of a V-Sync signal the 60 / 50 discriminator can use the embedded VP during recording and the D-FF (video head switching) signal during playback.

When the embedded VP is used, VP is generated and "1" is set in the embedded VP flag, CSYNCR<TPGF>. Reading the flag detects generation of the embedded VP. However, after the embedded VP flag is read, "1" must be set in the flag.

3.10.4 Control Registers

Figure 3.10 (7) shows C-Sync input circuit related registers.

P-CTL / C-FG Signal Control Register

PCFSCR (FFF2H)

Prohibit read-modify-write.

	7	6	5	4	3	2	1	0
bit Symbol	DVS	PCTLCK2	PCTLCK1	CFGPR4	CFGPR3	CFGPR2	CFGPR1	CFGPR0
Read/Write	W	W		W				
Value after reset	0	0	0	0	0	0	0	0
Function	SYNCDV Reg. Select 0: VPD.SYNC 1: FEP	PCTL Duty Detection Input Clock 00: TBC2 10: TBC6 01: TBC4 11: TBC8		C-FG 5bit Prescaler Control				

C-Sync control register select

See 3.8, Servo Input Circuit.

0	VPP0 / SYNP0 side (C-Sync input control register)
1	FEP0 side (odd / even discrimination control register)

(Note) See SYNCDV (address FFCFH in memory).

<DVS> = 0

C-Sync Input Control Register

SYNCDV (FFCFH)

Prohibit read-modify-write.

	7	6	5	4	3	2	1	0
bit Symbol		SYNP02	SYNP01	SYNP00	VPP04	VPP03	VPP02	VPP01
Read/Write		W			W			
Value after reset		0	0	0	0	0	0	0
Function		C-Sync mask control			C-Sync frequency divider control			

C-Sync mask control register
(Note) For settings, see Table 3.10 (2).

4-bit C-Sync frequency divider control register
(Note) For settings, see Table 3.10 (1).

<DVS> = 1

Odd/Even Discrimination Sampling Control Register

SYNCDV (FFCFH)

Prohibit read-modify-write.

	7	6	5	4	3	2	1	0
bit Symbol						FEP02	FEP01	FEP00
Read/Write						W		
Value after reset						0	0	0
Function						Even / Odd judgement		

Odd / even discrimination sampling control register.
(Note) For settings, see Table 3.10 (3).

(Note) To write data to a C-Sync control register, select the register using the C-Sync control register select bit, PCFSCR<DVS>. After reset, <DVS> = 0 and the C-Sync input control register is selected.

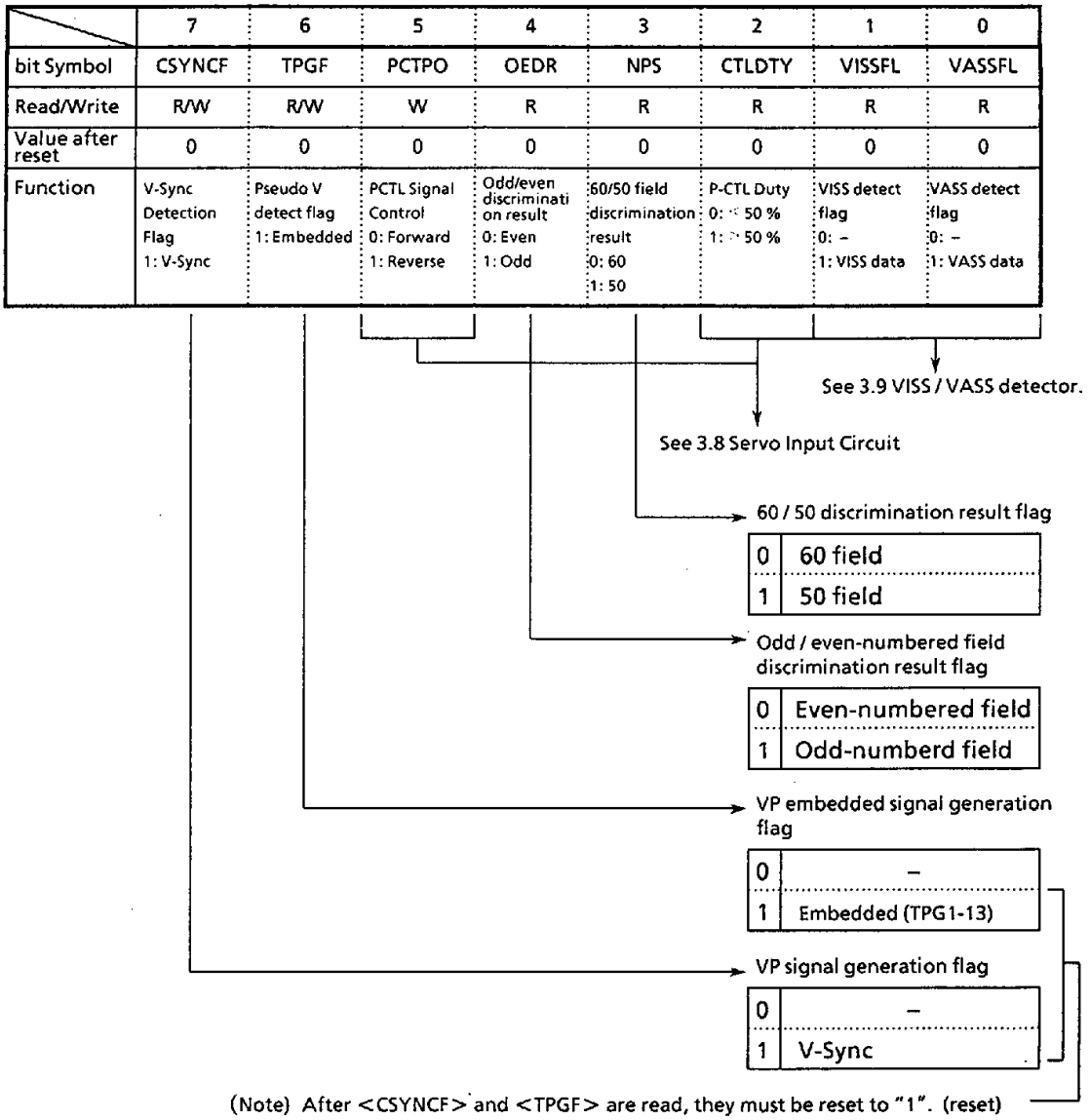
Figure 3.10 (7) C-Sync Input Circuit Related Registers

C-Sync Control Register

CSYNCR (FFEFH)

Prohibit read-modify-write.

	7	6	5	4	3	2	1	0
bit Symbol	CSYNCF	TPGF	PCTPO	OEDR	NPS	CTLDTY	VISSFL	VASSFL
Read/Write	R/W	R/W	W	R	R	R	R	R
Value after reset	0	0	0	0	0	0	0	0
Function	V-Sync Detection Flag 1: V-Sync	Pseudo V detect flag 1: Embedded	PCTL Signal Control 0: Forward 1: Reverse	Odd/even discrimination result 0: Even 1: Odd	60/50 field discrimination result 0: 60 1: 50	P-CTL Duty 0: < 50 % 1: > 50 %	VISS detect flag 0: – 1: VISS data	VASS detect flag 0: – 1: VASS data



(Note) After <CSYNCF> and <TPGF> are read, they must be reset to "1". (reset)

Figure 3.10 (7)-2 C-Sync Input Circuit Related Registers

Servo Input Control Register 2

SSINCR2 (FFFFH)

	7	6	5	4	3	2	1	0
bit Symbol					TP	DFMA	PB	CFGMCP
Read / Write					R/W	R/W	R/W	R
Value after reset					0	0	0	Undefined
Function					TPG0/TPG1 Reg. Control 0: TPG0 1: TPG1	Control of input signal for 60 / 50 field discrimination 0: TPG0-1 (D-FF) 1: TPG1-13 (V-Sync (VP) embedded)	V-Sync detector output control 0: Enable 1: Disable	CFG Malfunction Flag 0: — 1: Mal-function detect

See 3.12, Timing Pulse Generator.

See 3.8, Servo Input Circuit.

V-Sync detector output control register

0	Enable
1	Disable

Control of input signal for 60 / 50 field discrimination

0	TPG0-1 (D-FF (video head switching) signal)
1	TPG1-13 (V-Sync (VP) embedded)

Figure 3.10 (7)-3 C-Sync Input Circuit Related Registers

3.11 Capture Circuit

The capture circuit latches the contents (time data) of TBC1 to TBC18 and capture input status (input signal data) to a RAM using a 24-bit 8-step FIFO, using edge detect timing (see 3.8, Servo Input) for external input pulses from the servos.

The capture circuit latches data according to an input signal and generates an INTCAP interrupt (shared with TPG) to the CPU.

Using the capture circuit facilitates high precision time measuring necessary for servo control.

Figure 3.11 (1) is the block diagram of the capture circuit.

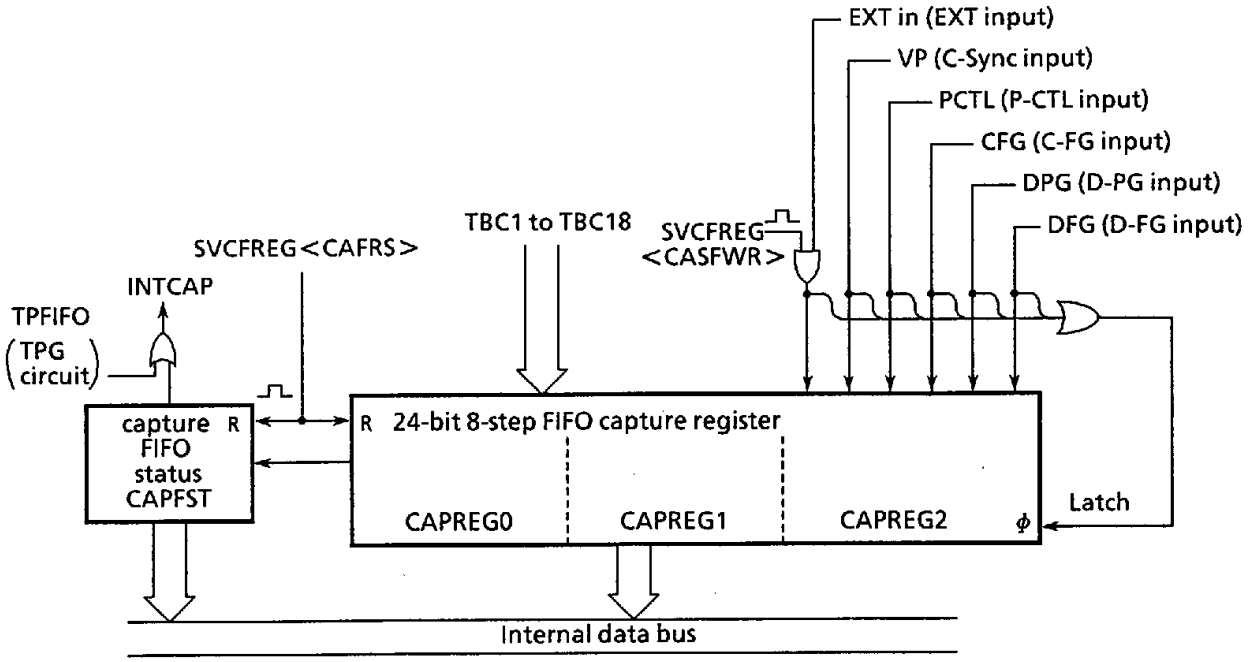


Figure 3.11 (1) Capture Circuit Block Diagram

3.11.1 Operation

(1) Capture

The capture circuit has the following six input sources: CAP0 (D-FG), CAP1 (D-PG), CAP2 (C-FG), CAP3 (P-CTL), EXT external input signal, and V-Sync (VP) signal separated from C-Sync signal. At the input signal edge, the capture circuit latches to the 3 bytes at addresses FFFAH to FFFCH (see 3.8, Servo Input Circuit) a total of 24 bits: 18-bit time base counter (TBC1 to TBC18) value and 6-bit input signal data. Setting servo flag control register SVCFREG (address FFFEH in memory) <CASFWR> to "1" performs latching. (Software capture saves the captured data as capture input status data for EXT input.)

These 24-bit data can be obtained by reading data from addresses FFFAH, FFFBH, then FFFCH in this order. *

(Note)* Reading data from address FFFCH shifts the FIFO address. Thus, data at address FFFCH must be read last.

(2) Capture FIFO status register

The capture circuit uses a FIFO to enable the first-latched time data to be read first. The capture FIFO status register, CAPFST, (address FFFDH in memory) indicates the internal status of the FIFO. The bit in the register corresponding to where 8-step FIFO data are stored is set to "1". If 8-step FIFO data are full, capture according to input signals are disabled. At this time, the capture FIFO status register indicates "FFH".

When the FIFO status register is "00H", reading the capture data reads "FFH". To read capture data, perform read when The FIFO status register is other than "0" or after an INTCAP interrupt is generated.

(3) CAP reset

The capture circuit has a software reset as well as a system reset.

Writing "1" to servo flag control register SVCFREG<CAFRS> (bit 0 at address FFFEH in memory) resets the following circuits:

① FIFO address counter

② FIFO status

(4) Capture interrupt

An INTCAP interrupt is generated by latching at the input signal edge. INTCAP interrupts are generated until the FIFO status becomes "0" (no data).

When an INTCAP interrupt is generated, check the interrupt source by reading the capture input status register, CAPREG2 (bits 7 to 2 at address FFFCH in memory).

Check whether data are in the FIFO, then read data in CAPREG0, 1, and 2 to RAM. Unless data are read, the FIFO may overflow.

Process interrupts using the interrupt processing according to the status of the capture input.

To clear the INTCAP interrupt, either read data from CAPFST until no data are left or write "1" to <CAFRS>.

(5) Data processing

The upper 6 bits of the 24-bit data at addresses FFFAH to FFFCH are latched according to an input signal representing the capture input status. The bit corresponding to the input signal is set to "1", therefore referencing the bit identifies the input signal.

The CPU saves the latched data to internal RAM. When the CPU detects the input signal next time, it can measure the rotation speed of the capstan motor or drum motor by subtracting the previous data in RAM from the last latched data. The detect precision is 200 ns (@ fc = 10 MHz) and quantization error is extremely low.

3.11.2 Control Registers

Figure 3.11 (2) shows the capture circut related register.

Capture FIFO Status Register

CAPFST (FFFDH)

	7	6	5	4	3	2	1	0
bit Symbol	CAPF7	CAPF6	CAPF5	CAPF4	CAPF3	CAPF2	CAPF1	CAPF0
Read/Write	R							
Value after reset	0	0	0	0	0	0	0	0
Function	0: No data					1: Data		

Capture FIFO status

Capture Data 0 Register

CAPREG0 (FFFAH)

	7	6	5	4	3	2	1	0
bit Symbol	CAPD7	CAPD6	CAPD5	CAPD4	CAPD3	CAPD2	CAPD1	CAPD0
Read/Write	R							
Value after reset	Undefined							
Function	Capture Data Low Byte							

Lower 8-bit capture data

Capture Data 1 Register

CAPREG1 (FFFBH)

	7	6	5	4	3	2	1	0
bit Symbol	CAPD15	CAPD14	CAPD13	CAPD12	CAPD11	CAPD10	CAPD9	CAPD8
Read/Write	R							
Value after reset	Undefined							
Function	Capture Data Middle Byte							

Middle 8-bit capture data

Capture Data 2 Register

CAPREG2 (FFFCH)

	7	6	5	4	3	2	1	0
bit Symbol	EXT	P-CTL	D-PG	C-SYNC	C-FG	D-FG	CAPD17	CAPD16
Read/Write	R						R	
Value after reset	Undefined						Undefined	
Function	Capture Input Status						Capture Data High Byte	

Capture input status

Upper 2-bit capture data

(Note) To read 3-byte capture data, read CAPREG2 last.

Figure 3.11 (2)-1 Capture Related Register

Servo Flag Control Register

SVCFREG (FFFEH)

	7	6	5	4	3	2	1	0
bit Symbol	VISFRS	VASFRS	TPFRS1	TPFRS0	CFGFRS	DPGFRS	CASFWR	CAFRS
Read/Write	R/W (Always "0" at read)							
Value after reset	0	0	0	0	0	0	0	0
Function	VISS Status Flag 0: - 1: Clear	VASS Status Flag 0: - 1: Clear	TPG1 FIF0 Counter 0: - 1: Reset	TPG0 FIF0 Counter 0: - 1: Reset	C-FG Malfunction Flag 0: - 1: Clear	D-PG input Status Flag 0: - 1: Clear	Software Capture 0: - 1: Capture	Capture FIF0 Counter 0: - 1: Reset

Capture FIFO reset

0	—
1	Reset

Software capture signal

0	—
1	Sofrware capture write

Software capture saves the captured data as capture input status data for EXT input.

D-PG input status flag clear

0	—
1	Clear

C-FG malfunction flag clear

0	—
1	Clear

TPG0 FIFO reset

0	—
1	Reset

TPG1 FIFO reset

0	—
1	Reset

VISS status flag clear

0	—
1	Clear

VASS status flag clear

0	—
1	Clear

(Note) After writing "1" to all the bits in SVCFREG, the bits are set to "0". Therefore, when reading data, "0" is always read.

Figure 3.11 (2)-2 Capture Related Registers

3.12 Timing Pulse Generator (TPG)

The following timing pulses are required for controlling VCR mechanisms.

- Rotating head switch signals (image head switch signal: D-FF and Hi-Fi head switch signal: A-FF (audio flip / flop))
- Pseudo vertical sync signal (pseudo V)
- Control recording signal
- Capstan motor on/off, positive direction control

Timing pulses are classified into signals synchronized with the servo reference signal (TBC) and signals synchronized with the D-PG signal indicating the phase of the rotating head.

The TMP91C642A combines a two-channel timing pulse generation circuit with a 32-bit 8-step FIFO to control signals and mechanical components and to facilitate generation of two types of asynchronous timing pulses.

The timing pulse generator (TPG) generates a 16-bit timing pulse synchronized with the time base counter (TBC) at a precision of 400 ns (@fc = 10 MHz). The upper 16 bits of the internal 32-bit FIFO, TPC0DAR1 and TPC0DAR0 (TPC1DAR1 and TPC1DAR0) are compared with 16-bit TBC2 to TBC17 data by the comparator. When a match is detected, the lower 16 bits of the 32-bit FIFO, TPO0DAR1 and TPO0DAR0 (TPO1DAR1 and TPO1DAR0) are latched. The latched data are generated as internal control signals (TPG0-12 to 15 and TPG1-12 to 15) or external data (TPG0-0 to 11 and TPG1-0 to 11) output directly from the port. The signal output directly from the port is OR-ed with the data registers of ports 0, 1, and 2. When outputting the contents of the TPG data register to the ports, set the control register of the ports to be used to output mode and write "0" to the data registers of the OR-ed ports. When ports 0, 1, and 2 are shared by TPG output and general-purpose port output, always write "0" to the output data register of the port used for TPG.

TPG0 is a circuit used to generate a pulse in sync with the D-PG signal. To synchronize the pulse with the D-PG signal, the capture circuit must be used and software must be used for processing. Eight bits <TPO07 to 00> out of the 16-bit TPG0 output buffer latch data can be directly output to port 0 as TPG0-7 to 0. <TPO0F> can control, as internal signal TPG0-15, the tri-state of P00. Four bits <TPO0B to 08> can be directly output to port 1 as TPG0-11 to 8 by switching TPG1 output. (<TPO0E> can control as internal signal TPG0-14 the 3-state of P10. <TPO0D> of the remaining 2 bits can generate, as internal signal TPG0-13, the INTTB signal (also used as TBC interrupt). (Write "0" in <TPO0C>. Internal signal TPG0-12 cannot be used.)

TPG1 is a circuit which generates a pulse synchronized with the reference signal (TBC output). Eight bits <TPO17 to 10> out of the 16-bit TPG1 output buffer latch data can be directly output to port 2 as TPG1-7 to 0. <TPO1F> can control, as internal signal TPG1-15, the 3-state of P20. Four bits <TPO1B to 18> can be directly output to port 1 as TPG1-11 to 8 by switching TPG0 output.

<TPO1E> can control, as internal signal TPG1-14 ,the 3-state of P10. <TPO1C> of the remaining 2 bits, as internal signal TPG1-12, is used as the mask function release signal for the V-Sync signal. <TPO1D> of the remaining 2 bits, as internal signal TPG1-13, is used as the V-Sync embedded signal (sync correction signal at special playback).

When using an INTTB interrupt (TPG0-13) for the TPG, do not share the interrupt with the TBC. (Note that if the INTTB interrupt is shared with the TBC, interrupt timing may be incorrect.)

Figure 3.12 (1) is the block diagram of the timing pulse generating circuit.

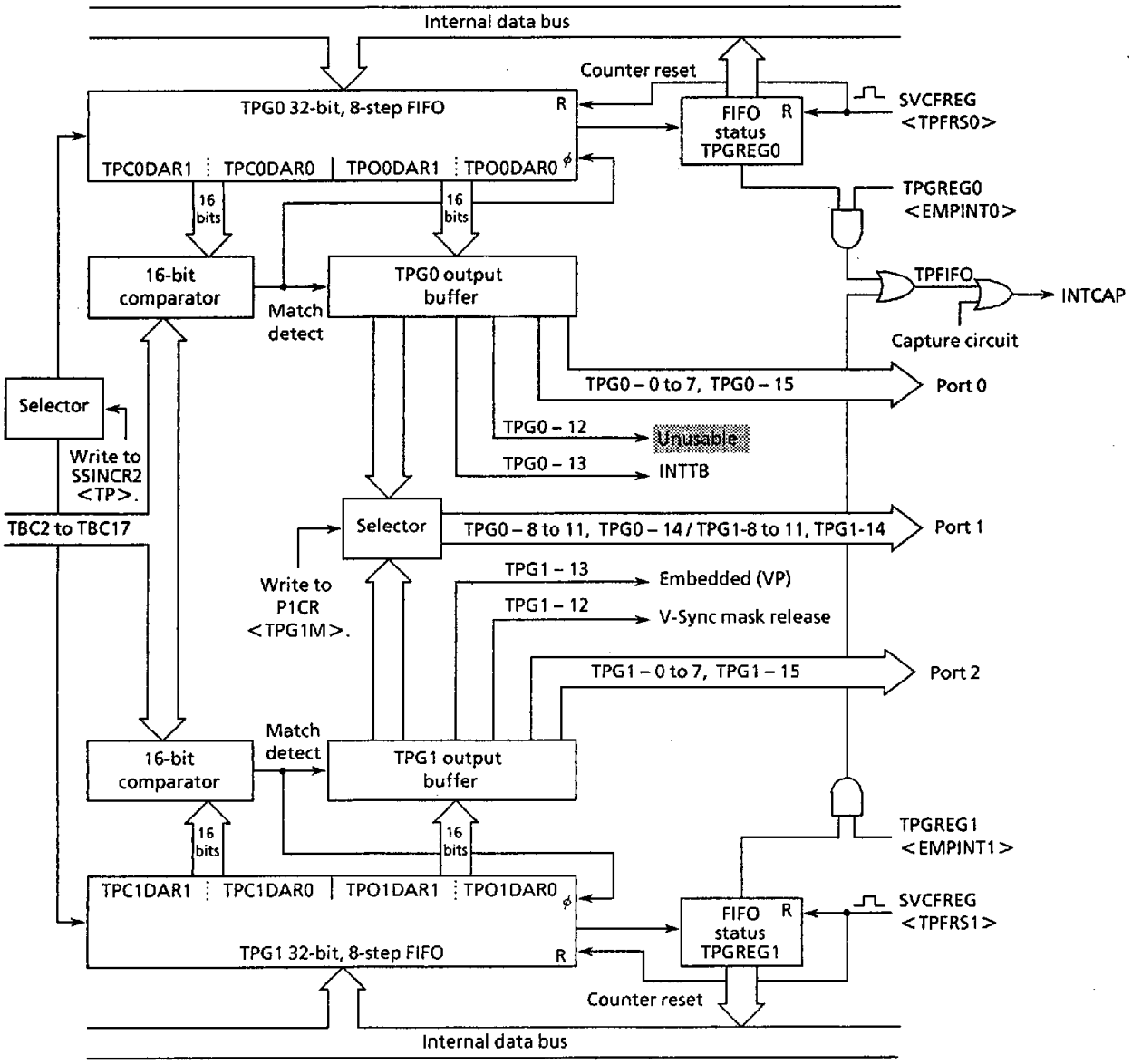


Figure 3.12 (1) Timing Pulse Generating Circuit Block Diagram

Table 3.12 (1) below shows TPG outputs and port connections, and port functions.

Table 3.12 (1) TPG Outputs and Ports

TPG No.	Output port / function		TPG No.	Output port / function	
TPG0 – 0	Port 0	P00 (PV / PH)	TPG1 – 0	Port 2	P20 (REC CTL)
1		P01 (D-FF)	1		P21
2		P02	2		P22
3		P03	3		P23
4		P04	4		P24
5		P05	5		P25
6		P06	6		P26
7		P07	7		P27
8	Port 1	P10	8	Port 1	P10
9		P11	9		P11
10		P12	10		P12
11		P13	11		P13
12	Unusable		12	C-Sync	V-Sync mask release
13	TBC	INTTB interrupt	13		V-Sync (VP) embedded
14	Port 1	P10 (3-state control signal)	14	Port 1	P10 (3-state control signal)
15	Port 0	P00 (3-state control signal)	15	Port 2	P20 (3-state control signal)

3.12.1 Operation

(1) Data Register

TPG Supports a 32-bit 8-step FIFO consisting of 16-bit output data register TPO0DAR0 / TPO0DAR1 (addresses FFF4H and FFF5H in memory) and a 16-bit comparator data register TPC0DAR0/TPC0DAR1 (addresses FFF6H and FFF7H in memory). Data registers TPG0 and TPG1 are set to the same address. To switch between TPG0 and TPG1, servo signal control register SSINCR2<TP> (bit 3 at FFFFH in memory) is used.*

When the comparator register value and the TBC2 to TBC17 value match, the value in the output data register is output. If there is no indication of the next TPG output data (output data and capture data) to the FIFO, the CPU needs to specify the next TPG data to the FIFO. When the TPG comparate data which is the time until the next TPG data is output is smaller than the value set by the CPU, the TPG data is not output at the specified timing because the TBC value is greater than that of the comparate data register. The specified TPG data is output at the timing of TBC after competing one cycle. Consequently, the TPG data must be specified as if the timing data (comparate register value) becomes longer than the CPU processing time.

(Note) * When SSINCR2<TP> is set to "0", TPG0 channel data are written; when set to "1", TPG1 channel data are written. Immediately after reset, <TP> = 0 and TPG0 is selected.

Writing data to address FFF7H increments the FIFO address. Therefore, write data in the following order: FFF4H, FFF5H, FFF6H, and FFF7H.

(2) FIFO

TPG has an 8-step FIFO for TPG0 and TPG1.

The interrupt signal is not generated immediately after reset or software TPG reset. After data are written to the data register, the FIFO is incremented, the contents of the output data register are output, the FIFO is empty, and an INTCAP interrupt is generated. The INTCAP interrupt is shared with the capture circuit.

Reading TPG status register TPGREG0,1<TPEMP0,1> using the INTCAP interrupt processing identifies the interrupt source. The interrupt request flip / flop can be cleared by writing data to the TPG FIFO.

(3) FIFO status

FIFO status registers TPGREG0 <TPF02 to 00> and TPGREG1 <TPF12 to 10> shows the status of the FIFOs. They can reference 3-bit status flag and full / empty signal in the FIFOs. Setting TPGREG0, 1 <EMPINT0, 1> controls an INTCAP interrupt when an empty signal is generated.

(4) TP reset

Servo flag control register SVCFREG<TPFRS1,0> (bits 4 and 5 at FFFEH in memory) is used to reset the TPG. Writing "1" to this register resets the following TPG1 and TPG0 circuits.

① FIFO address counter
② FIFO status
③ Empty interrupt flag

(Note) The 16-bit TPG output buffer is not reset. Thus, the value before the TP reset is maintained. All bits are cleared to "0" only by system reset.

3.12.2 Control Registers

Figure 3.12 (2) shows the TPG related register.

TPG0 Status Register

		7	6	5	4	3	2	1	0
TPGREG0 (FFF8H)	bit Symbol			EMPINT0	TPFUL0	TPEMP0	TPF02	TPF01	TPF00
	Read/Write			W	R	R	R		
Prohibit read-modify-write.	Value after reset			0	0	1	0	0	0
	Function			TPG0 Data Empty Interrupt Control Reg. 0: Disable 1: Enable	TPG0 Data Full Flag 0: – 1: Full	TPG0 Data Empty Flag 0: – 1: Empty	TPG0 FIFO Status Flag. 000 empty/full 001 1 data item 010 2 data items 011 3 data items 100 4 data items 101 5 data items 110 6 data items 111 7 data items When <TPEMP0> is "1" and 000, empty. When <TPFUL0> is "1" and 000, full.		

TPG0 FIFO status

000	Empty/full	100	4 data items
001	1 data item	101	5 data items
010	2 data items	110	6 data items
011	3 data items	111	7 data items

When <TPEMP0> is "1" and 000, empty.
When <TPFUL0> is "1" and 000, full.

TPG0 data empty flag

0	—
1	Empty

TPG0 data full flag

0	—
1	Full

TPG0 data empty interrupt control

0	Disable
1	Enable

For TPG0 reset, see Figure 3.8 (4)-6, Servo Input Circuit Related Register.

Figure 3.12 (2)-1 TPG Related Registers

TPG1 Status Register

		7	6	5	4	3	2	1	0
TPGREG1 (FFF9H)	bit Symbol			EMPINT1	TPFUL1	TPEMP1	TPF12	TPF11	TPF10
	Read/Write			W	R	R	R		
Prohibit read-modify-write.	Value after reset			0	0	1	0	0	0
	Function			TPG1 Data Empty Interrupt Control Reg. 0: Disable 1: Enable	TPG1 Data Full Flag 0: – 1: Full	TPG1 Data Empty Flag 0: – 1: Empty	TPG1 FIFO Status Flag. 000 empty/full 001 1 data item 010 2 data items 011 3 data items 100 4 data items 101 5 data items 110 6 data items 111 7 data items When <TPEMP1> is "1" and 000, empty. When <TPFUL1> is "1" and 000, full.		

TPG0FIFO status

000	Empty/full	100	4 data items
001	1 data item	101	5 data items
010	2 data items	110	6 data items
011	3 data items	111	7 data items

When <TPEMP1> is "1" and 000, empty.
When <TPFUL1> is "1" and 000, full.

TPG1 data empty flag

0	—
1	Empty

TPG1 data full flag

0	—
1	Full

TPG1 data empty interrupt control

0	Disable
1	Enable

For TPG1 reset, see Figure 3.8 (4)-6, Servo Input Circuit Related Register.

Figure 3.12 (2)-2 TPG Related Registers

TPG0 output data register / comparate data register

① When Servo flag control register SSINCR2<TP> (bit 3 at FFFFH in memory) is set to "0":

TPG0 Output Data Register (lower 8 bits)

		7	6	5	4	3	2	1	0
TPO0DAR0 (FFF4H)	bit Symbol	TPO07	TPO06	TPO05	TPO04	TPO02	TPO01	TPO0	TPO00
	Read/Write	W							
Prohibit read-modify-write.	Value after reset	Undefined							
	Function	TPG0-0 to TPG0-7 output data register							

TPG0 Output Data Register (upper 8 bits)

		7	6	5	4	3	2	1	0
TPO0DAR1 (FFF5H)	bit Symbol	TPO0F	TPO0E	TPO0D	TPO0C	TPO0B	TPO0A	TPO09	TPO08
	Read/Write	W							
Prohibit read-modify-write.	Value after reset	Undefined							
	Function	TPG0-8 to TPG0-15 output data register							

TPG0 Comparate Data Register (lower 8 bits)

		7	6	5	4	3	2	1	0
TPC0DAR0 (FFF6H)	bit Symbol	TPC07	TPC06	TPC05	TPC04	TPC03	TPC02	TPC01	TPC00
	Read/Write	W							
Prohibit read-modify-write.	Value after reset	Undefined							
	Function	TPG0-0 to TPG0-7 comparate data register							

TPG0 Comparate Data Register (upper 8 bits)

		7	6	5	4	3	2	1	0
TPC0DAR1 (FFF7H)	bit Symbol	TPC0F	TPC0E	TPC0D	TPC0C	TPC0B	TPC0A	TPC09	TPC08
	Read/Write	W							
Prohibit read-modify-write.	Value after reset	Undefined							
	Function	TPG0-8 to TPG0-15 comparate data register							

* After writing data to TPC0DAR1 (FFF7H), the FIFO address is incremented.

For selection of TPG0 or TPG1, see Figure 3.8 (4)-4, Servo Input Circuit Related Register.

Figure 3.12 (2)-3 TPG Related Registers

TPG1 output data register / comparate data register

② When Servo flag control register SSINCR2<TP> (bit 3 at FFFFH in memory) is set to "1":

TPG1 Output Data Register (lower 8 bits)

		7	6	5	4	3	2	1	0
TPO1DAR0 (FFF4H)	bit Symbol	TPO17	TPO16	TPO15	TPO14	TPO13	TPO12	TPO11	TPO10
	Read/Write	W							
Prohibit read-modify-write.	Value after reset	Undefined							
	Function	TPG1-0 to TPG1-7 output data register							

TPG1 Output Data Register (upper 8 bits)

		7	6	5	4	3	2	1	0
TPO1DAR1 (FFF5H)	bit Symbol	TPO1F	TPO1E	TPO1D	TPO1C	TPO1B	TPO1A	TPO19	TPO18
	Read/Write	W							
Prohibit read-modify-write.	Value after reset	Undefined							
	Function	TPG1-8 to TPG1-15 output data register							

TPG1 Comparate Data Register (lower 8 bits)

		7	6	5	4	3	2	1	0
TPC1DAR0 (FFF6H)	bit Symbol	TPC17	TPC16	TPC15	TPC14	TPC13	TPC12	TPC11	TPC10
	Read/Write	W							
Prohibit read-modify-write.	Value after reset	Undefined							
	Function	TPG1-0 to TPG1-7 comparate data register							

TPG1 Comparate Data Register (upper 8 bits)

		7	6	5	4	3	2	1	0
TPC1DAR1 (FFF7H)	bit Symbol	TPC1F	TPC1E	TPC1D	TPC1C	TPC1B	TPC1A	TPC19	TPC18
	Read/Write	W							
Prohibit read-modify-write.	Value after reset	Undefined							
	Function	TPG1-8 to TPG1-15 comparate data register							

* After writing data to TPC1DAR1 (FFF7H), the FIFO address is incremented.

For selection of TPG0 or TPG1, see Figure 3.8 (4)-4, Servo Input Circuit Related Register.

Figure 3.12 (2)-4 TPG Related Registers

3.13 PWM Circuit

TMP91C642A incorporates three channels of pulse width modulation (PWM) output circuits. Two channels consist of 12 bits; one channel consists of 8 bits. Connecting a low pass filter externally obtains D/A conversion output and facilitates motor control.

3.13.1 12-bit PWM Circuits (PW0, PW1)

12-bit PWM circuits (PW0 and PW1) are configured for use in controlling the drum and capstan motors. PW0 and PW1 both have a dedicated open-drain output pin for independent operation.

(1) Configuration

12-bit PWM circuits consist of a 12-bit PWM data register, PWM fundamental wave generator, and 1-bit weight circuit. Start and stop of PWM is controlled by timer control register TRUM<RUNPW1,0>.

7-bit data latch for PWM fundamental wave, 7-bit comparator, and output flip / flop.

1-bit weight circuit consists of a 5-bit data latch for weight, size comparator, and 1-bit weight pulse circuit.

Figure 3.13 (1) is a block diagram of PW0/PW1.

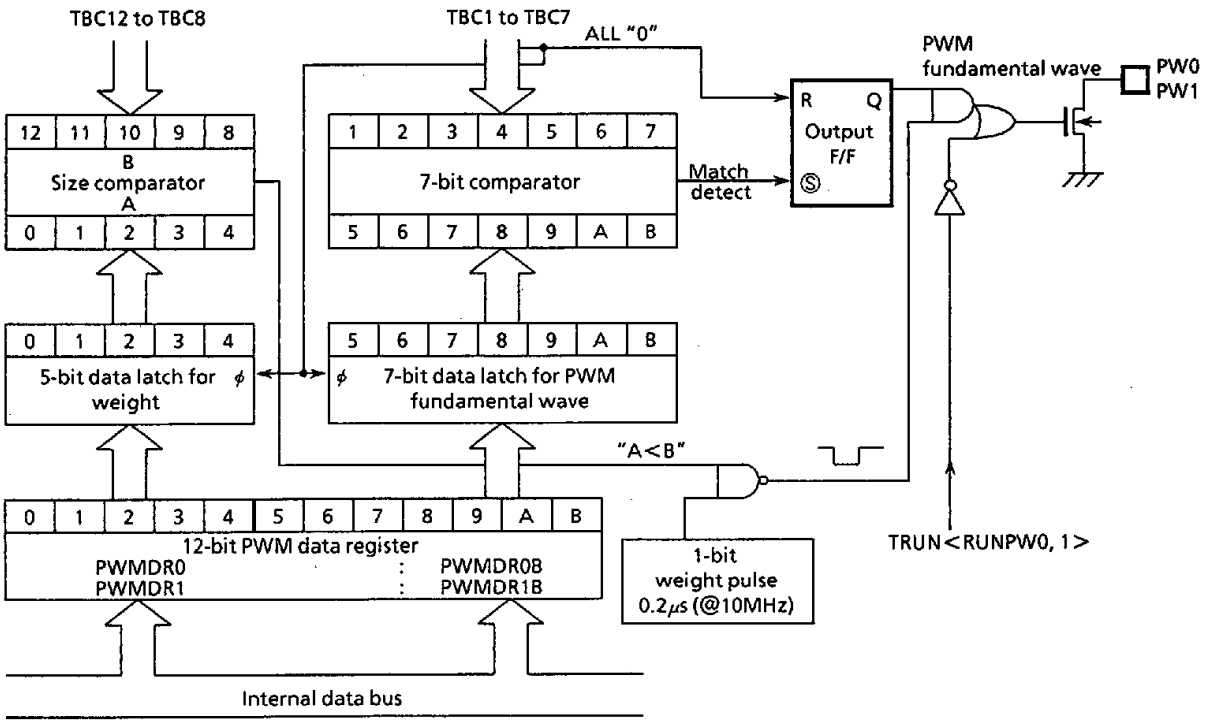


Figure 3.13 (1) PW0/PW1 Block Diagram

(2) Operation

The 12-bit PWM circuit generates a fundamental PWM wave using the upper 7 bits of data in the 12-bit PWM data register set in the 7-bit data latch for PWM fundamental wave. Then the circuit adds a pulse equivalent to the 1-bit PWM fundamental wave using the lower 5 bits of data set in the 5-bit data latch for weight, and generates PW0/PW1 output wave.

The PWM fundamental wave (PWM carrier wave) cycle is the TBC7 cycle (25.6 μs / 39.062 kHz @ fc = 10 MHz).

The PWM fundamental wave duty is determined by the upper 7 bits in the 12-bit PWM data register. The duration of high level for PW0/PW1 output (the pin is set to high impedance due to open-drain output) is determined by the value of the upper 7 bits.

The lower 5-bit data in the 12-bit PWM data is used to determine whether to add a weight pulse (0.2 μs @ fc = 10 MHz) to the PWM fundamental wave. Weight pulses are added at random positions to reduce the frequency spectrum for the 12-bit PWM output. (Output voltage fluctuations caused by the external low-pass filter are decreased.)

Even if the PWM basic pulse output is set to low level (setting 0 to the upper 7-bit of the 12-bit PWM data register), the weighted pulse is generated by setting the lower 5 bit of 12-bit PWM data register.

One cycle, T_M, of the 12-bit PWM output is 2^{12}/(fc/2)[s](819.2 μs @ 10 MHz). The PWM carrier wave cycle, T_S, is T_M/32 [s]. When the upper 7 bits of data in the 12-bit PWM data register are n(n = 0 to 127), the high-level pulse width in the T_S cycle is n*t(t = 1/(fc/2)). (t = 0.2 μs @ 10 MHz).

The lower 5 bits of data in the 12-bit PWM data register control additional pulses of width t (t = 0.2 μs @ 10 MHz) during T_M/32[s], T_S(0) to T_S(31). In the 32 T_S, when the additional pulses are output, the high-level pulse width becomes (n + 1)*t.

The data must not be written to the 12-bit PWM data register during TBC clearing (TBMOD <TBCCLR> = 1).

Figure 3.13 (2) is the operation timing chart of the PWM circuit.

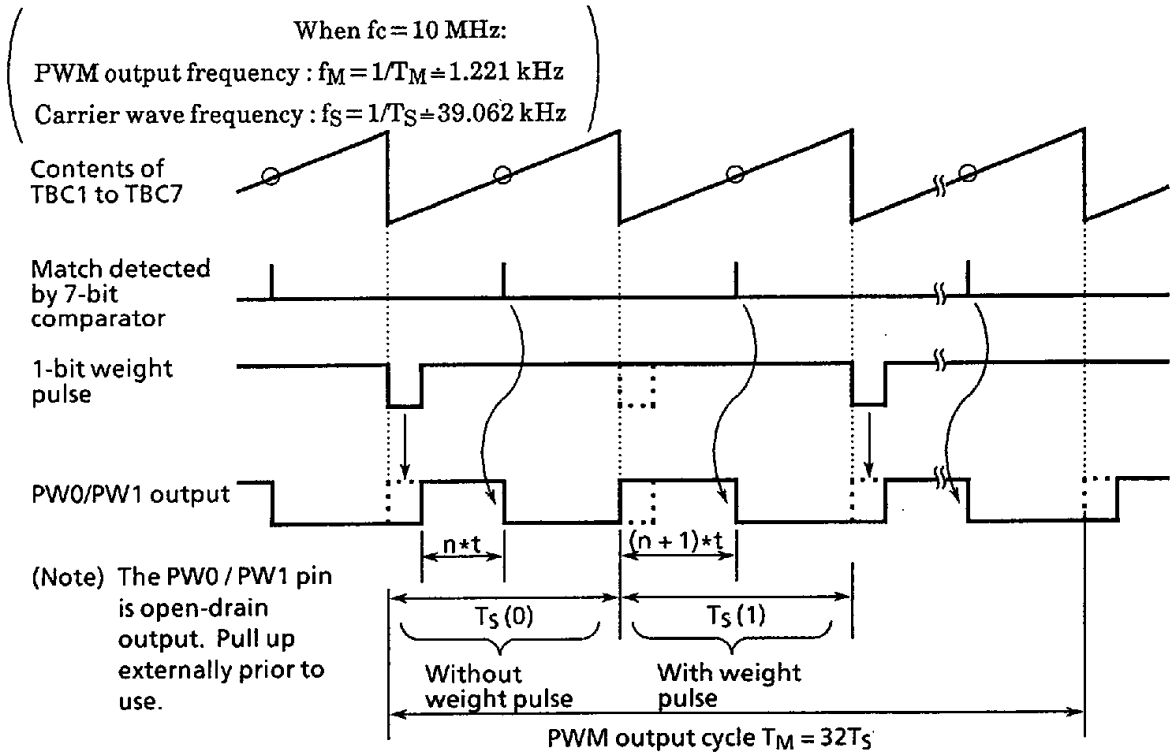


Figure 3.13 (2) 12-bit PWM Circuit Operating Timing Chart

3.13.2 8-bit PWM Circuit (PWM8)

The 8-bit PWM circuit (PWM8) is configured for use in controlling the current limiter of the motor driver. PWM8 has a resolution of 8 bits.

(1) Configuration

PWM8 consists of an 8-bit up counter, an 8-bit data register, an 8-bit comparator, and an output flip / flop circuit.

Figure 3.13 (3) is a block diagram of PWM8.

To output the PWM8 function to the port (P37), set TFFCR<TOSEL> and P3CR<P37M> to "0".

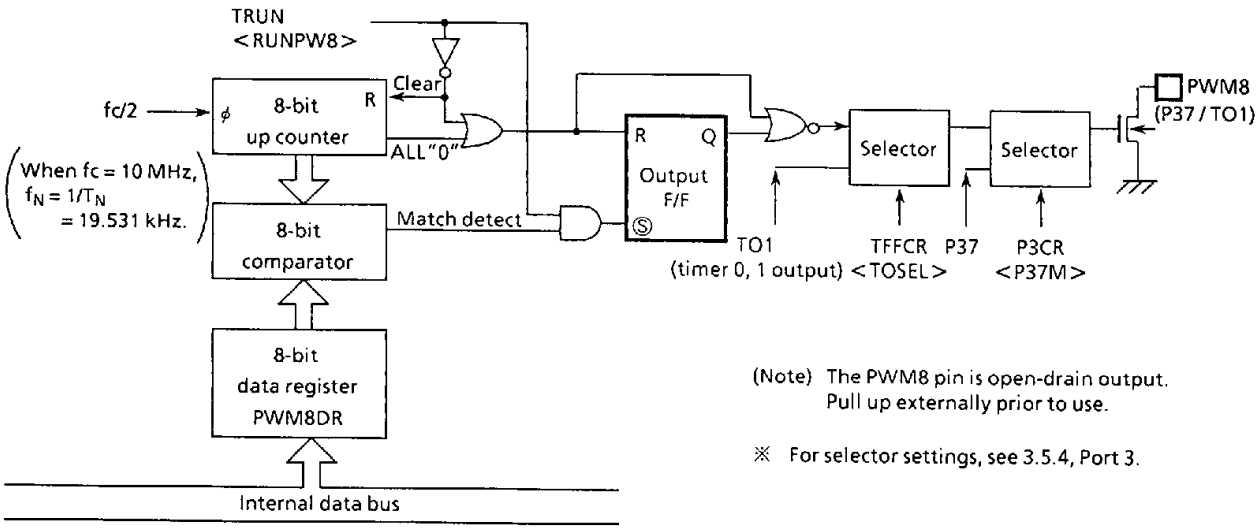


Figure 3.13 (3) PWM8 Block Diagram

(2) Operation

PWM8 is a low pulse control type 8-bit PWM circuit which controls the low pulse output duration using data set in the data register.

After reset is released, TFFCR<TOSEL> and P3CR<P37M> are set to "0". Thus, writing "1" to timer control register TRUN<RUNPW8> immediately activates P37 for PWM8 output. When all the 8-bit counter values become "0", the output flip/flop is reset and PWM8 output becomes "0". When the 8-bit up counter starts counting from the initial value, "0", and detects a match detect signal output by the comparator, the output flip/flop is set and PWM8 output is inverted.

When "0" is set in 8-bit data register PWM8DR, the output flip / flop is set to "1". PWM8/P37 output becomes high impedance. (P37 is open-drain output.)

One cycle T_N is 2^8/(fc/2)[s] (51.2 μs @ 10 MHz). When data are n (n=0 to 255), the low level pulse width in cycle T_N is n*to (to=1/(fc/2)).

3.13.3 Control Registers

The PWM circuit is controlled by control register TRUN and five data registers. For PWM8 output control, see 3.5.4, Port 3.

Figures 3.13 (4) show PWM related registers.

Timer Control Register

TRUN (FFDAH)

	7	6	5	4	3	2	1	0
bit Symbol		RUNPW1	RUNPW0	RUNPW8	T3RUN	T2RUN	T1RUN	T0RUN
Read/Write		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value after reset		0	0	0	0	0	0	0
Function		PW0, 1 Run/Stop Control 0 : Stop 1 : Run (Count up)		PWM8 Run / Stop Control 0 : Stop& Clear 1 : Run (Count up)	Timer Run / Stop Control 0 : Stop 1 : Run		Timer Run / Stop Control 0 : Stop & Clear 1 : Run (Count up)	

See 3.14, Timers.

PWM8 operation

0	Stop and clear
1	Count

PW0 (PWM12-0) operation

0	Stop and clear
1	Count

PW1 (PWM12-1) operation

0	Stop and clear
1	Count

PWM8 Data Register

PWM8DR (FFDBH)

Prohibit read-modify-write.

	7	6	5	4	3	2	1	0
bit Symbol	PW8D7	PW8D6	PW8D5	PW8D4	PW8D3	PW8D2	PW8D1	PW8D0
Read/Write	W							
Value after reset	Undefined							

PWM8 data register

Figure 3.13 (4)-1 PWM Related Registers

PW0 Data Register

		7	6	5	4	3	2	1	0
PWMDR0 (FFDCH)	bit Symbol	PWD07	PWD06	PWD05	PWD04	PWD03	PWD02	PWD01	PWD00
	Read/Write	W							
Prohibit read-modify-write.	Value after reset	Undefined							

PW0 data register (lower 8 bits)

PW0 Data Register B

		7	6	5	4	3	2	1	0
PWMDR0B (FFDDH)	bit Symbol					PWD0B	PWD0A	PWD09	PWD08
	Read/Write	W							
Prohibit read-modify-write.	Value after reset	Undefined							

PW0 data register (upper 4 bits)

PW1 Data Register

		7	6	5	4	3	2	1	0
PWMDR1 (FFDEH)	bit Symbol	PWD17	PWD16	PWD15	PWD14	PWD13	PWD12	PWD11	PWD10
	Read/Write	W							
Prohibit read-modify-write.	Value after reset	Undefined							

PW1 data register (lower 8 bits)

PW1 Data Register B

		7	6	5	4	3	2	1	0
PWMDR1B (FFDFH)	bit Symbol					PWD1B	PWD1A	PWD19	PWD18
	Read/Write	W							
Prohibit read-modify-write.	Value after reset	Undefined							

PW1 data register (upper 4 bits)

The data must not be written to the 12-bit PWM data register during TBC clearing (TBMOD <TBCCLR> = 1).

Figure 3.13 (4)-2 PWM Related Registers

3.14 Timers

The TMP91C642A integrates four 8-bit timer / counters: timers 0, 1, 2, and 3.

The four 8-bit timer / counters can be independently operated. Cascade-connecting timers 0 and 1 configures a 16-bit timer / counter.

Either the 18-bit time base counter (see 3.6, Time Base Counter), output clock signal, or external input signal (TI0, TI1, P66/C-FG, or P67/P-CTL) can be selected as an input clock source.

3.14.1 Configuration

Each timer consists of an 8-bit up counter (except timer 3, which is an up / down counter), an 8-bit comparator, and an 8-bit timer register. A timer flip / flop (TFF) is provided for a pair of timers 0 and 1.

8-bit timer operation and timer flip / flop are controlled by five control registers: TCLK (TMR01CR), TRUN, TFFCR, TMR2CR, and TMR3CR.

The configuration and functions of 8-bit timers are as explained below:

(1) Up counter

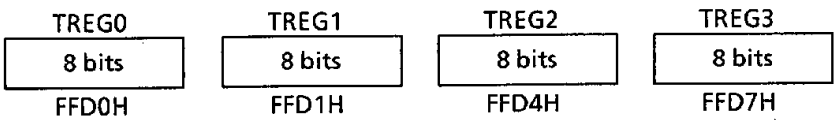
Timers 0 or 1 each has an 8-bit binary counter controlled by control register TMR01CR (TCLK) ; timer 2 has an 8-bit binary counter controller by control register TMR2CR; timer 3, an up/down counter, has an 8-bit binary counter controller by control register TMR3CR.

Timer 1 input clock is selected depending on operating mode. If the 16-bit timer mode is set (TCLK<TMOD> = 1), the overflow output of timer 0 is used as the input clock regardless of the <T1CLK0,1> setting.

At reset, TCLK<TMOD> = 0, that is, 8-bit timer mode is set.

The up counters can control count/stop for each timer using timer operation control register TRUN. At reset, all the up counters are cleared and timers are stopped.

(2) Timer registers



(Note) Write only.

The timer registers consist of 8 bits and set the interval time. When the values set in the timer register and the up counter match, the match detect signal of the comparator becomes active. When the value is set to 00H, the match detect signal becomes active at up counter overflow. When a new value is written to this register, it is input immediately to the comparator.

(3) Comparator

The comparator compares the up counter value with the value set in the timer register and if they match, the comparator zero-clears the up counter and generates an interrupt signal (INTT0 to 3). If timer flip / flop inversion is enabled, the comparator inverts the timer flip/flop value at the same time.

(4) Timer flip / flop (timer F/F)

The timer flip / flop inverts according to the match detect signals (output by the comparator) of timers 0 and 1, and outputs the value to timer output pin TO1 (also used as P37).

A timer flip / flop (TFF) is provided for timers 0 and 1, but not for 2 and 3.
The timer flip / flop is controlled by timer flip / flop control register TFFCR.
TFF (timer F/F for timers 0 and 1) is explained below: (See Figure 3.14 (5)-4.)

① TFFCR<TFFIS> is a select bit for the TFF inversion signal. In 8-bit timer mode, to invert the TFF by a match signal from timer 0, set <TFFIS> to "0"; to invert the TFF by a match signal from timer 1, set <TFFIS> to "1".
In 16-bit mode, always set <TFFIS> to "1". At reset, <TFFIS> is cleared to "0".

② TFFCR<TFFIE> is the inversion enable bit for the TFF. Setting the TFFCR<TFFIE> to "1" enables inversion; setting to "0" disables.
At reset, the TFFCR<TFFIE> is cleared to "0".

③ TFFCR<TFFC1,0> sets / resets the TFF or inverts the TFF by software. Writing "0,0" resets the TFF; writing "0,1" sets the TFF; writing "1,0" inverts the TFF value.

Timers 0, 1, 2, and 3 are as explained below.

3.14.2 8-bit Timers 0 and 1

The timer counters for timers 0 and 1 of the TMP91C642A consist of an 8-bit up counter, an 8-bit timer register, and an 8-bit comparator circuit. These timer counters can be independently operated. Cascade-connecting them configures a 16-bit timer counter.

The input clocks to the timer counters are obtained from time base counters TBC2, TBC6, or TBC10. Timer 0 is connected to external input pin TI0.

A timer counter is cleared when timer start control register TRUN<T1RUN, T0RUN>="0" or when a match signal of the 8-bit comparator is output.

The contents of timers 0 and 1 are read from the count data registers TCUT0 and TCUT1 for these timers. (The timer count data register is set to the same address as timers 0 and 1 register.) When timer operation control register TRUN<T1RUN, T0RUN>="0", the up counter is cleared to "0"; therefore, the read data are always "00H".

Figure 3.14 (1) is the block diagram of timers 0 and 1.

When the timer mode is switched from 8-bit to 16-bit or from 16-bit to 8-bit, the TRUN<T1RUN, T0RUN> must be set to "0, 0", and the timer counter is cleared.

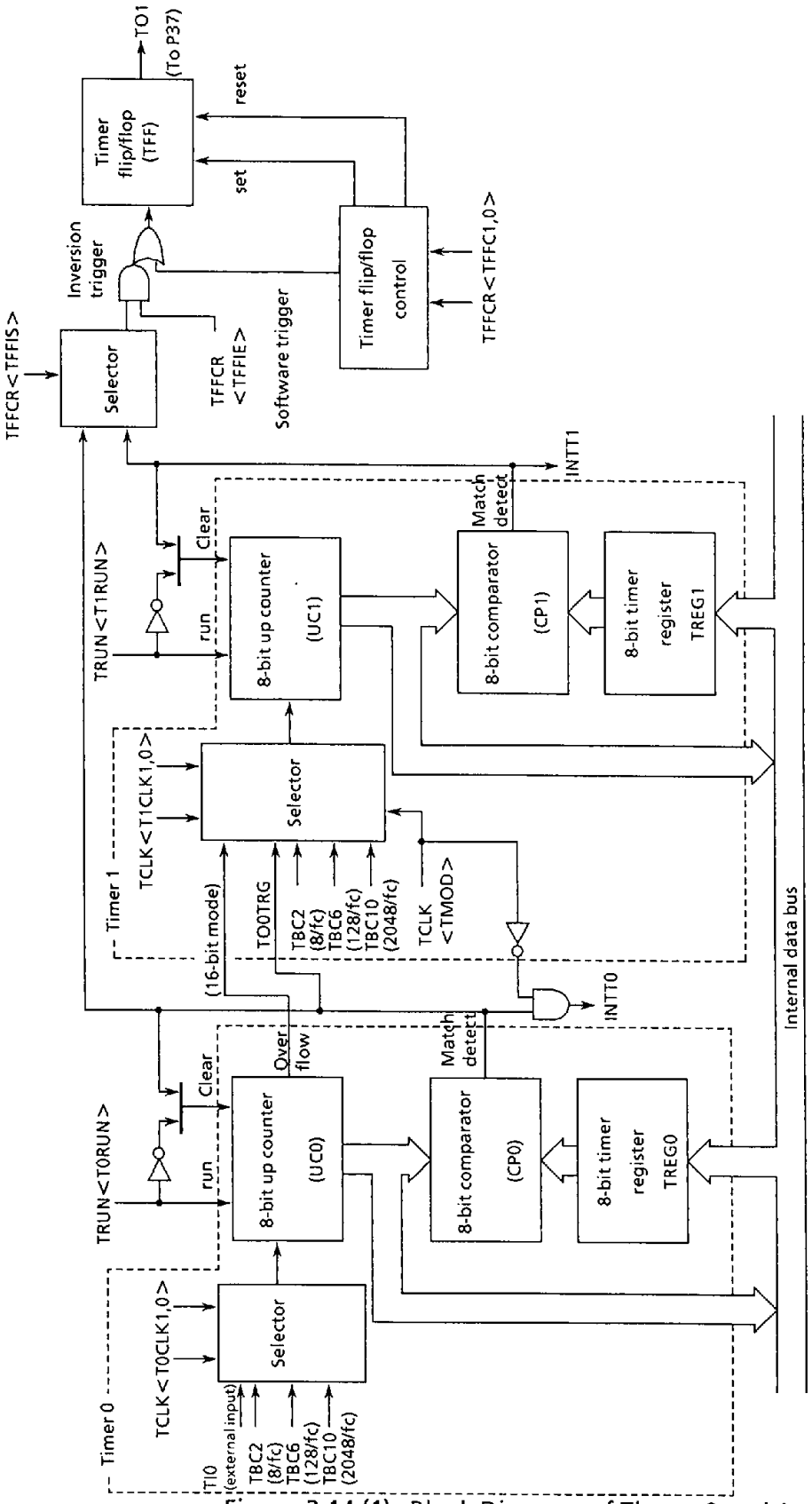


Figure 3.14 (1) Block Diagram of Timers 0 and 1

The 8-bit timer operates as explained below.
8-bit timers 0 and 1 have 8-bit and 16-bit timer modes.

(1) 8-bit timer mode

Timer 1 is used in the example.

① To generate an interrupt at a fixed cycle

To generate a timer 1 interrupt (INTT1) at a fixed cycle, first stop timer 1, then set the operating mode, input clock, and cycle in the TCLK and TREG1 registers. Then enable an INTT1 interrupt and start the timer 1 count.

Example : To generate a timer 1 interrupt every 40 μs at fc=10 MHz, set the registers as follows:

		MSB 7 6 5 4 3 2 1 0 LSB	
TRUN	←	- - - - - - 0 -	Stops timer 1 and zero-clears it.
TCLK	←	- - - 0 0 1 - -	Sets mode to 8-bit timer mode and sets input clock to TBC2 (0.8 μs @ fc 10 MHz).
TREG1	←	0 0 1 1 0 0 1 0	Sets 40 μs / TBC2 = 32H in timer register.
INTEL	←	- - 1 - - - - -	Enable INTT1 interrupt
TRUN	←	- - - - - - 1 -	Starts timer 1 count.

(Note) × ; don't care - ; no change

To select an input clock, see the table below:

Table 3.14 (1) Interrupt Cycle and Input Clock Select by 8-bit Timer

Interrupt cycle@ fc = 10 MHz	Resolution	Input clock
0.8μs to 204.8 μs	0.8μs	TBC2 (8 / fc)
12.8μs to 3.2768 ms	12.8μs	TBC6 (128 / fc)
204.8μs to 52.4288 ms	204.8μs	TBC10 (2048 / fc)

Please be sure to note the follwing point when using a 8-bit timer mode.

when using only the timer0	Subsequently to the data written on the TREG0, counting should be started after the dummy data is written to the TREG1. However when the data is written to the TREG0 after TCLK <T1CLK1, 0> is set to be other than "0, 0", the timer 0 operates as the 8-bit timer. (The dummy data does not need to be written to the TREG1.) Counting should be started after selecting the input clock.
when using only the timer1	Counting should be started after selecting the input clock from the TBC2, 6, 10.

② To output square wave with 50 % duty

Invert timer flip / flop every fixed cycle and output the timer flip / flop value to timer output pin TO1.

Example : To output a square wave every 4.8 μs at fc = 10 MHz, set the registers as follows:
This example uses timer 1, but the same operation can be effected by using timer 0.

	MSB 7 6 5 4 3 2 1 0 LSB	
TRUN ←	- - - - - - - 0 -	Stops timer 1 and zero-clears it.
TCLK ←	- - - 0 0 1 - -	Sets to 8-bit timer mode. Sets input clock to TBC2
TREG1 ←	0 0 0 0 0 0 1 1	Sets 40 μs / TBC2/2 = 3 in timer register.
TFFCR ←	0 - - 1 0 0 1 1	Zero-clears TFF and sets so that TFF inverts by a match detect signal from timer 1.
P3CR ←	- 0 - - - - - -	Sets P37 output to TO1.
TRUN ←	- - - - - - - 1 -	Starts timer 1 count.

(Note) × ; don't care - ; no change

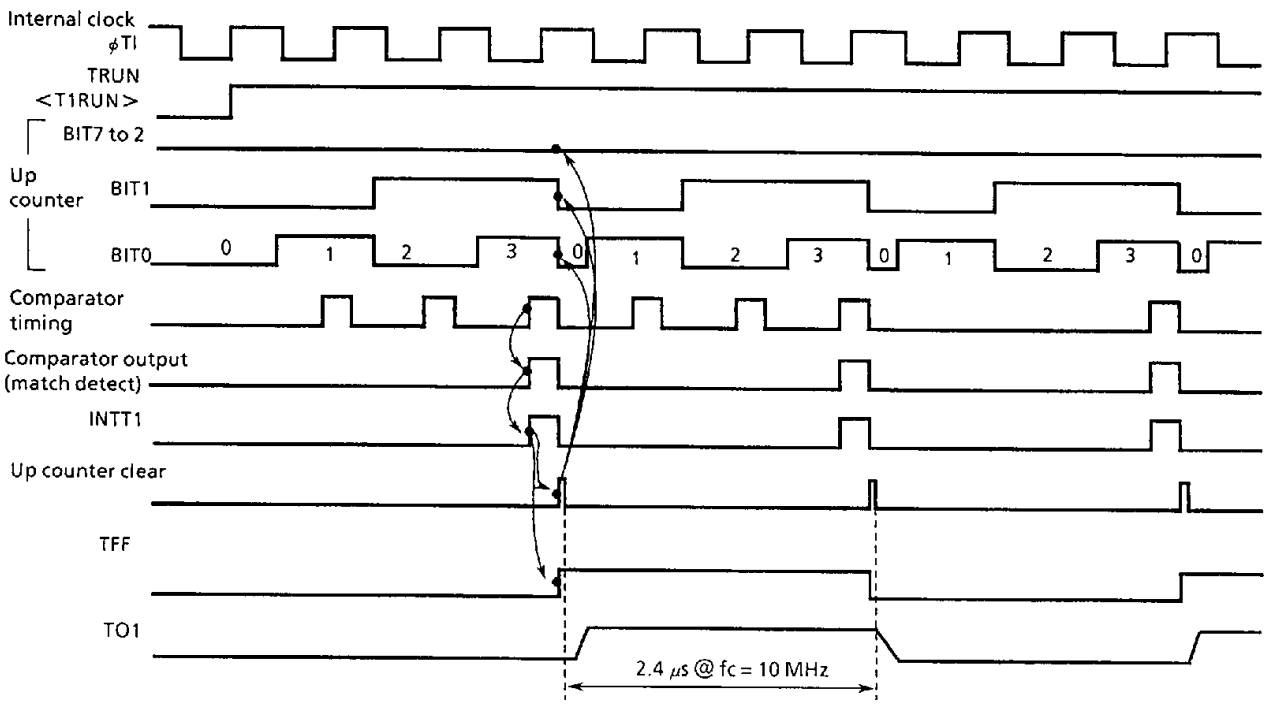


Figure 3.14 (2) Timing Chart for Square Wave (50 % duty) Output

③ To increment timer 1 using timer 0 match detect signal output.

Set mode to 8-bit timer mode and timer 1 input clock to timer 0 comparator output.

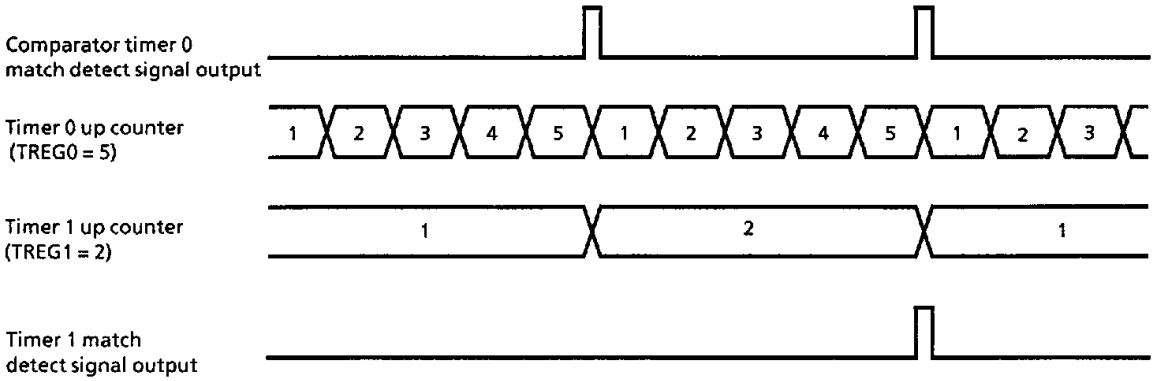


Figure 3.14 (3)

④ Output inversion by software

Regardless of timer operation, timer flip / flop (timer F/F) value can be inverted. Writing "1,0" to TFFCR<TFFC1,0> inverts the TFF value.

⑤ Timer flip/flop (timer F/F) initial setting

Regardless of timer operation, the initial timer F/F value can be set to 0 or 1.

For example, to set the TFF initial value to "0", write "0,0" to TFFCR<TFFC1,0>; to set the TFF initial value to "1", write "0,1" to TFFCR<TFFC1,0>.

(Note) The timer flip/flop or timer register value cannot be read.

(2) 16-bit timer mode

Combination of timers 0 and 1 configures a 16-bit interval timer.

To configure a 16-bit interval timer by cascade-connecting timers 0 and 1, set TCLK<TMOD> to "1".

Setting to 16-bit timer mode uses the timer 0 overflow output as timer 1 input clock regardless of clock control register TCLK. Set timer 0 input clock in TCLK. Table 3.14 (2) shows relations between timer (interrupt) cycle and input clock selected.

Table 3.14 (2) 16-bit Timer (Interrupt) Cycle and Input Clock Selected

Timer (interrupt) cycle @ fc = 10 MHz	Resolution	Timer 0 input clock
0.8 μs to 52.43 ms	0.8 μs	φTBC2 (8 / fc)
12.8 μs to 838.86 ms	12.8 μs	φTBC6 (128 / fc)
204.8 μs to 13.42 s	204.8 μs	φTBC10 (2048 / fc)

For timer (interrupt) cycle, set the lower 8 bits in timer register TREG0 and upper 8 bits in TREG1. Always set TREG0 first. (Writing data to TREG0 temporarily disables compare; writing data to TREG1 starts compare.)

Setting example: To generate an INTT1 interrupt every 0.2 s at fc=10 MHz, set the following values in timer registers TREG0 and 1.
When TBC6 (=12.8 μs @ 10 MHz) is used as input clock,
0.2 s / 12.8 μs=15625=3D09H
Therefore, set TREG1=3DH and TREG0=09H.

The timer 0 comparator match detect signal is output every time the values in up counter UC0 and TREG0 match. But an INTT0 is not generated.

When the values in upcounter UC1 and TREG1 match, timer 1 comparator outputs a match detect signal every comparator timing. When the match detect signals of the comparators of both timers 0 and 1 are output at the same time, an INTT1 interrupt is generated. If inversion is enabled, the timer flip / flop value is inverted.

Table 3.14 (3) Differences between 16-bit Timer Mode and 8-bit Timer Mode

	Timer 0			Timer 1		
	INTT0 interrupt	Output to TO1	Counter Operation when match detection	INTT1 interrupt	Output to TO1	Counter Operation when match detection
16-bit timer mode (Increments timer 1 by timer 0 overflow)	Interrupt is not generated.	Output disabled. (Output of a match with TREG0 is disabled.)	TREG0 (Increments even if values match.)	Interrupt generated.	Output enabled. (Matches of both timers 0 and 1 can be output.)	TREG1*2^8 + TREG0 (Full 16 bits) (<CLBC16> 0 : Counts up when a match signal 1 : Clears when a match signal)
8-bit timer mode (Increments timer 1 by timer 0 overflow)	Interrupt generated.	Output enabled. (Output of match of either timer 0 or 1 match is enabled.)	TREG0 (<CLBC0> 0 : Counts up when a match signal 1 : Clears when a match signal)	Interrupt generated.	Output enabled. (Output of match of either timer 0 or 1 match is enabled.)	TREG1*TREG0 (multiplied value <CLBC1> 0 : Counts up when a match signal 1 : Clears when a match signal)

Example : When TREG1 = 04 H and TREG0 = 80 H:

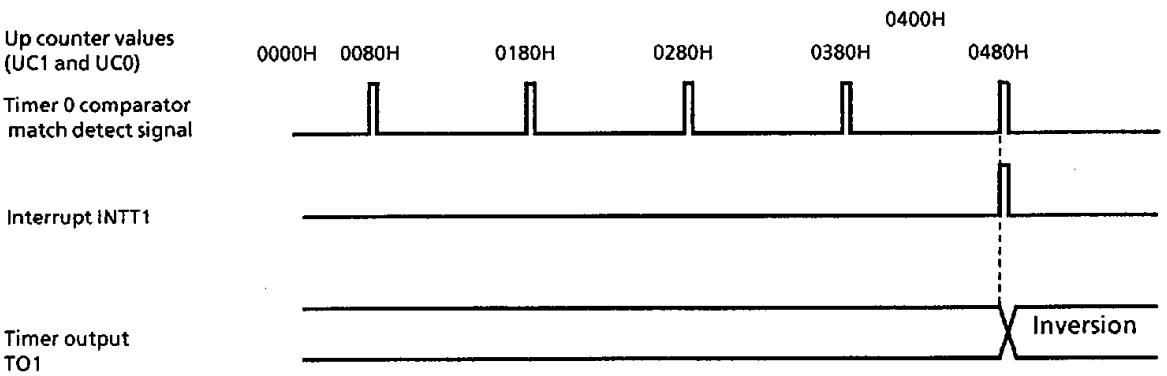


Figure3.14 (4) Timing Chart for 16-bit Timer Mode

(3) Control registers

Figure 3.14 (5) shows timer 0 and 1 related control registers.

Timer 0 Register

	7	6	5	4	3	2	1	0
Read/Write	W							
Value after reset	Undefined							

TREG0 (FFD0H)

Prohibit read-modify-write.

Timer 0 Count Data Register

	7	6	5	4	3	2	1	0
Read/Write	R							
Value after reset	Undefined							

TCUT0 (FFD0H)

Prohibit read-modify-write.

Timer 1 Register

	7	6	5	4	3	2	1	0
Read/Write	W							
Value after reset	Undefined							

TREG1 (FFD1H)

Prohibit read-modify-write.

Timer 1 Count Data Register

	7	6	5	4	3	2	1	0
Read/Write	R							
Value after reset	Undefined							

TCUT1 (FFD1H)

Prohibit read-modify-write.

* Reading timer registers 0 and 1 reads the current data of the timer/counters 0 and 1.Data can only be read from the timer/counters of timers 0 and 1, not written to them (whereas data can be written to the timer/counter of timer 3).

Figure 3.14 (5)-1 Timers 0 and 1 Related Registers

Timer 0 and 1 Control Register

TCLK [TMR01CR] (FFD2H)

	7	6	5	4	3	2	1	0
bit Symbol	CLBC16	CLBC1	CLBC0	TMOD	T1CLK1	T1CLK0	T0CLK1	T0CLK0
Read/Write	R/W	R/W	R/W	R/W	R/W		R/W	
Value after reset	0	0	0	0	0	0	0	0
Function	16-bit timer/counter clear control 0: Disable 1: Enable	Timer 1 counter clear control 0: Disable 1: Enable	Timer 0 counter clear control 0: Disable 1: Enable	Timer Mode 0: 8bit 1: 16bit	Timer 1 CLK-in control 00: TO0TRG 01: TBC2 10: TBC6 11: TBC10		Timer 0 CLK-in control 00: TBC2 01: TBC6 10: TBC10 11: TI0	

Timer 0 input clock

00	TBC2 (8/fc)
01	TBC6 (128/fc)
10	TBC10 (2048/fc)
11	TI0 (external input)

Timer 1 input clock

00	TO0TRG (timer 0 match detect signal output)
01	TBC2 (8/fc)
10	TBC6 (128/fc)
11	TBC10 (2048/fc)

(Note) When 16-bit timer mode<TMOD> = 1, TO0TRG (timer 0 match detect signal) is selected as timer 1 input clock.

Timer 0/1 operating mode

0	8-bit timers x 2
1	16-bit timer

Counter clear by timer 0 match detect signal output

0	Disable
1	Enable

Counter clear by 16-bit timer match detect signal output

0	Disable
1	Enable

Counter clear by timer 1 match detect signal output

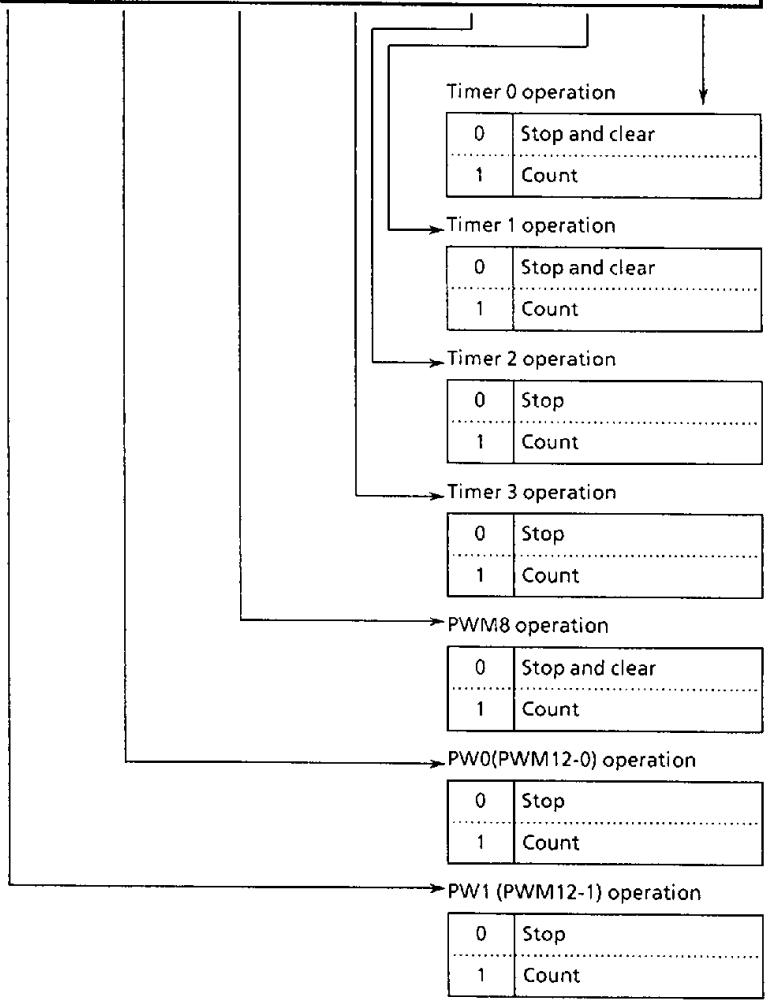
0	Disable
1	Enable

Figure 3.14 (5)-2 Timers 0 and 1 Related Register

Timer Operation Control Register

TRUN (FFDAH)

	7	6	5	4	3	2	1	0
bit Symbol		RUNPW1	RUNPW0	RUNPW8	T3RUN	T2RUN	T1RUN	T0RUN
Read/Write		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value after reset		0	0	0	0	0	0	0
Function		PW0, 1 Run/Stop Control 0: Stop 1: Run (Count up)		PWM8 Run / Stop Control 0: Stop & Clear 1: Run (Count up)	Timer Run / Stop Control 0 : Stop 1 : Run		Timer Run / Stop Control 0 : Stop & Clear 1 : Run (Count up)	



(Note) To start / stop timers when 16-bit mode <TMOD> = 1, set both <T0RUN> and <T1RUN> to "1" or "0" simultaneously.

Figure 3.14 (5)-3 Timer 0 and 1 Related Register

Timer Flip/Flop Control Register

	7	6	5	4	3	2	1	0
TFFCR (FFD9H) bit Symbol	(Note) Always write "0".			TOSEL	TFFC1	TFFC0	TFFIE	TFFIS
Read/Write				R/W	W		R/W	
Value after reset				0	—		0	0
Function				P37 output select 0: PWM8 1: TO1	TFF control 00: Clear TFF 01: Set TFF 10: Invert TFF 11: Don't care		TFF Invert 0: Disable 1: Enable	0: Inverts by timer 0. 1: Inverts by timer 1.

Prohibit read-modify-write.

(Note) When writing data to the TFFCR, always write "0". If read, "1" is always read.

Timer flip / flop (TFF) inversion signal select

0	Timer 0
1	Timer 1

Timer flip / flop (TFF) inversion

0	Disable
1	Enable

Timer flip / flop (TFF) control

00	Clears TFF to "0".
01	Sets TFF to "1".
10	Inverts TFF value (software inversion).
11	Don't care (If read, "11" is always read.)

P37 output select

0	PWM8
1	TO1

(Note) To use the PWM8 or TO1 output function, set P3CTR<P37M> to "0".

Figure 3.14 (5)-4 Timer 0 and 1 Related Register

3.14.3 8-bit Timer 2

Timer 2 consists of an 8-bit up counter, an 8-bit timer register, and an 8-bit comparator circuit.

An input clock to timer 2 is selected from time base counters TBC2, TBC6, external input pin TI0, or C-FG. (When C-FG is used as an input clock, set servo input control register SINCR<C-FG> = "0".)

The timer counter is cleared by reset, by a match detect signal when timer 2 control register TMR2CR<CLBC21> = "1", or by software, TMR2CR<CLBC20> = 1.

For timer interrupts (INTT2), see timers 0 and 1 8-bit timer mode. (Note that TFF is not supported.)

Figure 3.14 (6) is the block diagram of timer 2.

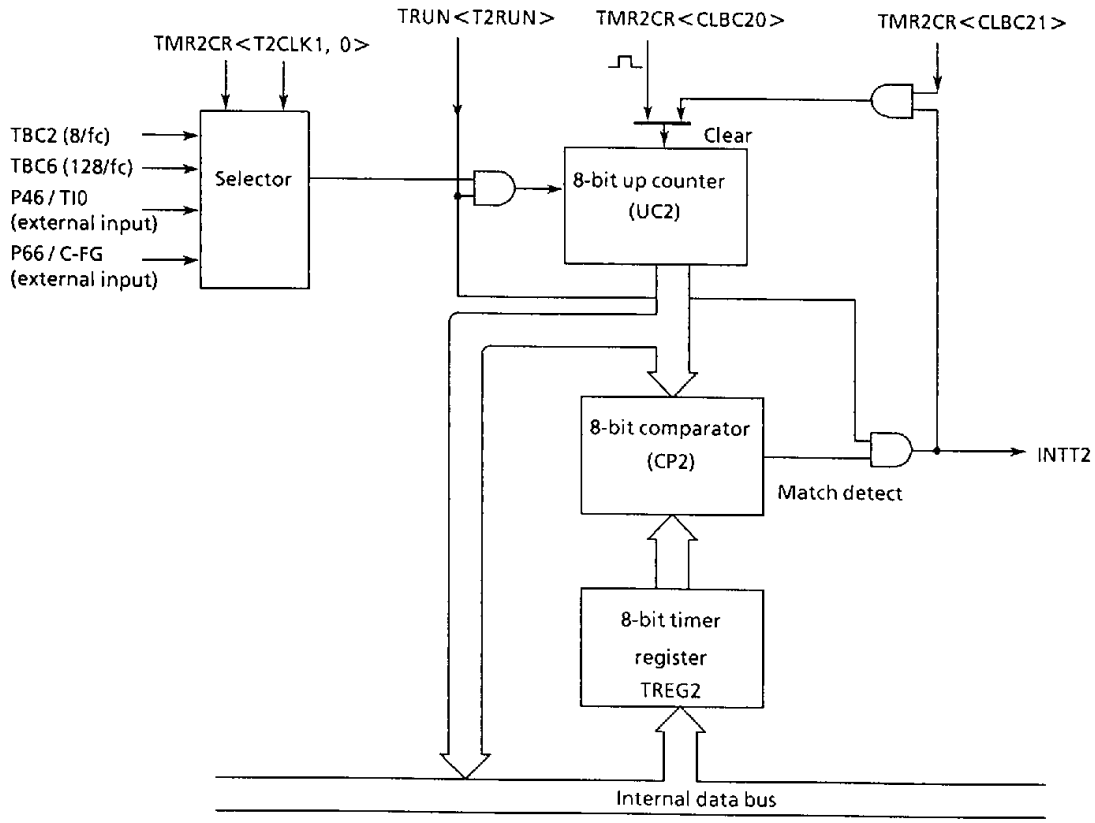


Figure 3.14 (6) Timer 2 Block Diagram

(1) Control register

Figure 3.14 (7) shows timer 2 related register.

Timer 2 Count Data Register

		7	6	5	4	3	2	1	0
TCUT2 (FFD3H)	Read/Write	R							
	Value after reset	Undefined							

Timer 2 Register

		7	6	5	4	3	2	1	0
TREG2 (FFD4H)	Read/Write	W							
	Value after reset	Undefined							

Prohibit read-modify-write.

Timer 2 Control Register

		7	6	5	4	3	2	1	0
TMR2CR (FFD5H)	bit Symbol					CLBC21	CLBC20	T2CLK1	T2CLK0
	Read/Write					R/W	R/W	R/W	
	Value after reset					0	0	0	0
	Function					Counter clear control 0: Disable 1: Enable	Counter Soft Clear 0: – 1: Clear	Timer 2 CLK-in control 00: TBC2 01: TBC6 10: TI0 11: C-FG	

Timer 2 input clock

00	TBC2 (8/fc)
01	TBC6 (128/fc)
10	TI0 (external input)
11	C-FG (external input)

(Note) To use C-FG as input clock, set SINCR<C-FG> = "0".

Counter clear by timer 2 match detect signal output

0	Disable
1	Enable

Timer 2 counter software clear

0	—
1	Clear (one-shot)

(Note) Reading <CLBC20> always reads "0".

(Note) TREG2 is a write-only register. Reading TREG2 always reads "1". For timer start and stop, see Figure 3.14 (5)-3, Timer Operation Control Register TRUN.

Figure 3.14 (7) Timer 2 Related Registers

3.14.4 8-bit Timer 3

Timer 3 consists of an 8-bit up / down counter, an 8-bit counter buffer register, 8-bit timer register, and an 8-bit comparator circuit.

An input clock to timer up/down counter is selected from time base counters TBC2, TBC6, external input pin TI1, or PCTL. (When PCTL is used as an input clock, set SINCR<P-CTL> = "0".)

In relation to the P-CTL external input signal, the PCTL input signal is normal when CSYNCR<PCTPO> = "0"; inverted when <PCTPO> = "1".

The up/down counter is cleared by reset, by a match detect signal when timer 3 control register TMR3CR<CLBC31> = "1", or by software, TMR3CR<CLBC30> = 1 (software clear).

As with timers 0,1, and 2, the count data can be read from the 8-bit up/down counter for timer 3. However, in the case of timer 3, count data can also be written. (reload function)

Timer 3 interrupts (INTT3) are controlled by timer 3 control register TMR3CR<INTC1,0>. Either 8-bit up/down counter overflow or 8-bit comparator match detect can be selected, or both can be selected at the same time.

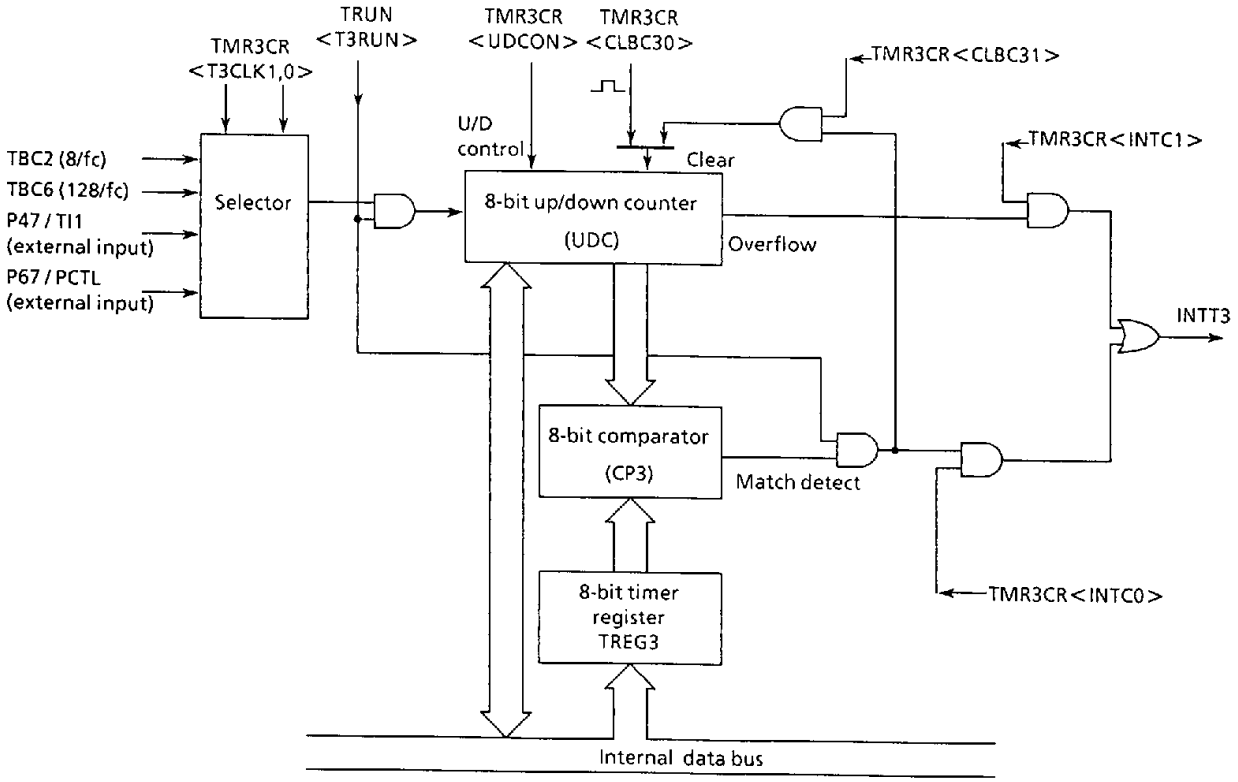


Figure 3.14 (8) Timer 3 Block Diagram

(1) Control Register

Figure 3.14 (9) shows timer 3 related register.

Timer 3 Count Data Register

	7	6	5	4	3	2	1	0
TCUT3 (FFD6H) Read/Write	R/W							
Value after reset	Undefined							

Timer 3 Register

	7	6	5	4	3	2	1	0
TREG3 (FFD7H) Read/Write	W							
Value after reset	Undefined							

Prohibit read-modify-write.

Timer 3 Control Register

	7	6	5	4	3	2	1	0
TMR3CR (FFD8H) bit Symbol		INTC1	INTC0	CLBC31	CLBC30	UDCON	T3CLK1	T3CLK0
Read/Write		R/W		R/W	R/W	R/W	R/W	
Value after reset		0	0	0	0	0	0	0
Function		INTT3 Interrupt Control 00: Disable INT 01: Match detect signal output 10: Overflow 11: Match detect signal output and overflow		Counter Clear Control 0: Disable 1: Enable	Counter Soft Clear 0: – 1: Clear	Counter up/down control 0: Up 1: Down	Timer 3 CLK-in control 00: TBC2 01: TBC6 10: TI1 11: PCTL	

Timer 3 interrupt control

00	Disable
01	Match detect signal output
10	Overflow
11	Match detect signal output and overflow

Timer 3 input clock

00	TBC2 (8/fc)
01	TBC6 (128/fc)
10	TI1 (external input)
11	PCTL (external input)

(Note) To use PCTL input, set SINCR<P-CTL> = "0".

Counter clear by timer 3 match detect signal output

0	Disable
1	Enable

Timer 3 counter software clear

0	—
1	Clear (one-shot)

(Note) Reading <CLBC30> always reads "0".

Timer 3 operating mode

0	Increment
1	Decrement

(Note) To switch timer 3 interrupt output, stop timer 3. For timer start / stop, see timer operation control register TRUN in Figure 3.14 (5)-3.

Figure 3.14 (9) Timer 3 Related Registers

3.15 Serial Channels

The TMP91C642A integrates two 8-bit synchronous serial interface channels. Serial channel 0 is connected to an external circuit via P40 (SCLK0), P41 (TxD0), and P42 (RxD0); serial channel 1 is connected to an external circuit via P43 (SCLK1), P44 (TxD1), and P45 (RxD1). To use the SIO function, set port 4 mode control register P4MR to SIO pin function. Serial channels 0 and 1 are identical circuits, configured independently.

The serial channels have serial buffers. In receive mode, data in the first frame are read from the data buffer by the time data in the second frame are received. In send mode, after data in the first frame are received, data in the second frame are written to the send buffer. In send-receive mode, data must be processed one frame at a time.

Figure 3.15 (1) is the block diagram of the serial channel.

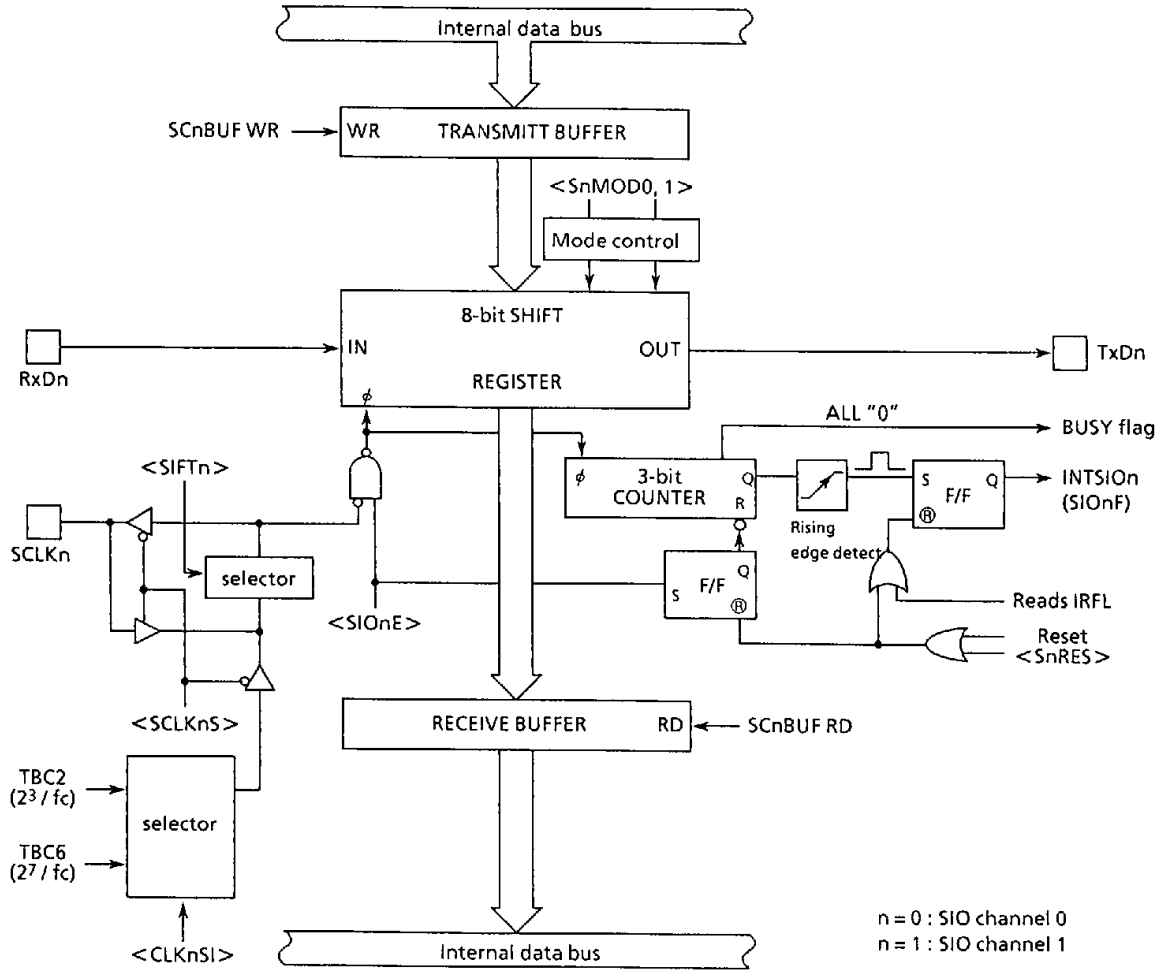


Figure 3.15 (1) Serial Channel Block Diagram

3.15.1 Serial Clock

The serial clock can select the following according to serial channel mode registers SC0MOD and SC1MOD (addresses FFE3H and FFE5H in memory).

(1) Clock Source Select

Either an internal or an external clock can be selected by SC0MOD<SCLK0S> (SC1MOD<SCLK1S> for channel 1).

① Internal clock

Either TBC2 (2^3/fc) or TBC6 (2^7fc) can be selected as the serial clock by <CLK0SI> (<CLK1SI> for channel 1). Figure 3.15 shows the maximum transfer speed possible using the internal clock operation. The serial clock is output from SCLK0 (SCLK1 for channel 1).

The serial clock automatically stops after ending one-frame serial operation, then waits for the next serial operation. The serial clock holds high level when data are not transferred.

Table 3.15 Maximum Transfer Speed Using Internal Clock Operation

Internal clock	Maximum transfer speed (@ fc = 10 MHz)
TBC 2 (2^3/fc)	1250000 bps
TBC 6 (2^7/fc)	78125 bps

② External clock

The clock input to the SCLK0 (SCLK1 for channel 1) pin is used as the serial clock. Using external clock operation, set serial transfer internal clock select register <CLK0SI> (<CLK1SI> for channel 1) to "0".

(2) Shift Edge select

Leading or trailing edge shift can be selected using SC0MOD <SIFT0> (SC1MOD <SIFT1> for channel 1).

① Leading edge shift

Shifts data at the leading edge of the serial clock (I/O signal falling edge on SCLK0 or SCLK1 pin).

② Trailing edge shift

Shifts data at the trailing edge of the serial clock (I/O signal rising edge on SCLK0 or SCLK1 pin). Note that trailing edge shift is not supported in send mode.

3.15.2 Operation

Serial channels 0 and 1 have send, receive, and send-receive modes. Mode can be selected using SC0MOD<S0MD1, 0> (SC1MOD<S1MD1, 0> for channel 1). After reset, both <S0MD1,0> and <S1MD1, 0> are set to "0,0" and send mode is selected. The following explains operation in each transfer mode.

(1) Send mode

After setting send mode to the control register, write the first send data to buffer registers SC0BUF and SC1BUF (addresses FFE2H and FFE4H in memory). (If send mode is not set, data cannot be written to the buffer register.) Setting serial transfer control register SC0MOD<SIO0E> or SC1MOD<SIO1E> to "1" starts sending. At this time, send data are synchronized with the falling edge of the serial clock (leading edge shift) and output to the TxD pin starting from the LSB. When TxD is output from the LSB, the send data are transferred from the buffer register to the shift register. The buffer register is then empty. The buffer empty interrupt, INTSIO (internal signal INTSIO0 or INTSIO1), is generated to request the next send data. Writing the next send data to the buffer register using the interrupt processing routine clears the interrupt request signal. When the interrupt service program writes the next send data to the buffer register, the interrupt request is cleared.

The channel data when an interrupt is generated can be obtained by reading interrupt request flag IREL<SIO1F, SIO0F> (bits 1 and 0 at address FFECH in memory). Identify the channel where the interrupt is generated and process it using software. The flag is cleared when read. It must be read at the beginning of the interrupt processing routine.

(Internal clock)

When an internal clock is used, if the next data are not set after all data are sent, the serial clock stops and waits.

Figure 3.15 (2)-(a) is the timing chart of channel 0 send mode using internal clock operation (with wait).

(External clock)

When an external clock is used, before the next data can be shifted the next data, the data must first be set in the buffer register. Therefore, the transfer speed is determined by the maximum delay time from interrupt generation to data write to the buffer register by the interrupt service program.

Figure 3.15 (2)-(b) is the timing chart of channel 0 send mode using external clock operation.

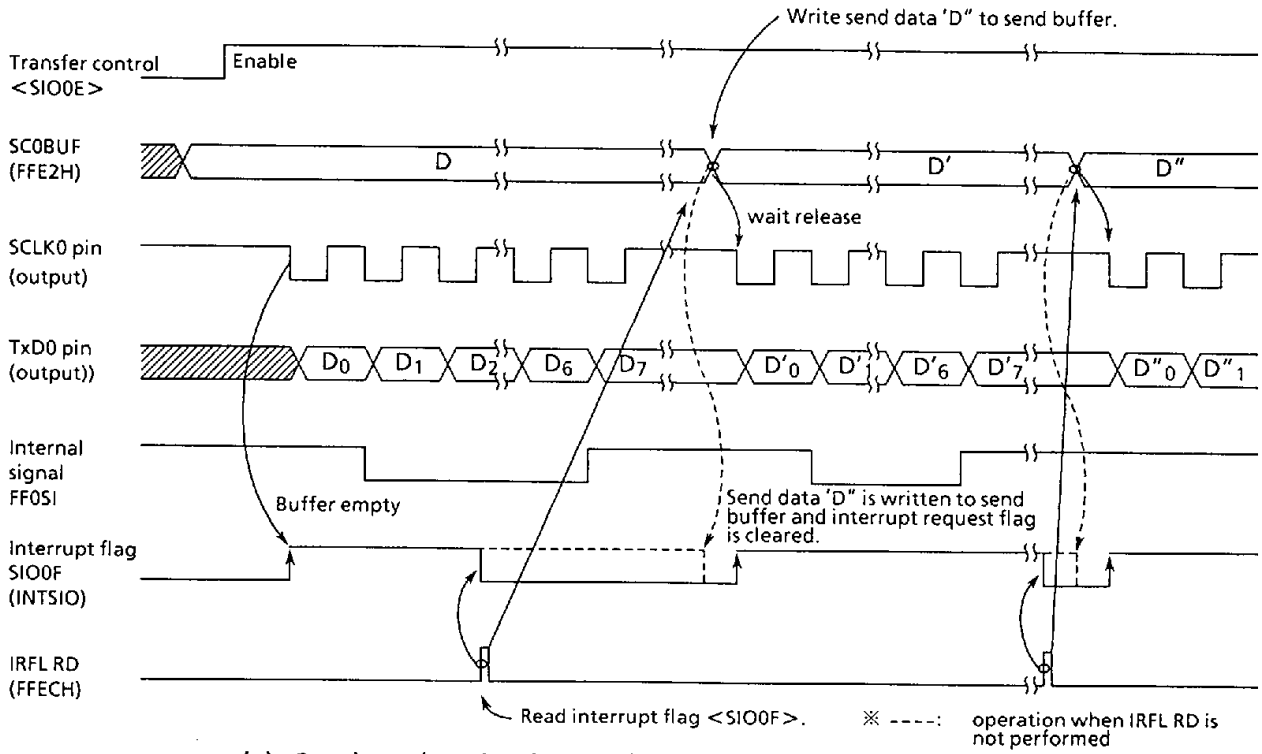
To end sending, the interrupt service program for buffer empty disables (zero-clears) serial transfer control register SC0MOD<SIO0E> or SC1MOD<SIO1E>.

When serial transfer control is disabled, sending stops after the data currently shifted out are sent.

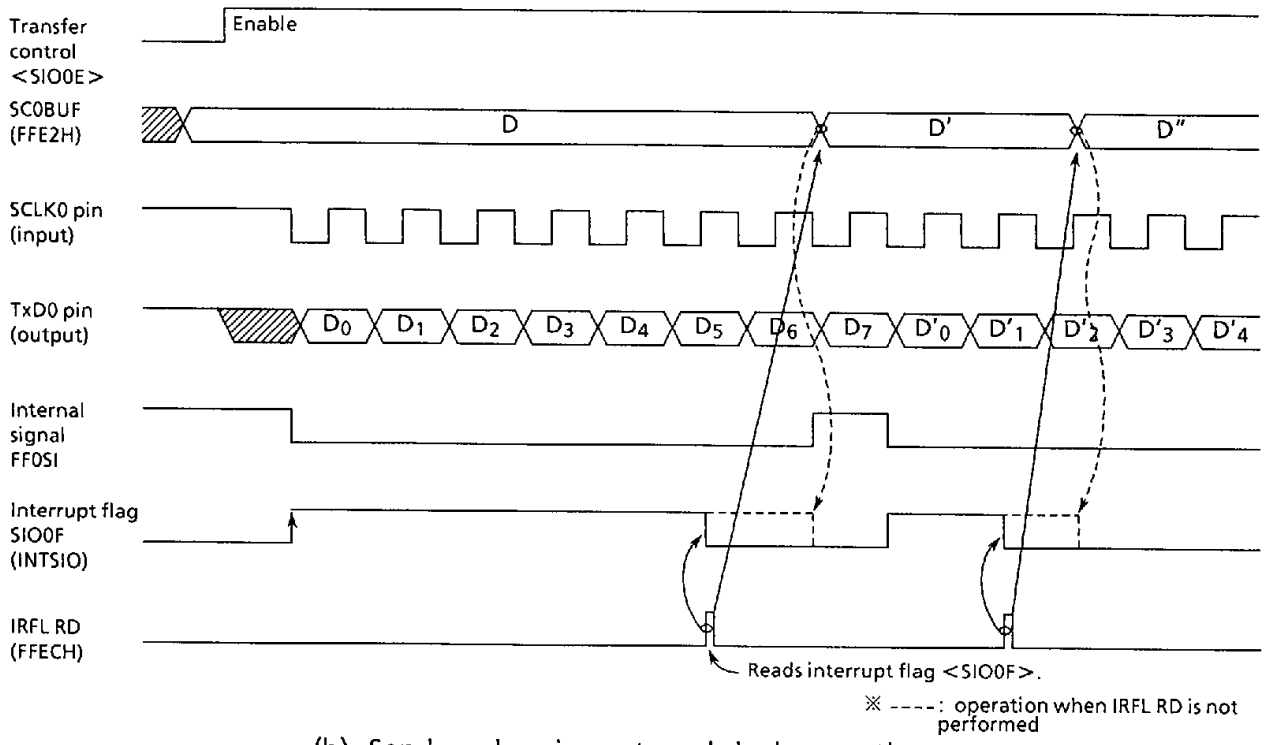
Sending end can be detected by the status of serial transfer monitor flag SC0MOD<FF0SI> or SC1MOD<FF1SI>. (The serial transfer monitor flag is set to "1" at send completion.)

When an external clock is used, before the next send data are shifted out, the serial transfer control register must first be disabled. If the serial transfer control register is not disabled, send stops after sending the next send data (dummy).

SIO send mode (only in leading edge shift operation)



(a) Send mode using internal clock operation (with wait)



(b) Send mode using external clock operation

Figure 3.15 (2) Serial Channel Send Mode Timing Chart (Channel 0)

(2) Receive mode

Data receive is enabled by setting the control register to receive mode, then setting serial transfer control SC0MOD<SIO0E> or SC1MOD<SIO1E> to enable. The shift data are synchronized with the serial clock and fetched from the RxD pin. Data to be shifted are transferred from the shift register to the buffer register. The buffer full interrupt, INTSIO (INTSIO0 or INTSIO1), requesting receive data read is generated.

The received data are read from the buffer register by the interrupt processing routine. Reading the received data clears the interrupt request signal. After interrupt generation, the next data are read continuously. After the interrupt request signal is cleared, the next data are transferred from the shift register to the buffer register.

The channel data when an interrupt are generated can be obtained by reading interrupt request flag IREL<SIO1F, SIO0F>. The flag is cleared when read. It must be read at the beginning of the interrupt processing routine.

(Internal clock)

When an internal clock is used, if the previous data are not read from the buffer register after the next data are fetched, the serial clock stops and waits until the previous data are read.

Figure 3.15 (3)-1-(a) is the timing chart of channel 0 receive mode using internal clock operation (leading edge shift with wait).

Figure 3.15 (3)-2-(a) is the timing chart of channel 0 receive mode using internal clock operation (trailing edge shift with wait).

(External clock)

When an external clock is used, shifting data are synchronized with the external clock. The data are read before the next receive data are transferred to the buffer register. If the previous data are not read, the receive data are not transferred to the buffer register and subsequent receive data to be input are cancelled. The maximum transfer speed is determined by the maximum delay time from interrupt generation to receive data read by the interrupt service program.

Figure 3.15 (3)-1-(b) is the timing chart of channel 0 receive mode using external clock operation (leading edge shift/with wait).

Figure 3.15 (3)-2-(b) is the timing chart of channel 0 receive mode using external clock operation (trailing edge shift/with wait).

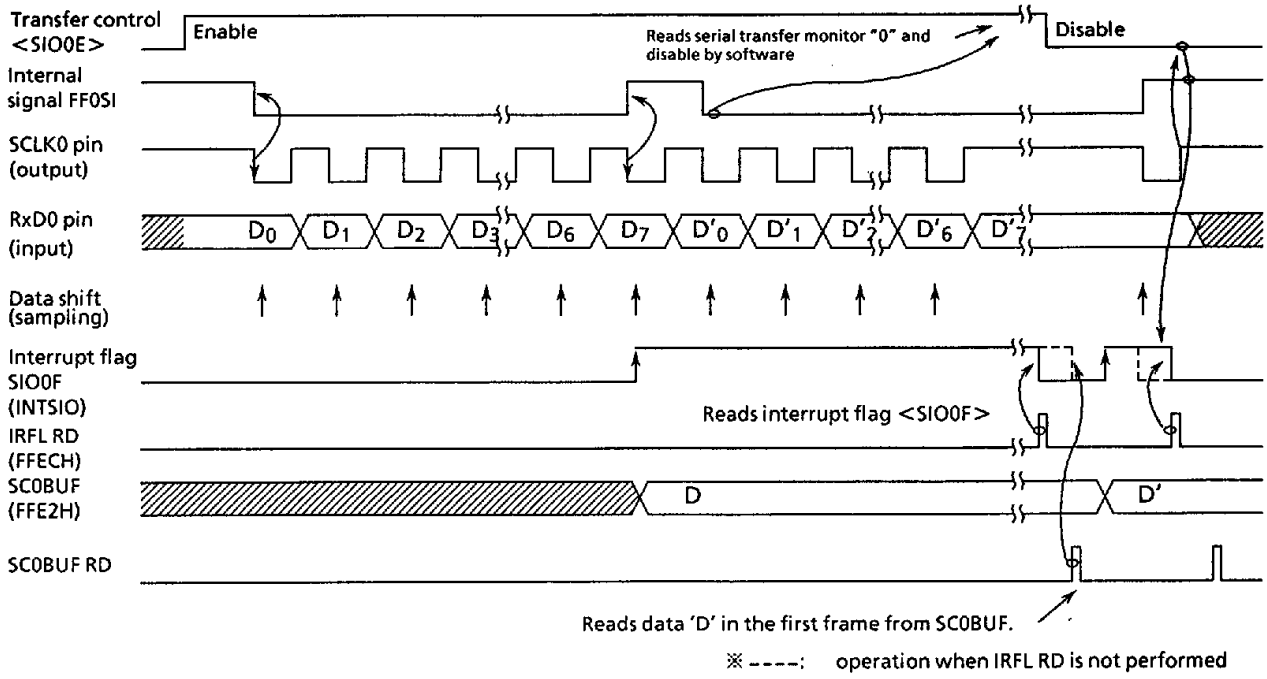
In receive mode, either leading edge shift or trailing edge shift can be selected. At leading edge shift, data are fetched at the rising edge of the serial clock. Thus the first shift data must be input to the RxD pin before the first serial clock is applied at the start of data transfer.

To end data receive disable the serial transfer control register. After the serial transfer control register is disabled, data receive ends when all 8 bits are received and transferred to the buffer register.

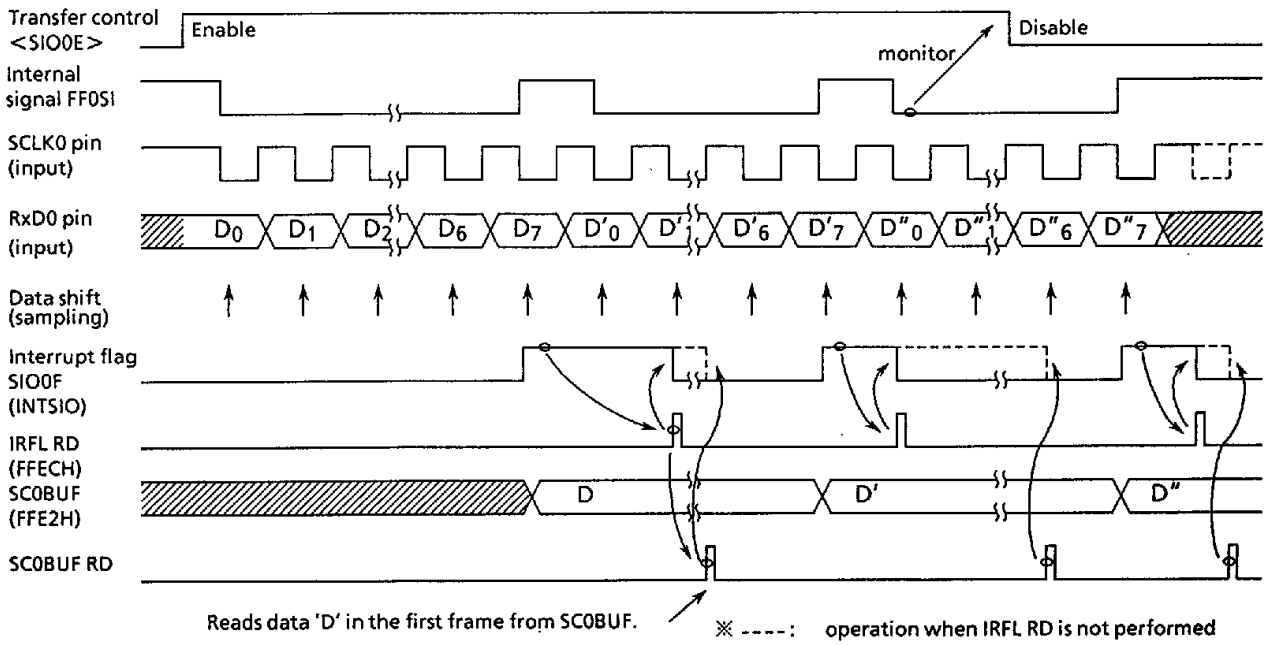
Completion of data receive by the program is checked by reading the serial transfer monitor flag. (The flag is set to "1" when receive is complete.)

(Note) When the transfer mode is switched, the contents of the buffer register are not maintained. Before switching the transfer control register and read the last received data.

SIO receive mode (leading edge shift operation)



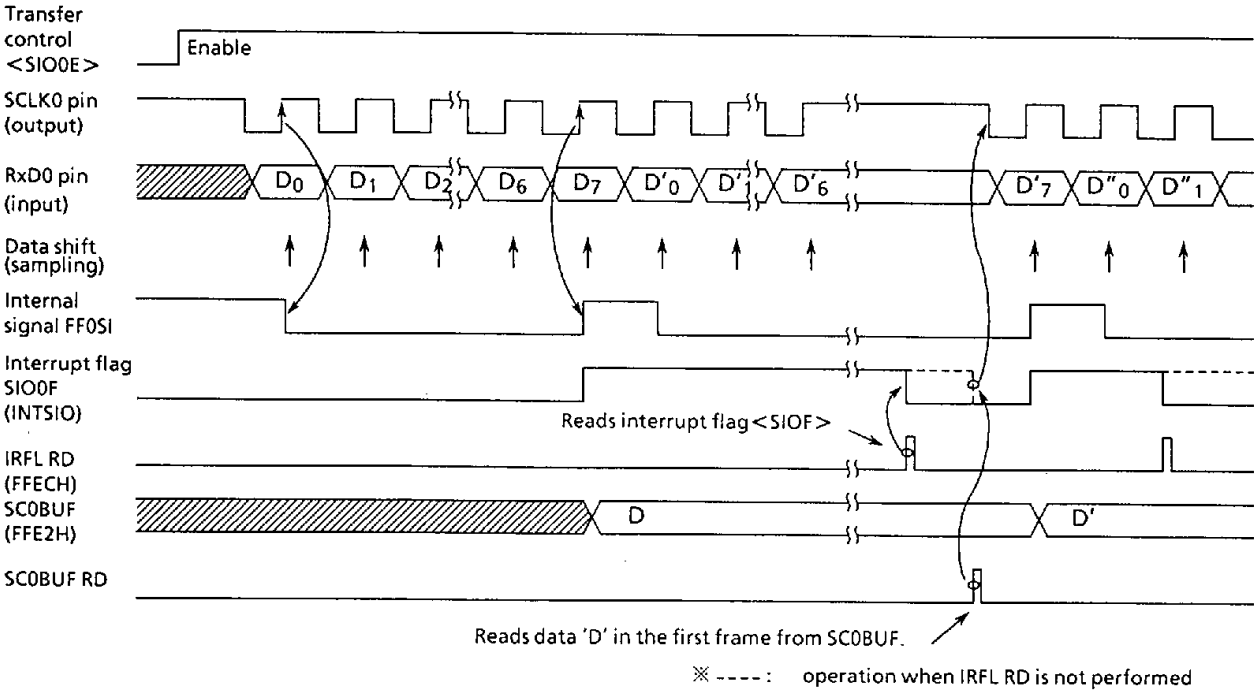
(a) Receive mode using internal clock operation (leading edge shift/with wait)



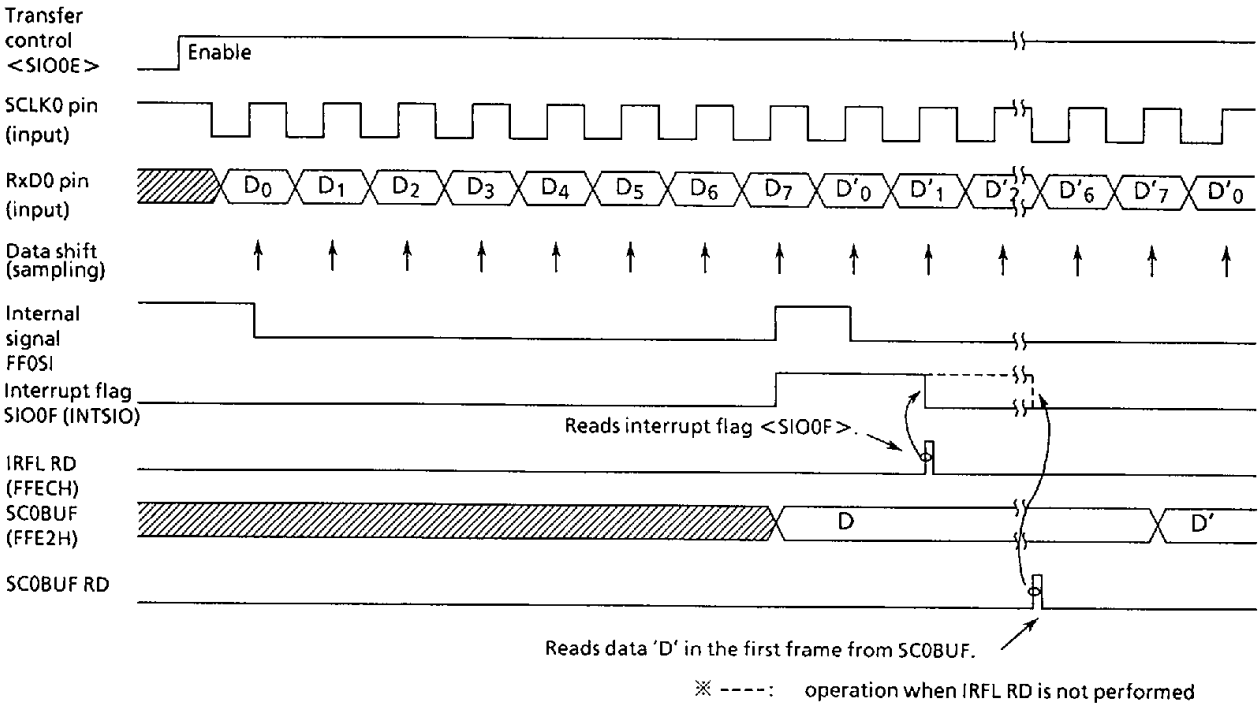
(b) Receive mode using external clock operation (leading edge shift)

Figure 3.15 (3)-1 Serial Channel Receive Mode (Leading Edge Shift) Timing Chart (Channel 0)

SIO receive mode (trailing edge shift operation)



(a) Receive mode using internal clock operation (trailing edge shift/with wait)



(b) Receive mode using external clock operation (trailing edge shift)

Figure 3.15 (3)-2 Serial Channel Receive Mode (Trailing Edge Shift) Timing Chart (Channel 0)

(3) Send-receive mode

Send-receive mode is set to the control register, then the first send data are written to buffer register SC0BUF or SC1BUF. Enabling (setting to "1") serial transfer control register SC0MOD<SIO0E> or SC1MOD<SIO1E> enables data send-receive. Send data are output from the TxD pin at the leading edge of the serial clock. Receive data are fetched from the RxD pin at the trailing edge.

Data are fetched then transferred from the shift register to the buffer register. The buffer full interrupt, INTSIO (INTSIO0 or INTSIO1), requesting for receive data read is generated. The interrupt service program reads the receive data from the buffer register, then writes the send data.

The channel data when an interrupt are generated can be obtained by reading interrupt request flag IREL<SIO1F, SIO0F>. The flag is cleared when read. It must be read at the beginning of the interrupt processing routine.

(Internal clock)

When an internal clock is used, waits until the receive data are read and the next send data are written.

Figure 3.15 (4)-(a) is the timing chart of channel 0 send-receive mode using internal clock operation (with wait).

(External clock)

When an external clock is used, data to be shifted are synchronized with the external clock. The data must be read and the next send data written before the next data shift. The maximum transfer speed is determined by the maximum delay time from interrupt generation to receive data read and send data read by the interrupt service program.

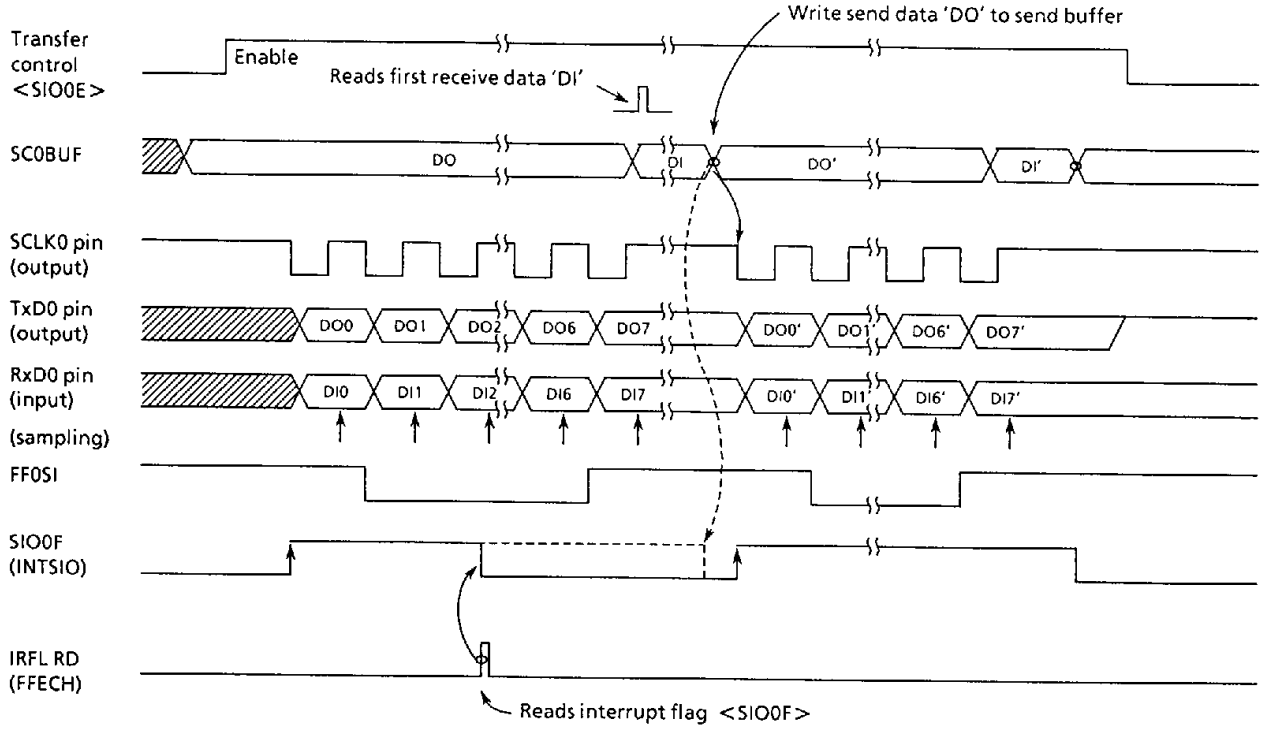
Figure 3.15 (4)-(b) is the timing chart of channel 0 send-receive mode using external clock operation.

The buffer register is used for both send and receive data. Send data are written after the 8-bit receive data are read.

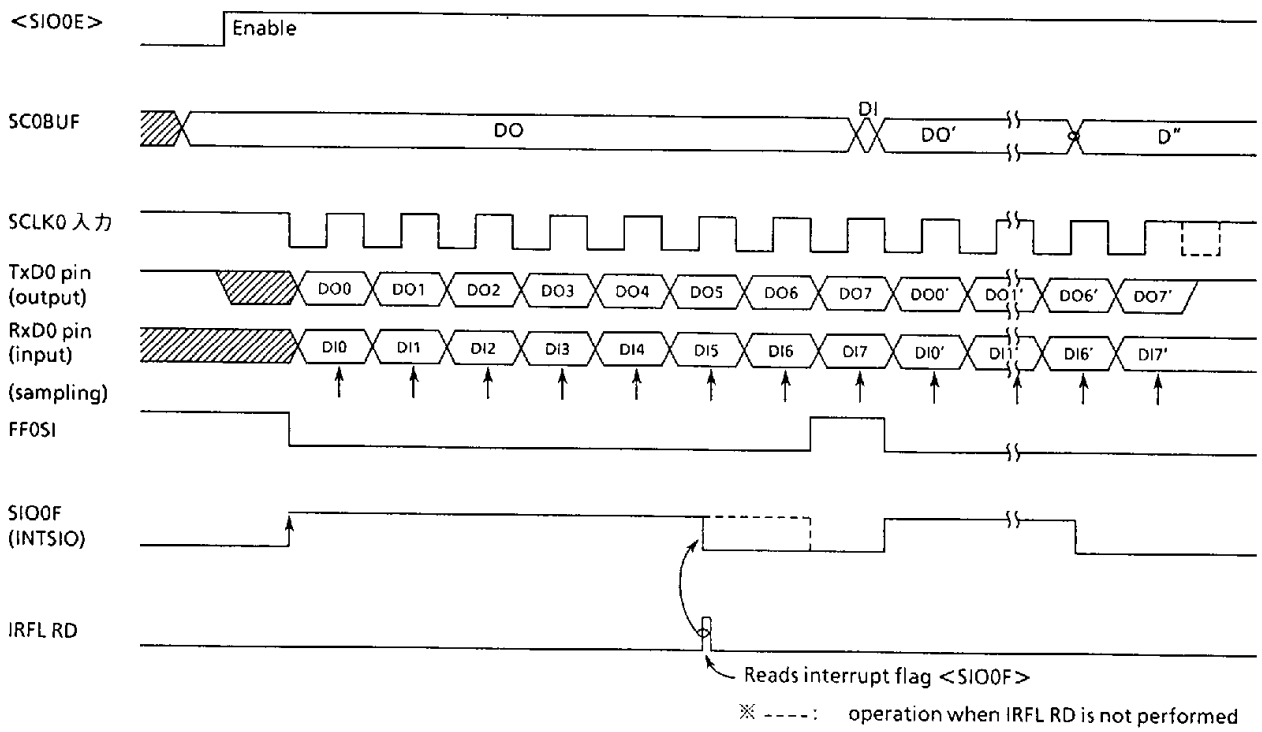
To end send-receive, disable the serial transfer control register. When the serial transfer control register is disabled, send data are disabled. Send-receive ends after moving the receive data to the buffer register.

To check send-receive end by program, read serial transfer monitor flag SC0MOD<FF0SI> or SC1MOD<FF1SI>.

SIO Send-receive mode (send : leading edge shift operation/receive : trailing edge shift operation)



(a) Send-receive mode using internal clock operation (with wait)



(b) Send-receive mode using external clock operation

Figure 3.15 (4) Serial Channel Send-Receive Mode Timing Chart (Channel 0)

3.15.3 Control Registers

Serial channels (SIO) are controlled by two control registers (SC0MOD and SC1MOD) and two buffer registers (SC0BUF and SC1BUF).

Figure 3.15 (5) shows serial channel related registers.

Serial Channel 0 Control Register

SC0MOD (FFE3H)	7	6	5	4	3	2	1	0
bit Symbol	FF0SI	S0RES	S0MD1	S0MD0	SIFT0	CLK0SI	SCLK0S	SIO0E
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value after reset	1	0	0	0	0	0	0	0
Function	Transfer monitor 0: Busy 1: Stop	Transfer software reset 0: - 1: Reset	Transfer mode 00: Send 01: Receive 10: Don't Care 11: Send-receive		Transfer shift 0: Leading edge 1: Trailing edge	Transfer internal clock 0: TBC2 1: TBC6	Transfer clock 0: Internal clock 1: External clock	Transfer control 0: Disable 1: Enable

Serial transfer control

0	Disable
1	Enable

Serial transfer clock control

0	Internal clock
1	External clock

(Note) When using an external clock, set <CLK0SI> to "0".

Serial transfer internal clock select

0	TBC2 (8/fc)
1	TBC6 (128/fc)

Serial transfer shift operation

0	Shifts at leading edge.
1	Shifts at trailing edge.

(Note) In send mode, set to leading edge shift.

Serial transfer mode control

00	Send mode
01	Receive mode
10	Don't use.
11	Send-receive mode

Serial transfer monitor

0	Serial transfer in operation
1	Serial transfer stopped

Serial transfer software reset

0	—
1	Reset (one shot)

Figure 3.15 (5)-1 Serial Channel Related Register

Serial Channel 1 Control Register

SC1MOD (FFE5H)

	7	6	5	4	3	2	1	0
bit Symbol	FF1SI	S1RES	S1MD1	S1MD0	SIFT1	CLK1SI	SCLK1S	SIO1E
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value after reset	1	0	0	0	0	0	0	0
Function	Transfer monitor 0: Busy 1: Stop	Transfer software reset 0: - 1: Reset	Transfer mode 00: Send 01: Receive 10: Don't Care 11: Send-receive		Transfer shift 0: leading edge 1: Trailing edge	Transfer internal clock 0: TBC2 1: TBC6	Transfer clock 0: Internal clock 1: External clock	Transfer control 0: Disable 1: Enable

Serial transfer control

0	Disable
1	Enable

Serial transfer clock control

0	Internal clock
1	External clock

(Note) When using an external clock, set <CLK1SI> to "0".

Serial transfer internal clock select

0	TBC2 (8/fc)
1	TBC6 (128/fc)

Serial transfer shift operation

0	Shifts at leading edge.
1	Shifts at trailing edge.

(Note) In send mode, set to leading edge shift.

Serial transfer mode control

00	Send mode
01	Receive mode
10	Don't use.
11	Send-receive mode

Serial transfer monitor

0	Serial transfer in operation
1	Serial transfer stopped

Serial transfer software reset

0	—
1	Reset (one shot)

Figure 3.15 (5)-2 Serial Channel Related Register

Serial Send-Receive Buffer Register 0

		7	6	5	4	3	2	1	0
SC0BUF (FFE2H)	bit Symbol	RB07	RB06	RB05	RB04	RB03	RB02	RB01	RB00
		TB07	TB06	TB05	TB04	TB03	TB02	TB01	TB00
Prohibit read-modify-write.	Read/Write	R (receive) / W (send)							
	Value after reset	Undefined							

Serial Send-Receive Buffer Register 1

		7	6	5	4	3	2	1	0
SC1BUF (FFE4H)	bit Symbol	RB17	RB16	RB15	RB14	RB13	RB12	RB11	RB10
		TB17	TB16	TB15	TB14	TB13	TB12	TB11	TB10
Prohibit read-modify-write.	Read/Write	R (receive) / W (send)							
	Value after reset	Undefined							

Figure 3.15 (5)-3 Serial Channel Related Register

3.16 Analog / Digital Converter (A/D converter)

TMP91C642A incorporates a high-speed, high-precision 8-bit sequential A/D converter which accepts analog inputs from 12 channels (8 + 4).

The 12 channel analog input pins are also used as ports: P50 to P57 (AN00 to AN07) as input ports and P60 to P63 (AN10 to AN13) as I/O ports.

A/D conversion speed is high: 95 states (19 μs @ fc = 10 MHz).

Figure 3.16 (1) is a block diagram of the A/D converter.

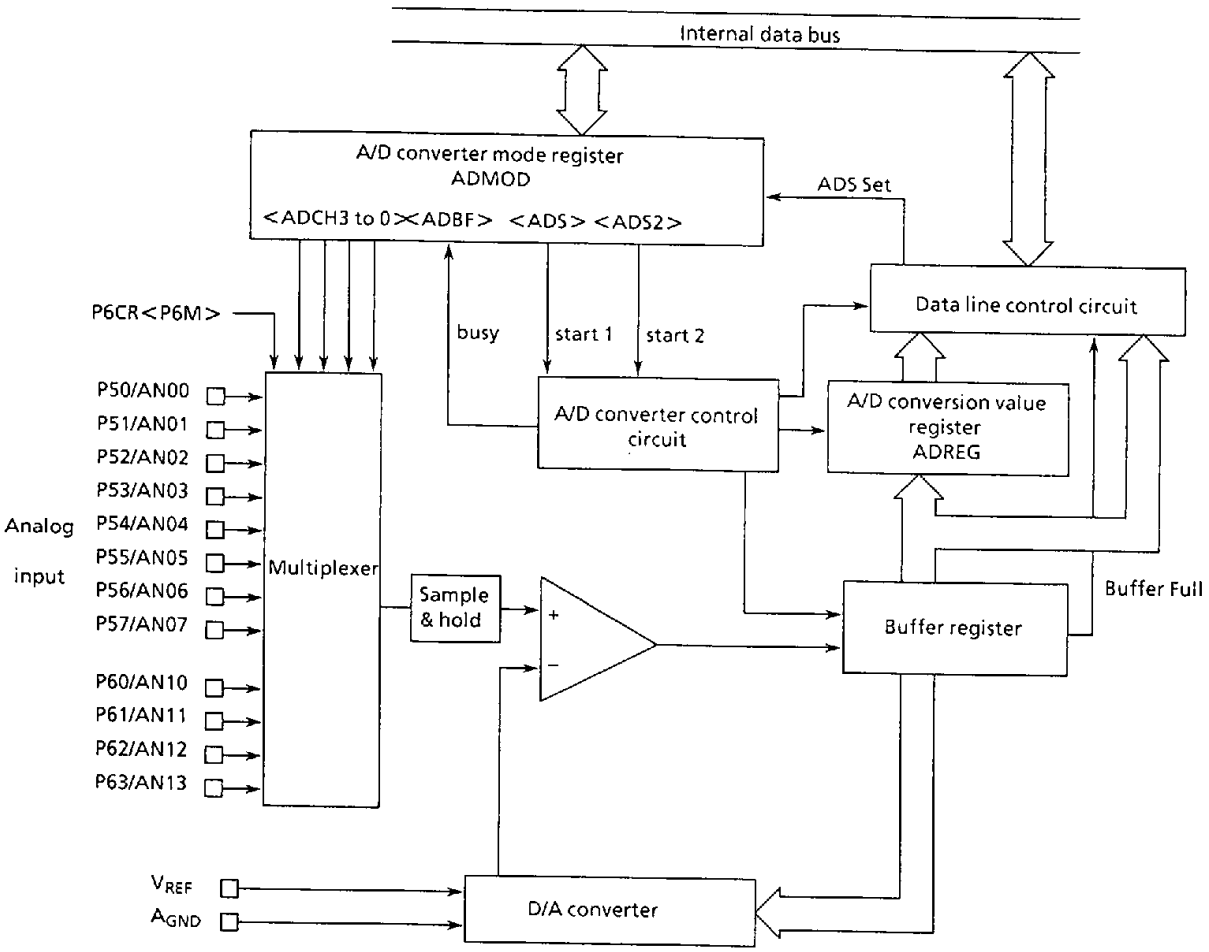


Figure 3.16 (1) A/D Converter Block Diagram

3.16.1 Operation

(1) Analog Reference Voltage

Analog reference voltage on the high side is applied to the VREF pin; on the low side, to the AGND pin.

The reference voltage between VREF and AGND is divided into 256 using a ladder resistor and compared with the analog voltage input for A/D conversion.

(2) A/D conversion mode select

Prior to A/D conversion, the mode must be selected using the A/D conversion mode register, ADMOD.

When ADMOD<ADS2>=0, A/D conversion single mode is selected. When ADMOD<ADS2>=1, A/D conversion repeat mode is selected.

Reset initializes <ADS2>=1, thus selecting repeat mode.

(3) Analog input channel

Using the analog input channel select register, ADMOD<ADCH3 to ADCH0>, one of the 12 channels is selected as the analog input channel: AN00 (P50) to AN07 (P57) and AN10 (P60) to AN13 (P63). When AN10 (P60) to AN13 (P63) are used as ports (P6CR<P6M>=0), the analog input channel must be selected from AN00 to AN07.

Reset initializes the port 6 A/D input control register P6CR<P6M>=0, and the A/D conversion channel register ADMOD<ADCH3,2,1,0>=0,0,0,0; thus selecting the AN00 pin as the analog input channel.

The pins not used as the analog input channel can be used as input port P5 and P60 to P63.

Change analog input channels after A/D conversion.

(4) A/D conversion start

Writing "1" to the A/D conversion start register, ADMOD<ADS>, starts A/D conversion. When A/D conversion is started, the A/D conversion busy flag, ADMOD<ADBF> is set to "1", indicating A/D conversion. When restarting A/D conversion, confirm that the <ADBF> is set to "0".

If A/D conversion is restarted when <ADBF> is set to "1", A/D conversion may stop. Therefore, before restarting A/D conversion, do not forget to check that <ADBF> is set to "0". (Do not write "1" to <ADS> during A/D conversion.)

(5) A/D conversion repeat specification

Repeat or A/D conversion single mode can be selected using the A/D conversion mode register, ADMOD<ADS2>.

In repeat mode, A/D conversion automatically repeats after A/D conversion.

Reset initializes <ADS2> = 1, thus selecting repeat mode. To use A/D conversion single mode, first set <ADS2> = 0, then start A/D conversion.

Change the A/D conversion mode after A/D conversion ends.

(6) A/D conversion end and interrupt

① In A/D conversion single mode

When A/D conversion ends, <ADBF> is cleared to "0". That is, <ADBF> = 0 indicates that conversion ended.

② In A/D conversion repeat mode

To end A/D conversion in A/D conversion repeat mode, write "0" to <ADS2>. A/D conversion repeat mode ends when the conversion in progress ends.

(7) A/D conversion value read

The result of A/D conversion is saved to the A/D conversion value register, ADREG. It can then be read.

Note that reading ADREG during A/D conversion results in an undefined value. (In A/D conversion repeat mode, the latest conversion value is latched in ADREG. Except during the first A/D conversion, ADREG can be read any time.)

In RUN mode, only A/D conversion repeat mode is enabled. That is, A/D conversion is repeatedly performed.

3.16.2 Control Registers

The A/D converter is controlled by the A/D converter mode register, ADMOD, and the port 6 control register, P6CR. The result of A/D conversion is saved in the A/D conversion value register, ADREG.

Figures 3.16 (2) -1 and -2 show A/D converter related registers.

A/D Converter Mode Register

		7	6	5	4	3	2	1	0
ADMOD (FFE0H)	bit Symbol	ADS2	ADBF	ADS	(Note) Always write "0".	ADCH3	ADCH2	ADCH1	ADCH0
	Read/Write	W	R	R/W		R/W			
Prohibit read-modify-write.	Value after reset	1	0	0		0	0	0	0
	Function	A/D conversion repeat control 0: Single 1: Repeat	A/D conversion busy flag 0: Don't Busy 1: Busy	A/D conversion start 0: Stop 1: Start		Analog Input Channel Select			

Analog input channel select

	P6CR<P6M>	
	0	1
0000	AN00	AN00
0001	AN01	AN01
0010	AN02	AN02
0011	AN03	AN03
0100	AN04	AN04
0101	AN05	AN05
0110	AN06	AN06
0111	AN07	AN07
1000	Cannot be used.	AN10
1001		AN11
1010		AN12
1011		AN13
1100		Cannot be used.
1101		
1110		
1111		

A/D conversion repeat control

0	A/D conversion single mode
1	A/D conversion repeat mode

A/D conversion busy flag

0	A/D conversion not busy
1	A/D conversion busy

A/D conversion start

0	No A/D conversion
1	A/D conversion start

(Note) After writing "1" to <ADS>, do not write "1" again.

Figures 3.16 (2) - 1 A/D Converter Related Register

A/D Conversion Value Register

ADREG (FFE1H)

	7	6	5	4	3	2	1	0
bit Symbol								
Read/Write	R							
Value after reset	Undefined							
Function	Saves A/D conversion result.							

Port 6 Control Register

P6CR (FFCDH)

	7	6	5	4	3	2	1	0
bit Symbol		(Note) Always write "0".		P6M	P63C	P62C	P61C	P60C
Read/Write				R/W	R/W			
Value after reset				0	0			
Function				A/D input control 0: Port 1: A/D input	0 : In 1 : Out (Specifies I/O in units of bits.)			

See 3.5.7, Port 6.

Port 6 (P60 to P63) setting

0	Port 6
1	A/D input (AN10 to AN13)

Figure 3.16 (2)-2 A/D Converter Related Register

4. ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

Parameter	Symbol	Pins	Rating	Unit
Power supply voltage	V_{CC}		−0.5 to +6.5	V
Input voltage	V_{IN}		−0.5 to V_{CC} + 0.5	V
Output voltage	V_{OUT}		−0.5 to V_{CC} + 0.5	V
Output current (per 1 pin)	I_{OUT1}	P20	−20	mA
	I_{OUT2}	P00 to P03, P10 to P13, P30 to P34, P40 to P47, P60 to P63	−3	
	I_{OUT3}	P04 to P07, P24 to P27, PW0, PW1	30	
	I_{OUT4}	P20	20	
	I_{OUT5}	P21 to P23	10	
	I_{OUT6}	P00 to P03, P10 to P13, P30 to P34, P40 to P47, P60 to P63	2	
	I_{OUT7}	P37	3.5	
Total Input/Output current (all pins)	ΣI_{OUT1}	Total current for I_{OUT1} and I_{OUT2}.	−60	mA
	ΣI_{OUT2}	Total current for I_{OUT3} to I_{OUT6}.	120	
Power dissipation (T_{OPR} = 70 °C)	P_{DF}	Flat package	500	mW
	P_{DS}	Shrink DIP package	600	
Soldering temperature (time)	T_{SOLDER}		260 (10 s)	°C
Storage temperature	T_{STG}		−65 to +150	°C
Operating temperature	T_{OPR}		−20 to +70	°C

4.2 DC Electrical Characteristics

V_{CC} = 5 V ± 10 % Ta = − 20 to 70 °C f_{OSC} = 10 MHz
Typical values are when V_{CC} = 5 V and Ta = 25 °C.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}	− 0.3		0.3V_{CC}	V	
	V_{IL1}	− 0.3		0.25V_{CC}	V	Schmitt input circuit P33 to P35, P64 to P67, $\overline{RESET}$
	V_{IL2}	− 0.3		0.2V_{CC}	V	X1
Input High Voltage	V_{IH}	0.7V_{CC}		V_{CC} + 0.3	V	
	V_{IH1}	0.75V_{CC}		V_{CC} + 0.3	V	Schmitt input circuit P33 to P35, P64 to P67, $\overline{RESET}$
	V_{IH2}	0.8V_{CC}		V_{CC} + 0.3	V	X1
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.6 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = − 200 μA
	V_{OH1}	0.9V_{CC}			V	I_{OH} = − 20 μA
Output Low Current (open drain ports)	I_{OL1}		2		mA	V_{OL} = 0.45 V / P37
	I_{OL2}		20		mA	V_{OL} = 1.0 V / P04 to P07, P24 to P27, PW0, PW1
	I_{OL3}		5		mA	V_{OL} = 0.45 V / P21 to P23
Output Low Current	I_{OLC}	10	15		mA	V_{OL} = 1.0 V / P20
Output High Current	I_{OHC}		− 15	− 10	mA	V_{OH} = 2.4 V / P20
Hysteresis Voltage	V_{HS}		0.7		V	V_{CC} = 5 V, Ta = 25 °C
Input Leakage Current	I_{LI}		0.02	± 10	μA	0.2 ≦ Vin ≦ VCC − 0.2
Output Leakage Current	I_{LO}		0.05	± 20	μA	0.2 ≦ Vin ≦ VCC − 0.2
Power Down Voltage	V_{STOP}	2 RAM BACK UP		6	V	at STOP Mode
$\overline{RESET}$ pull-up current	I_{RST}	30		110	μA	
Operating Current	I_{CC1}		15	50	mA	f_{OSC} = 10 MHz

4.3 AC Electrical Characteristics

V_{CC} = 5 V ± 10 % Ta = − 20 to 70 °C

Symbol	Item	10 MHz Clock		Unit
		Min	Max	
t_{OSC}	OSC. Period	100		ns

4.4 8-bit Event Counter

V_{CC} = 5 V ± 10 %, Ta = − 20 to 70 °C

Symbol	Parameter	10 MHz Clock		Unit
		Min	Max	
t_{VCK}	External input clock cycle (TI0, TI1, C-FG, PCTL)	900		ns
t_{VCKL}	External input Low clock pulse width	440		ns
t_{VCKH}	External input High clock pulse width	440		ns

4.5 Serial Channel Timing

V_{CC} = 5 V ± 10 % Ta = − 20 to 70 °C C_L = 50 pF

Symbol	Parameter	Condition	10 MHz Clock		Unit
			Min	Max	
t_{SCY}	Serial Port Clock Cycle Time	@TBC2 (8/fc) Internal	800		ns
		@TBC6 (128/fc)	12800		
		External	1600		
t_{SCL}	SCLK Low Width	@TBC2 (8/fc) Internal	350		ns
		@TBC6 (128/fc)	6350		
		External	750		
t_{SCH}	SCLK High Width	@TBC2 (8/fc) Internal	350		ns
		@TBC6 (128/fc)	6350		
		External	750		
t_{SKDO}	SCLK → TxD (Output Data) delay time	Internal	150		ns
		External	700		
t_{SRD}	SCLK Rising Edge to Input DATA Valid	Internal	640		ns
		External	1900		
t_{HSR}	Input Data Hold After SCLK Rising Edge	Internal	200		ns
		External	700		

4.6 A/D Conversion Characteristics

V_{CC} = 5 V ± 10 %, Ta = − 20 to 70 °C, f_{OSC} = 10 MHz

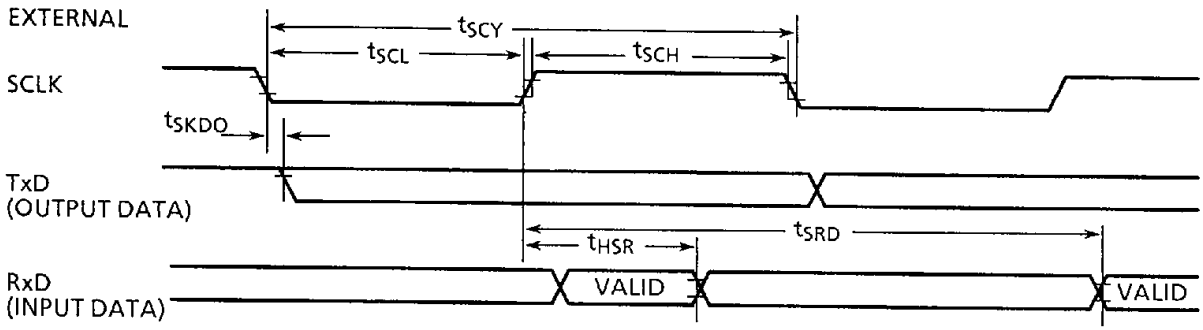
Symbol	Parameter	Min	Typ	Max	Unit
V_{REF}	Analog reference voltage	Vcc − 1.5	Vcc	Vcc	V
A_{GND}	Analog reference voltage	V_{SS}	V_{SS}	Vss	
V_{AIN}	Allowable analog input voltage	V_{SS}		Vcc	
I_{REF}	Supply current for analog reference voltage		0.6	1.0	mA
Error	Total error (Ta = 25 °C, Vcc = VREF = 5 V)			3	LSB

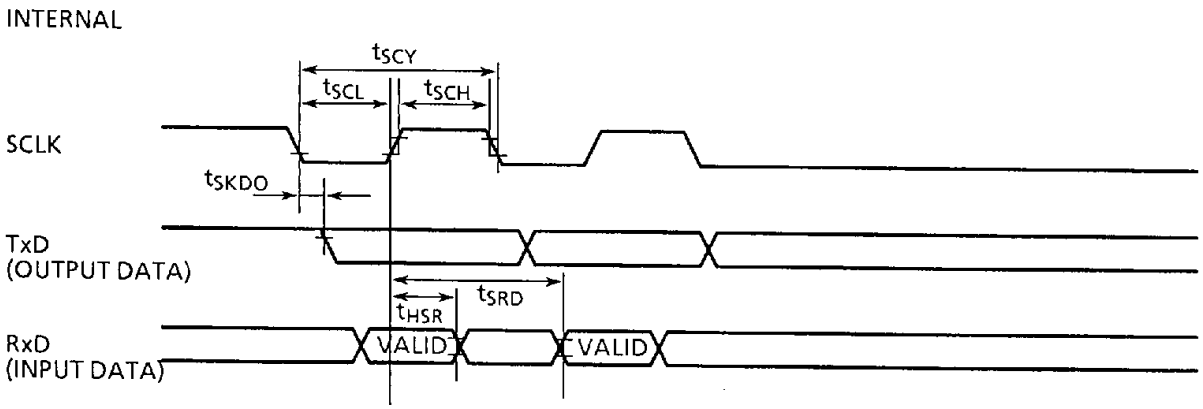
4.7 Interrupt Operation

V_{CC} = 5 V ± 10 %, Ta = − 20 to 70 °C

Symbol	Parameter	10MHz Clock		Unit
		Min	Max	
t_{INTAL}	INT0 Low-level pulse width (⌐‾¬)	400		ns
t_{INTAH}	INT0 High-level pulse width (_⌐¬_)	400		ns
t_{INTBL}	INT1, INT2 Low-level pulse width (⌐‾¬)	900		ns
t_{INTBH}	INT1, INT2 High-level pulse width (_⌐¬_)	900		ns

4.8 Serial Channel Timing Charts





5. TABLE OF SPECIAL FUNCTION REGISTERS (SFR)

Special function registers (SFR) are registers used to control I/O ports and peripherals. They are assigned to the 64-byte address space from 0FFC0H to 0FFFFH.

1) I/O port
2) I/O port control
3) Watchdog timer/time base counter/interrupt control
4) Servo input control
5) P-CTL (VISS / VASS) / C-Sync control
6) Capture control
7) TPG control
8) Timer / PWM control
9) Serial channel control
10) A/D converter control

Table configuration

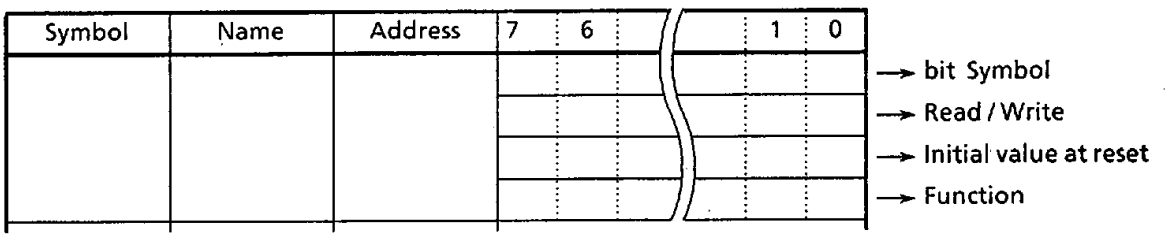


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Table of TMP91C642A SFR Addresses

Address	Symbol	Address	Symbol	Address	Symbol	Address	Symbol
FFC0	P0	FFD0	TREG0 (TCUT0)	FFE0	ADMOD	FFF0	PCFCR1
FFC1	P0CR	FFD1	TREG1 (TCUT1)	FFE1	ADREG	FFF1	PCDFCR
FFC2	P1	FFD2	TCLK (TMR01CR)	FFE2	SC0BUF	FFF2	PCFSCR
FFC3	P1CR	FFD3	TCUT2	FFE3	SC0MOD	FFF3	PCTLD
FFC4	P2	FFD4	TREG2	FFE4	SC1BUF	FFF4	TPO0DAR0(TPO1DAR0)
FFC5	P2CR	FFD5	TMR2CR	FFE5	SC1MOD	FFF5	TPO0DAR1(TPO1DAR1)
FFC6	P3	FFD6	TCUT3	FFE6	WDMOD	FFF6	TPC0DAR0(TPC1DAR0)
FFC7	P3CR	FFD7	TREG3	FFE7	WDCR	FFF7	TPC0DAR1(TPC1DAR1)
FFC8	P4	FFD8	TMR3CR	FFE8	TBMOD	FFF8	TPGREG0
FFC9	P4CR	FFD9	TFFCR	FFE9	INTEL	FFF9	TPGREG1
FFCA	P4MR	FFDA	TRUN	FFEA	INTEH (DMAEL)	FFFA	CAPREG0
FFCB	P5	FFDB	PWM8DR	FFEB	DMAEH	FFFB	CAPREG1
FFCC	P6	FFDC	PWMDR0	FFEC	IRFL	FFFC	CAPREG2
FFCD	P6CR	FFDD	PWMDR0B	FFED	IRFH	FFFD	CAPFST
FFCE	SINCR	FFDE	PWMDR1	FFEE	SSINCR1	FFFE	SVCFREG
FFCF	SYNCDV	FFDF	PWMDR1B	FFEF	CSYNCR	FFFF	SSINCR2

1) I/O port

Symbol	Name	Address	MSB 7	6	5	4	3	2	1	LSB 0
P0	Port0	0FFC0H	P07	P06	P05	P04	P03	P02	P01	P00
		(Prohibit RMW)	R/W							
			Input mode							
			Also used for TPG output (TPG0-0 to TPG0-7) / 3-state output only for P00							
P1	Port1	0FFC2H					P13	P12	P11	P10
		(Prohibit RMW)					R/W			
							Input mode			
							Also used for TPG output (TPG0-8 to 0-11/TPG1-8 to 1-11) / 3-state output only for P10			
P2	Port2	0FFC4H	P27	P26	P25	P24	P23	P22	P21	P20
		(Prohibit RMW)	R/W							
			Input mode							
			Also used for TPG output (TPG1-0 to TPG1-7) / 3-state output only for P20							
P3	Port3	0FFC6H	P37	P36	P35	P34	P33	P32	P31	P30
			R/W *1	R		R/W				
			PWM8 output	Input only		Input mode				
			Also used for TO1 / PWM8	Also used for INT1	Also used for INT0	Also used for EXT	Also used for C-Sync			
P4	Port4	0FFC8H	P47	P46	P45	P44	P43	P42	P41	P40
			R/W							
			Input mode							
			Also used for TI1	Also used for TI0/INT2	Also used for RxD1	Also used for TxD1	Also used for SCLK1	Also used for RxD0	Also used for TxD0	Also used for SCLK0
P5	Port5	0FFCBH	P57	P56	P55	P54	P53	P52	P51	P50
			R							
			Input only							
			Also used for analog input pin (AN00 to AN07)							
P6	Port6	0FFCCH	P67	P66	P65	P64	P63	P62	P61	P60
			R				R/W			
			Input only				Input mode			
			Also used for servo signal trigger input (CAP0 to CAP3)				Also used for analog input pin (AN10 to AN13)			

*1) <P37> data can be read from the port output latch. The port is for output only.

(Note) Read / Write

R / W : Either read or write is possible.

R : Only read is possible.

W : Only write is possible.

Prohibit RMW : Prohibit read-modify-write. (RES or SET instruction cannot be used.)

2) I/O port control

MSB LSB

Symbol	Name	Address	7	6	5	4	3	2	1	0
P0CR	Port0 Control Reg.	0FFC1H						P2S	P0S	P0C
								W	W	W
								0	0	0
		(Prohibit RMW)						Output of P20 3-state (TPG1-15 control) 0 : Disable 1 : Enable	Output of P00 3-state (TPG0-15 control) 0 : Disable 1 : Enable	P0 control 0 : In 1 : Out
P1CR	Port1 Control Reg.	0FFC3H		(Note) Always write "0".	TPG1M	P1S	P13C	P12C	P11C	P10C
					W	W	W			
					0	0	0			
		(Prohibit RMW)			TPG output control 0 : TPG0 1 : TPG1	Output of P10 3-state (TPG0-14 / TPG1-14 control) 0 : Disable 1 : Enable	0 : In 1 : Out (Specifies I/O in units of bits)			
P2CR	Port2 Control Reg.	0FFC5H	P27C	P26C	P25C	P24C	P23C	P22C	P21C	P20C
			W							
		(Prohibit RMW)	0							
			0 : In				1 : Out (Specifies I/O in units of bits)			
P3CR	Port3 Control Reg.	0FFC7H		P37M	P35M	P34C	P33C	P32C	P31C	P30C
				R/W	R/W			R/W		
				0	0			0		
				P37 function control 0 : PWM8/TO1 1 : Port	INT0 control 0 : level 1 : ↑ edge			0 : In 1 : Out (Specifies I/O in units of bits)		
P4CR	Port4 Control Reg.	0FFC9H	P47C	P46C	P45C	P44C	P43C	P42C	P41C	P40C
			R/W							
			0							
			0 : In				1 : Out (Specifies I/O in units of bits)			
P4MR	Port4 Mode Control Reg.	0FFCAH					P45M	P44M	P42M	P41M
							R/W	R/W	R/W	R/W
							0	0	0	0
							SIO1 receive control 0 : Port 1 : RxD1	SIO1 send control 0 : Port 1 : TxD1	SIO0 receive control 0 : Port 1 : RxD0	SIO0 send control 0 : Port 1 : TxD0
P6CR	Port6 Control Reg.	0FFCDH		(Note) Always write "0".		P6M	P63C	P62C	P61C	P60C
						R/W	R/W			
						0	0			
						A/D input control 0 : Port 1 : A/D input	0 : In 1 : Out (Specifies I/O in units of bits)			
SINCR	Servo Input Control Reg.	0FFCEH			C-Sync	EXT	P-CTL	C-FG	D-PG	D-FG
					R/W	R/W	R/W	R/W	R/W	R/W
					0	0	0	0	0	0
					Servo Input Singnal 0 : Enable 1 : Disable					

3) Watchdog / time base counter / interrupt control

Symbol	Name	Address	MSB 7	6	5	4	3	2	1	LSB 0
WDMOD	Watch Dog Timer Mode Reg.	0FFE6H		FTBC2	FTBC1	WDTE	FTPG	HALT	EXF	DRVE
				R/W	R/W	R/W	R/W	R/W	R	R/W
				0	0	1	0	0	Undefined	0
				1 : TBC15 to 18 interrupt flag	1 : TBC11 to 14 interrupt flag	1 : WDT Enable	1 : TPG0 to 13 interrupt flag	HALT mode 0 : RUN mode 1 : STOP mode	Inverted by execution of the EXX instruction.	1 : Drives pin in STOP mode.
WDCR	Watch Dog Timer Control Reg.	0FFE7H								
									W	
									–	
									81H : WDT Disable Code 4EH : WDT Clear Code	
TBMOD	Time Base Counter Mode Reg.	0FFE8H		TBCCLR	INTS2	INTS1	INTTBC2		INTTBC1	
				R/W	R/W	R/W	R/W		R/W	
				0	0	0	0	0	0	0
				TBC clear 0 : – 1 : Clear	TBC interrupt enable register 00 : Disable 01 : INT TBC1 10 : INT TBC2 11 : INT TBC1 & INT TBC2		TBC interrupt source select 2 00 : TBC15 01 : TBC16 10 : TBC17 11 : TBC18		TBC interrupt source select 1 00 : TBC11 01 : TBC12 10 : TBC13 11 : TBC14	
INTEL	Interrupt Enable Mask Reg.	0FFE9H	ENISIO	ENIT0	ENIT1	ENIT2	ENIT3	ENITB	ENI1	ENI2VA
				R/W						
			0	0	0	0	0	0	0	0
				1 : Enable			0 : Disable			
INTEH (DMAEL)	Interrupt Enable Mask Reg.	0FFEAH	(Note) Always write "0".	DE0	DECAP	* DEAD	INT2S	ENI0	ENICAP	* ENIAD
				R/W			R/W			
				0	0	0	0	0	0	0
				1 : Enable 0 : Disable			0 : INTVA 1 : INT2	1 : Enable 0 : Disable		
DMAEH	Micro DMA Enable Flag	0FFEBH	(Note) Always write "0".	DET0	DET1	DET2	DET3	DETB	DE1	DE2VA
				R/W						
				0	0	0	0	0	0	0
				1 : Enable				0 : Disable		
IRFL	Interrupt Request Flag	0FFECH		IRF0	IRFCAP	* IRFAD			SIO1F	SIO0F
				R					R	R
				0	0	0			0	0
				Interrupt request flag 1 : Interrupt being requested					1 : SIO1 Request	1 : SIO0 Request
IRFH		0FFEDH	IRFSIO	IRFT0	IRFT1	IRFT2	IRFT3	IRFTB	IRF1	IRF2VA
				R (Only IRF clear code can be used to write.)						
		(Prohibit PMW)	0	0	0	0	0	0	0	0
				1 : Interrupt being requested. (IRF is cleared to "0" by writting IRF clear code.)						

(DMAEL) is a synonym for INTEH.
* : INTAD cannot be used.

4) Servo input control

Symbol	Name	Address	MSB 7	6	5	4	3	2	1	LSB 0
SINCR	Servo Input Control Reg.	0FFCEH			C-Sync	EXT	P-CTL	C-FG	D-PG	D-FG
					R/W	R/W	R/W	R/W	R/W	R/W
					0	0	0	0	0	0
					Servo Input Signal 0 : Enable 1 : Disable					
SSINCR1	Servo Signal Control Reg.1	0FFEEH		EXTPO	DFGPO	CFWPR	CFWEG	DPFG	DPGPO	DPGIN
				W	W	W	W	W	W	R
				0	0	0	0	0	0	0
		(Prohibit RMW)		EXT Edge Detection 0 : ↑ 1 : ↓	DFG Edge Detection 0 : ↑ 1 : ↓	CFG frequency division Selector 0 : 1 1 : 1/2	CFG Edge Detection 0 : ↑↓ 1 : ↑	DFG/DPG Sync register 0 : Disable 1 : Enable	DPG Edge Detection 0 : ↑ 1 : ↓	DPG Edge Detect Flag 1 : D-PG edge detect
SSINCR2	Servo Signal Control Reg.2	0FFFFH					TP	DFMA	PB	CFGMCP
							R/W	R/W	R/W	R
							0	0	0	Undefined
							TPG0/TPG1 Reg. Control 0 : TPG0 1 : TPG1	*1	*2	CFG Malfunction Flag 1 : Malfunction detect
CSYNCR	C-Sync Control Reg.	0FFEFH	CSYNCF	TPGF	PCTPO	OEDR	NPS	CTLDTY	VISSFL	VASSFL
			R/W	R/W	W	R	R	R	R	R
			0	0	0	0	0	0	0	0
		(Prohibit RMW)	V-Sync Detection Flag 1 : V-Sync *3	Pseudo V Detection Flag 1 : embedded *3	PCTL Signal Control 0 : Forward 1 : Reverse	Odd/even discrimination result 0 : Odd 1 : Even	60/50 discrimination result 0 : 60 1 : 50	P-CTL Duty 0 : ≤ 50% 1 : ≥ 50%	VISS detect flag 0 : – 1 : VISS data	VASS detect flag 0 : – 1 : VASS data
SVCFREG	Servo Flag Control Reg.	0FFFEH	VISFRS	VASFRS	TPFRS1	TPFRS0	CFGFRS	DPGFRS	CASFWR	CAFRS
			R/W (Always "0" at read.)							
			0	0	0	0	0	0	0	0
			VISS Status Flag 0 : – 1 : Clear	VASS Status Flag 0 : – 1 : Clear	TPG1 FIFO Counter 0 : – 1 : Reset	TPG0 FIFO Counter 0 : – 1 : Reset	C-FG Malfunction Flag 0 : – 1 : Clear	D-PG Input Status Flag 0 : – 1 : Clear	Software Capture 0 : – 1 : Capture	Capture FIFO Counter 0 : – 1 : Reset
PCFCR1	C-FG Mask /VISS Control Reg.	0FFF0H	CFMSK3	CFMSK2	CFMSK1	CFMSK0	VISS3	VISS2	VISS1	VISS0
			W				W			
		(Prohibit RMW)	0	0	0	0	0	0	0	0
			C-FG Mask Time Control				VISS discrimination control			
PCDFCR	P-CTL /D-FG Control Reg.	0FFF1H	DFGPR2	DFGPR1	DFGPR0	PCTPR4	PCTPR3	PCTPR2	PCTPR1	PCTPR0
			W			W				
		(Prohibit RMW)	0	0	0	0	0	0	0	0
			D-FG 3bit Prescaler Control			P-CTL 5bit Prescaler Control				
PCFSCR	P-CTL /C-FG Signal Control Reg.	0FFF2H	DVS	PCTLCK2	PCTLCK1	CFGPR4	CFGPR3	CFGPR2	CFGPR1	CFGPR0
			W	W		W				
			0	0	0	0	0	0	0	0
		(Prohibit RMW)	SYNCDV Reg. Select 0 : VPD. SYNC 1 : FEP	PCTL Duty Detection Input Clock 00 : TBC2 10 : TBC6 01 : TBC4 11 : TBC8		C-FG 5bit Prescaler Control				

*1 : Input signal control for 60/50 field discrimination 0 : TPG0-1 (D-FF) 1 : TPG1-13 (embedded VP)

*2 : Output control of V-Sync detector 0 : Enable 1 : Disable

*3 : Write "1" after read.

5) P-CTL (VISS / VASS) / C-Sync control

Symbol	Name	Address	MSB 7	6	5	4	3	2	1	LSB 0
PCFCR1	C-FG Mask / VISS Control Reg.	0FFF0H (Prohibit RMW)	CFMSK3	CFMSK2	CFMSK1	CFMSK0	VISS3	VISS2	VISS1	VISS0
			W				W			
			0	0	0	0	0	0	0	0
			C-FG Mask Time Control				VISS discrimination control			
PCFSCR	P-CTL /C-FG Signal Control Reg.	0FFF2H (Prohibit RMW)	DVS	PCTLCK2	PCTLCK1	CFGPR4	CFGPR3	CFGPR2	CFGPR1	CFGPR0
			W	W			W			
			0	0	0	0	0	0	0	0
			SYNCDV Reg. Select 0 : VPD, SYNC 1 : FEP	PCTL Duty Detection Input Clock 00 : TBC2 10 : TBC6 01 : TBC4 11 : TBC8		C-FG 5bit Prescaler Control				
SYNCDV	C-Sync Input Control Reg.	0FFCFH (<DVS> = 0) (Prohibit RMW)		SYNP02	SYNP01	SYNP00	VPP04	VPP03	VPP02	VPP01
				W			W			
				0	0	0	0	0	0	0
				C-Sync mask control			C-Sync frequency divider control			
	Even / Odd Sampling Control Reg.	(<DVS> = 1) (Prohibit RMW)						FEP02	FEP01	FEP00
								W		
								0	0	0
								Even / Odd judgement		
PCTLD	VASS Data Reg.	0FFF3H ①	VASS7	VASS6	VASS5	VASS4	VASS3	VASS2	VASS1	VASS0
			R							
			0	0	0	0	0	0	0	0
			VASS Data Low Byte							
		②	VASSF	VASSE	VASSD	VASSC	VASSB	VASSA	VASS9	VASS8
			R							
			0	0	0	0	0	0	0	0
			VASS Data High Byte							
CSYNCR	C-Sync Control Reg.	0FFEFH (Prohibit RMW)	CSYNCF	TPGF	PCTPO	OEDR	NPS	CTLDTY	VISSFL	VASSFL
			R/W	R/W	W	R	R	R	R	R
			0	0	0	0	0	0	0	0
			V-Sync Detection Flag 1 : V – Sync *3	Pseudo V detection flag 1 : Embedded *3	PCTL Signal Control 0 : Forward 1 : Reverse	Odd/even discriminati on result 0 : Odd 1 : Even	60/50 discriminati on result 0 : 60 1 : 50	P-CTL Duty 0 : ≤ 50% 1 : > 50%	VISS detect flag 0 : – 1 : VISS data	VASS detect flag 0 : – 1 : VASS data
SVCFREG	Servo Flag Control Reg.	0FFFEH	ViSFRS	VASFRS	TPFRS1	TPFRS0	CFGFRS	DPGFRS	CASFWR	CAFRS
			R/W (Always "0" at read.)							
			0	0	0	0	0	0	0	0
			ViSS Status Flag 0 : – 1 : Clear	VASS Status Flag 0 : – 1 : Clear	TPG1 FIF0 Counter 0 : – 1 : Reset	TPG0 FIF0 Counter 0 : – 1 : Reset	C-FG Malfunction Flag 0 : – 1 : Clear	D-PG Input Status Flag 0 : – 1 : Clear	Software Capture 0 : – 1 : Capture	Capture FIF0 Counter 0 : – 1 : Reset
SSINCR2	Servo Signal Control Reg.2	0FFFFH					TP	DFMA	PB	CFGMCP
							R/W	R/W	R/W	R
							0	0	0	Undefined
							TPG0 / TPG1 Reg. Control 0 : TPG0 1 : TPG1	*1	*2	CFG Malfunction Flag 1 : Malfunction detect

*1 : Input signal control for 60/50 field discrimination 0 : TPG0-1 (D-FF) 1 : TPG1-13 (embedded VP)

*2 : Output control of V-Sync detector 0 : Enable 1 : Disable

*3 : Write "1" after read.

6) Capture control

Symbol	Name	Address	MSB 7	6	5	4	3	2	1	LSB 0
CAPFST	Capture FIFO Status Reg.	0FFFDH	CAPF7	CAPF6	CAPF5	CAPF4	CAPF3	CAPF2	CAPF1	CAPF0
			R							
			0	0	0	0	0	0	0	0
			0 : No data					1 : Data		
CAPREG0	Capture Data0 Reg.	0FFFAH	CAPD7	CAPD6	CAPD5	CAPD4	CAPD3	CAPD2	CAPD1	CAPD0
			R							
			Undefined							
			Capture Data Low Byte							
CAPREG1	Capture Data1 Reg.	0FFF8H	CAPD15	CAPD14	CAPD13	CAPD12	CAPD11	CAPD10	CAPD9	CAPD8
			R							
			Undefined							
			Capture Data Middle Byte							
CAPREG2	Capture Data2 Reg.	0FFFCH	EXT	P-CTL	D-PG	C-SYNC	C-FG	D-FG	CAPD17	CAPD16
			R						R	
			Undefined						Undefined	
			Capture Input Status						Capture Data High Byte	
SVCFREG	Servo Flag Control Reg.	0FFFEH	VISFRS	VASFRS	TPFRS1	TPFRS0	CFGFRS	DPGFRS	CASFWR	CAFRS
			R/W (Always "0" at read.)							
			0	0	0	0	0	0	0	0
			VISS Status Flag 0: – 1: Clear	VASS Status Flag 0: – 1: Clear	TPG1 FIFO Counter 0: – 1: Reset	TPG0 FIFO Counter 0: – 1: Reset	C-FG Malfunction Flag 0: – 1: Clear	D-PG Input Status Flag 0: – 1: Clear	Software Capture 0: – 1: Capture	Capture FIFO Counter 0: – 1: Reset

7) TPG control (1/2)

Symbol	Name	Address	MSB 7	6	5	4	3	2	1	LSB 0
TPGREG0	TPG0 Status Reg.	0FFF8H			EMPINT0	TPFUL0	TPEMP0	TPF02	TPF01	TPF00
					W	R	R	R		
					0	0	1	0	0	0
		(Prohibit RMW)			TPG0 Data Empty Interrupt Control 0: Disable 1: Enable	TPG0 Data Full Flag 0: – 1: Full	TPG0 Data Empty Flag 0: – 1: Empty	TPG0 FIFO Status Flag 000 empty/full 100 data 4 001 data 1 101 data 5 010 data 2 110 data 6 011 data 3 111 data 7 Empty when <TPEMP0> = 1 and the flag = 000 Full when <TPFUL0> = 1 and the flag = 000		
TPGREG1	TPG1 Status Reg.	0FFF9H			EMPINT1	TPFUL1	TPEMP1	TPF12	TPF11	TPF10
					W	R	R	R		
					0	0	1	0	0	0
		(Prohibit RMW)			TPG1 Data Empty Interrupt Control 0: Disable 1: Enable	TPG1 Data Full Flag 0: – 1: Full	TPG1 Data Empty Flag 0: – 1: Empty	TPG1 FIFO Status Flag 000 empty/full 100 data 4 001 data 1 101 data 5 010 data 2 110 data 6 011 data 3 111 data 7 Empty when <TPEMP1> = 1 and the flag = 000 Full when <TPFUL1> = 1 and the flag = 000		

7) TPG control (2/2)

Symbol	Name	Address	MSB 7	6	5	4	3	2	1	LSB 0
TPC0DAR0	TPG Comparate Data Reg.0	0FFF6H (<TP> = 0)	TPC07	TPC06	TPC05	TPC04	TPC03	TPC02	TPC01	TPC00
		(Prohibit RMW)	W							
			Undefined							
			TPG0-0 to TPG0-7 comparate data register							
TPC1DAR0		0FFF6H (<TP> = 1)	TPC17	TPC16	TPC15	TPC14	TPC13	TPC12	TPC11	TPC10
		(Prohibit RMW)	W							
			Undefined							
			TPG1-0 to TPG1-7 comparate data register							
TPC0DAR1	TPG Comparate Data Reg.1	0FFF7H (<TP> = 0)	TPC0F	TPC0E	TPC0D	TPC0C	TPC0B	TPC0A	TPC09	TPC08
		(Prohibit RMW)	W							
			Undefined							
			TPG0-8 to TPG0-15 comparate data register							
TPC1DAR1		0FFF7H (<TP> = 1)	TPC1F	TPC1E	TPC1D	TPC1C	TPC1B	TPC1A	TPC19	TPC18
		(Prohibit RMW)	W							
			Undefined							
			TPG1-8 to TPG1-15 comparate data register							
TPO0DAR0	TPG Output Data Reg.0	0FFF4H (<TP> = 0)	TPO07	TPO06	TPO05	TPO04	TPO03	TPO02	TPO01	TPO00
		(Prohibit RMW)	W							
			Undefined							
			TPG0-0 to TPG0-7 output data register							
TPO1DAR0		0FFF4H (<TP> = 1)	TPO17	TPO16	TPO15	TPO14	TPO13	TPO12	TPO11	TPO10
		(Prohibit RMW)	W							
			Undefined							
			TPG1-0 to TPG1-7 output data register							
TPO0DAR1	TPG Output Data Reg.1	0FFF5H (<TP> = 0)	TPO0F	TPO0E	TPO0D	TPO0C	TPO0B	TPO0A	TPO09	TPO08
		(Prohibit RMW)	W							
			Undefined							
			TPG0-8 to TPG0-15 output data register							
TPO1DAR1		0FFF5H (<TP> = 1)	TPO1F	TPO1E	TPO1D	TPO1C	TPO1B	TPO1A	TPO19	TPO18
		(Prohibit RMW)	W							
			Undefined							
			TPG1-8 to TPG1-15 output data register							
SVCFREG	Servo Flag Control Reg.	0FFFEH	VISFRS	VASFRS	TPFRS1	TPFRS0	CFGFRS	DPGFRS	CASFWR	CAFRS
			R/W (Always "0" at read.)							
			0	0	0	0	0	0	0	0
			VISS Status Flag 0 : – 1 : Clear	VASS Status Flag 0 : – 1 : Clear	TPG1 FIF0 Counter 0 : – 1 : Reset	TPG0 FIF0 Counter 0 : – 1 : Reset	C-FG Malfunction Flag 0 : – 1 : Clear	D-FG Input Status Flag 0 : – 1 : Clear	Software Captur 0 : – 1 : Capture	Capture FIF0 Counter 0 : – 1 : Reset
SSINCR2	Servo Signal Control Reg. 2	0FFFFH					TP	DFMA	PB	CFGMCP
							R/W	R/W	R/W	R
							0	0	0	Undefined
							TPG0 / TPG1 Reg. Control 0 : TPG0 1 : TPG1	*1	*2	CFG Malfunction Flag 1: Malfunction detect

*1 : Input signal control for 60/50 field discrimination 0 : TPG0-1 (D-FF) 1 : TPG1-13 (embedded VP)

*2 : Output control of V-Sync detector 0 : Enable 1 : Disable

8) Timer / PWM control (1/2)

MSB LSB

Symbol	Name	Address	7	6	5	4	3	2	1	0
TREG0 (TCUT0)	8bit Timer Reg.0	0FFD0H (Prohibit RMW)	–							
			W							
			Undefined							
	8bit Timer Count Data Reg.0	0FFD0H (Prohibit RMW)	–							
			R							
			Undefined							
TREG1 (TCUT1)	8bit Timer Reg.1	0FFD1H (Prohibit RMW)	–							
			W							
			Undefined							
	8bit Timer Count Data Reg.1	0FFD1H (Prohibit RMW)	–							
			R							
			Undefined							
TCLK (TMR01CR)	Timer0, 1 Control Reg.	0FFD2H	CLBC16	CLBC1	CLBC0	TMOD	T1CLK1	T1CLK0	T0CLK1	T0CLK0
			R/W	R/W	R/W	R/W	R/W		R/W	
			0	0	0	0	0	0	0	0
			16-bit timer/counter clear control 0 : Disable 1 : Enable	Timer 1 counter clear control 0 : Disable 1 : Enable	Timer 0 counter clear control 0 : Disable 1 : Enable	Timer Mode 0 : 8bit 1 : 16bit	Timer 1 CLK-in control 00 : TO0TRG 01 : TBC2 10 : TBC6 11 : TBC10		Timer 0 CLK-in control 00 : TBC2 01 : TBC6 10 : TBC10 11 : TI0	
TCUT2	8bit Timer Count Data Reg.2	0FFD3H	–							
			R							
			Undefined							
TREG2	8bit Timer Reg.2	0FFD4H (Prohibit RMW)	–							
			W							
			Undefined							
TMR2CR	Timer 2 Control Reg.	0FFD5H					CLBC21	CLBC20	T2CLK1	T2CLK0
							R/W	R/W	R/W	
							0	0	0	0
							Counter clear control 0 : Disable 1 : Enable	Counter software clear 0 : – 1 : Clear	Timer 2 CLK-in control 00 : TBC2 01 : TBC6 10 : TI0 11 : C-FG	
TCUT3	8bit Timer Count Data Reg.3	0FFD6H	–							
			R/W							
			Undefined							
TREG3	8bit Timer Reg.3	0FFD7H (Prohibit RMW)	–							
			W							
			Undefined							
TMR3CR	Timer3 Control Reg.	0FFD8H		INTC1	INTC0	CLBC31	CLBC30	UDCON	T3CLK1	T3CLK0
				R/W		R/W	R/W	R/W	R/W	
				0	0	0	0	0	0	0
				INTT3 interrupt control 00 : Disable INT 01 : Match detect signal output 10 : Overflow 11 : Match detect signal output and overflow		Counter clear control 0 : Disable 1 : Enable	Counter Soft Clear 0 : – 1 : Clear	Counter up/down control 0 : Up 1 : Down	Timer 3 CLK-in control 00 : TBC2 01 : TBC6 10 : TI1 11 : PCTL	

8) Timer / PWM control (2/2)

Symbol	Name	Address	MSB 7	6	5	4	3	2	1	LSB 0
TFFCR	8bit Timer Flip-Flop Control Reg.	0FFD9H	(Note) Always write "0".			TOSEL	TFFC1	TFFC0	TFFIE	TFFIS
						R/W	W		R/W	
						0	–		0	0
		(Prohibit RMW)				P37 output select 0 : PWM8 1 : TO1	TFF control 00 : Clear TFF 01 : Set TFF 10 : Invert TFF 11 : Don't care		TFF Invert 0 : Diable 1 : Enable	0 : Inverted by timer 0 1 : Inverted by timer 1
TRUN	Timer & PWM Run / Stop Control Reg.	0FFDAH		RUNPW1	RUNPW0	RUNPW8	T3RUN	T2RUN	T1RUN	T0RUN
				R/W	R/W	R/W	R/W	R/W	R/W	R/W
				0	0	0	0	0	0	0
				PW0, 1 Run/Stop Control 0 : Stop 1 : Run (Count up)		PWM8 Run/Stop Control 0 : Stop & Clear 1 : Run (Count up)	Timer Run/Stop Control 0 : Stop 1 : Run		Timer Run/Stop Control 0 : Stop&Clear 1 : Run (Count up)	
PWM8DR	PWM8 Data Reg.	0FFDBH	PW8D7	PW8D6	PW8D5	PW8D4	PW8D3	PW8D2	PW8D1	PW8D0
		(Prohibit RMW)	W							
			Undefined							
PWMDR0	PWM Data Reg.0	0FFDCH	PWD07	PWD06	PWD05	PWD04	PWD03	PWD02	PWD01	PWD00
		(Prohibit RMW)	W							
			Undefined							
PWMDR0B	PWM Data Reg.0B	0FFDDH					PWD0B	PWD0A	PWD09	PWD08
		(Prohibit RMW)					W			
							Undefined			
PWMDR1	PWM Data Reg.1	0FFDEH	PWD17	PWD16	PWD15	PWD14	PWD13	PWD12	PWD11	PWD10
		(Prohibit RMW)	W							
			Undefined							
PWMDR1B	PWM Data Reg.1B	0FFDFH					PWD1B	PWD1A	PWD19	PWD18
		(Prohibit RMW)					W			
							Undefined			

9) Serial channel control

MSB LSB

Symbol	Name	Address	7	6	5	4	3	2	1	0
SC0BUF	Serial Channel0 Buffer Reg.	0FFE2H (Prohibit RMW)	RB07	RB06	RB05	RB04	RB03	RB02	RB01	RB00
			TB07	TB06	TB05	TB04	TB03	TB02	TB01	TB00
			R (receive) / W (send)							
			Undefined							
SC0MOD	Serial Channel0 Control Reg.	0FFE3H	FF0SI	S0RES	S0MD1	S0MD0	SIFT0	CLK0SI	SCLK0S	SIO0E
			R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
			1	0	0	0	0	0	0	0
			Transfer monitor 0 : Busy 1 : Stop	Transfer software reset 0 : – 1 : Reset	Transfer mode 00 : Send 01 : Receive 10 : Don't care 11 : Send-receive		Transfer shift 0 : Leading edge 1 : Trailing edge	Transfer internal clock 0 : TBC2 1 : TBC6	Transfer clock 0 : Internal clock 1 : external clock	Transfer control 0 : Disable 1 : Enable
SC1BUF	Serial Channel1 Buffer Reg.	0FFE4H (Prohibit RMW)	RB17	RB16	RB15	RB14	RB13	RB12	RB11	RB10
			TB17	TB16	TB15	TB14	TB13	TB12	TB11	TB10
			R (receive) / W (send)							
			Undefined							
SC1MOD	Serial Channel1 Control Reg.	0FFE5H	FF1SI	S1RES	S1MD1	S1MD0	SIFT1	CLK1SI	SCLK1S	SIO1E
			R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
			1	0	0	0	0	0	0	0
			Transfer monitor 0 : Busy 1 : Stop	Transfer software reset 0 : – 1 : Reset	Transfer mode 00 : Send 01 : Receive 10 : Don't care 11 : Send-receive		Transfer shift 0 : Leading edge 1 : Trailing edge	Transfer internal clock 0 : TBC2 1 : TBC6	Transfer clock 0 : Internal clock 1 : External clock	Transfer control 0 : Disable 1 : Enable
P4	Port4	0FFC8H	P47	P46	P45	P44	P43	P42	P41	P40
			R/W							
			Input mode							
			Also used for TI1	Also used for TI0/INT2	Also used for RxD1	Also used for TxD1	Also used for SCLK1	Also used for RxD0	Also used for TxD0	Also used for SCLK0
P4MR	Port4 Mode Control Reg.	0FFCAH					P45M	P44M	P42M	P41M
							R/W	R/W	R/W	R/W
							0	0	0	0
							SIO1 receive control 0 : Port 1 : RxD1	SIO1 send control 0 : Port 1 : TxD1	SIO0 receive control 0 : Port 1 : RxD0	SIO0 send control 0 : Port 1 : TxD0

10) A/D converter control

Symbol	Name	Address	MSB 7	6	5	4	3	2	1	LSB 0
ADMOD	A-D Converter mode Reg.	0FFE0H	ADS2	ADBF	ADS	(Note) Always write "0".	ADCH3	ADCH2	ADCH1	ADCH0
			W	R	R/W		R/W			
			1	0	0		0	0	0	0
		(Prohibit RMW)	A/D conversion repeat control 0 : Single 1 : Repeat	A/D conversion busy flag 0 : Don't Busy 1 : Busy	A/D conversion start 0 : Stop 1 : Start		Analog Input Channel Select			
ADREG	A-D Result Reg.	0FFE1H	–							
			R							
			Undefined							
			Saves A/D conversion result							
P6CR	Port6 Control Reg.	0FFCDH		(Note) Always write "0".		P6M	P63C	P62C	P61C	P60C
						R/W	R/W			
						0	0			
						A/D input control 0 : Port 1 : A/D input	0 : In 1 : Out (Specifies I/O in units of bits)			

6. PORT SECTION EQUIVALENT CIRCUIT DIAGRAM

- Explanation of circuit diagram

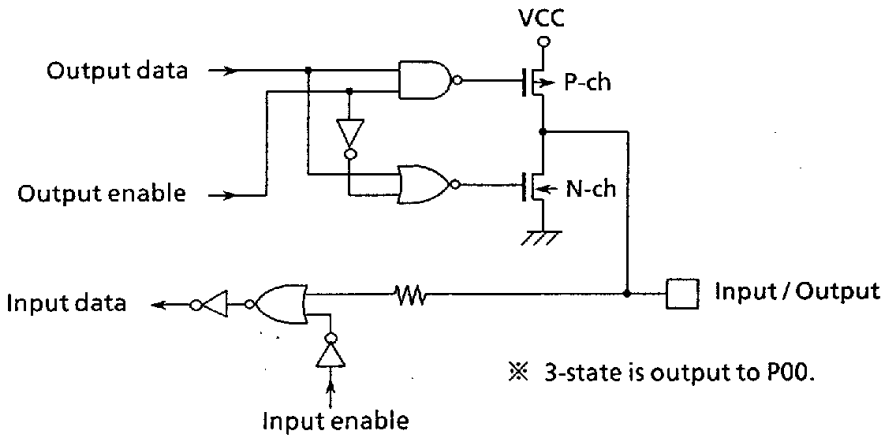
  Gate symbols are the same as those used for standard CMOS logic IC 74HCxx series.

  Special signal name is as follows:

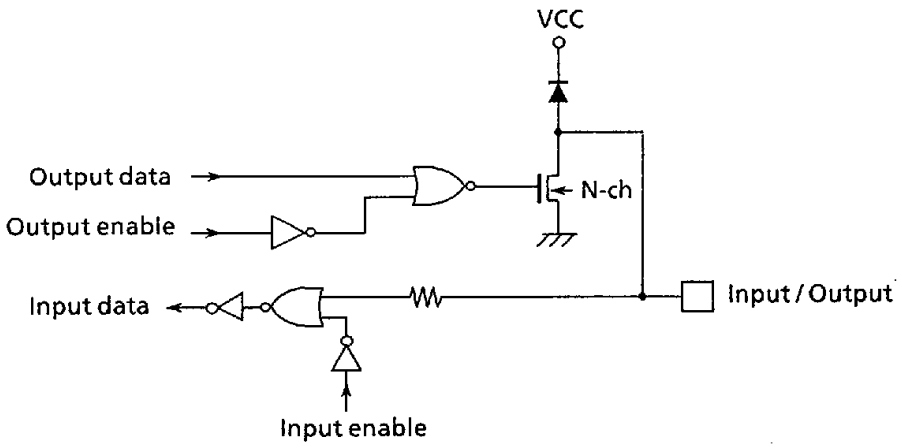
  STOP : Used to set the halt mode setting register to STOP mode. When the CPU executes the HALT instruction, STOP becomes active "1". However, if the drive enable bit <DRVE> is set to "1", STOP remains "0".

- The input protect resistance is approximately several tens to several hundreds of ohms.

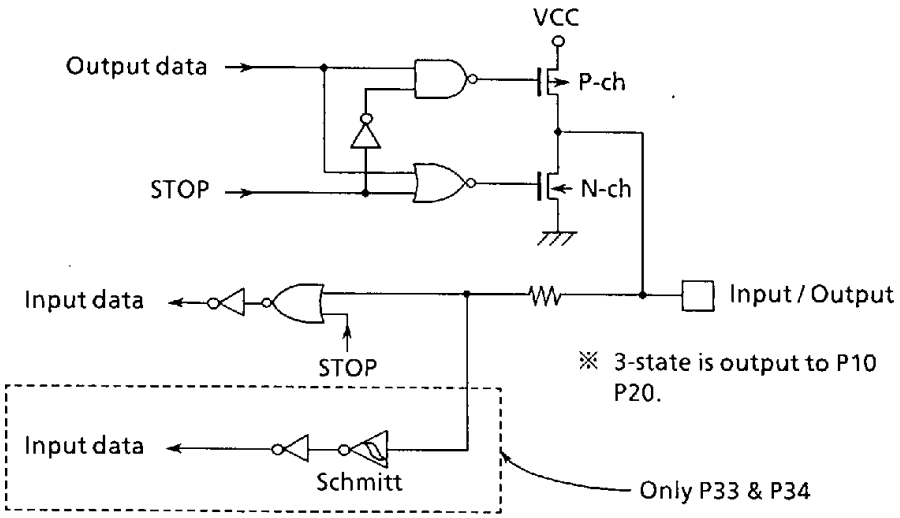
■ P0 (P00 to P03)



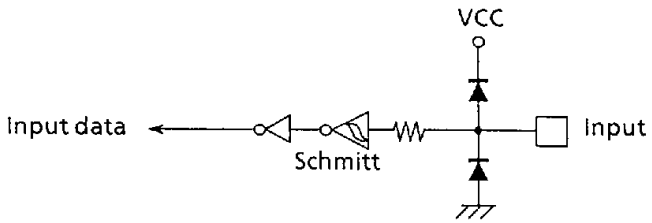
■ P0 (P04 to P07), P2 (P21 to P27)



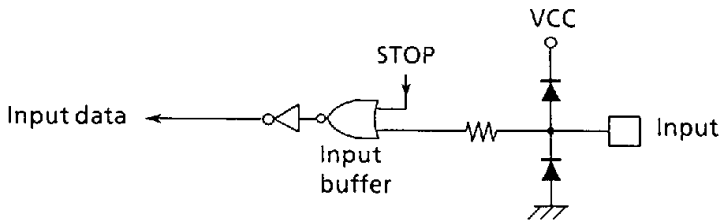
■ P1, P20, P3 (P30 to P34), P4



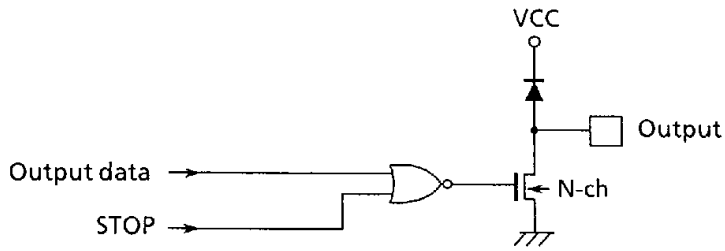
■ P35



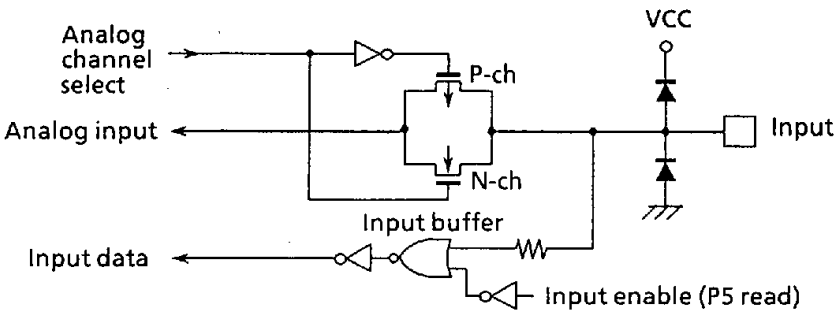
■ P36



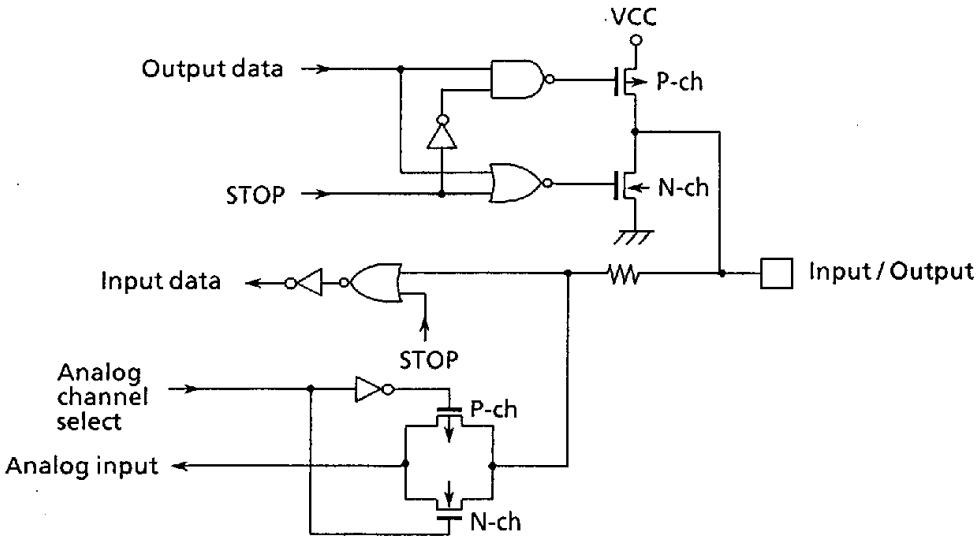
■ P37



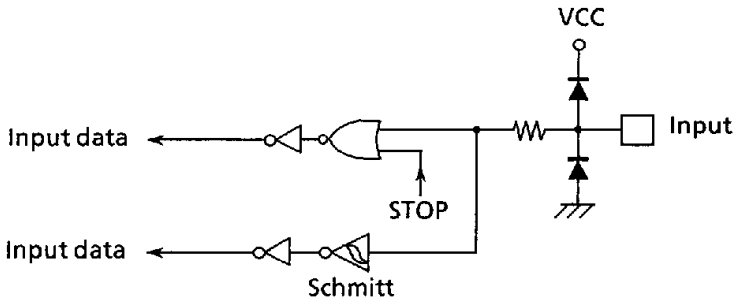
■ P5



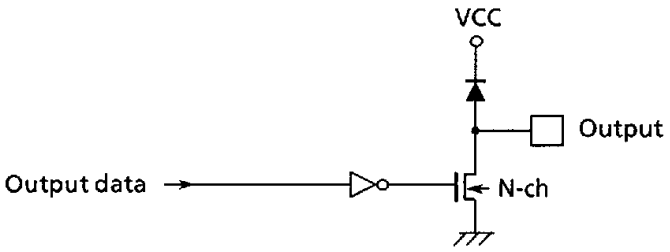
■ P6 (P60 to P63)



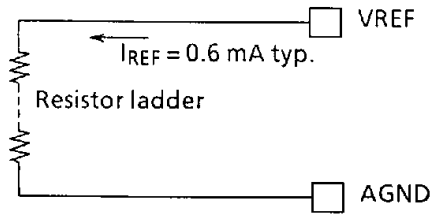
■ P6 (P64 to P67)



■ PW0, PW1

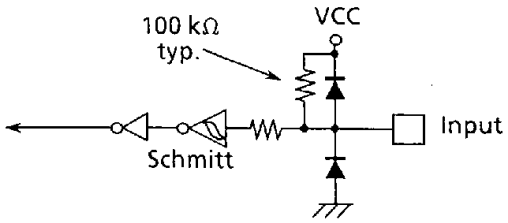


■ VREF, AGND

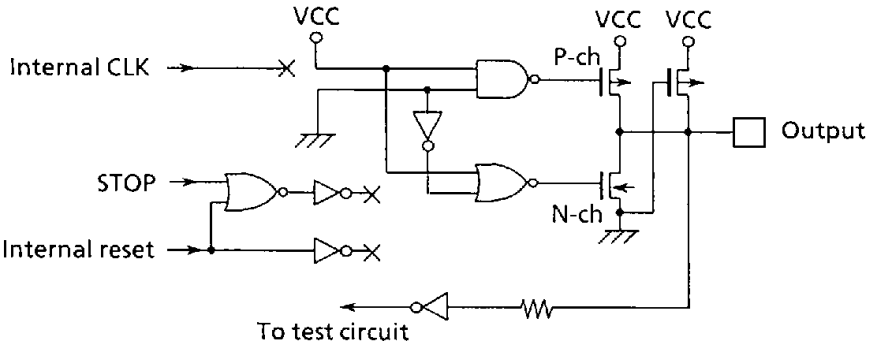


(Note) IREF continues to flow in standby mode, too.

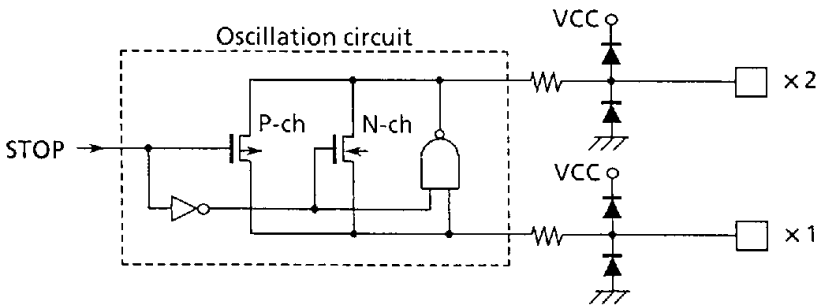
■ $\overline{\text{RESET}}$



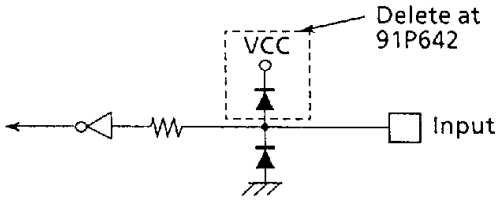
■ CLK



■ X1, X2

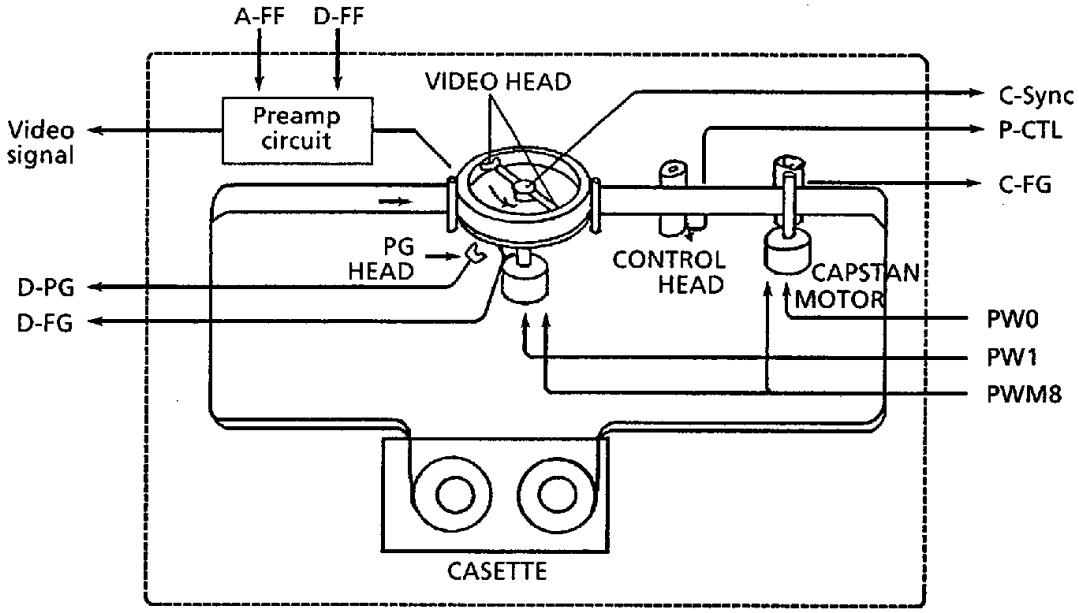


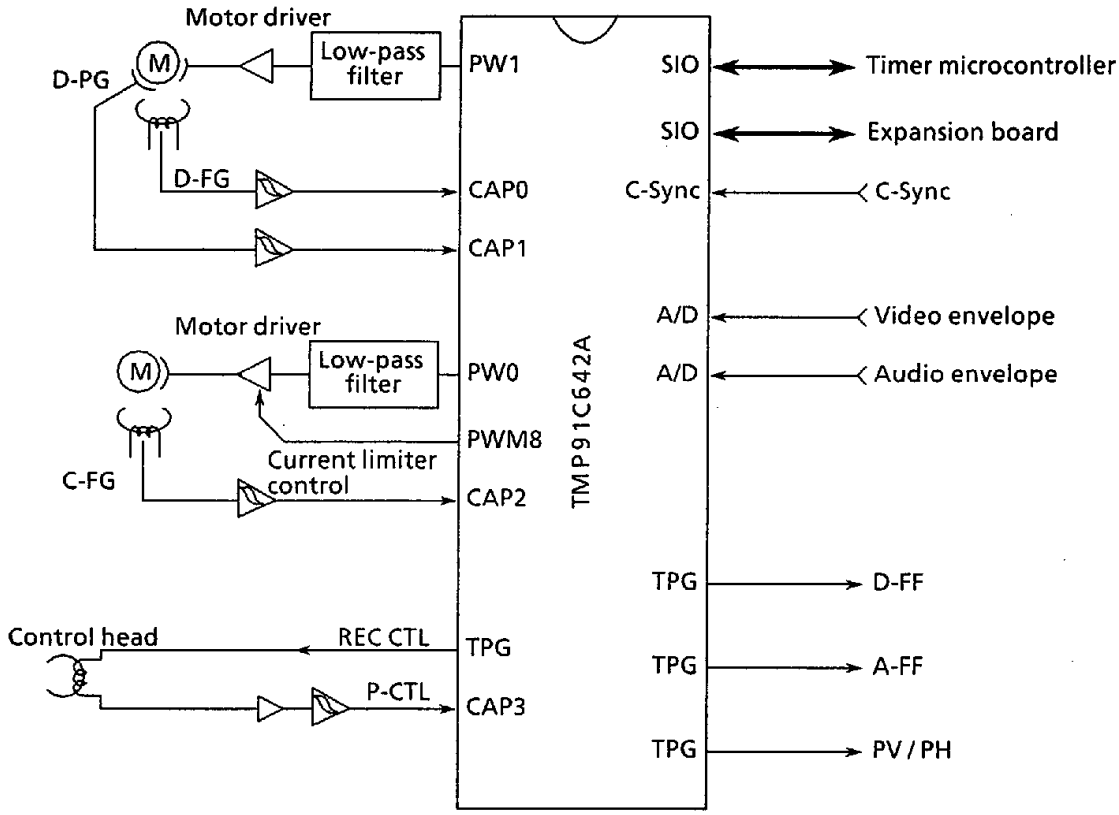
■ TEST



7. APPLICATION CIRCUIT

Shown below is an example of VCR servo control using TMP91C642A.





8. VCR TERMINOLOGY

VCR terminology used in the TMP91C642A users manual is explained below.

Embed

Also called insert. During special playback, tape speed and drum rotation speed are different, so the head cannot scan the video track correctly. At this time, tracing using CH2 the track recorded by CH1 does not obtain a playback signal. Thus, where there is no playback signal, noise is generated on the screen.
To eliminate noise, a special head other than the one used during ordinary playback is provided. The special head is used to switch the ordinary head and special head signals. Eliminating noise on the screen is called embedding. Embedding is used for CUE / REV, double speed, and reverse speed.

Capstan motor

Used to run the tape. During playback and recording, the tape is inserted between the capstan motor shaft and the pinch roller and run. At the same time, the reel spindle on the take-up side is rotated. During FF / REW, the capstan motor and pinch roller are open. Only the reel is driven.

Servo

Servo mechanism. Follows any changes in the target values of position, direction, and angle. Servo in VCR means detecting the motor rotation speed or phase and controlling it according to the fixed value. Servo is applied to the drum and capstan motors.
Servo in VCRs means detection of motor rotation speed and control at a fixed speed or phase. In other words, servo applies to the drum and capstan motors.

Drum motor

Also called cylinder motor. Used to rotate the cylinder in which the heads are installed. The drum motor is usually rotated at a standard speed (NTSC : 60 Hz, PAL : 50 Hz).

Field

Two half-screens making up one frame. In TV broadcasting, a screen is drawn using interlace scanning. That is, odd lines are scanned first, then even lines. Fields are classified into odd and even fields depending on whether the number of scanning lines is odd or even.

Frame

In NTSC broadcasting, motion is represented using 30 frames per second. The frequency is usually 30Hz, the same as that of the CTL pulse; thus, detecting the CTL pulse enables the tape to be edited in units of frames.

Head amp

Signals retrieved from the video head are very small. They are easily affected by noise if a cable is used to transfer them. Thus, the signals must be amplified as near the head as possible to a level where noise does not affect them. The amplifier used is called the head amp or preamp.

A-FF signal

During normal audio/video recording, audio signals are recorded on a dedicated audio track. In VHS Hi-Fi recording, the audio signal is recorded on the video signal track using the deep-level recording method. Thus, the audio head is also installed on the drum motor like the video head. The video and audio heads are switched using the A-FF signal.

AFC

Automatic Frequency Control. Maintains a fixed speed by feeding back the difference between the target frequency and the current frequency to the control output.

AGC

Automatic Gain Control. Maintains a fixed gain by feeding back the difference between the target gain and the current gain to the control output.

APC

Automatic Phase Control. Maintains a fixed phase by feeding back the difference between the target phase and the current phase to the control output.

C-FG

Capstan Frequency Generator. Detects the rotation speed of the capstan motor. Usually at 720Hz to 1080Hz frequency.

C-Sync

Composite sync signal. Composite of H-Sync, V-Sync. Usually referred to as the video signal. Inputting the C-Sync signal to the video input produces the image.

CTL pulse (P-CTL)

Maintains tape speed the same during recording and playback. P-CTL is used to record VISS / VASS signals.

CTL head

Records/plays back CTL pulses on the tape. Usually located next to the normal audio head.

CUE

System control mode: fast forward during playback.

D-FF signal

Head switching signal. VCRs have at least two heads used to retrieve signals from the tape. This is because TV broadcasting uses the interlace method. That is, one frame made up of two interlaced screens consisting of scanning lines divided into odd and even fields. Signals are retrieved from the odd and even fields by separate heads. The D-FF signal is used to switch these heads.

D-FG

Drum Frequency Generator. Detects the rotation speed of the drum motor.

D-PG

Drum Phase Generator. Detects the positions of heads on the drum.

FF

System control mode: fast forward

H-Sync

Horizontal sync signal. 15.734 kHz for NTSC ; 15.625 kHz for PAL / SECAM.

INSERT signal

Enables head switching for embedding.

NTSC

National Television System Committee. Broadcasting standard used in USA, Canada, Japan and Korea.

PAL

Phase Alternation by Line. Broadcasting standard developed as an improvement on NTSC. Used in Germany, Italy, UK, China, and some Southeast Asian countries.

PG adjustment

Ensures compatibility between tapes recorded on different VCRs under VHS specifications. Adjusts the D-FF phase, by playing back PG adjustment master tape, so that the difference between the D-FF signal and the played-back V-Sync signal is within 6.5H ± 1H.

REVIEW

Abbreviated REV. System control mode: rewind during playback.

REW

System control mode : rewind.

VASS

VHS Address Search System. Assigns absolute addresses on the tape by changing the duty of CTL signals like VISS. Data can be stored at the assigned addresses.

VISS

VHS Index Search System. Makes index marks on the tape by changing the duty of CTL signals. Reading these marks enables the detection of the tape position at high speed.

V-PULSE

Also referred to as pseudo-V or PV/PH. To avoid the monitor going out of sync when the sync signal on the tape is lost during special playback, adds sync signals to the video signal. These additional sync signals are called pseudo-V or pseudo-H.

V-Sync

Vertical sync signal. 60 Hz for NTSC ; 50 Hz for PAL / SECAM.