TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/L1 Series

TMP91PW12

TOSHIBA CORPORATION

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, "Points of Note and Restrictions".
Especially, take care below cautions.

CAUTION

How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, INT0 to INT4, INTRTC), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 5 clocks of f_{FPH}) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

Low Voltage/Low Power CMOS 16-Bit Microcontroller

TMP91PW12F

1. Outline and Device Characteristics

TMP91PW12 is OTP type MCU which includes 128-Kbyte one-time PROM. Using the adapter-socket, you can write and verify the data for TMP91PW12. TMP91PW12 has the same pin assignment with TMP91CW12 (Mask ROM type).
Writing the program to Built-in PROM, TMP91PW12 operates as the same way with TMP91CW12.

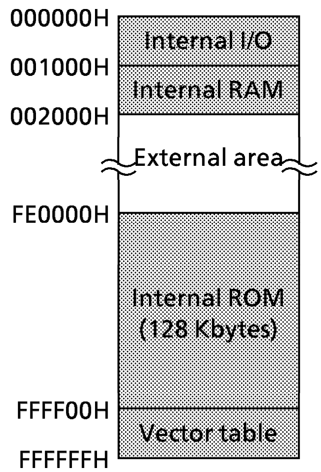


Figure 1.1 Memory Map of TMP91CW12/PW12

MCU	ROM	RAM	Package	Adapter Socket
TMP91PW12F	OTP 128 Kbytes	4 Kbytes	P-LQFP100-1414-0.50C	BM11149

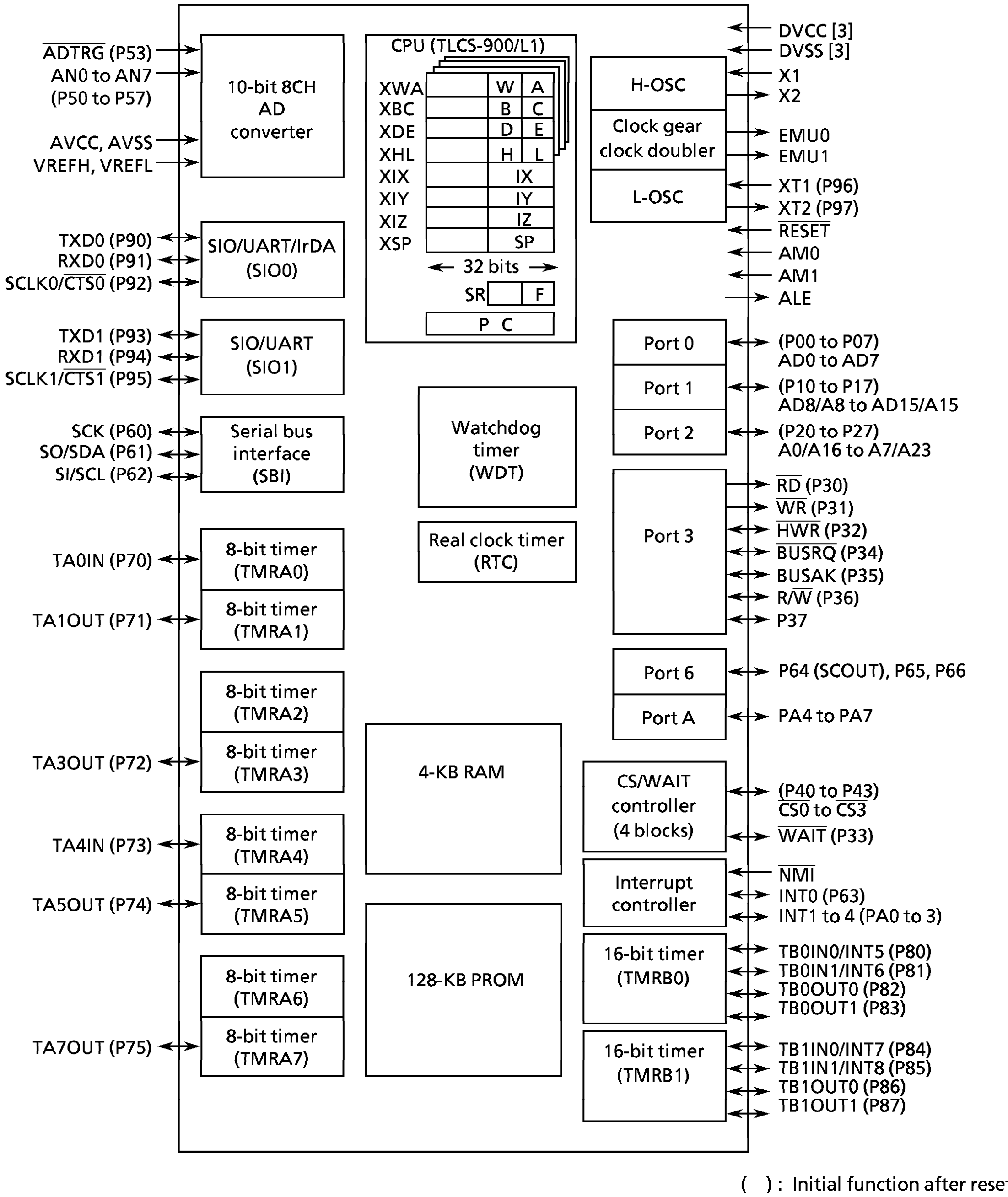


Figure 1.1 TMP91PW12 Block Diagram

2. Pin Assignment and Pin Functions

This section shows the TMP91PW12F pin assignment, and the names and an outline of the functions of the input/output pins.

2.1 Pin Assignment Diagram

Figure 2.1.1 is a pin assignment diagram for TMP91PW12F.

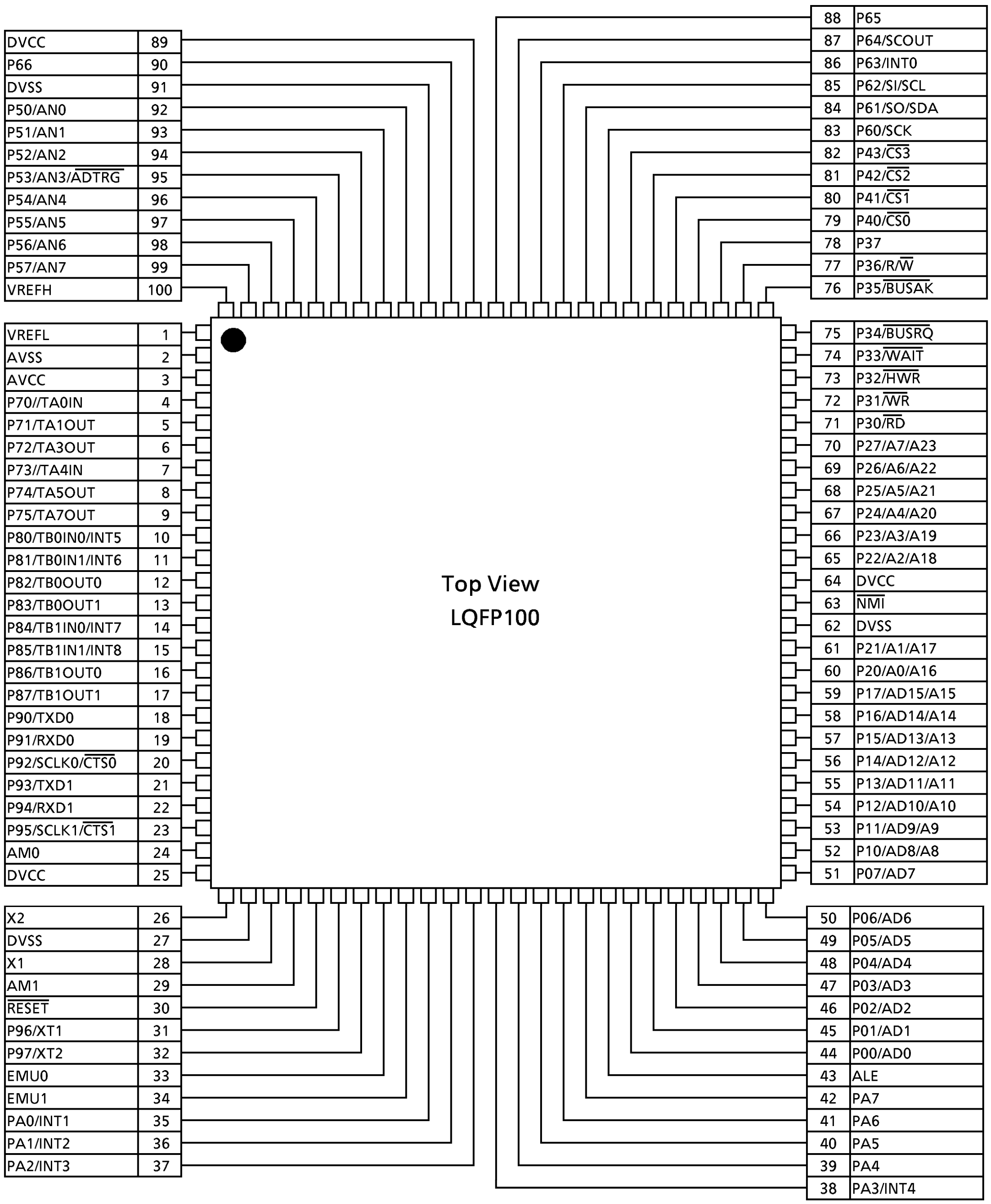


Figure 2.1.1 Pin Assignment Diagram (100-Pin LQFP)

2.2 Pin Names and Functions

The names of the input/output pins and their functions are described below.
Table 2.2.1 Pin Names and Functions.

Table 2.2.1 Pin Names and Functions (1/4)

Pin Name	Number of Pins	I/O	Functions
P00 to P07 AD0 to AD7	8	I/O Tri-state	Port 0: I/O port that allows I/O to be selected at the bit level Address and data (lower): Bits 0 to 7 for address and data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O Tri-state Output	Port 1: I/O port that allows I/O to be selected at the bit level Address and data (upper): Bits 8 to 15 for address and data bus Address: Bits 8 to 15 for address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows to be selected at the bit level (with pull-down resistor) Address: Bits 0 to 7 for address bus Address: Bits 16 to 23 for address bus
P30 $\overline{RD}$	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory
P31 $\overline{WR}$	1	Output Output	Port 31: Output port Write: Strobe signal for writing data on pins AD0 to 7
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data on pins AD8 to 15
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait
P34 $\overline{BUSRQ}$	1	I/O Input	Port 34: I/O port (with pull-up resistor) Bus request: Signal used to request bus release.
P35 $\overline{BUSAK}$	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus acknowledge: Signal used to acknowledge bus release.
P36 R/$\overline{W}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/write: 1 represents read or dummy cycle; 0 represents write cycle.
P37	1	I/O	Port 37: I/O port (with pull-up resistor)
P40 $\overline{CS0}$	1	I/O Output	Port 40: I/O port (with pull-up resistor) Chip select 0: Outputs 0 when address is within specified address area.
P41 $\overline{CS1}$	1	I/O Output	Port 41: I/O port (with pull-up resistor) Chip select 1: Outputs 0 if address is within specified address area.
P42 $\overline{CS2}$	1	I/O Output	Port 42: I/O port (with pull-up resistor) Chip select 2: Outputs 0 if address is within specified address area.
P43 $\overline{CS3}$	1	I/O Output	Port 43: I/O port (with pull-up resistor) Chip select 3: Outputs 0 if address is within specified address area.
P50 to P57 AN0 to AN7 $\overline{ADTRG}$	8	Input Input Input	Port 5: Pin used to input port Analog input: Pin used to input to AD converter AD trigger: Signal used to request AD start.

Note: This device's built-in memory or built-in I/O cannot be accessed by an external DMA controller, using the $\overline{BUSRQ}$ and $\overline{BUSAK}$ signals.

Table 2.2.1 Pin Names and Functions (2/4)

Pin Name	Number of Pins	I/O	Functions
P60 SCK	1	I/O I/O	Port 60: I/O port Serial bus interface clock at SIO mode.
P61 SO SDA	1	I/O Output I/O	Port 61: I/O port Serial bus interface output data at SIO mode. Serial bus interface data at I^2C bus mode.
P62 SI SCL	1	I/O Input I/O	Port 62: I/O port Serial bus interface input data at SIO mode. Serial bus interface clock at I^2C bus mode.
P63 INT0	1	I/O Input	Port 63: I/O port Interrupt request pin 0: Interrupt request pin with programmable level/rising edge/falling edge
P64 SCOUT	1	I/O Output	Port 64: I/O port System clock output: Output f_{FPH} or fs clock
P65	1	I/O	Port 65: I/O port
P66	1	I/O	Port 66: I/O port
P70 TA0IN	1	I/O Input	Port 70: I/O port Timer A0 input
P71 TA1OUT	1	I/O Output	Port 71: I/O port Timer A1 output
P72 TA3OUT	1	I/O Output	Port 72: I/O port Timer A3 output
P73 TA4IN	1	I/O Input	Port 73: I/O port Timer A4 input
P74 TA5OUT	1	I/O Output	Port 74: I/O port Timer A5 output
P75 TA7OUT	1	I/O Output	Port 75: I/O port Timer A7 output
P80 TB0IN0 INT5	1	I/O Input Input	Port 80: I/O port Timer B0 input 0 Interrupt request pin 5: Interrupt request pin with programmable rising edge/falling edge
P81 TB0IN1 INT6	1	I/O Input Input	Port 81: I/O port Timer B0 input 1 Interrupt request pin 6: Interrupt request pin with rising edge
P82 TB0OUT0	1	I/O Output	Port 82: I/O port Timer B0 output 0
P83 TB0OUT1	1	I/O Output	Port 83: I/O port Timer B0 output 1

Table 2.2.1 Pin Names and Functions (3/4)

Pin Name	Number of Pins	I/O	Functions
P84 TB1IN0 INT7	1	I/O Input Input	Port 84: I/O port Timer B1 input 0 Interrupt request pin 7: Interrupt request pin with programmable rising edge/falling edge
P85 TB1IN1 INT8	1	I/O Input Input	Port 85: I/O port Timer B1 input 1 Interrupt request pin 8: Interrupt request pin with rising edge
P86 TB1OUT0	1	I/O Output	Port 86: I/O port Timer B1 output 0
P87 TB1OUT1	1	I/O Output	Port 87: I/O port Timer B1 output 1
P90 TXD0	1	I/O Output	Port 90: I/O port Serial send data 0
P91 RXD0	1	I/O Input	Port 91: I/O port Serial receive data 0
P92 SCLK0 $\overline{\text{CTS0}}$	1	I/O I/O Input	Port 92: I/O port Serial clock I/O 0 Serial data send enable 0 (Clear to send)
P93 TXD1	1	I/O Output	Port 93: I/O port Serial send data 1
P94 RXD1	1	I/O Input	Port 94: I/O port (with pull-up resistor) Serial receive data 1
P95 SCLK1 $\overline{\text{CTS1}}$	1	I/O I/O Input	Port 95: I/O port (with pull-up resistor) Serial clock I/O 1 Serial data send enable 1 (Clear to send)
P96 XT1	1	I/O Input	Port 96: I/O port (Open-drain output) Low-frequency oscillator connecting pin
P97 XT2	1	I/O Output	Port 97: I/O port (Open-drain output) Low-frequency oscillator connecting pin
PA0 to PA3 INT1 to INT4	4	I/O Input	Port A0 to A3: I/O port Interrupt request pin 1 to 4: Interrupt request pin with programmable rising edge/falling edge
PA4 to PA7	4	I/O	Port A4 to A7: I/O port
ALE	1	Output	Address latch enable Can be disabled for reducing noise.
$\overline{\text{NMI}}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge or both edges.
AM0/AM1	2	Input	Address mode: The Vcc pin should be connected.
EMU0/EMU1	2	Output	Test pin: Open pins.
$\overline{\text{RESET}}$	1	Input	Reset: Initializes TMP91CW12. (With pull-up resistor)

Table 2.2.1 Pin Names and Functions (4/4)

Pin Name	Number of Pins	I/O	Functions
VREFH	1	Input	Pin for reference voltage input to AD converter (H)
VREFL	1	Input	Pin for reference voltage input to AD converter (L)
X1/X2	2	I/O	High Frequency Oscillator connecting pin
AVCC	1		Power supply pin for AD converter
AVSS	1		GND pin for AD converter (0 V)
DVCC	3		Power supply pin (All Vcc pins should be connected with the power supply pin.)
DVSS	3		GND pin (0 V) (All Vss pins should be connected with GND (0 V).)

Note: All pins that have built-in pull-up resistors (other than the $\overline{\text{RESET}}$ pin) can be disconnected from the built-in pull-up resistor by software.

2.3 PROM Mode

Table 2.2.2 Name and function of PROM mode

Pin Function	Number of Pins	Input/ Output	Function	Pin Name (MCU mode)
A7 to A0	8	Input		P27 to P20
A15 to A8	8	Input	Memory address of program	P17 to P10
A16	1	Input		P33
D7 to D0	8	I/O	Memory data of pfogram	P07 to P00
$\overline{CE}$	1	Input	Chip enable	P32
$\overline{OE}$	1	Input	Output control	P30
$\overline{PGM}$	1	Input	Program control	P31
VPP	1	Power supply	12.75 V/5 V (Power supply of program)	AM1
VCC	4	Power supply	6.25 V/5 V	DVCC, AVCC
VSS	4	Power supply	0 V	DVSS, AVSS

Pin Function	Number of Pins	Input/ Output	Disposal of Pin
P34	1	Input	Fix to low level (security pin)
$\overline{RESET}$	1	Input	Fix to low level (PROM mode)
AM0	1	Input	
ALE	1	Output	Open
X1	1	Input	Crystal
X2	1	Output	
P42 to P40 P37 to P35 P75 to P70	12	Input	Fix to high level
P43 P57 to P50 P66 to P60 P87 to P80 P97 to P90 PA7 to PA0 VREFH VREFL $\overline{NMI}$ EMU1, 0	51	I/O	Open

3. Operation

This section describes in blocks the functions and basic operations of TMP91PW12.
The TMP91PW12 has PROM in place of the mask ROM which is included in the TMP91CW12. The other configuration and functions are the same as the TMP91CW12. Regarding the function of the TMP91PW12, which is not described herein, see the TMP91CW12.
The TMP91PW12 has two operational modes: MCU mode and PROM mode.

3.1 MCU Mode

(1) Mode setting and function

The MCU mode is set by driving High the AM1 and AM0 pin. In the MCU mode, the operation is same as TMP91CW12.

3.2 Memory Map

Figure 3.2.1, 3.2.2 are memory map of the TMP91PW12.

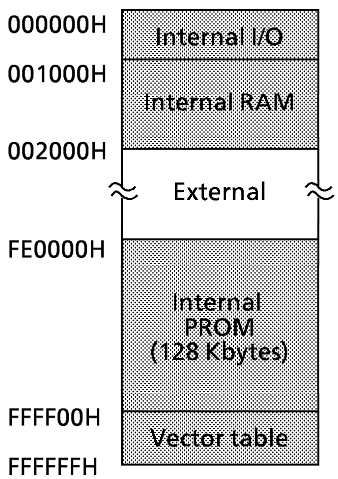


Figure 3.2.1 Memory Map in MCU Mode

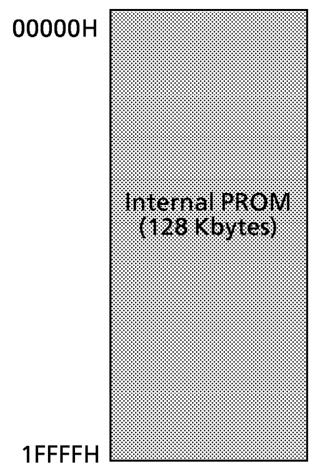


Figure 3.2.2 Memory Map in PROM Mode

3.3 PROM Mode

(1) Mode setting and function

PROM mode is set by setting the $\overline{RESET}$ and AM0 pins to the L level, and set by setting the AM1 pin to "VPP" level. The programming and verification for the internal PROM is achieved by using a general PROM programmer with the adaptor socket.

① OTP adaptor
BM11149: TMP91PW12F adaptors

② Setting OTP adaptor
Set the switch (SW1) to N side.

③ Setting PROM programmer

i) Set PROM type to TC571000D.
Size: 1 M bit (128K × 8 bits)
VPP: 12.75 V
tpw: 100 μs

The electric signature mode (hereinafter referred to as signature.) is not supported. Therefore if signature is used, the device is damaged because 12.75 V is applied to A9 of address. Do not use signature.

ii) Transferring the data (copy)

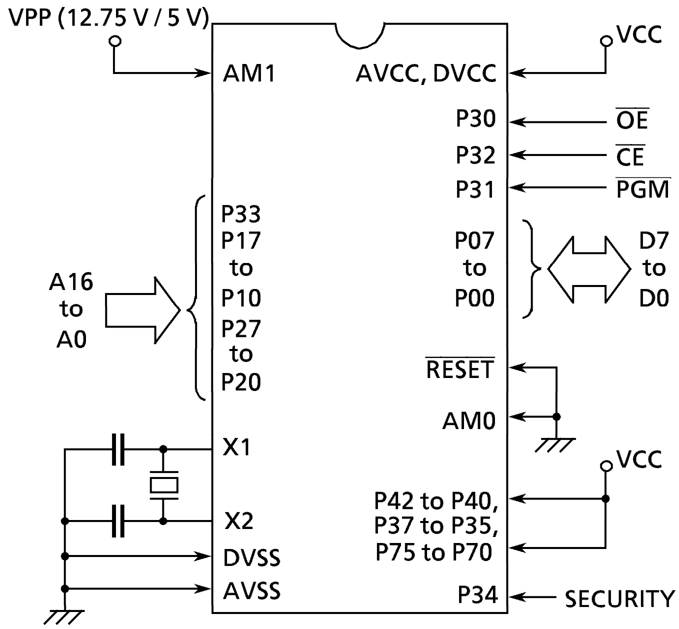
In TMP91PW12, PROM is placed on addresses 00000 to 1FFFFH in PROM mode, and addresses FE0000H to FFFFFFH in MCU mode. Therefore data should be transferred to addresses 00000 to 1FFFFH in PROM mode using the object converter (tuconv) or the block transfer mode (see instruction manual of PROM programmer.) or making the object data.

iii) Setting the programming address

Start address: 00000H
End address: 1FFFFH

④ Programming

Program/verify according to the procedures of PROM programmer.



* Use the 10 MHz resonator in case of programming and verification by a general EPROM programmer.

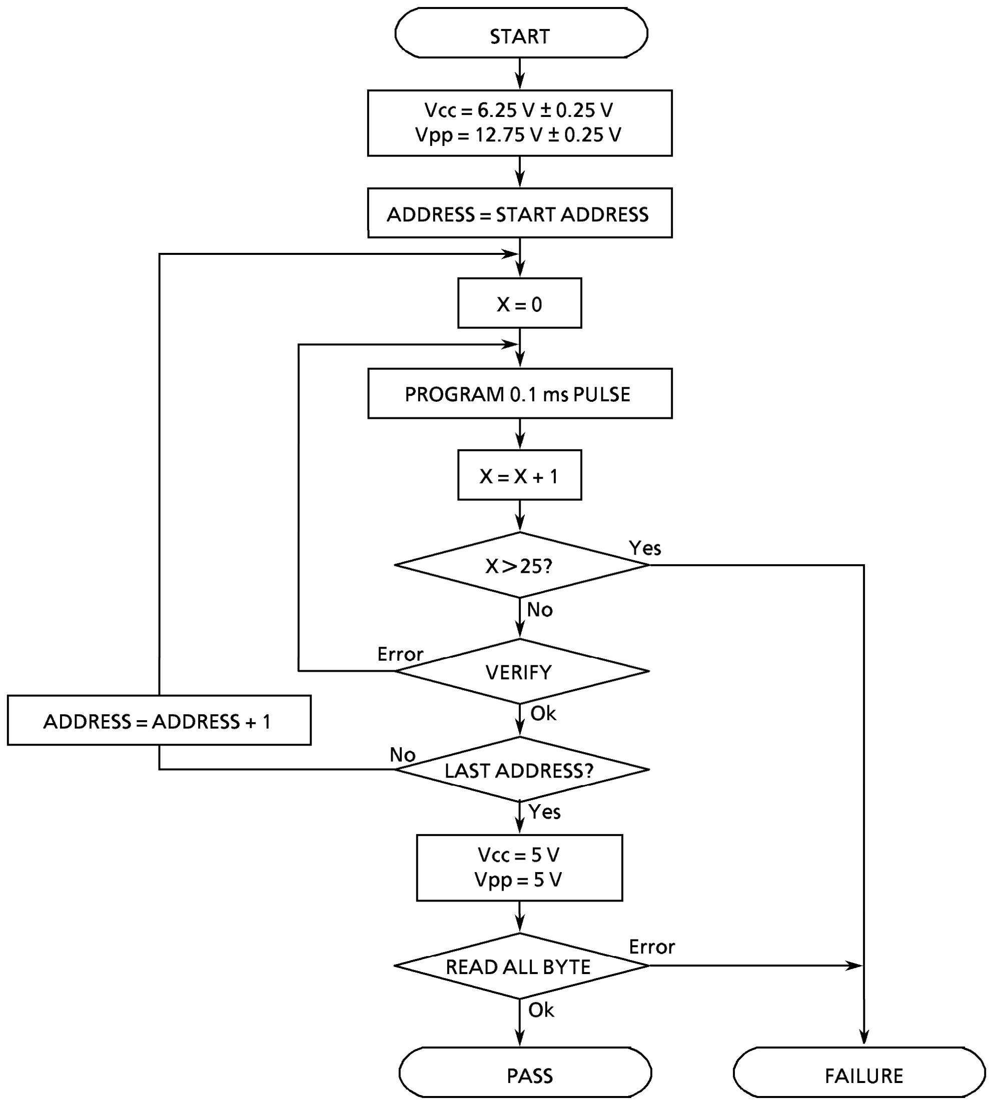
Figure 3.3.1 PROM Mode Pin Setting

(2) Programming flow chart

The programming mode is set by applying 12.75 V (programming voltage) to the AM1 pin when the following pins are set as follows,
(VCC : 6.25 V, $\overline{RESET}$: L level, AM0 : L level).
While address and data are fixed and $\overline{CE}$ pin is set to L level, 0.1 ms of L level pulse is applied to $\overline{PGM}$ pin to program the data.
Then the data in the address is verified.
If the programmed data is incorrect, another 0.1 ms pulse is applied to $\overline{PGM}$ pin.
This programming procedure is repeated until correct data is read from the address. (25 times maximum)
Subsequently, all data are programmed in all addresses.
The verification for all data is done under the condition of AM1 = Vcc = 5 V after all data were written.
Figure 3.3.2 shows the programming flow chart.

High Speed Program Writing.

Flow chart



Note: V_{PP} means AM1 pin.

Figure 3.3.2 Flow Chart

(3) Security bit

The TMP91PW12 has a security bit.
If the security bit is programmed to 0, the content of the PROM can not be read in PROM mode. (outputs data FFH)

How to program the security bit.

The difference from the programming procedures described in section 3.3.1 are follows.

① Setting OTP adapter
Set the switch (SW1) to S side.

② Setting PROM programmer

ii) Transferring the data

iii) Setting programming address

The security bit is in bit 0 of address 00000H.
Set the start address 00000H and the end address 00000H.
Set the data FEH at the address 00000H.

4. Electrical Characteristics

4.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Power supply voltage	Vcc	– 0.5 to 6.5	V
Input voltage	V_{IN}	– 0.5 to Vcc + 0.5	V
Output current	I_{OL}	2	mA
Output current	I_{OH}	– 2	mA
Output current (Total)	ΣI_{OL}	80	mA
Output current (Total)	ΣI_{OH}	– 80	mA
Power dissipation (Ta = 85 °C)	P_D	600	mW
Soldering temperature (10 s)	T_{SOLDER}	260	°C
Storage temperature	T_{STG}	– 65 to 150	°C
Operating temperature	T_{OPR}	– 40 to 85	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2)

Parameter		Symbol	Condition		Min	Typ. (Note)	Max	Unit
Power supply voltage (AVcc = DVcc) (AVss = DVss = 0 V)		Vcc	fc = 2 to 16 MHz	fs = 30 to 34 kHz	2.7		5.5	V
			fc = 4 to 25 MHz		4.5			
Input low voltage	P00 to P17 (AD0 to 15)	V_{IL}	Vcc < 4.5 V		– 0.3		0.6	V
			Vcc ≧ 4.5 V				0.8	
	P20 to PA7 (Except P63)	V_{IL1}	Vcc = 2.7 to 5.5 V				0.3Vcc	
	$\overline{RESET}$, $\overline{NMI}$, P63 (INT0)	V_{IL2}					0.25Vcc	
	AM0, 1	V_{IL3}					0.3	
	X1	V_{IL4}					0.2Vcc	
Input high voltage	P00 to P17 (AD0 to 15)	V_{IH}	Vcc<4.5 V		2.0		Vcc + 0.3	
			Vcc≧4.5 V		2.2			
	P20 to PA7 (Except P63)	V_{IH1}	Vcc = 2.7 to 5.5 V		0.7Vcc			
	$\overline{RESET}$, $\overline{NMI}$, P63 (INT0)	V_{IH2}			0.75Vcc			
	AM0, 1	V_{IH3}			Vcc – 0.3			
	X1	V_{IH4}			0.8Vcc			
Output low voltage		V_{OL}	I_{OL} = 1.6 mA (Vcc = 2.7 to 5.5 V)				0.45	V
Output high voltage		V_{OH}	I_{OH} = – 400 μA (Vcc = 3.0 V ± 10%)		2.4			
			I_{OH} = – 400 μA (Vcc = 5.0 V ± 10%)		4.2			

Note: Typical values are for Ta = 25°C and V_{CC} = 3.0 V unless otherwise noted.

DC Characteristics (2/2)

Parameter	Symbol	Condition		Min	Typ. (Note1)	Max	Unit
Input leakage current	I_{LI}	$0.0 \leqq V_{IN} \leqq Vcc$			0.02	± 5	μA
Output leakage current	I_{LO}	$0.2 \leqq V_{IN} \leqq Vcc - 0.2$			0.05	± 10	μA
Power down voltage (at STOP, RAM back up)	V_{STOP}	$V_{IL2} = 0.2$ Vcc, $V_{IH2} = 0.8$ Vcc		2.0		6.0	V
$\overline{RESET}$ pull-up resister	R_{RST}	Vcc = 3 V ± 10%		100		400	kΩ
		Vcc = 5 V ± 10%		50		230	
Pin capacitance	C_{IO}	fc = 1 MHz				10	pF
Schmitt width $\overline{RESET}$, $\overline{NMI}$, INT0	V_{TH}			0.4	1.0		V
Programmable pull-up resister	P_{KH}	Vcc = 3 V ± 10%		100		400	kΩ
		Vcc = 5 V ± 10%		50		230	
NORMAL (Note 2)	Icc	Vcc = 3 V ± 10% fc = 16 MHz			8.8	14.0	mA
IDLE2					3.0	4.5	
IDLE1					0.9	1.8	
NORMAL (Note 2)		Vcc = 5 V ± 10% fc = 25 MHz (Typ.: Vcc = 5.0 V)			23.5	35.0	mA
IDLE2					9.5	15.0	
IDLE1					4.4	9.0	
SLOW (Note 2)		Vcc = 3 V ± 10 % fs = 32.768 kHz			30.0	60.0	μA
IDLE2					11.0	25.0	
IDLE1					8.0	15.0	
STOP		Ta ≦ 50°C	Vcc = 2.7 to 5.5 V		0.2	10	μA
		Ta ≦ 70°C				20	
		Ta ≦ 85°C				50	

Note 1: Typical values are for Ta = 25°C and V_{CC} = 3.0 V unless otherwise noted.
Note 2: I_{CC} measurement condition (NORMAL, SLOW):
All functions are operational; output pins are open and input pins are fixed.

4.3 AC Characteristics

(1) Vcc = 3.0 V ± 10%

No.	Symbol	Parameter	Variable		16 MHz		Unit
			Min	Max	Min	Max	
1	t_{FPH}	f_{FPH} period (= x)	62.5	31250	62.5		ns
2	t_{AL}	A0 to 15 valid → ALE fall	0.5x – 26		5		ns
3	t_{LA}	ALE fall → A0 to 15 hold	0.5x – 26		5		ns
4	t_{LL}	ALE high width	x – 52		10		ns
5	t_{LC}	ALE fall → $\overline{RD}$/$\overline{WR}$ fall	0.5x – 28		3		ns
6	t_{CLR}	$\overline{RD}$ rise → ALE rise	0.5x – 26		5		
7	t_{CLW}	$\overline{WR}$ rise → ALE rise	x – 26		36		ns
8	t_{ACL}	A0 to 15 valid → $\overline{RD}$/$\overline{WR}$ fall	x – 41		21		ns
9	t_{ACH}	A0 to 23 valid → $\overline{RD}$/$\overline{WR}$ fall	1.5x – 50		43		ns
10	t_{CAR}	$\overline{RD}$ rise→ A0 to 23 hold	0.5x – 31		0		
11	t_{CAW}	$\overline{WR}$ rise→ A0 to 23 hold	x – 31		31		ns
12	t_{ADL}	A0 to 15 valid→ D0 to 15 input		3.0x – 87		100	ns
13	t_{ADH}	A0 to 23 valid→ D0 to 15 input		3.5x – 98		120	ns
14	t_{RD}	$\overline{RD}$ fall → D0 to 15 input		2.0x – 75		50	ns
15	t_{RR}	$\overline{RD}$ low width	2.0x – 40		85		ns
16	t_{HR}	$\overline{RD}$ rise → D0 to 15 hold	0		0		ns
17	t_{RAE}	$\overline{RD}$ rise → A0 to 15 output	x – 25		37		ns
18	t_{WW}	$\overline{WR}$ low width	1.5x – 55		39		ns
19	t_{DW}	D0 to 15 valid → $\overline{WR}$ rise	1.5x – 78		15		ns
20	t_{WD}	$\overline{WR}$ rise →D0 to 15 hold	x – 49		13		ns
21	t_{AWH}	A0 to 23 valid → $\overline{WAIT}$ input ((1 + N) WAIT mode)		3.5x – 118		100	ns
22	t_{AWL}	A0 to 15 valid → $\overline{WAIT}$ input ((1 + N) WAIT mode)		3.0x – 117		70	ns
23	t_{CW}	$\overline{RD}$/$\overline{WR}$ fall →$\overline{WAIT}$ hold ((1 + N) WAIT mode)	2.0x + 0		125		ns
24	t_{APH}	A0 to 23 valid → Port input		3.5x – 168		50	ns
25	t_{APH2}	A0 to 23 valid → Port hold	3.5x		218		ns
26	t_{AP}	A0 to 23 valid → Port valid		3.5x + 100		319	ns

AC Measuring Conditions

- Output level: High 0.7 Vcc/Low 0.3 Vcc, CL = 50 pF
- Input level: High 0.9 Vcc/Low 0.1 Vcc

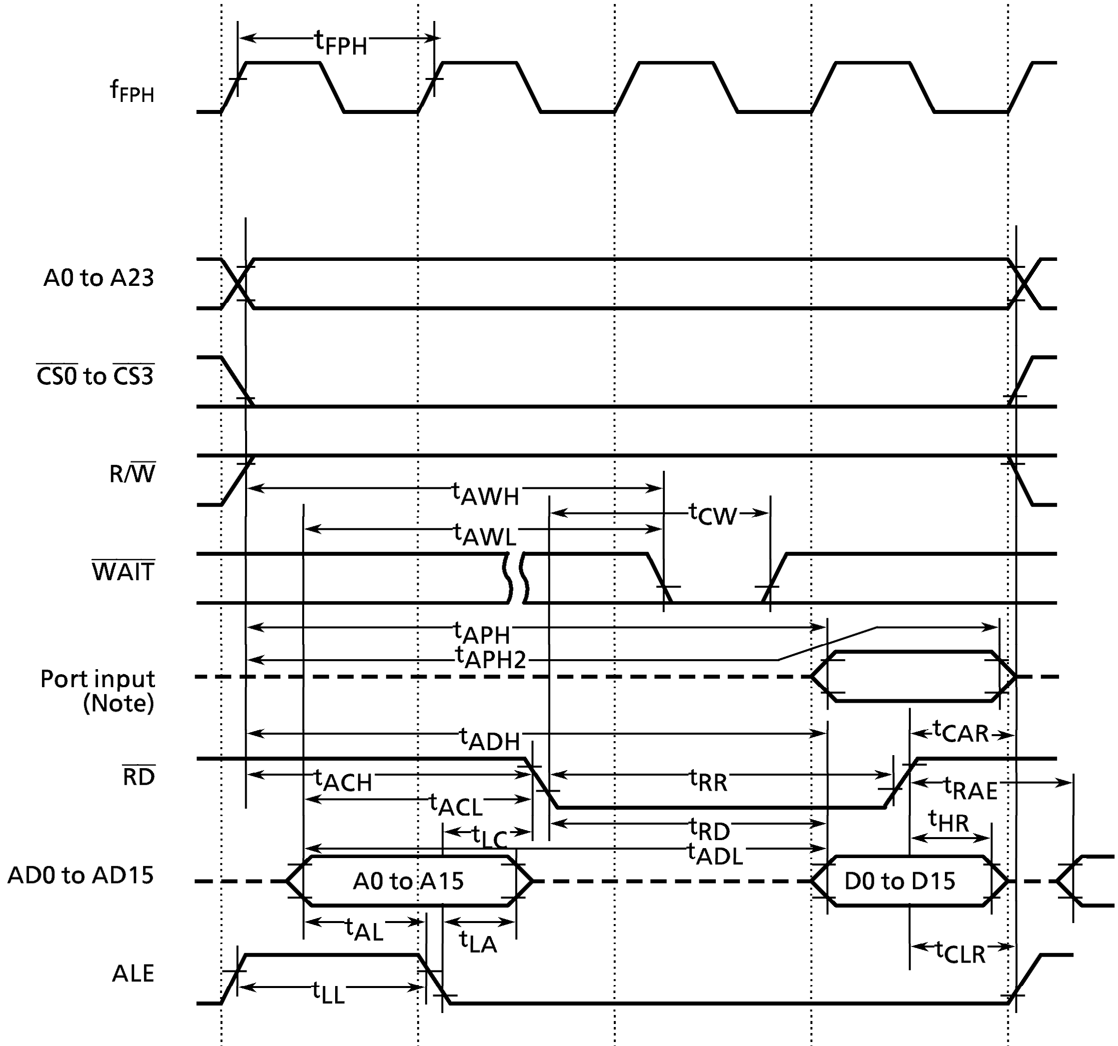
(2) Vcc = 5.0 V ± 10%

No.	Symbol	Parameter	Variable Min	Variable Max	25 MHz Min	25 MHz Max	Unit
1	t_{FPH}	f_{FPH} period (= x)	40	31250	40		ns
2	t_{AL}	A0 to 15 valid → ALE fall	0.5x – 15		5		ns
3	t_{LA}	ALE fall → A0 to 15 hold	0.5x – 15		5		ns
4	t_{LL}	ALE high width	x – 20		20		ns
5	t_{LC}	ALE fall → $\overline{RD}$/$\overline{WR}$ fall	0.5x – 20		0		ns
6	t_{CLR}	$\overline{RD}$ rise → ALE rise	0.5x – 15		5		
7	t_{CLW}	$\overline{WR}$ rise → ALE rise	x – 15		125		ns
8	t_{ACL}	A0 to 15 valid → $\overline{RD}$/$\overline{WR}$ fall	x – 25		15		ns
9	t_{ACH}	A0 to 23 valid → $\overline{RD}$/$\overline{WR}$ fall	1.5x – 50		10		ns
10	t_{CAR}	$\overline{RD}$ rise→ A0 to 23 hold	0.5x – 20		0		
11	t_{CAW}	$\overline{WR}$ rise→ A0 to 23 hold	x – 20		10		ns
12	t_{ADL}	A0 to 15 valid→ D0 to 15 input		3.0x – 45		75	ns
13	t_{ADH}	A0 to 23 valid→ D0 to 15 input		3.5x – 35		105	ns
14	t_{RD}	$\overline{RD}$ fall → D0 to 15 input		2.0x – 40		40	ns
15	t_{RR}	$\overline{RD}$ low width	2.0x – 20		40		ns
16	t_{HR}	$\overline{RD}$ rise → D0 to 15 hold	0		0		ns
17	t_{RAE}	$\overline{RD}$ rise → A0 to 15 output	x – 15		25		ns
18	t_{WW}	$\overline{WR}$ low width	1.5x – 20		25		ns
19	t_{DW}	D0 to 15 valid → $\overline{WR}$ rise	1.5x – 50		15		ns
20	t_{WD}	$\overline{WR}$ rise →D0 to 15 hold	x – 15		25		ns
21	t_{AWH}	A0 to 23 valid → $\overline{WAIT}$ input ((1 + N) WAIT mode)		3.5x – 90		50	ns
22	t_{AWL}	A0 to 15 valid → $\overline{WAIT}$ input ((1 + N) WAIT mode)		3.0x – 80		40	ns
23	t_{CW}	$\overline{RD}$/$\overline{WR}$ fall →$\overline{WAIT}$ hold ((1 + N) WAIT mode)	2.0x + 0		80		ns
24	t_{APH}	A0 to 23 valid → Port input		3.5x – 120		20	ns
25	t_{APH2}	A0 to 23 valid → Port hold	3.5x		140		ns
26	t_{AP}	A0 to 23 valid → Port valid		3.5x + 100		319	ns

AC Measuring Conditions

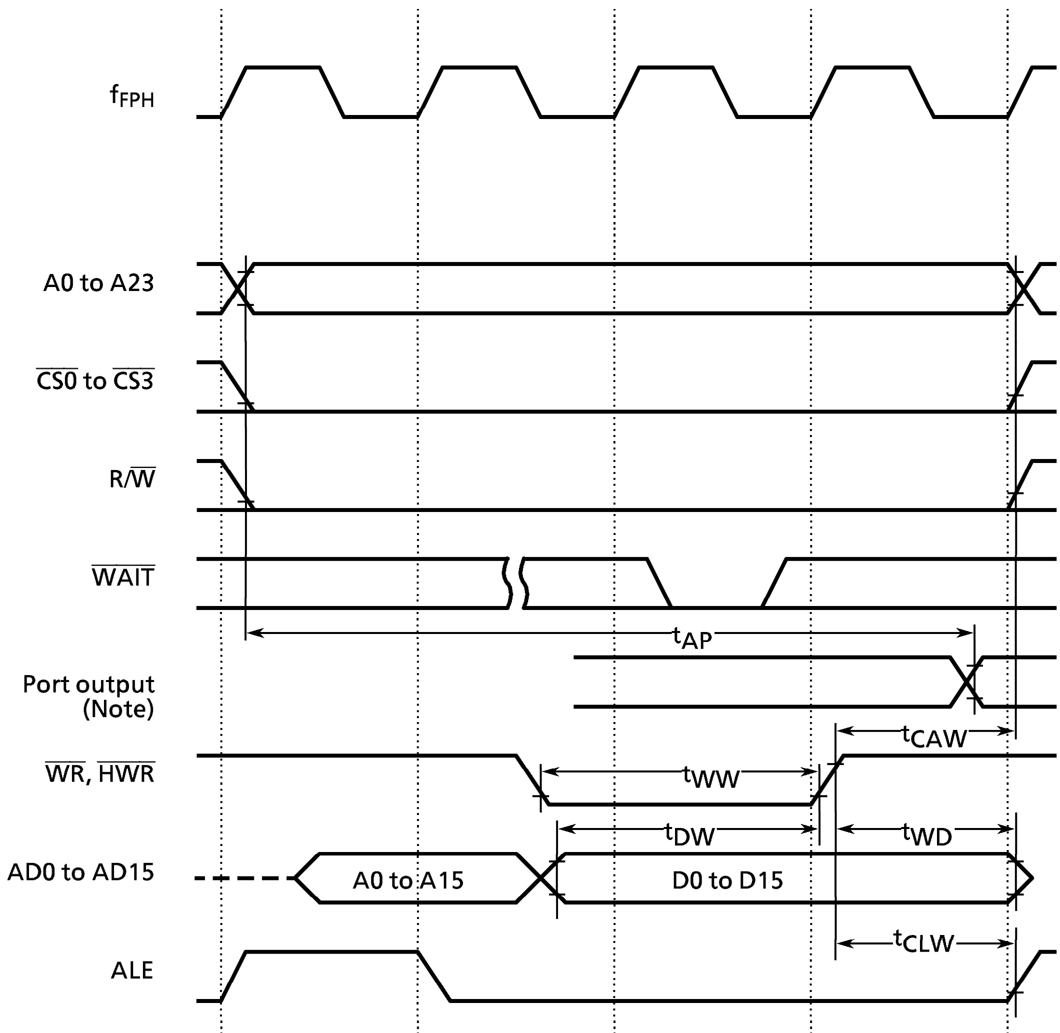
- Output level: High 2.2 V/Low 0.8 V, CL = 50 pF
- Input level: High 2.4 V/Low 0.45 V (AD0 to AD15)
  High 0.8 Vcc/Low 0.2 Vcc (except AD0 to AD15)

(1) Read cycle



Note: Since the CPU accesses the internal area to read data from a port, the control signals of external pins such as $\overline{RD}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

(2) Write cycle



Note: Since the CPU accesses the internal area to write data to a port, the control signals of external pins such as $\overline{WR}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

4.4 AD Conversion Characteristics

$AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage (+)	VREFH	V_{CC} = 3 V ± 10%	V_{CC} – 0.2 V	V_{CC}	V_{CC}	V
		V_{CC} = 5 V ± 10%	V_{CC} – 1.5 V	V_{CC}	V_{CC}	
Analog reference voltage (–)	VREFL	V_{CC} = 3 V ± 10%	V_{SS}	V_{SS}	V_{SS} + 0.2 V	
		V_{CC} = 5 V ± 10%	V_{SS}	V_{SS}	V_{SS} + 0.2 V	
Analog input voltage range	VAIN		VREFL		VREFH	
Analog current for analog reference voltage <VREFON> = 1	IREF (VREFL = 0 V)	V_{CC} = 3 V ± 10%		0.85	1.20	mA
		V_{CC} = 5 V ± 10%		1.44	2.00	
<VREFON> = 0		V_{CC} = 2.7 to 5.5 V		0.02	5.0	μA
Error (not including quantizing errors)	–	V_{CC} = 3 V ± 10%		± 1.0	± 4.0	LSB
		V_{CC} = 5 V ± 10 %		± 1.0	± 4.0	

Note 1: 1LSB = (VREFH – VREFL)/1024 [V]

Note 2: The operation above is guaranteed for $f_{FPH} \geqq 4$ MHz.

Note 3: The value I_{CC} includes the current which flows through the AVCC pin.

4.5 Serial Channel Timing (I/O internal mode)

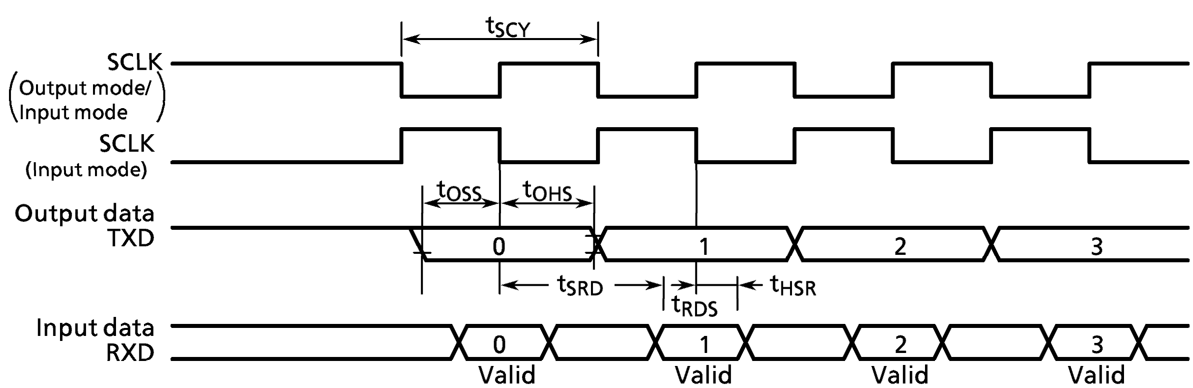
(1) SCLK input mode

Symbol	Parameter	Variable		25 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK period	16X		0.64		1.0		μs
t_{OSS}	Output data → SCLK rising/falling edge*	$t_{SCY}/2 - 4X - 85$ ($V_{CC} = 5\ V \pm 10\%$)		75		165		ns
		$t_{SCY}/2 - 4X - 130$ ($V_{CC} = 3\ V \pm 10\%$)		–		120		
t_{OHS}	SCLK rising/falling edge* → Output data hold	$t_{SCY}/2 + 2X + 0$		400		625		ns
t_{HSR}	SCLK rising/falling edge* → Input data hold	3X + 10		130		198		ns
t_{SRD}	SCLK rising/falling edge* → Valid data input		$t_{SCY} - 0$		640		1000	ns
t_{RDS}	Valid data input → SCLK rising/falling edge	0		0		0		ns

*) SCLK rising/falling edge: The rising edge is used in SCLK rising mode.
The falling edge is used in SCLK falling mode.

(2) SCLK output mode

Symbol	Parameter	Variable		25 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK period (Programable)	16X	8192X	0.64	327	1.0	512	μs
t_{OSS}	Output data → SCLK rising/falling edge	$t_{SCY}/2 - 40$		280		460		ns
t_{OHS}	SCLK rising/falling edge → Output data hold	$t_{SCY}/2 - 40$		280		460		ns
t_{HSR}	SCLK rising/falling edge → Input data hold	0		0		0		ns
t_{SRD}	SCLK rising/falling edge → Valid data input		$t_{SCY} - 1X - 90$		510		847	ns
t_{RDS}	Valid data input → SCLK rising/falling edge	1X + 90		130		153		ns



4.6 Event Counter (TA0IN, TA4IN, TB0IN0, TB0IN1, TB1IN0, TB1IN1)

Symbol	Parameter	Variable		25 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{VCK}	Clock period	8X + 100		420		600		ns
t_{VCKL}	Clock low level width	4X + 40		200		290		ns
t_{VCKH}	Clock high level width	4X + 40		200		290		ns

4.7 Interrupt, Capture

(1) $\overline{NMI}$, INT0 to 4 interrupts

Symbol	Parameter	Variable		25 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{INTAL}	$\overline{NMI}$, INT0 to 4 low level width	4X + 40		200		290		ns
t_{INTAH}	$\overline{NMI}$, INT0 to 4 high level width	4X + 40		200		290		ns

(2) INT5 to 8 interrupt, capture

The INT5 to 8 input width depends on the system clock select mode, prescaler clock mode.

System Clock Selected <SYSCK>	Prescaler Clock Selected <PRCK1:0>	t_{INTBL} (INT5 to 8 low level width)		t_{INTBH} (INT5 to 8 high level width)		Unit
		Variable	25 MHz	Variable	25 MHz	
		Min	Min	Min	Min	
0 (fc)	00 (f_{FPH})	8X + 100	420	8X + 100	420	ns
	10 (fc/16)	128Xc + 0.1	5.22	128Xc + 0.1	5.22	μs
1 (fs)	00 (f_{FPH})	8X + 0.1	244.3	8X + 0.1	244.3	

Note: Xc = Period of Clock fc

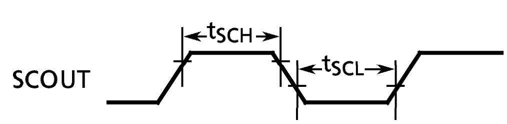
4.8 SCOUT pin AC characteristics

Symbol	Parameter	Variable		25 MHz		16 MHz		Condition	Unit
		Min	Max	Min	Max	Min	Max		
t_{SCH}	Low level width	0.5T − 20		–		11		V_{CC} = 3 V ± 10%	ns
		0.5T − 15		5		16		V_{CC} = 5 V ± 10%	
t_{SCL}	High level width	0.5T − 20		–		11		V_{CC} = 3 V ± 10%	ns
		0.5T − 15		5		16		V_{CC} = 5 V ± 10%	

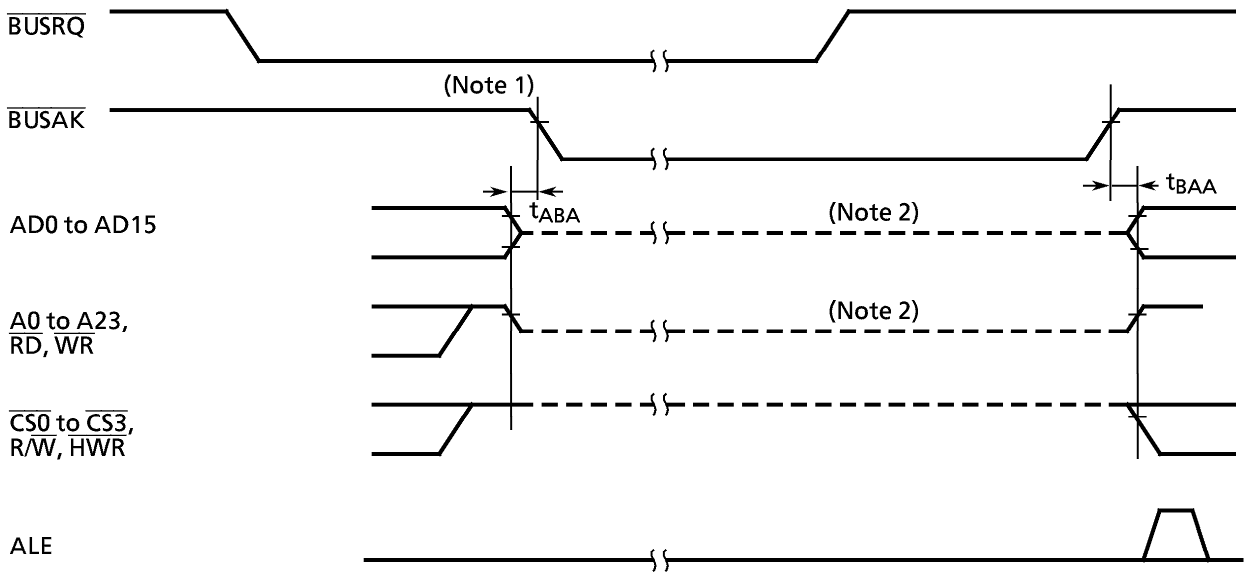
Note: T = Period of SCOUT

Measrement Condition

- Output level: High 0.7 V_{CC}/Low 0.3 V_{CC}, CL = 10 pF



4.9 Bus Request/Bus Acknowledge



Parameter	Symbol	Variable		25 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Output buffer off to $\overline{\text{BUSAK}}$ low	t_{ABA}	0	80	0	80	0	80	ns
$\overline{\text{BUSAK}}$ high to output buffer on	t_{BAA}	0	80	0	80	0	80	ns

Note 1: Even if the $\overline{\text{BUSRQ}}$ signal goes low, the bus will not be released while the $\overline{\text{WAIT}}$ signal is low. The bus will only be released when $\overline{\text{BUSRQ}}$ goes low while $\overline{\text{WAIT}}$ is high.

Note 2: This line shows only that the output buffer is in the off state.
It does not indicate that the signal level is fixed.
Just after the bus is released, the signal level set before the bus was released is maintained dynamically by the external capacitance. Therefor, to fix the signal level using an external resistor during bus release, careful design is necessary, as fixing of the level is delayed.
The internal programmable pull-up/pull-down resistor is switched between the active and non-active states by the internal signal.

4.10 Read Operation in PROM Mode

DC/AC characteristics

Ta = 25 ± 5 °C Vcc = 5 V ± 10 %

Parameter	Symbol	Condition	Min	Max	Unit
V_{PP} read voltage	V_{PP}	–	4.5	5.5	V
Input high voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IH1}	–	2.2	V_{CC} + 0.3	V
Input low voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IL1}	–	– 0.3	0.8	V
Address to output delay	t_{ACC}	C_L = 50 pF	–	2.25TCYC + α	ns

TCYC = 400 ns (10 MHz Clock)
α = 200 ns

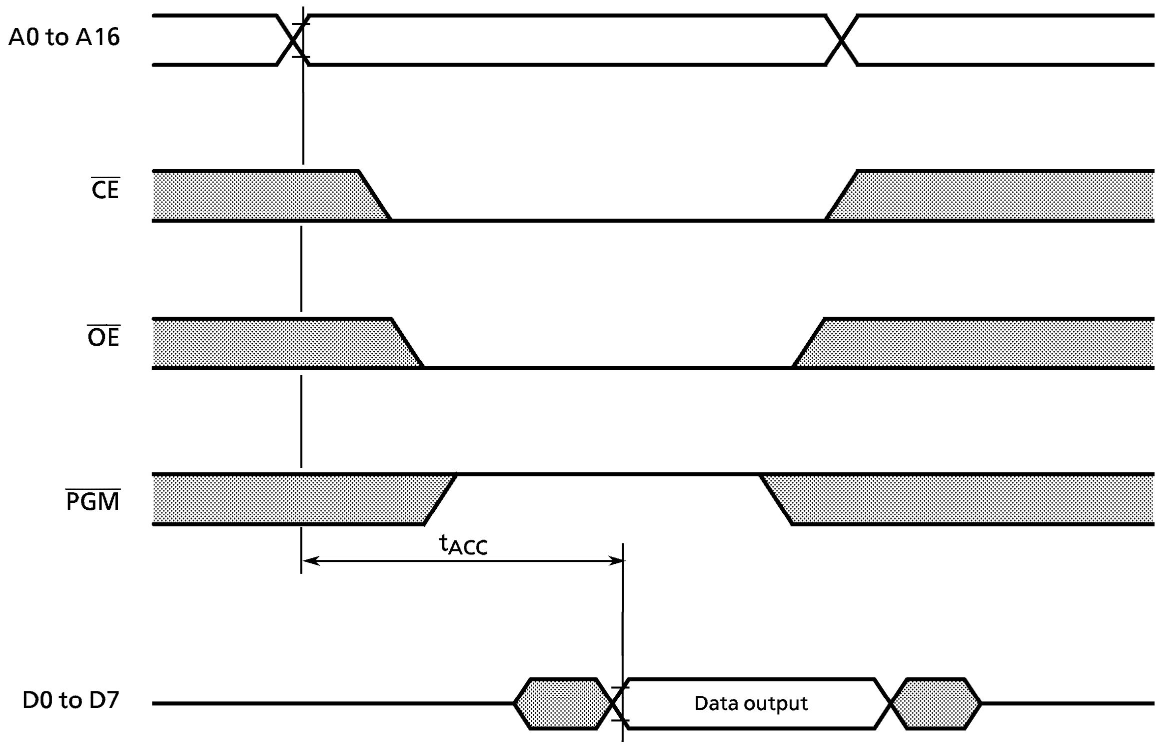
4.11 Program Operation in PROM Mode

DC/AC characteristics

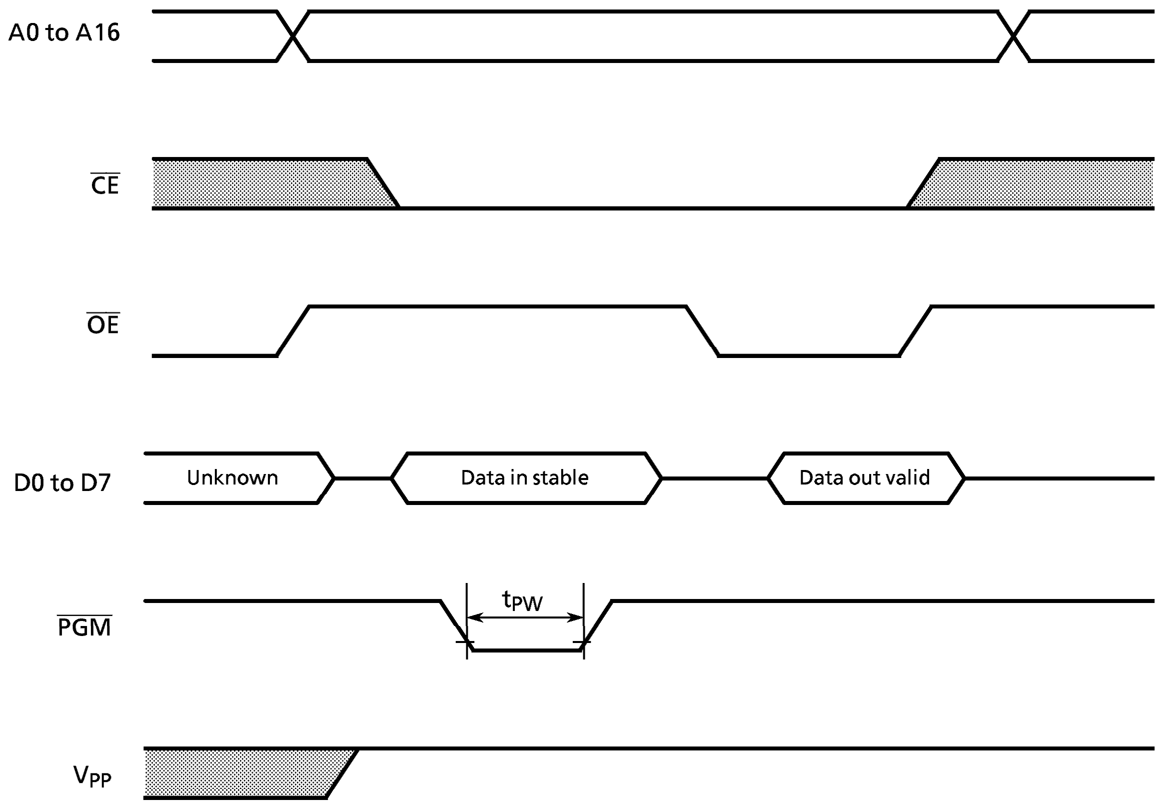
Ta = 25 ± 5 °C Vcc = 6.25 V ± 0.25 V

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Programming supply voltage	V_{PP}	–	12.50	12.75	13.00	V
Input high voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IH}	–	2.6		V_{CC} + 0.3	V
Input low voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IL}	–	– 0.3		0.8	V
V_{CC} supply current	I_{CC}	fc = 10 MHz	–		50	mA
V_{PP} supply current	I_{PP}	V_{PP} = 13.00 V	–		50	mA
$\overline{PGM}$ program pulse width	t_{PW}	C_L = 50 pF	0.095	0.1	0.105	ms

4.12 Timing Chart of Read Operation in PROM Mode



4.13 Timing Chart of Program Operation in PROM Mode



Note

1. The power supply of V_{PP} (12.75 V) must be turned on at the same time or the later time for a power supply of V_{CC} and must be turned off at the same time or early time for a power supply of V_{CC}.
2. The device suffers a damage taking out and putting in on the condition of $V_{PP} = 12.75$ V.
3. The maximum spec of V_{PP} pin is 14.0 V. Be carefull a overshoot at the programming.

5. **Package Dimentions**

P-LQFP100-1414-0.50C

Unit: mm