32bit

TLCS-900 Family TLCS-900/H1 Series

Under Development **TMP92CD23AFG/DFG**

100pin

32-bit microcontroller with large capacity memory and various serial interfaces

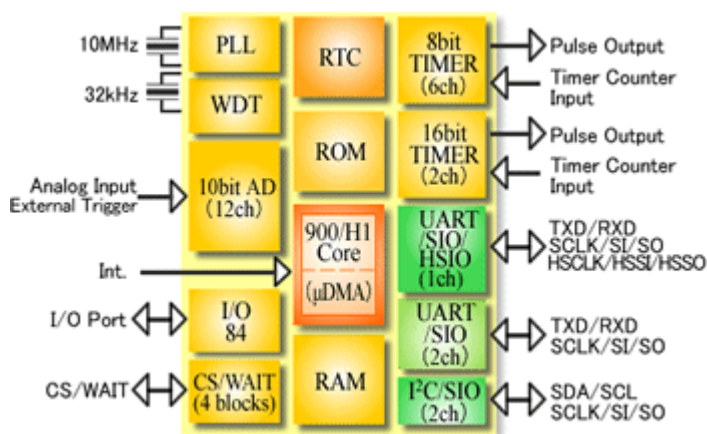# Features

● TLCS-900/H1 CPU Core

· Operating voltage:
   3.0 to 3.6 V

· Minimum instruction execution time:
   50 ns (at 20 MHz/ 3.0 to 3.6 V internal)

● Built-in Functions

· 10-bit AD converter	:	12 channels
· UART/SIO/HSIO	:	1 channel
· UART /SIO	:	2 channels
· I²C/SIO	:	2 channels
· 8-bit timer	:	6 channels
· 16-bit timer	:	2 channels
· Key-on wake-up	:	8 channels
· Program patch logic	:	8 banks

● Memory Size

**:Under development

Part number	ROM	RAM
TMP92CD23AFG/DFG**	512 Kbytes	32 Kbytes
TMP92CY23FG/DFG	256 Kbytes	16 Kbytes

› For further information about Toshiba microcomputers, please visit http://www.semicon.toshiba.co.jp/eng/prd/micro/index.html.

Development Systems

● Software Products

Toshiba Integrated Development Environment (TIDE)		Real-Time OS (μITRON 3.0)
C Compiler	Integrated Development Environment	
SW96CN0-ZCC: 1 license SW96CN3-ZCC: 10 licenses	SW96MN0-ZCC: 1 license SW96MN3-ZCC: 10 licenses	SW96RN2-ZCC: Object code can be freely copied SW96RNC-ZCC: Object code can be freely copied. With source code.

● Hardware Products

**:Under development

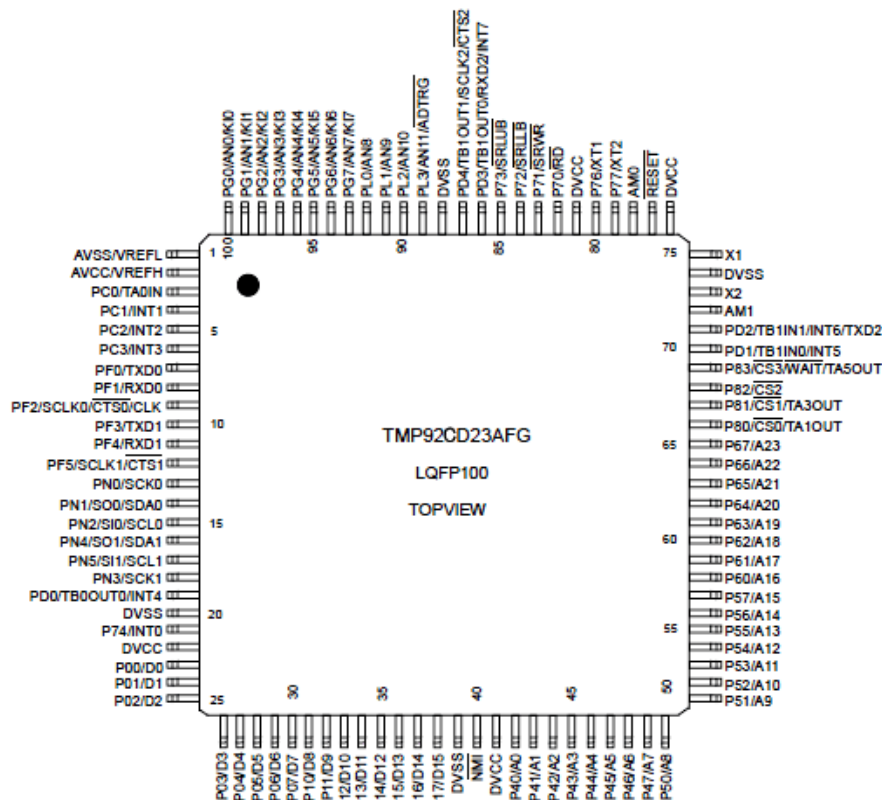| Part number	Test tool	
	Controller	Emulation pod
TMP92CD23AFG**	BM1040R0A/BM1055R0C	BM92FD23AF0A-M15**
TMP92CD23ADFG**		
TMP92CY23FG		BM92CY23F0A-M15
TMP92CY23DFG		

› As to hardware products, additional accessories are also needed.
› For further information about Toshiba microcomputer development systems, please visit http://www.semicon.toshiba.co.jp/mctool/index_e.htm.
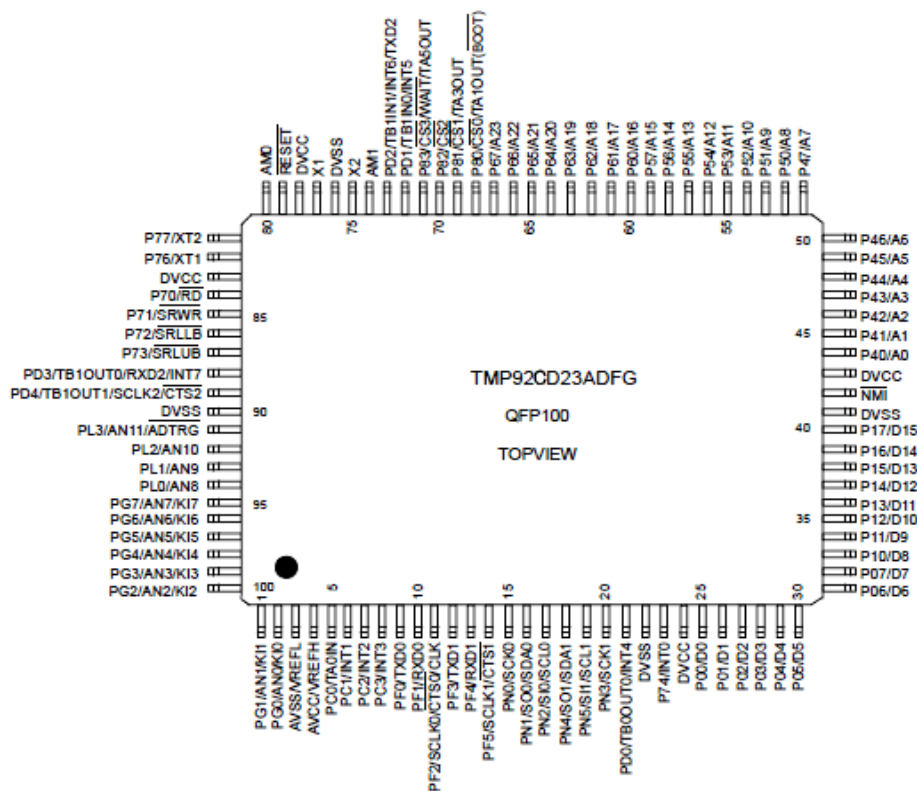
Package Information

●Pin Assignments

Package name FG:P-LQFP100-1414-0.50F

Package Name DFG:P-QFP100-1420-0.65A

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