CMOS 16-Bit Microcontroller

TMP93CF76/CF77/CW76/CU76/CT76

1. Outline and Feature

TMP93CF76/CF77/CW76/CU76/CT76 are a high-speed advanced 16-bit microcontroller developed for application with VCR system control, software servo motor control, VFT driver and timer control.

In addition to basics such as I/O ports, the TMP93CF76/CF77/CW76/CU76/CT76 have high-speed/high-precision signal measuring circuit, PWM (Pulse-Width-Modulator) and high-precision real timing pulse generator.

The device characteristics are as follows:

(1) Original 16-bit CPU (900/L CPU)

- TLCS-90 instruction mnemonic upward compatible
- 16 Mbyte linear address space
- General-purpose registers and register bank system
- 16-bit multiplication/division and bit transfer/arithmetic instructions
- High-speed micro DMA: 4 channels (2 μs/2 byte at 16 MHz)

(2) Minimum instruction execution time: 250 ns at 16 MHz

(3) Internal ROM:

TMP93CF76	192 KB
TMP93CF77	160 KB
TMP93CW76	128 KB
TMP93CU76	96 KB
TMP93CT76	72 KB

(4) Internal RAM:

TMP93CF76	4.0 KB
TMP93CF77	4.0 KB
TMP93CW76	2.5 KB
TMP93CU76	2.5 KB
TMP93CT76	2.0 KB

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(5) 20-bit time-base-counter (TBC)
- Free running counter
- Accuracy: 125 ns (at fc = 16 MHz)
- Overflow: 131 ms (at fc = 16 MHz)

(6) 8-bit timer (TC0): 1 channel
- For CTL linear time counter

(7) 16-bit timer (TC1 to 5): 5 channels
- C.sync count, capstan FG count, general: 3 channels

(8) Timing pulse generator (TPG): 2 channels
- (16-bit timing data + 6-bit output data) with 8-stages FIFO : 1 channel
- (16-bit timing data + 4-bit output data) : 1 channel
- Accuracy: 500 ns (at 16 MHz)

(9) Pulse width modulation outputs (PWM)
- 14-bit PWM: 3 channels (for controlling capstan, drum and tuner)
- 8-bit PWM: 1 channel (for controlling volume)
- Carrier frequency: 31.25 kHz (at 16 MHz)

(10) 24-bit time base counter capture circuit (Capture 0)
- (18-bit timing data + 6 bit trigger data) with 8-stages FIFO: 1 channel
- Capture input sources: Remote-control-input (RMTIN), V.sync, CTL, Drum-PG, general (1 channel)
- Accuracy: 500 ns (at 16 MHz)

(11) 17-bit time base counter capture circuit (Capture 1/2)
- (16-bit timing data + 1-bit trigger data): 2 channels
- Capture input sources: Drum-FG, Capstan-FG
- Accuracy: 125 ns (at 16 MHz)

(12) VISS/VASS detection circuit (VISS/VASS)
- CTL duty detection
- VASS data 16-bit latch

(13) Composite-sync-signal (C.sync) input
- Vertical-sync-signal (V.sync) separation
- Horizontal-sync-signal (H.sync) separation

(14) Head Amp switch/Color Rotary control (HA/CR)

(15) Pseudo-V/H generator (PV/PH)

(16) 8-bit AD converter (ADC): 10 channels
- Conversion speed: 95 states (11.8 μs at 16 MHz)

(17) Serial Channel (SIO): 1channel

(18) Serial bus I/F
- I^2C bus with 8-stages FIFO: 1 channel/2 ports

(19) Watch dog timer (WDT)

(20) Interrupt controller (INTC)

- CPU: 8 sources → SWI instruction and illegal instruction
- Internal: 17 sources
- External: 5 sources

7-level priority can be set.

(21) I/O ports

- 67 I/O ports (multiplexed functional pins.)
  High Break Down Voltage PortE, F are Included: 14 I/O ports
- 8 input ports (P40/AIN2 to P47/AIN9)
- 10 output ports
  PC0/G0 to PC7/G7, PD0/G8 to PD1/G9: High Break Down Voltage

(22) Standby function: 4 halt modes (RUN, IDLE2, IDLE1, STOP)

(23) System clock function

- Dual clock operation 16 MHz (High-speed: normal)/32 kHz (Low-speed:slow)
  … 17-bit Real Time Counter built in

(24) Operating Voltage

- Vcc = 2.7 to 5.5 V (at 32 kHz)
- Vcc = 4.5 to 5.5 V (at 16 MHz)

(25) Package

- 100 pin QFP 14 mm × 20 mm (Pin pitch: 0.65 mm)
- Product name: P-QFP100-1420-0.65A

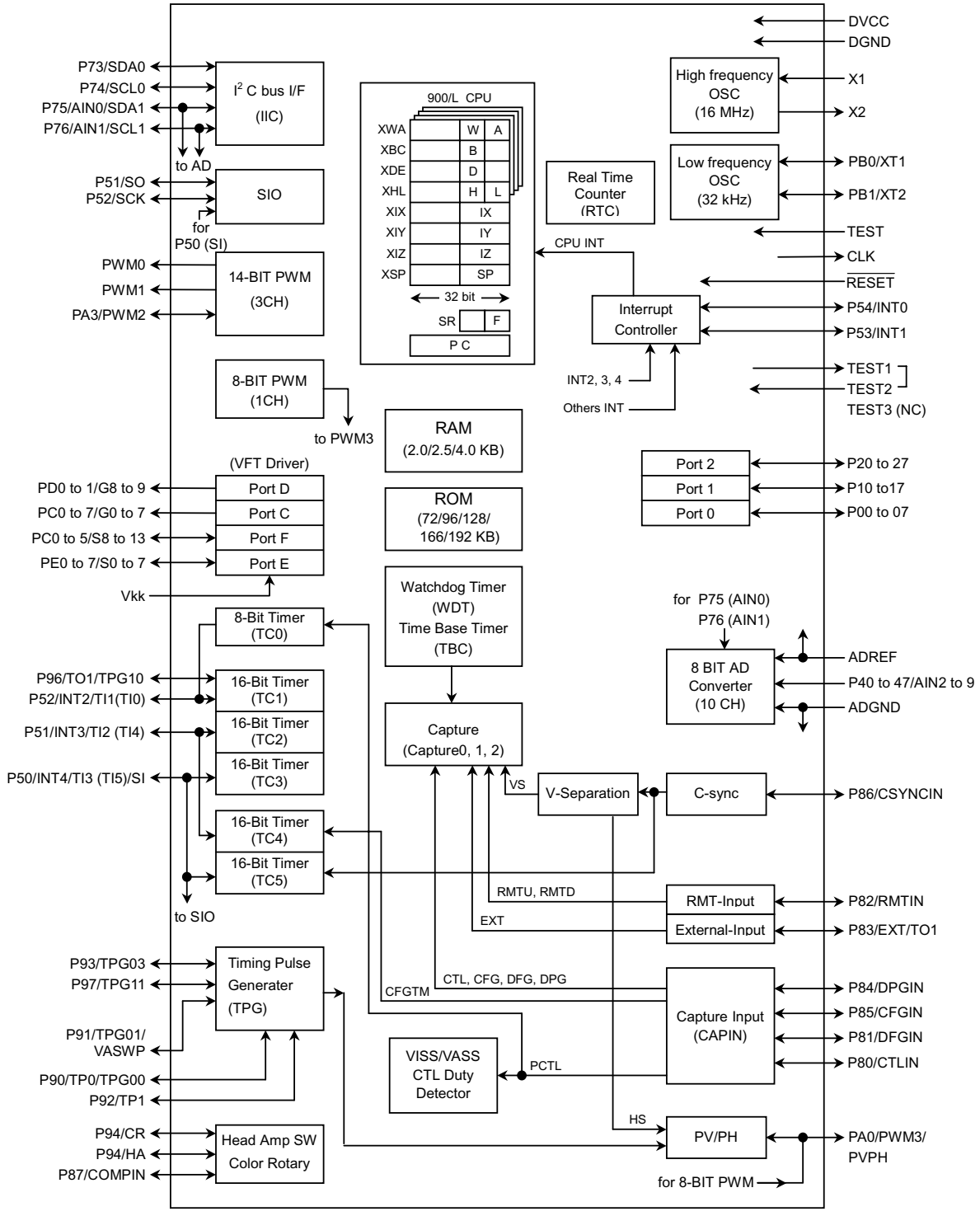


Figure 1.1 TMP93CF76/CF77/CW76/CU76/CT76 block diagram

2. Pin Assignment and Functions

The assignment of input and output pins for the TMP93CF76/CF77/CW76/CU76/CT76, their names and functions are described below.

2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of the TMP93CF76/CF77/CW76/CU76/CT76.

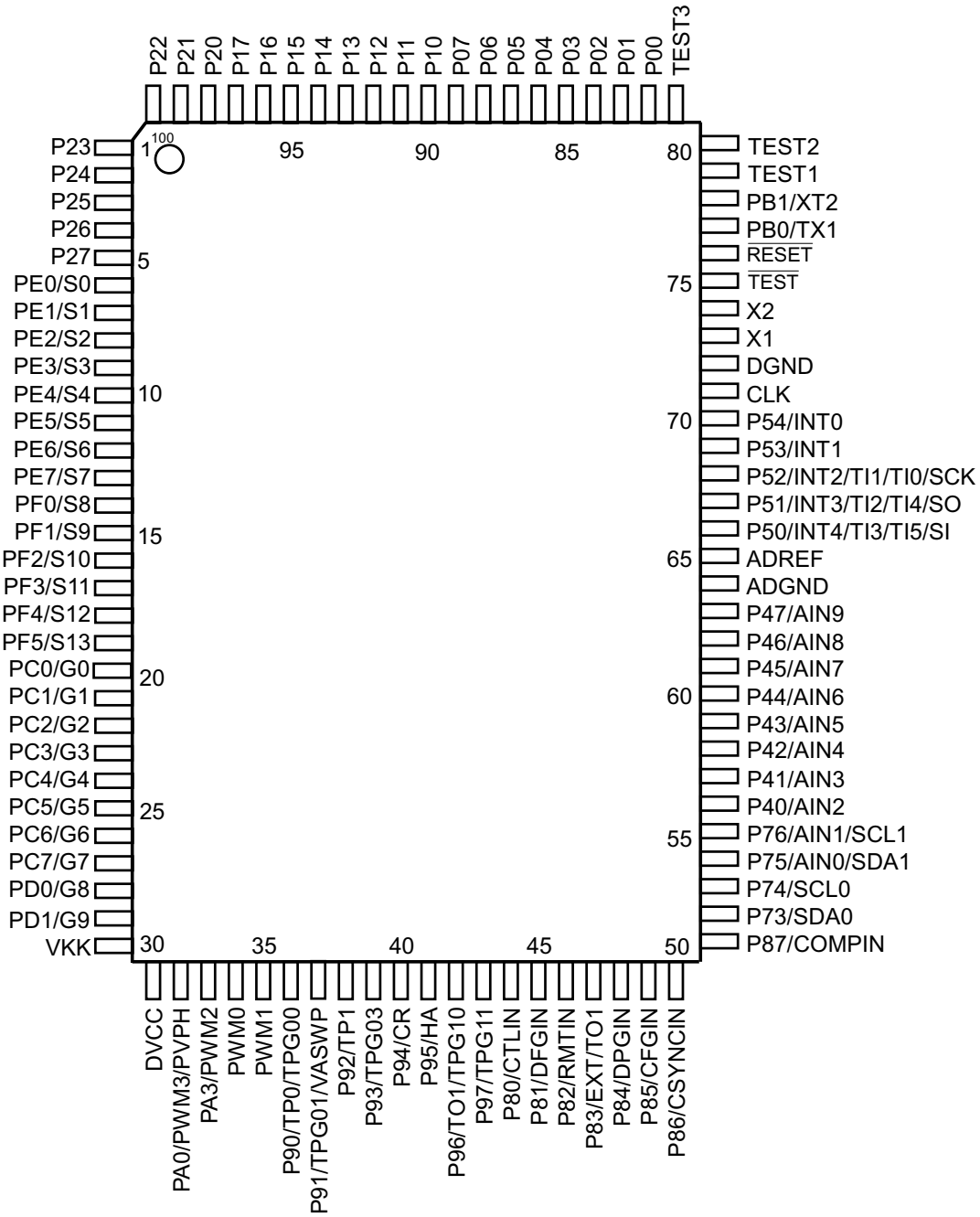


Figure 2.1.1 Pin assignment (100-pin QFP)

2.2 Pin Names and Functions

The names of input/output pins and their functions are described below.

Table 2.2.1 Pin names and function (1/3)

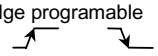
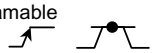
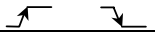
Pin name	Number of pins	I/O	Functions
P00 to P07	8	I/O	port0: I/O ports
P10 to P17	8	I/O	port1: I/O ports
P20 to P27	8	I/O	port2: I/O ports
P40 to P47	8	Input	port4: Input ports
AIN2 to AIN9		Input	Analog input: Input to AD converter
P50	1	I/O	Port50: I/O port (schmitt input)
INT4		Input	External Interrupt request input 4: Rising edge/Falling edge programable
TI3		Input	16-bit timer3 (TC3) Input 3 
TI5		Input	16-bit timer5 (TC5) input 5
SI		Input	SIO received data
P51	1	I/O	Port51: I/O port (schmitt input)
INT3		Input	External Interrupt request input 3: Rising edge/Falling edge programable
TI2		Input	16-bit timer2 (TC2): Input 2 
TI4		Input	16-bit timer4 (TC4): input 4
SO		Output	SIO sending data
P52	1	I/O	Port52: I/O port (schmitt input)
INT2		Input	External Interrupt request input 2: Rising edge/Falling edge programable
TI1		Input	16-bit timer1 (TC1) Input 1 
TI0		Input	8-bit Timer0 (TC0) Input 0
SCK		I/O	SIO clock line
P53	1	I/O	Port53: I/O port (schmitt input)
INT1		Input	External Interrupt request pin1: Rising edge/Level programable 
P54	1	I/O	Port54: I/O port (schmitt input)
INT0		Input	External Interrupt request pin0: Rising edge/Falling edge programable 
P73	1	I/O	Port73: I/O port (schmitt input, Push-pull or open-drain output selectable)
SDA0		I/O	I^2C bus SDA0 line
P74	1	I/O	Port74: I/O port (schmitt input, Push-pull or open-drain output selectable)
SCL0		I/O	I^2C bus SCL0 line
P75	1	I/O	Port75: I/O port (schmitt input, Push-pull or open-drain output selectable)
SDA1		I/O	I^2C bus SDA1 line
AIN0		Input	Analog input 0: Analog input signal for AD converter
P76	1	I/O	Port76: Input port (schmitt input, Push-pull or open-drain output selectable)
SCL1		I/O	I^2C bus SCL1 line
AIN1		Input	Analog input 1: Analog input signal for AD converter
P80	1	I/O	Port80: I/O port (schmitt input)
CTLIN		Input	CTL Capture input (Capture 0)
P81	1	I/O	Port81: I/O port (schmitt input)
DFGIN		Input	DFG Capture input (Capture 1)

Table 2.2.1 Pin names and function (2/3)

Pin name	Number of pins	I/O	Functions
P82	1	I/O	Port82: I/O port (schmitt input)
RMTIN		Input	Remote Control Signal Capture input
P83	1	I/O	Port83: I/O port (schmitt input)
EXT		Input	External Capture input (Capture 0)
TO1		Output	Timer Out 1
P84	1	I/O	Port84: I/O port (schmitt input)
DPGIN		Input	DPG Capture input (Capture 0)
P85	1	I/O	Port85: I/O port (schmitt input)
CFGIN		Input	CFG Capture input (Capture 2)
P86	1	I/O	Port86: I/O port (schmitt input)
CSYNCIN		Input	C.sync Capture input
P87	1	I/O	Port87: I/O port (schmitt input)
COMPIN		Input	Envelope Comparate Input (to HA/CR)
P90	1	I/O	Port90: I/O port (Push-pull or open-drain output selectable)
TP0		Output	Timing Pulse output 0
TPG00		Output	TPG00: TPG0 output
P91	1	I/O	Port91: I/O port (Push-pull or open-drain output selectable)
VASWP		Output	Video/Audio head switching control signal output
TPG01		Output	TPG01: TPG0 output
P92	1	I/O	Port92: I/O port (Push-pull or open-drain output selectable)
TP1		Output	Timing Pulse output 1
P93	1	I/O	Port93: I/O port (Push-pull or open-drain output selectable)
TPG03		Output	TPG03: TPG0 output
P94	1	I/O	Port94: I/O port (Push-pull or open-drain output selectable)
CR		Output	Color Rotary Output
P95	1	I/O	Port95: I/O port (Push-pull or open-drain output selectable)
HA		Output	Head Amp Switching Control Output
P96	1	I/O	Port96: I/O port (Push-pull or open-drain output selectable)
TO1		Output	Timer Out 1
TPG10		Output	TPG10: TPG1 output
P97	1	I/O	Port97: I/O port (Push-pull or open-drain output selectable)
TPG11		Output	TPG11: TPG1 output
PA0	1	I/O	PortA0: I/O port
PVPH		Output	PVPH 3-state Output
PWM3		Output	PWM(8 bits) output 3
PA3	1	I/O	PortA3: I/O port (Push-pull or open-drain output selectable)
PWM2		Output	PWM(14 bits) output 2

Table 2.2.1 Pin names and function (3/3)

Pin name	Number of pins	I/O	Functions
PWM0	1	Output	PWM(14 bits) output 0 (Push-pull or open-drain output selectable)
PWM1	1	Output	PWM(14 bits) output 1 (Push-pull or open-drain output selectable)
PB0 XT1	1	I/O Input	PortB0: I/O port (Open-drain Output) Low Frequency Oscillator connecting pin
PB1 XT2	1	I/O Output	PortB1: I/O port (Open-drain Output) Low Frequency Oscillator connecting pin
PC0 to PC7 G0 to G7	8	Output Output	PortC: Output (High break down voltage outputs with pull-down resistor) Grid Drivers
PD0,1 G8, 9	2	Output Output	PortD: Output (High break down voltage outputs with pull-down resistor) Grid Drivers
PE0 to PE7 S0 to S7	8	I/O Output	PortE: I/O ports (High break down voltage outputs with pull-down resistor) Segment Drivers
PF0 to PF5 S8 to S13	6	I/O Output	PortF: I/O ports (High break down voltage outputs with pull-down resistor) Segment Drivers
TEST1	1	Output	TEST1 should be connected with TEST2 pin.
TEST2	1	Input	
TEST3(NC)	1	Output	TEST3 should be open connection.
CLK	1	Output	Clock output: Output (System Clock ÷ 2) clock. Pulled-up during reset. Can be set to output disable for reducing noise. (Initial Disable)
$\overline{\text{TEST}}$	1	Input	Test pin: Always set to “Vcc” level
$\overline{\text{RESET}}$	1	Input	Reset: Initializes LSI. (with pull-up resistor)
X1	1	Input	High Frequency Oscillator connecting pins (16 MHz)
X2	1	Output	High Frequency Oscillator connecting pins (16 MHz)
VKK	1		VFT Driver power supply pin
DVCC	1		Power supply pin
DGND	1		GND pin (0 V)
ADREF	1		Reference voltage input for AD converter
ADGND	1		GND pin for AD converter

3. Operation

This section describes the functions and basic operational blocks of TMP93CF76/CF77/CW76/CU76/CT76 devices.

See the "7. Points of Concern and Restrictions" for the using notice and restrictions for each block.

3.1 CPU

TMP93CF76/CF77/CW76/CU76/CT76 devices have a built-in high-performance 16-bit CPU (900/L CPU). (For CPU operation, see TLCS-900/L CPU in the previous section).

This section describes CPU functions unique to the TMP93CF76/CF77/CW76/CU76/CT76 that are not described in the previous section.

3.1.1 Reset

To reset the TMP93CF76/CF77/CW76/CU76/CT76, the RESET input must be kept at 0 for at least 10 system clocks. (1.25 μs at 16 MHz) within the operating voltage range and with a stable oscillation.

When reset is accepted, the CPU sets as follows:

- Program Counter (PC) according to Reset Vector that is stored FFFF00H to FFFF02H.

  PC (7:0) ← stored data in location FFFF00H
  PC (15:8) ← stored data in location FFFF01H
  PC (23:16) ← stored data in location FFFF02H
- Stack pointer (XSP) for system mode to 100H.
- IFF2 to 0 bits of status register to 111. (Sets mask register to interrupt level 7.)
- MAX bit of status register to 1. (Sets to maximum mode)
- Bits RFP2 to 0 of status register to 000. (Sets register banks to 0.)

When reset is released, instruction execution starts from PC (reset vector). CPU internal registers other than the above are not changed.

When reset is accepted, processing for built-in I/Os, ports, and other pins is as follows

- Initializes built-in I/O registers as per specifications.
- Sets port pins (including pins also used as built-in I/Os) to general-purpose input/output port mode.

Note: By resetting, register in the CPU except program counter (PC), status register (SR) and stack pointer (XSP) and the data in internal RAM are not changed.

3.2 Memory Map

Figure 3.2.1 is a memory map of the TMP93CF76/CF77/CW76/CU76/CT76.

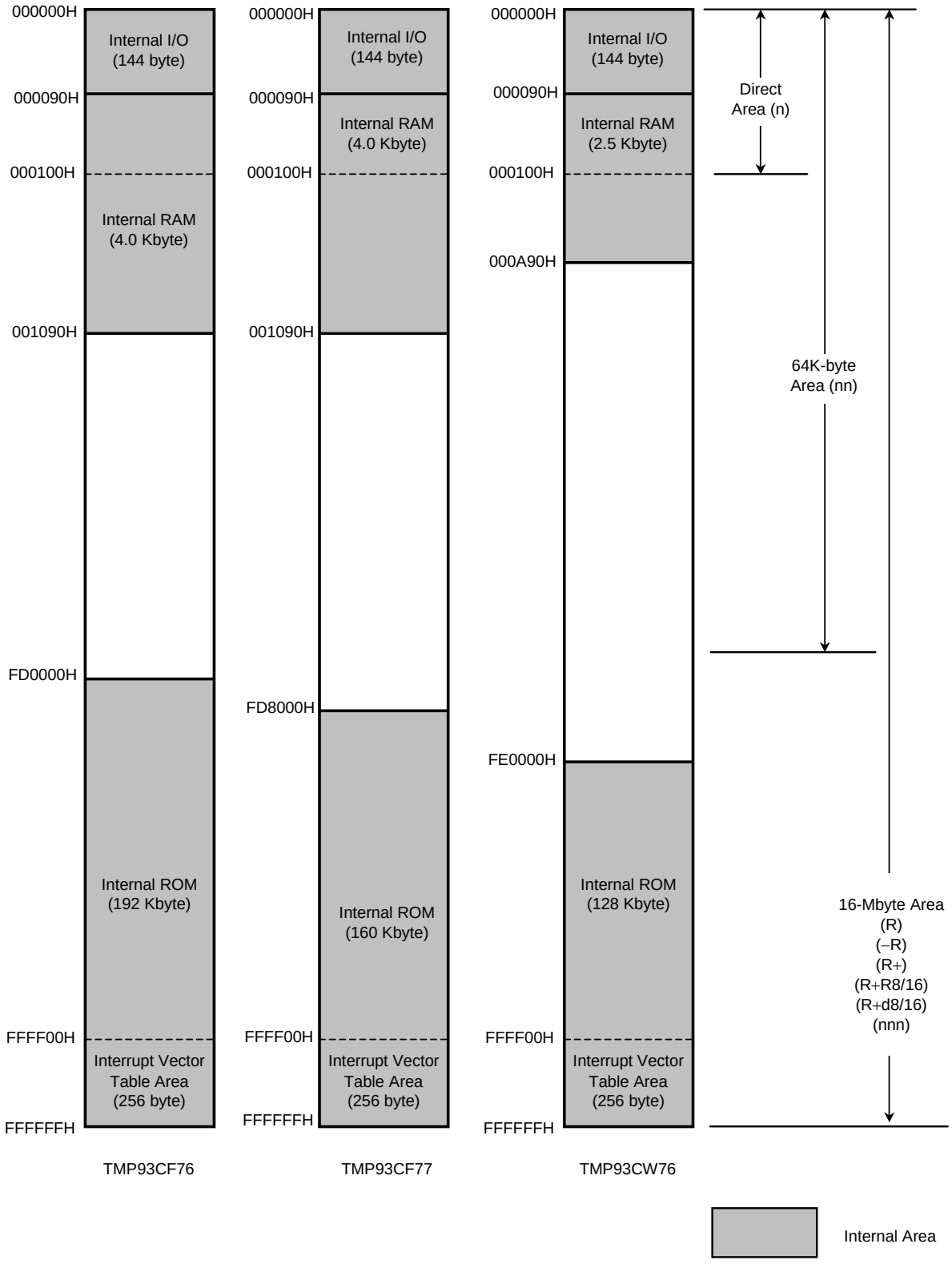


Figure 3.2.1 Memory map (1/2)

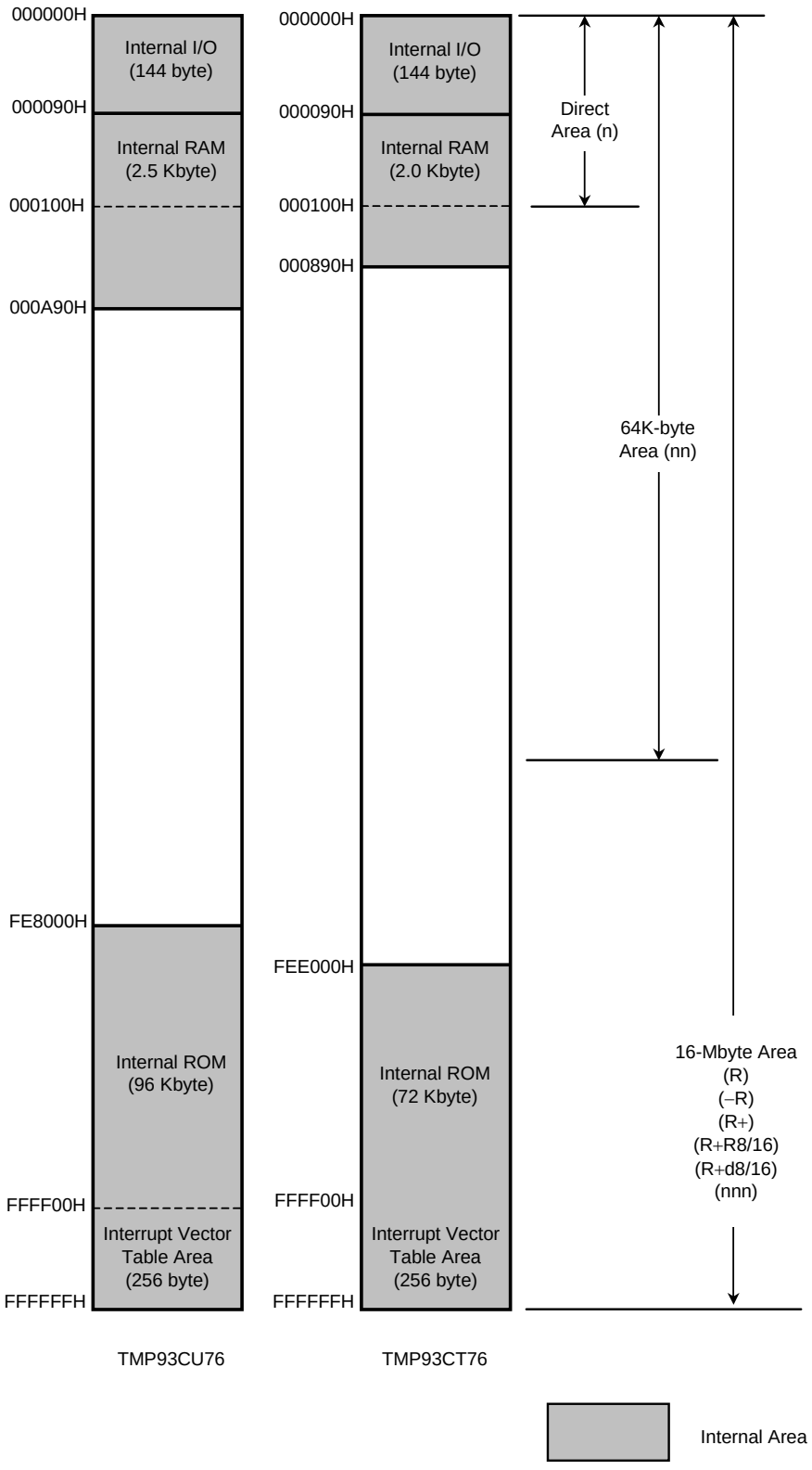


Figure 3.2.1 Memory map (2/2)

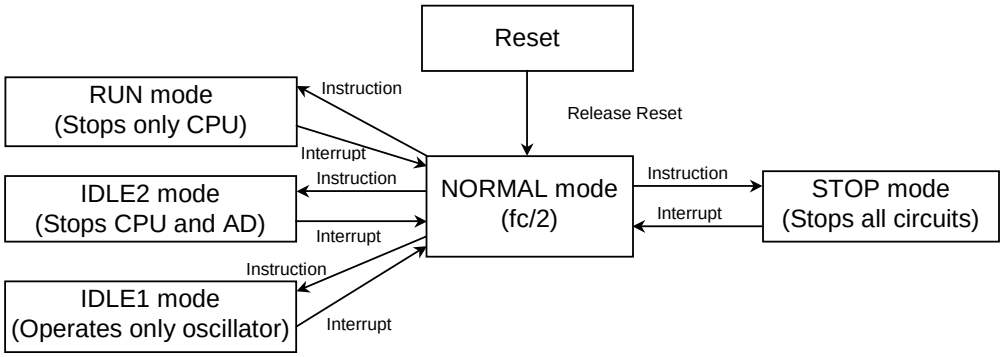
3.3 Dual Clock, Standby Function

Dual Clock, Stand by Control Circuits consist of System clock Controller, Timing clock Generator for I/O Block, Real Time Clock Generator, and Standby Controller.

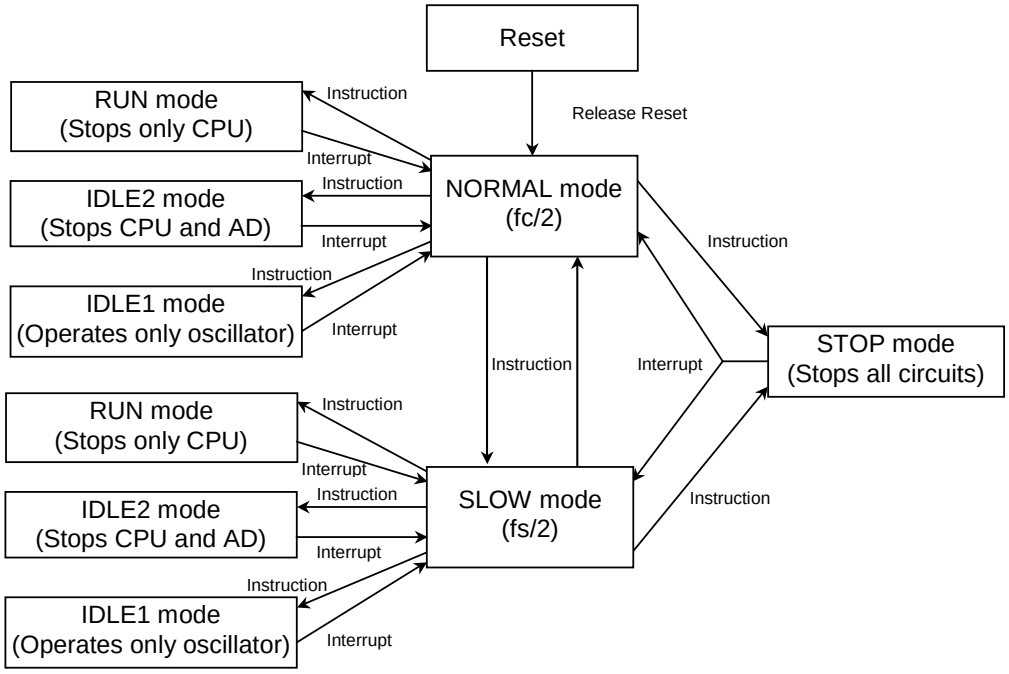
The Oscillator operating mode is classified to Single Clock mode (only X1, X2 pin) and Dual Clock mode (X1, X2, XT1, XT2 pin).

Figure 3.3.1 shows a transition figure. Figure 3.3.2 shows the block diagram.

Figure 3.3.3 shows I/O registers. Table 3.3.1 shows the internal operation and system clock.



(a) Single Clock mode transition figure



(b) Dual Clock mode transition figure

Figure 3.3.1 Transition figure

The clock frequency input from X1, X2 pin is called fc, and the clock frequency input from XT1, XT2 pin is called fs. The clock frequency selected by SYSCR1<SYSCK> is called system clock f_{FPH}. The devided clock of f_{FPH} is called system clock f_{SYS}, and the 1 cycle of f_{SYS} is called 1 state.

Table 3.3.1 Internal operation and system clock

Operating Mode		Oscillator: High Frequency (fc)	Oscillator: Low Frequency (fs)	CPU	Internal I/O	System clock f_{SYS}
Single Clock	RESET	Oscillation	Stop	Reset	Reset	fc/2
	NORMAL			Operate	Operate	
	RUN			Stop		
	IDLE2				Stop only AD	
	IDLE1				Stop	
	STOP	Stop				Stop
Dual Clock	RESET	Oscillation	Stop	Reset	Reset	fc/2
	NORMAL		Progamable	Operate	Operate	
	SLOW	Programable	Oscillation			fs/2
	RUN	Oscillator being used as system clock: oscillation Other oscillator: programmable		Stop		Programable (fc/2, fs/2)
	IDLE2				Stop only AD	
	IDLE1				Stop	
	STOP	Stop				Stop

Note: The TMP93CF76/CF77/CW76/CU76/CT76 does not have a clock gear circuit.

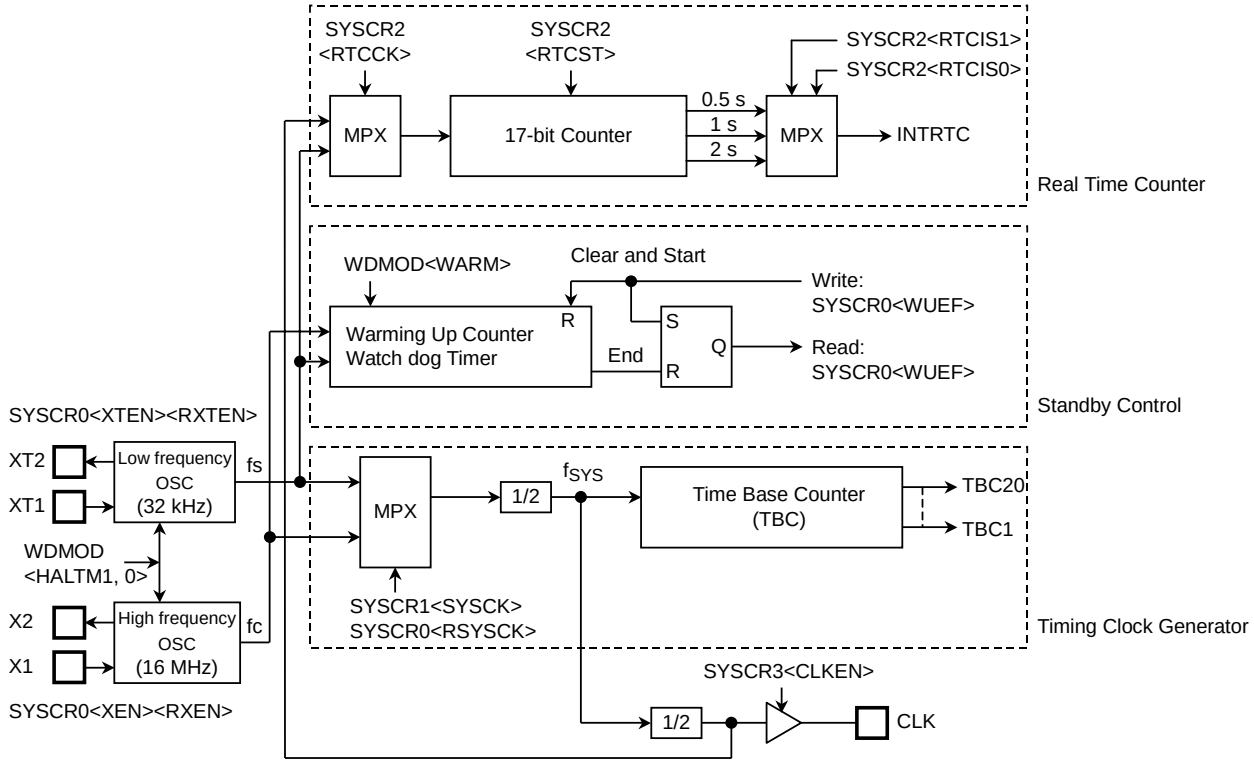


Figure 3.3.2 Block diagram of dual clock, standby circuits

System Clock Control Register 0

SYSCR0	7	6	5	4	3	2	1	0	
(006EH)	XEN	XTEN	RXEN	RXTEN	RSYSCK	WUEF			(Initial Value: 1010 00**)

XEN	High Frequency oscillator (fc)	0: Stop 1: Oscillation	R/W
XTEN	Low Frequency oscillator (fs)	0: Stop 1: Oscillation	
RXEN	High Frequency oscillator (fc) after released STOP mode	0: Stop 1: Oscillation	
RXTEN	Low Frequency oscillator (fs) after released STOP mode	0: Stop 1: Oscillation	
RSYSCK	Clock selection after released STOP mode	0: fc 1: fs	
WUEF	Warm-Up Timer	(READ) 0: End warmming-up 1: Under warmming-up (WRITE) 0: Don't care 1: Timer start	

Note: The bit 1 to 0 are always read out as 1.

System Clock Control Register 1

SYSCR1	7	6	5	4	3	2	1	0	
(006FH)	0				SYSCK	0	0	0	(Initial Value: 0*** 0000)

SYSCK	System clock selection	0: fc 1: fs	R/W

Note 1: The bit 7 should be cleared to 0.

Note 2: The bit 6 to 4 are always read out as 1.

Note 3: Writing 0 to SYSCR1<SYSCK> enables the high-frequency oscillator regardless of the value of SYSCR0<XEN>. Additionally, writing 1 to SYSCR1<SYSCK> enables the low-frequency oscillator regardless of the value of SYSCR0<XTEN>.

System Clock Control Register 2

SYSCR2	7	6	5	4	3	2	1	0	
(006CH)	0	0		RTCCK	RTCST	RTCIS1	RTCIS0		(Initial Value: 00*0 000*)

RTCCK	RTC input clock select	0: fs (32 kHz) 1: $f_{SYS}/2$	R/W
RTCST	RTC count control	0: Stop & Clear 1: Start	
RTCIS1	Interval time control of RTC interrupt	00: $f_{SYS}/2^{16}$ or $fs/2^{15}$ 01: $f_{SYS}/2^{17}$ or $fs/2^{16}$ 10: $f_{SYS}/2^{15}$ or $fs/2^{14}$ 11: Reserved	
RTCIS0			

Note 1: The bit 7 and 6 should be cleared to 0.

Note 2: When SYSCR2<RTCCK> is 1, RTC input clock is fc/4 or fs/4 depending on operation mode.

Watchdog Timer Control Register

WDMOD (005CH)	7	6	5	4	3	2	1	0	(Initial Value: 1000 0000)
	WDTE	WDTP1	WDTP0	WARM	HALTM1	HALTM0	RESCR	DRVE	

WDTE	WDT control	0: Disable 1: Enable	R/W
WDTP1 WDTP0	WDT detection time	00: $2^{15}/f_{SYS}$ 01: $2^{17}/f_{SYS}$ 10: $2^{19}/f_{SYS}$ 11: $2^{21}/f_{SYS}$	
WARM	Warming-up timer source clock selection	0: 2^{14}/ selected clock frequency 1: 2^{16}/ selected clock frequency	
HALTM1 HALTM0	HALT mode selection	00: RUN mode 01: STOP mode 10: IDLE1 mode 11: IDLE2 mode	
RESCR	WDT internal reset control	0: — 1: Connects WDT output to RESET internaly	
DRVE	Pin control of STOP mode	0: I/O off 1: Remains the state before HALT	

Figure 3.3.3 I/O registers about dual clock, standby

3.3.1 System Clock Controller

The system clock controller generates system clock (f_{SYS}) for CPU core and internal I/O. It contains two oscillation circuits. The register SYSCR1<SYSCK> changes system clock to either fc or fs, SYSCR0<XEN>, <XTEN> controls enable/disable each oscillator.

The system clock (f_{SYS}) is set to fc/2 because of <XEN> = 1, <XTEN> = 0, <SYSCK> = 0 by resetting.

For example, f_{SYS} is set to 8 MHz by resetting the case of 16-MHz oscillator is connected to X1, X2 pins.

The high frequency (fc) and low frequency (fs) clocks can be easily obtained by connecting a resonator to the X1/X2, XT1/XT2 pins, respectively. Clock input from an external oscillator is also possible.

The XT1, XT2 pins have also Port PB0, PB1 function. Therefore the case of single clock mode, the XT1, XT2 pins can be used as I/O port pins.

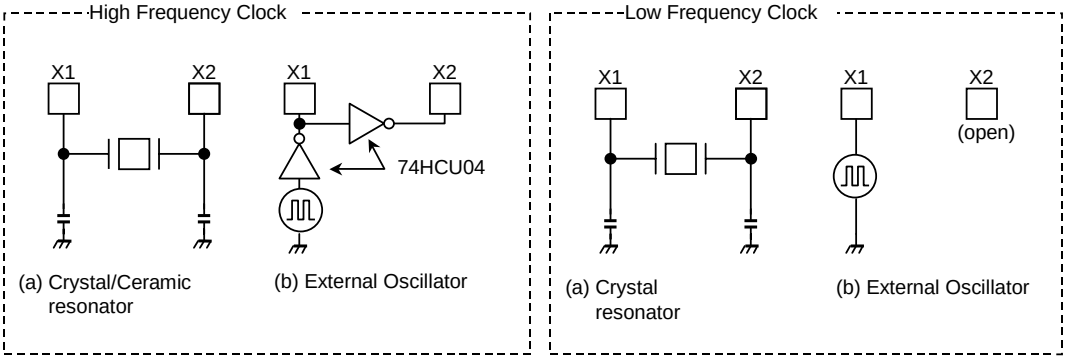


Figure 3.3.4 Examples of resonator connection

Note: In connecting the low frequency resonator to ports PB0 and PB1, it is necessary to make the following settings to reduce the power consumption.
Connecting with resonators
PBCR<PB0C, PB1C> = 11, PB<PB0, PB1> = 00
Connecting with oscillators
PBCR<PB0C, PB1C> = 11, PB<PB0, PB1> = 10

(1) Switching from NORMAL to SLOW mode or from SLOW to NORMAL mode

When the resonator is connected to X1, X2, or XT1, XT2 pin, the warm-up timer is used to change the operation frequency after getting stabilized oscillation.

The warm-up time can be selected by WDMOD<WARM>.

This starting and ending of warm-up timer are performed like the following example 1, 2 by program.

Note 1: The warm-up timer is also used as a watchdog timer. So, when it is used as a warm-up timer, the watchdog timer must be disabled.

Note 2: The case of using oscillator (not resonator) with stabilized oscillation, a warm-up timer is not need.

Note 3: The warm-up timer is operated by a oscillation clock. Therefore, warm-up time has an error.

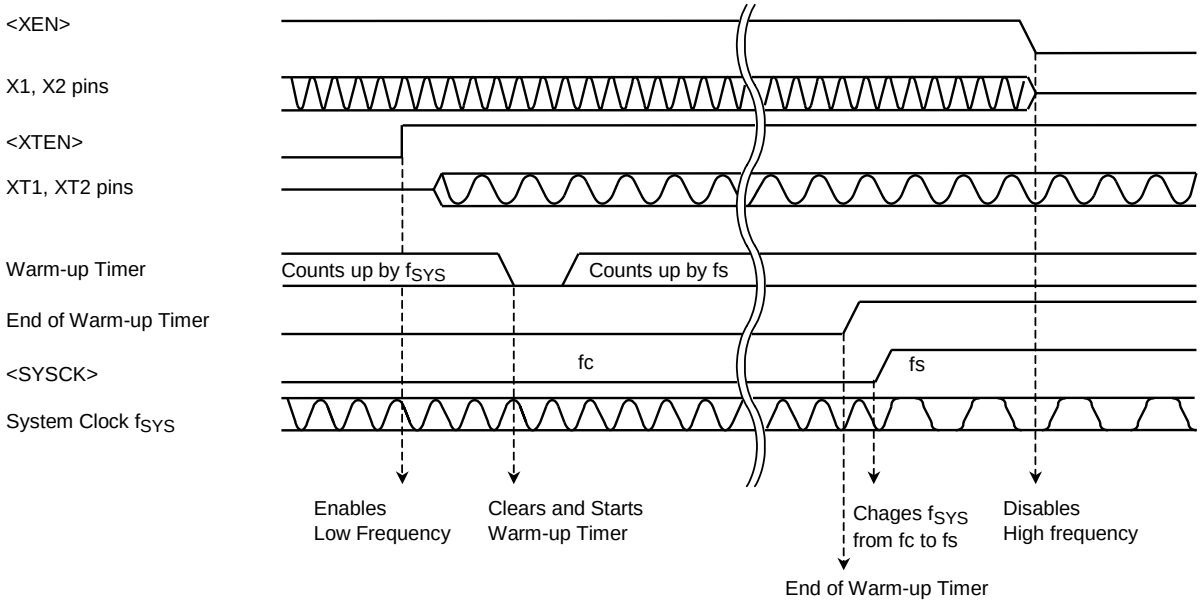
Table 3.3.2 Warm-up time (at fc = 16 MHz, fs = 32.768 kHz)

Warm-up Time WDMOD<WARM>	Change to NORMAL	Change to SLOW
0 (2^{14}/frequency)	1.024 ms	500 ms
1 (2^{16}/frequency)	4.096 ms	2000 ms

Clock Setting Example 1:

Changing from the high frequency (fc) to the low frequency (fs).

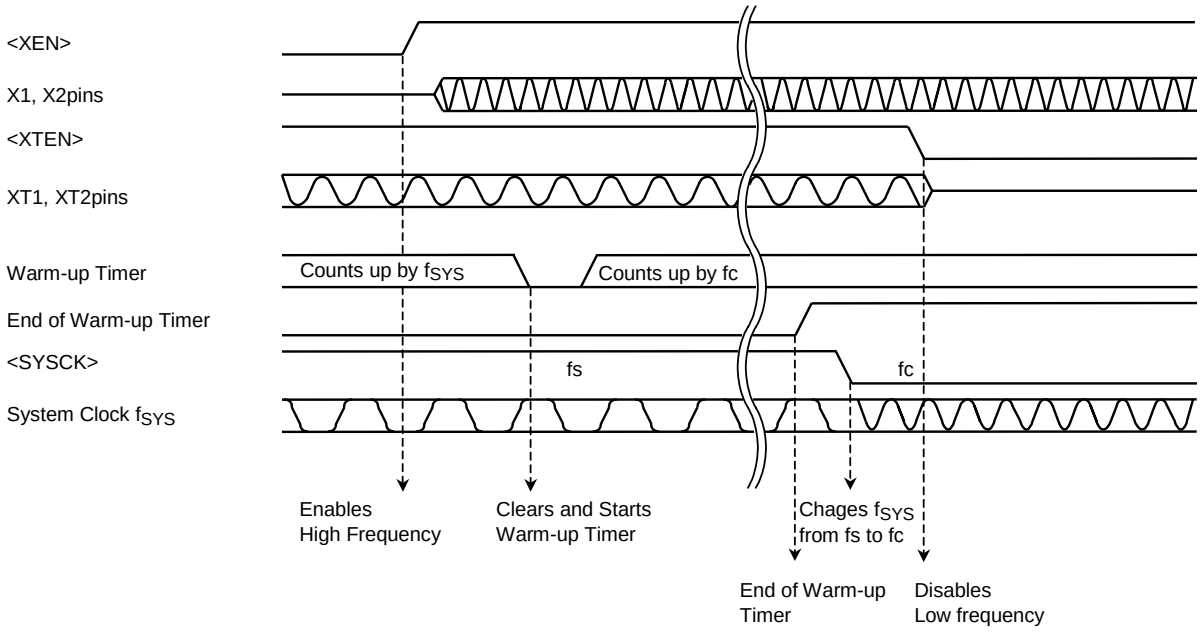
```
SYSCR0   EQU  006EH
SYSCR1   EQU  006FH
WDCR     EQU  005DH
WDMOD    EQU  005CH
         RES  7,(WDMOD)     ;
         LD   (WDCR),0B1H   ;   } Disables Watchdog Timer.
         SET  4,(WDMOD)     ;   Sets Warm-up Time to 2^16/fs.
         SET  6,(SYSCR0)    ;   Enables Low Frequency (fs).
         SET  2,(SYSCR0)    ;   Clears and stars Warm-up Timer.
WUP:     BIT  2,(SYSCR0)    ;
         JR   NZ,WUP        ;   } Detects End of Warm-up Timer.
         SET  3,(SYSCR1)    ;   Changes f_SYS from fc to fs.
         RES  7,(SYSCR0)    ;   Disables High Frequency Oscillation.
         SET  7,(WDMOD)     ;   Enables Watchdog Timer.
```



Clock Setting Example 2:

Changing from the low frequency (fs) to the high frequency (fc).

```
SYSCR0   EQU  006EH
SYSCR1   EQU  006FH
WDCR     EQU  005DH
WDMOD    EQU  005CH
         RES  7,(WDMOD)      ;
         LD   (WDCR),0B1H    ; } Disables Watchdog Timer.
         RES  4,(WDMOD)      ;   Sets Warm-up Time to 2^14/fc.
         SET  7,(SYSCR0)     ;   Enables High Frequency (fc).
         SET  2,(SYSCR0)     ;   Clears and stars Warm-up Timer.
WUP:     BIT  2,(SYSCR0)     ;
         JR   NZ,WUP         ; } Detects End of Warm-up Timer.
         RES  3,(SYSCR1)     ;   Changes fSYS from fs to fc.
         RES  6,(SYSCR0)     ;   Disables Low Frequency Oscillation.
         SET  7,(WDMOD)      ;   Enables Watchdog Timer.
```



3.3.2 Timing Clock Generator

The timing clock generator generates sorts of system clock from the basic clock (fc or fs), providing for CPU core and peripheral hardwares.

(1) Architecture

The timing clock generator consists of the system clock generator and the Time Base Counter (TBC) which generates system clock for peripheral hardwares. After resetting, the system clock is generated from high frequency clock (fc) (NORMAL mode). Both executing the instruction and operating the internal hardwares are synchronized by this system clock.

(2) Time Base Counter (TBC)

The time base counter consists of a 20-bit up-counter counted by a basic clock f_{SYS}, 16-bit data register and control register.

Figure 3.3.5 Shows the composition of the time base counter.

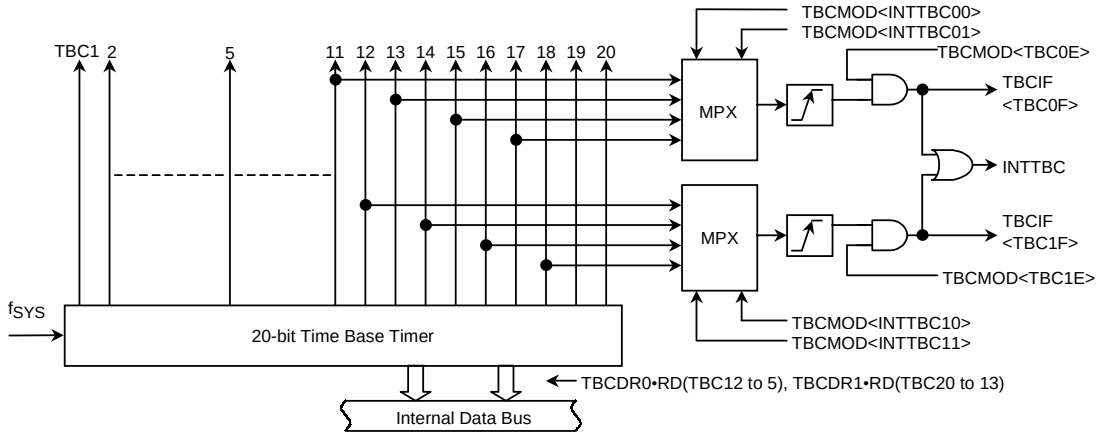


Figure 3.3.5 Composition of time base counter (TBC)

Time Base Counter mode Register

TBCMOD	7	6	5	4	3	2	1	0	
(0023H)	0	0	TBC1E	TBC0E	INTTBC11	INTTBC10	INTTBC01	INTTBC00	(Initial Value: **00 0000)

TBC1E	INTTBC Interrupt Enable/Disable	00: INTTBC0/INTTBC1 interrupt disable 01: INTTBC0 interrupt enable 10: INTTBC1 interrupt enable 11: INTTBC0/INTTBC1 interrupt enable	R/W
TBC0E			
INTTBC11	INTTBC1 Interrupt Source Clock Selection	00: TBC12 01: TBC14 10: TBC16 11: TBC18	
INTTBC10			
INTTBC01	INTTBC0 Interrupt Source Clock Selection	00: TBC11 01: TBC13 10: TBC15 11: TBC17	
INTTBC00			

Note 1: The bit 7 and 6 should be cleared to 0.

Note 2: The bit 7 and 6 are always read out as 1.

Note 3: Prohibt read-modify-write.

Time Base Counter Data Register 0

TBCDR0	7	6	5	4	3	2	1	0	
(0024H)	TBC12	TBC11	TBC10	TBC9	TBC8	TBC7	TBC6	TBC5	(Initial Value: 0000 0000) Read only

Time Base Counter Data Register 1

TBCDR1	7	6	5	4	3	2	1	0	
(0025H)	TBC20	TBC19	TBC18	TBC17	TBC16	TBC15	TBC14	TBC13	(Initial Value: 0000 0000) Read only

Note: A value of TBC20 to 13 is latched to TBCDR1 at reading out TBCDR0.
TBCDR1 must be read out after reading TBCDR0.

Time Base Counter Interrupt Flag Register 0

TBCIF	7	6	5	4	3	2	1	0	
(0026H)	0	0	TBC1F	TBC0F		0			(Initial Value: 0000 *0**)

TBC1F	TBC1 interrupt request flag	(write) 0: Clear request flag 1: Don't set to 1 (read) 0: — 1: Interrupt request	R/W
TBC0F	TBC0 interrupt request flag	(write) 0: Clear request flag 1: Don't set to 1 (read) 0: — 1: Interrupt request	

Note 1: The bit 7, 6 and 2 should be cleared to 0.

Note 2: The bit 7, 6 and 2 are always read as 1.

Note 3: Prohibit read-midify-write.

a. Operation

Time base counter outputs (TBC1 to TBC20) are used as clock source or timing data for Timer/Counter, Capture (CAP0/CAP1/CAP2), timing pulse generator (TPG) and other peripheral I/O blocks. The contents of time base counter outputs TBC5 to TBC20 can be read by reading the time base counter data registers, TBCDR0 and TBCDR1. Note that the data registers must be read in order of TBCDR0 and then TBCDR1.

Time base counter interrupt requests (INTTBC) can be generated on the rising edges of counter outputs TBC11 to TBC18. The interrupt source is selected by the time base counter mode register TBCMOD <INTTBC11, INTTBC10, INTTBC01 and INTTBC00>. The INTTBC interrupt requests are comprised of two interrupt request signals INTTBC0 and INTTBC1 that are logical OR'ed to generate an interrupt request. Which interrupt is requested can be identified by reading the time base counter interrupt request flag register TBCIF <TBC0F> and <TBC1F>.

The INTTBC0 flag <TBC0F> and INTTBC1 flag <TBC1F> can be cleared by writing 0 in the register.

Table 3.3.3 lists the interval time of time base counter outputs.

Table 3.3.3 Interval time of time base counter

	TBC1	TBC2	TBC3	TBC4	TBC5	TBC6	TBC7	TBC8	TBC9	TBC10
Interval Time [s]	$2/f_{SYS}$	$2^2/f_{SYS}$	$2^3/f_{SYS}$	$2^4/f_{SYS}$	$2^5/f_{SYS}$	$2^6/f_{SYS}$	$2^7/f_{SYS}$	$2^8/f_{SYS}$	$2^9/f_{SYS}$	$2^{10}/f_{SYS}$
at fc = 16 MHz [μs]	0.25	0.5	1.0	2.0	4.0	8.0	16.0	32.0	64.0	128.0

TBC11	TBC12	TBC13	TBC14	TBC15	TBC16	TBC7	TBC18	TBC19	TBC20
$2^{11}/f_{SYS}$	$2^{12}/f_{SYS}$	$2^{13}/f_{SYS}$	$2^{14}/f_{SYS}$	$2^{15}/f_{SYS}$	$2^{16}/f_{SYS}$	$2^{17}/f_{SYS}$	$2^{18}/f_{SYS}$	$2^{19}/f_{SYS}$	$2^{20}/f_{SYS}$
256	512	1024	2048	4096	8192	16384	32768	65536	131072

3.3.3 Real Time Counter (RTC)

The TMP93CF76/CF77/CW76/CU76/CT76 have the real time counter (RTC) which generates a periodic interrupt request. The RTC is controlled by System Control Register2 (SYSCR2).

The RTC is a 17bit binary counter and its clock source is selected either low frequency clock (fs) or system clock ($f_{SYS}/2$) by <RTCCK>. To start/stop the counter is controlled by <RTCST>.

The period of interrupt request INTRTC is selected from 3 types by setting <RTCIS1, RTCIS0>.

Table 3.3.4 shows the period of interrupt request INTRTC.

System Clock Control Register 2

SYSCR2	7	6	5	4	3	2	1	0	
(006CH)	0	0		RTCCK	RTCST	RTCIS1	RTCIS0		(Initial Value: 00*0 0000)

RTCCK	RTC input clock select	0: fs 1: $f_{SYS}/2$	R/W
RTCST	RTC count control	0: Stop & Clear 1: Start	
RTCIS1 RTCIS0	Interval time control of RTC interrupt	00: $f_{SYS}/2^{16}$ or $fs/2^{15}$ 01: $f_{SYS}/2^{17}$ or $fs/2^{16}$ 10: $f_{SYS}/2^{15}$ or $fs/2^{14}$ 11: Reserved	

Note 1: When SYSCR2<RTCCK> is set to 1, RTC input clock is assigned to fc/4 or fs/4 depending on the peration mode.

Note 2: The bit 7 and 6 must be cleared to 0.

Table 3.3.4 INTRTC interrupt interval

<RTCCK>	<RTCIS>	INTRTC interrupt interval
0 (fs = 32.768 kHz)	00 01 10	1 s 2 s 0.5 s
1 [f_{SYS} = fc/2 fc = 16 MHz]	00 01 10	8.192 ms 16.384 ms 4.096 ms
1 [f_{SYS} = fs/2 fs = 32.768 kHz]	00 01 10	4 s 8 s 2 s

3.3.4 Standby Controller

(1) Halt mode

When the HALT instruction is executed, the operating mode changes into RUN, IDLE2, IDLE1 or STOP mode depending on the contents of watchdog timer mode register WDMOD<HALTM1,0>. Figure 3.3.6 shows the alternative states of watchdog timer mode registers.

Watchdog Timer Mode Register

WDMOD	7	6	5	4	3	2	1	0	
(005CH)	WDTE	WDTP1	WDTP0	WARM	HALTM1	HALTM0	RESCR	DRVE	(Initial Value: 1000 0000)

WDTE	WDT timer enable/disable control	0: Disable 1: Enable	R/W
WDTP1 WDTP0	WDT detection time	00: $2^{15}/f_{SYS}$ 01: $2^{17}/f_{SYS}$ 10: $2^{19}/f_{SYS}$ 11: $2^{21}/f_{SYS}$	
WARM	Warming-up timer source clock selection	0: 2^{14}/ selected clock frequency 1: 2^{16}/ selected clock frequency	
HALTM1 HALTM0	HALT mode selection	00: RUN mode 01: STOP mode 10: IDLE1 mode 11: IDLE2 mode	
RESCR	WDT internal reset control	0: — 1: Connects WDT output to RESET internaly	
DRVE	Pin control of STOP mode	0: I/O off 1: Remains the state before HALT	

Figure 3.3.6 Watchdog timer mode register

The features of RUN, IDLE2, IDLE1 and STOP modes are as follows.

a. RUN: Only the CPU halts; power consumption remains unchanged.
b. IDLE2: The built-in oscillator and the specified I/O operates. The Power Consumption is redced to 1/2 than that during NORMAL operation.
c. IDLE1: Only the built-in oscillator operates, while all other built-in circuits stop. The Power Consumption is reduced to 1/5 or less than that during NORMAL operation.
d. STOP: All internal circuits including the built-in oscillator stop. This greatly reduces power consumption.

The operations in the halt state is described in Table 3.3.5.

Note: CAPCR<TPRS0> must be set to 1 before setting HALT mode such as STOP, IDLE1, IDLE2. Otherwise Icc may be increased.

Table 3.3.5 I/O operation during Halt mode

Halt mode	RUN	IDLE2	IDLE1	STOP
WDMOD<HALTM1,0>	00	11	10	01
CPU	Stop			
I/O port	Keep the state when the "HALT" instruction was executed.			Refer to Table 3.3.8
8-bit Timer(TC0)	Operate		Stop	
16-bit Timer (TC1,2,3,4,5)				
Dual Clock				
Watchdog Timer				
Interrupt controller				
SIO				
I^2C bus				
8-bit PWM				
14-bit PWM				
Timing Pulse Generator (TPG 0,1)				
Color Rotary				
VISS/VASS				
CSYNC				
PV/PH				
Capture input (Capture1/2)				
Capture 0				
Remote Control Input (RMTIN)				
Time Base Counter (TBC)				
AD Converter				
Real Time Counter (RTC)				

(2) How to Release the Halt mode

These HALT states can be released by resetting or requesting an interrupt. The HALT release sources are determined by the combinations between the states of interrupt mask register <IFF2:0> and the halt modes. The details for releasing the HALT status are shown in Table 3.3.6.

- Released by requesting an interrupt

The operating released from the HALT mode depends on the interrupt enabled status. When the interrupt request level set before executing the HALT instruction exceeds the value of the interrupt mask register, the interrupt due to the source is processed after releasing the halt mode, and CPU starts executing an instruction that follows the HALT instruction. When the interrupt request level set before executing the HALT instruction is less than the value of the interrupt mask register, releasing the halt mode is not executed. (in non-maskable interrupts, interrupt processing is processed after releasing the halt mode regardless of the value of the mask register.)

However only for INT0 and INT1 interrupts, even if the interrupt request level set before executing the HALT instruction is less than the value of the interrupt mask register, releasing the halt mode is executed. In this case, interrupt processing is not processed, and CPU starts executing the instruction next to the HALT instruction, but the interrupt request flag is held at 1.

Note: Usually, interrupts can release all halts status. However, the interrupts = (INT0, INT1), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of fc or fs) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

- Release by resetting

Releasing all halt status is executed by resetting.

When the STOP mode is released by RESET, it is necessary enough resetting time (3 ms or more) to set the operation of the oscillator to be stable.

When releasing the halt mode by resetting, the internal RAM data keeps the state before the “HALT” instruction is executed. However the other setting contents are initialized. (Releasing due to interrupts keep the state before the “HALT” instruction is executed.)

Table 3.3.6 Halt releasing source and Halt releasing operation

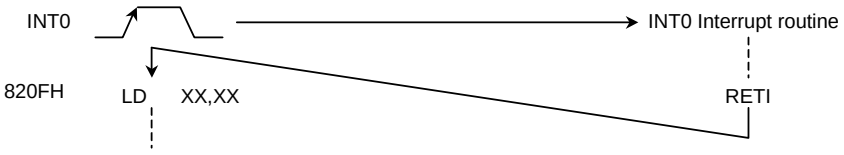
Interrupt Receiving Status			Interrupt Enable (Interrupt level)≥(Interrupt mask)				Interrupt Disable (Interrupt level)<(Interrupt mask)			
Halt mode			RUN	IDLE2	IDLE1	STOP	RUN	IDLE2	IDLE1	STOP
Halt releasing source	Interrupt	INTWD	♦	×	×	×	—	—	—	—
		INT0,1	♦	♦	♦	♦*1	○	○	○	○*1
		INTCAP0, 1	♦	♦	×	×	×	×	×	×
		INTTTG0, 1	♦	♦	×	×	×	×	×	×
		INTI2CB	♦	♦	×	×	×	×	×	×
		INTTBC	♦	♦	×	×	×	×	×	×
		INTSIO	♦	♦	×	×	×	×	×	×
		INTVA	♦	♦	×	×	×	×	×	×
		INT2, 3, 4	♦	♦	×	×	×	×	×	×
		INTT0 to 5	♦	♦	×	×	×	×	×	×
		INTAD	♦	×	×	×	×	×	×	×
		INTRTC	♦	♦	×	×	×	×	×	×
	Reset Input		♦	♦	♦	♦	♦	♦	♦	♦

♦ : After releasing the halt mode, CPU starts interrupt processing (RESET initalizes LSI)
○ : After releasing the halt mode, CPU starts executing an instruction that follows the HALT instruction.
× : It can not be used to release the halt mode.
— : This combination type does not exist because the priority level (interrupt request level) of non-maskable interrupts is fixed to highest priority level 7.
*1: Releasing the halt mode is executed after passing the warming-up time.
Note: When releasing the halt mode is executed by INT1 interrupt of the level mode in the interrupt enabled status, hold level “H” until starting interrupt processing . If level “L” is set before starting interrupt processing, interrupt processing is incorrently started.

(Example releasing “IDLE1” mode)

INT0 interrupt releases HALT state when the IDLE mode is on.

```
Address  ¦
8200H    LD    (IIMC0),01H     ; INT0 interrupt input enable
8203H    LD    (IIMC1),00H     ; Selects interrupt rising edge for INT0
8206H    LD    (INT0CP1),06H   ; Sets interrupt level to 6 for INT0
8209H    EI    5               ; Sets interrupt level to 5 for CPU
820BH    LD    (WDMOD),08H     ; Sets HALT mode to ‘IDLE1’
820EH    HALT                  ; halts CPU
         ¦
```



(3) Operation

a. RUN mode

In the RUN mode, the system clock continues to operate even after a HALT instruction is executed. Only the CPU stops executing the instruction. In the HALT state, an interrupt request is sampled with the falling edge of the internal "CLK" signal.

Releasing the RUN mode is executed by the external/internal interrupts. (See Table 3.3.6 Halt releasing source and Halt releasing operation.)

Figure 3.3.7 shows the interrupt timing for releasing the HALT state by interrupts in the RUN/IDLE2 mode.

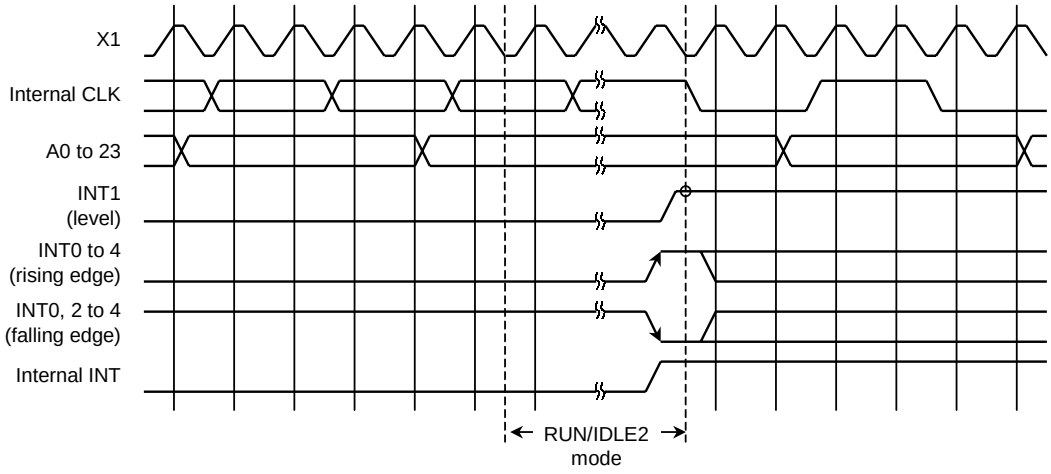


Figure 3.3.7 Timing chart for releasing the HALT state by Interrupt in RUN/IDLE2 modes

b. IDLE2 mode

In the IDLE2 mode, the system clock is supplied to only specific internal I/O devices, and the CPU stops executing the current instruction.

In the IDLE2 mode, the HALT state is released by an interrupt with the same timing as in the RUN mode. The IDLE2 mode is released by external/internal interrupt, except INTWD/INTAD interrupts. (See table 3.3.6 Halt releasing source and Halt releasing operation.)

In the IDLE2 mode, the watchdog timer should be disabled before entering the halt status to prevent the watchdog timer interrupt occurring just after releasing the halt mode.

c. IDLE1 mode

In the IDLE1 mode, only the internal oscillator operates. The system clock in the MCU stops.

In the HALT state, and interrupt request is sampled aynchronunsly with the system clock, however the HALT release (restart of operation) is performed synchronously with it.

IDLE1 mode is released by external interrupts (INT0, INT1). (See table 3.3.6 Halt releasing source and Halt releasing operation.)

Figure 3.3.8 illustrates the timing for releasing the HALT state by interrupts in the IDLE1 mode.

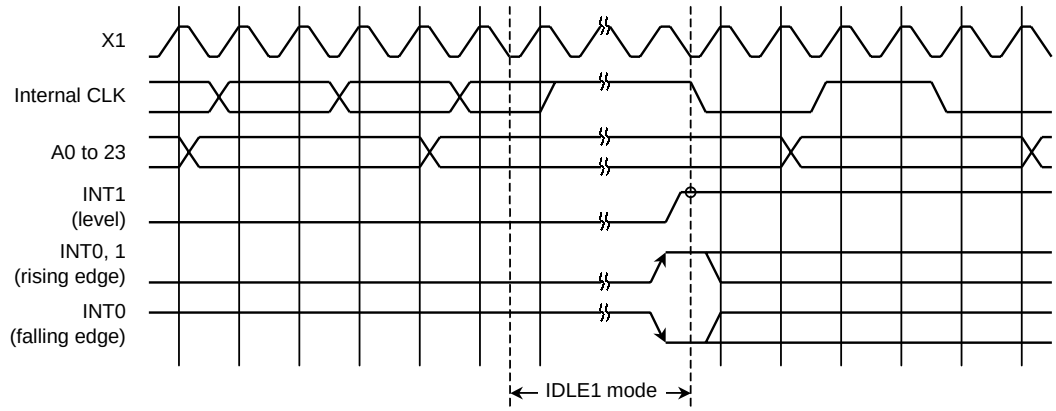


Figure 3.3.8 Timing chart of HALT released by interrupts in IDLE1 mode

d. STOP mode

The STOP mode is selected to stop all internal circuits including the internal oscillator. The pin status in the STOP mode depends on setting of a bit in the watchdog timer mode register WDMOD<DRVE>. (See Figure 3.3.6 for setting of WDMOD <DRVE>.) Table 3.3.8 summarizes the state of these pins in the STOP mode.

The STOP mode is released by external interrupts (INT0, INT1). When the STOP mode is released, the system clock output starts after warm-up time required to attain stable oscillation. The warm-up time can be set using WDMOD<WARM>. See the example of warm-up time (Table 3.3.7).

Figure 3.3.9 illustrates the timing for releasing the HALT state by interrupts during the STOP mode.

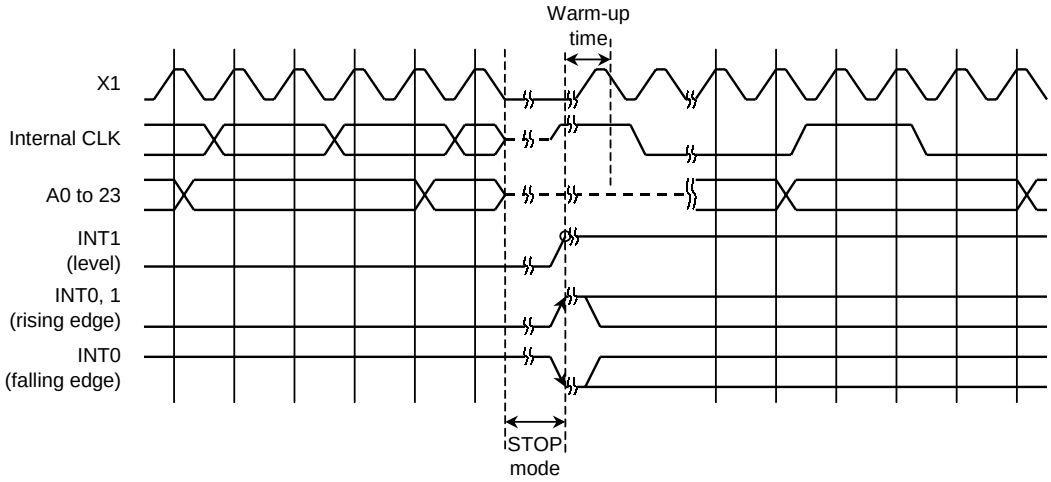


Figure 3.3.9 Timing chart of HALT state release by interrupts in STOP mode

Table 3.3.7 The example of warm-up time after releasing the stop mode

Clock Operation Frequency after the Stop Mode	Warm-up Time [ms]		Clock Frequency
	WDMOD<WARM> = 0	WDMOD<WARM> = 1	
fc	1.024	4.096	fc = 16 MHz
fs	500	2000	fs = 32.768 kHz

How to calculate the warm-up time

WDMOD<WARM> = 0: 2^{14}/selected clock frequency

WDMOD<WARM> = 1: 2^{16}/selected clock frequency

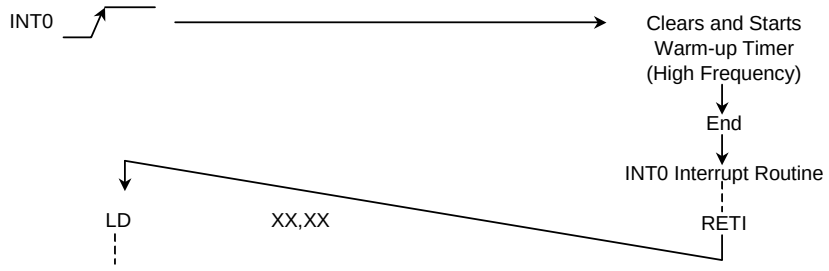
The NORMAL/SLOW mode selection is possible after released STOP mode.

This is selected by SYSCR0 <RSYSCK>. Therefore, Setting to <RSYSCK>, <RXEN>, <RXTEN> is necessary before “HALT” instruction is executed.

Example:

The STOP mode is entered when the low frequency (fs) operates, and after that high frequency (fc) operates after releasing by INT0.

```
Address
            SYSCR0 EQU          006EH
            SYSCR1 EQU          006FH
            WDMOD  EQU          005CH
8FFDH       LD     (SYSCR1),08H     ; fSYS = fs/2
9000H       RES    4,(WDMOD)        ; Sets Warm-up Time to 2^14/fc
9002H       LD     (SYSCR0),-11000- -B ; Operates High Frequency after relesed.
                                        (Note) -: no change
9005H       HALT
```




```
9006H       LD     XX,XX
```

Note: When different modes are used before and after STOP mode as the above mentioned, there is possible to release the HALT mode without changing the operation mode by acceptance of the halt release interrupt request during execution of “HALT” instruction (during 8 states). In the system which accepts the interrupts during execution “HALT” instruction, set the same operation mode before and after the STOP mode.

Table 3.3.8 Pin states in STOP mode

Pin Name	I/O	TMP93CF76/CF77/CW76/CU76/CT76	
		WDMOD <DRVE> = 0	WDMOD <DRVE> = 1
CLK	Output	High-Z	"H" Level Output
X1	Input	—	—
X2	Output	"H" Level Output	"H" Level Output
PB0/PB1	Input/Output	— /High-Z	— /Output
XT1	Input	—	—
XT2	Output	"H" Level Output	"H" Level Output
P40 to P47/AIN2 to AIN9	Input	—	—
P00 to P07, P10 to P17, P20 to P27, P50 to P54, P73 to P76, P80 to P87, P90 to P97, PA0, PA3	Input Output	— High-Z	— Output
PWM0, 1	Output	High-Z	Output
PE0 to PE7, PF0 to PF5	Input Output	— High-Z	— Output
PD0, PD1,PC0 to PC7	Output	High-Z	Output
P53/INT1, P54/INT0	Input Output	Input High-Z	Input Output
$\overline{\text{TEST}}$	Input	"H" Level fixed	"H" Level fixed
$\overline{\text{RESET}}$	Input	Input	Input
ADREF	Input	Open state is available	Open state is available

— : Inputs are not accepted.
Input : Input gate in operation. Fix input voltage level to "L" or "H" so that the input pin stays constant.
Output : Output state
High-Z : High-Impedance

3.4 Interrupts

The interrupts are controlled by the CPU interrupt mask flip-flop <IFF2 to 0> and the built-in interrupt controller.

Altogether the TMP93CF76/CF77/CW76/CU76/CT76 have the following 30 interrupt sources:

- Interrupts from the CPU: 8 sources (software interrupt and illegal instrction execution interrupt)
- Interrupts from the internal peripheral function blocks: 17 sources
- External interrupts (INT0 to INT4): 5 sources

A fixed individual interrupt vector number is assigned to each interrupt source; six levels of priority can also be assigned to each maskable interrupt. Non-maskable interrupts have a fixed priority of 7.

When an interrupt is generated, the interrupt controller sends the value of the priority of the interupt source to the CPU. When more than one interrupt is generated simultaneously, the interrupt controller sends the value of the highest priority (7 for non-maskable interrupts is the highest) to the CPU.

The CPU compares the value of the priority with the value in the CPU interrupt mask register (IFF2 to 0). If the value is greater than the value in the mask register, the interrupt is accepted. The value in the mask register (IFF2 to 0) can be changed by EI instruction (Executing EI n changes the contents of <IFF2 to 0> to n). For example, programming EI 3 enables acceptance of maskable interrupts with a priority of 3 or more, which are set in the interrupt controller, and non-maskable interrupts. However, if programmed as "EI" or "EI 0," maskable interrupts with priority levels 1 or more and nonmaskable interrupts are accepted (same as for "EI 1"). The DI instruction (<IFF2 to 0> = 7) operates in the same way as the EI 7 instruction. Since the priority values for maskable interrupts are 0 to 6, the DI instruction is used to disable acceptance of maskable interrupts. The EI instruction becomes effective immediately after execution (With the TLCS-90, the EI instruction becomes effective after execution of the subsequent instruction).

In addition to the general-purpose interrupt processing mode described above, there is also a Micro DMA processing mode . Micro DMA is a mode used by the CPU to automatically transfer byte or word data. It enables the CPU to process interrupts such as data saves to built-in I/Os at high speed.

Figure 3.4.1 shows a general flow of interrupt handling.

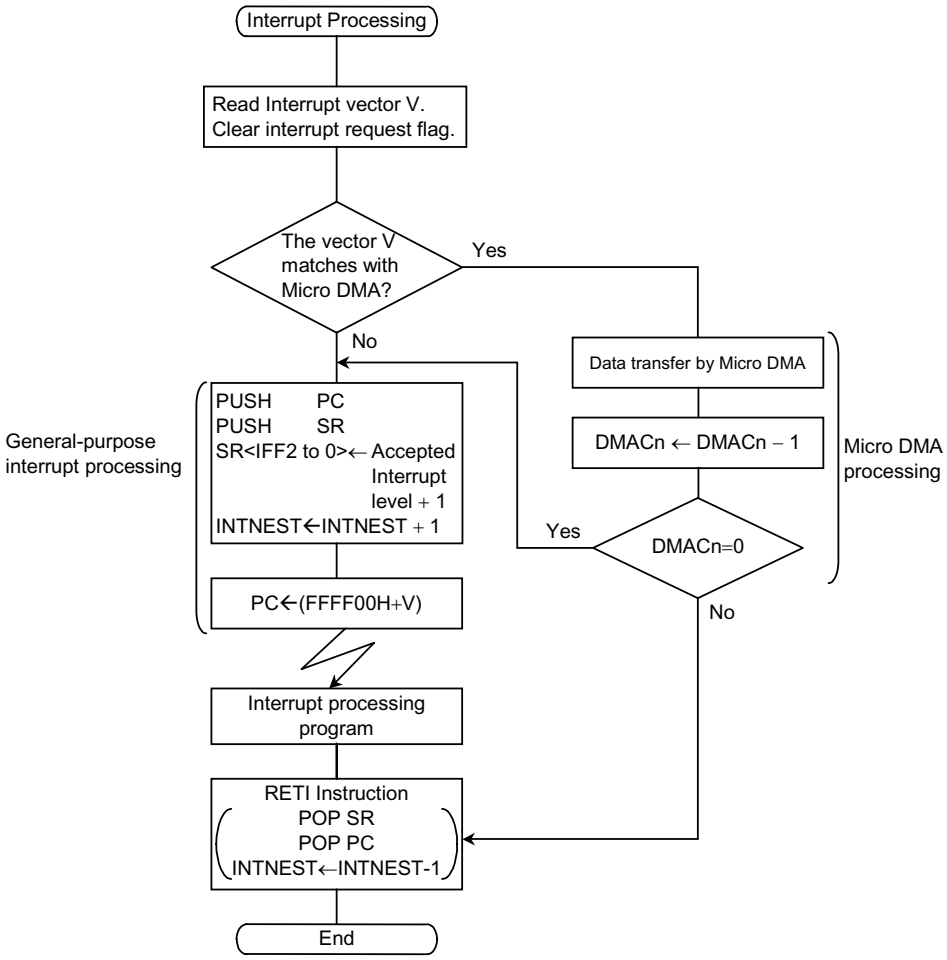


Figure 3.4.1 Interrupt processing flowchart

3.4.1 General-Purpose Interrupt Processing

When accepting an interrupt, the CPU operates as follows. Software interrupt and illegal instruction execution interrupt execute (2), (4) and (5) except (1) and (3).

(1) The CPU reads the interrupt vector from the interrupt controller. When more than one interrupt with the same level is generated simultaneously, the interrupt controller generates interrupt vectors in accordance with the default priority (which is fixed as follows: the smaller the vector value, the higher the priority), then clears the interrupt request.

(2) The CPU pushes the program counter (PC) and the status register (SR) to the system stack area indicated by the system mode stack pointer (XSP).

(3) The CPU sets a value in the CPU interrupt mask register <IFF2 to 0> that is higher by 1 than the value of the accepted interrupt level. However, if the value is 7, 7 is set without an increment.

(4) The CPU increments the INTNEST (Interrupt Nesting Counter).

(5) The CPU jumps to address indicated by data at FFFF00H + interrupt vector, then starts the interrupt processing routine.

The following diagram shows all the above processing state number.

Bus Width of Stack Area	Bus Width of Interrupt Vector Area	Interrupt processing state number
16 bits	16 bits	25

To return to the main routine after completion of the interrupt processing, the RETI instruction is usually used. Executing this instruction restores the contents of the program counter (PC) and the status register (SR) and decrements INTNEST (Interrupt Nesting Counter).

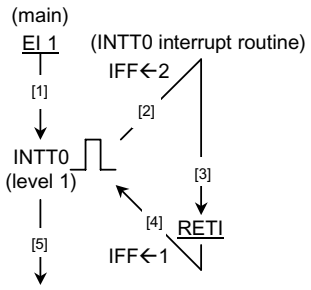
Though acceptance of non-maskable interrupts cannot be disabled by program, acceptance of maskable interrupts can. A priority can be set for each source of maskable interrupts. The CPU accepts an interrupt request with a priority higher than the value in the mask register <IFF2 to 0>. The mask register <IFF2 to 0> is set to a value higher by 1 than the priority of the accepted interrupt. Thus, if an interrupt with a level higher than the interrupt being processed is generated, the CPU accepts the interrupt with the higher level, causing interrupt processing to nest.

The interrupt request with a priority higher than the now accepted interrupt during processing above (1) to (5) is accepted before the 1'st instruction in the interrupt processing routine, causing interrupt processing to nest. (This is the same case of over lapped each Non-Maskable interrupt (level 7).) The CPU does not accept an interrupt request of the same level as that of the interrupt being processed.

The mask register <IFF2 to 0> is initialized 7 after reset. It disables maskable interrupt.

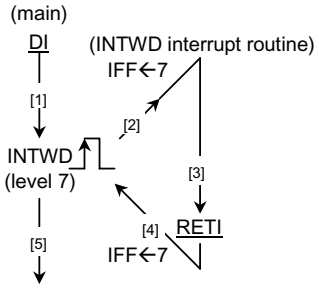
The following (1) to (5) show a flowchart of interrupt processing.

(1) Maskable interrupt



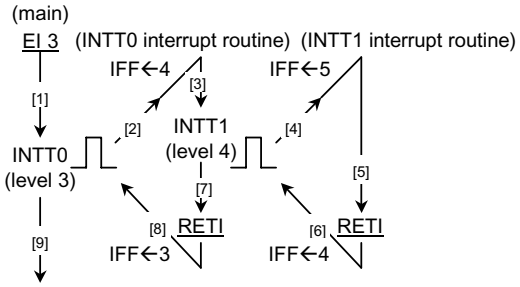
During execution of the main program, the CPU accepts an interrupt request. The CPU increments the IFF so that the interrupts of level 1 are not accepted during processing the interrupt routine.

(2) Non-maskable interrupt



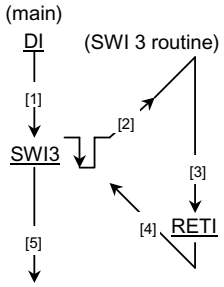
DI instruction is excuted in the main program, so that the interrupts of only level 7 are accepted. The CPU does not increment the IFF even if the CPU accepts an interrupt request of level 7.

(3) Interrupt nesting



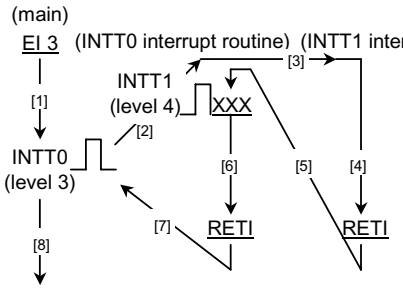
During processing the interrupts of level 3, the IFF is set to 4. When an interrupt with a level higher than level 4 is generated, the CPU accepts the interrupt processing to nest.

(4) Software interrupt



The CPU accepts the software interrupt request during DI status(IFF = 7) because of the level 7. The IFF is not changed by the software interrupts.

(5) Interrupt sampling timing



If an interrupt with a level higher than the interrupt being processed is generated, the CPU accepts the interrupt with the higher level. The program counter which returns at ⑤ is the start address of INTT0 interrupt routine.

___(underline) : Instruction
[1], [2],··· : Execution flow

The address FFFF00H to FFFFFFH (256 bytes) of the TMP93CF76/CF77/CW76/CU76/CT76 are assigned for interrupt vector area.

Table 3.4.1 TMP93CF76/CF77/CW76/CU76/CT76 Interrupt table

Default priority	Type	Interrupt source	Vector value "V"	Address refer to vector	Micro DMA start vector	Interrupt Input (Level/Edge)
1		Reset or SWI0 instruction	0000H	FFFF00H	—	
2		SWI1 instruction	0004H	FFFF04H	—	
3		INTUNDEF: illegal instruction or SWI2 instruction	0008H	FFFF08H	—	
4		SWI3 instruction	000CH	FFFF0CH	—	
5	Non-	SWI4 instruction	0010H	FFFF10H	—	
6	maskable	SWI5 instruction	0014H	FFFF14H	—	
7		SWI6 instruction	0018H	FFFF18H	—	
8		SWI7 instruction	001CH	FFFF1CH	—	
9		(Reserved)	0020H	FFFF20H	—	
10		INTWD: watchdog timer	0024H	FFFF24H	09H	Edge
11		INT0: External interrupt input 0	0028H	FFFF28H	0AH	Edge
12		INTCAP1: Capture 1 interrupt	002CH	FFFF2CH	0BH	Level
13		INTCAP0: Capture 0 interrupt	0030H	FFFF30H	0CH	Level
14		INTTPG0: Timing Pulse Generator 0 interrupt	0034H	FFFF34H	0DH	Edge/Level (Note1)
15		INTTPG1: Timing Pulse Generator1 interrupt	0038H	FFFF38H	0EH	Edge
16		INTI2CB: I^2C bus interrupt	003CH	FFFF3CH	0FH	Edge
17		INTTBC: Time Base Counter interrupt	0040H	FFFF40H	10H	Edge
18		INTVA: VISS/VASS detection	0044H	FFFF44H	11H	Edge
19		INT1: External interrupt input 1	0048H	FFFF48H	12H	Edge/Level
20	Maskable	INT2/INTSIO: External input 2/SIO interrupt	004CH	FFFF4CH	13H	Edge/Level (Note2)
21		INT3: External interrupt input 3	0050H	FFFF50H	14H	Edge
22		INT4: External interrupt input 4	0054H	FFFF54H	15H	Edge
23		INTT0: 8-bit Timer 0 (TC0)	0058H	FFFF58H	16H	Edge
24		INTT1: 16-bit Timer 1 (TC1)	005CH	FFFF5CH	17H	Edge
25		INTT2: 16-bit Timer 2 (TC2)	0060H	FFFF60H	18H	Edge
26		INTT3: 16-bit Timer 3 (TC3)	0064H	FFFF64H	19H	Edge
27		INTT4: 16-bit Timer 4 (TC4)	0068H	FFFF68H	1AH	Edge
28		INTT5: 16-bit Timer 5 (TC5)	006CH	FFFF6CH	1BH	Edge
29		INTAD: AD conversion completion	0070H	FFFF70H	1CH	Level
30		INTRTC: Real Time Counter (RTC)	0074H	FFFF74H	1DH	Edge
—		(Reserved)	0078H	FFFF78H	1EH	
to		to	to	to	to	
—		(Reserved)	00FCH	FFFFFCH	3FH	

Note 1: When the INTTPG0 is used for a FIFO empty interrupt (a level signal), the interrupt request itself is cleared by setting next TPG0 data in the interrupt routine but the request flag (Flip/Flop). Therefore, in this case, the INTTPG0 request flag has to be cleared by an instruction before executing RETI instruction.

Note 2: The serial channel interrupt (INTSIO) and external interrupt 2 (INT2) share one interrupt request flag. Use the Interrupt Source Control Register (ISCR)'s <SELINT> bit to specify which interrupt is requested.

Interrupt Source Control Register

ISCR (008FH)	7	6	5	4	3	2	1	0	
	SELINT								(Initial Value: 0*** ****)

SELINT	Interrupt source select	0: INT2 1: INTSIO	R/W

Setting to Reset/Interrupt Vector

a. Reset Vector

FFFF00H	PC(7:0)
FFFF01H	PC(15:8)
FFFF02H	PC(23:16)
FFFF03H	XX

XX: Don't care

Vector base address	PC setting sequence after reset	
FFFF00H	PC(7:0)	← stored data in location FFFF00H
	PC(15:8)	← stored data in location FFFF01H
	PC(23:16)	← stored data in location FFFF02H

b. Interrupt Vector (except Reset Vector)

Address refer to vector	+0	PC(7:0)
	+1	PC(15:8)
	+2	PC(23:16)
	+3	XX

XX: Don't care

Setting Example

Sets the Reset Vector: 0FF0000H, INTWD Vector: 0FF9ABCH, INTAD Vector: 0FE3456H.

```
ORG     0FFFF00H
DL      0FF0000H      ; Reset = FF0000H

ORG     0FFFF24H
DL      0FF9ABCH      ; INTWD = FF9ABCH

ORG     0FFFF84H
DL      0FE3456H      ; INTAD = FE3456H

ORG     0FE0000H
LD      A,B
        ⋮
ORG     0FF9ABCH
LD      B,C

ORG     0FE3456H
LD      C,A
        ⋮
```

Note:
ORG, DL are Assembler Directives.
ORG: control location counter
DL: defines long word (32 bits) data

3.4.2 Micro DMA

In addition to the conventional interrupt processing, the TMP93CF76/CF77/CW76/CU76/CT76 also has a Micro DMA function. When an interrupt is accepted, in addition to an interrupt vector, the CPU receives data indicating whether processing is Micro DMA mode or general-purpose interrupt. If Micro DMA mode is requested, the CPU performs Micro DMA processing.

(1) Micro DMA operation

Micro DMA operation starts when the accepted interrupt vector value matches the Micro DMA start vector value set in the interrupt controller. The Micro DMA has four channels so that it can be set for up to four types of interrupt source.

When a Micro DMA interrupt is accepted, data is automatically transferred from the transfer source address to the transfer destination address set in the control register, and the transfer counter is decremented. If the value in the counter after decrementing is other than 0, Micro DMA processing is completed; if the value in the counter after decrementing is 0, general-purpose interrupt processing is performed.

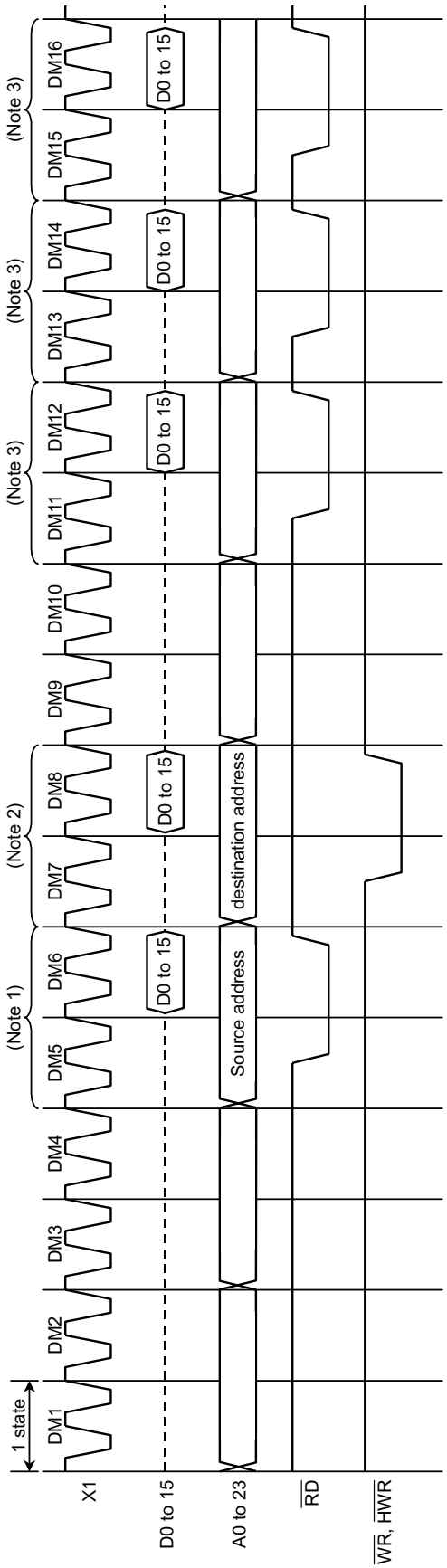
There are two data transfer modes: one-byte mode and one-word mode. Incrementing, decrementing, and fixing the transfer source/destination address after transfer can be done in both modes. Therefore data can easily be transferred between I/O and memory and between I/Os. For details of transfer modes, see the description of transfer mode registers.

The transfer counter has 16 bits, so up to 65536 transfers (the maximum when the initial value of the transfer counter is 0000H) can be performed for one interrupt source by Micro DMA processing.

When the transfer counter is decremented to 0 after data is transferred with micro DMA, general-purpose interrupt processing is performed. After processing the general-purpose interrupt, starting interrupt of the same channel restarts the transfer counter from 65536. Reset the count times to the transfer counter.

Interrupt sources processed by Micro DMA are those with the Micro DMA start vectors listed in Table 3.4.1.

The following timing chart is a Micro DMA cycle of the Transfer Address INC rement mode.



Note 1: These 2 states are added in case the source address is odd or internal I/O.
Note 2: These 2 states are added in case the source address is odd or internal I/O.
Note 3: This may be a dummy cycle with an instruction queue buffer status.
Note 4: D0 to 15, A0 to 23, $\overline{RD}$, $\overline{WR}$ and $\overline{HWR}$ are internal signals.

Figure 3.4.2 Micro DMA cycle (COUNT ≠ 0)

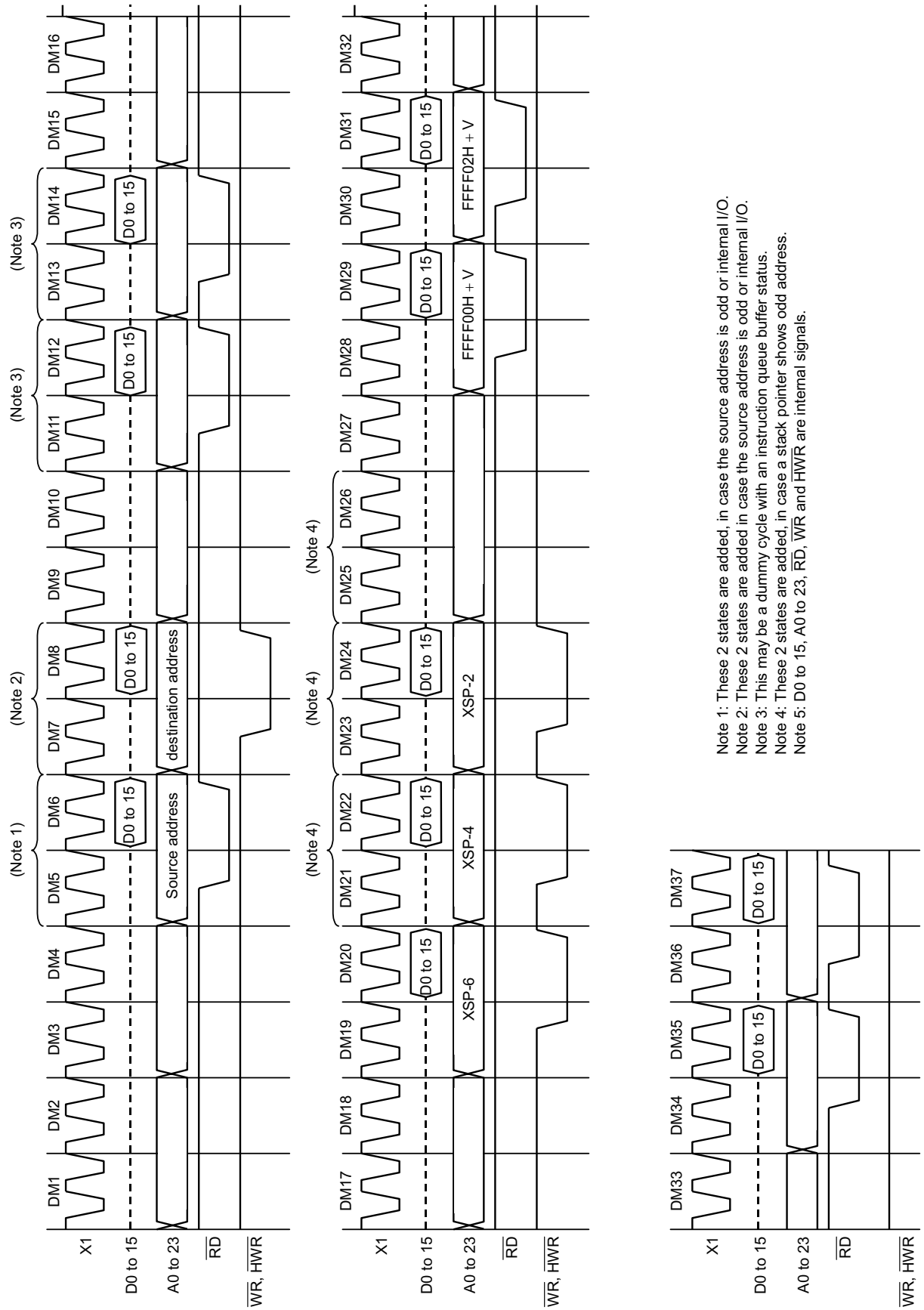
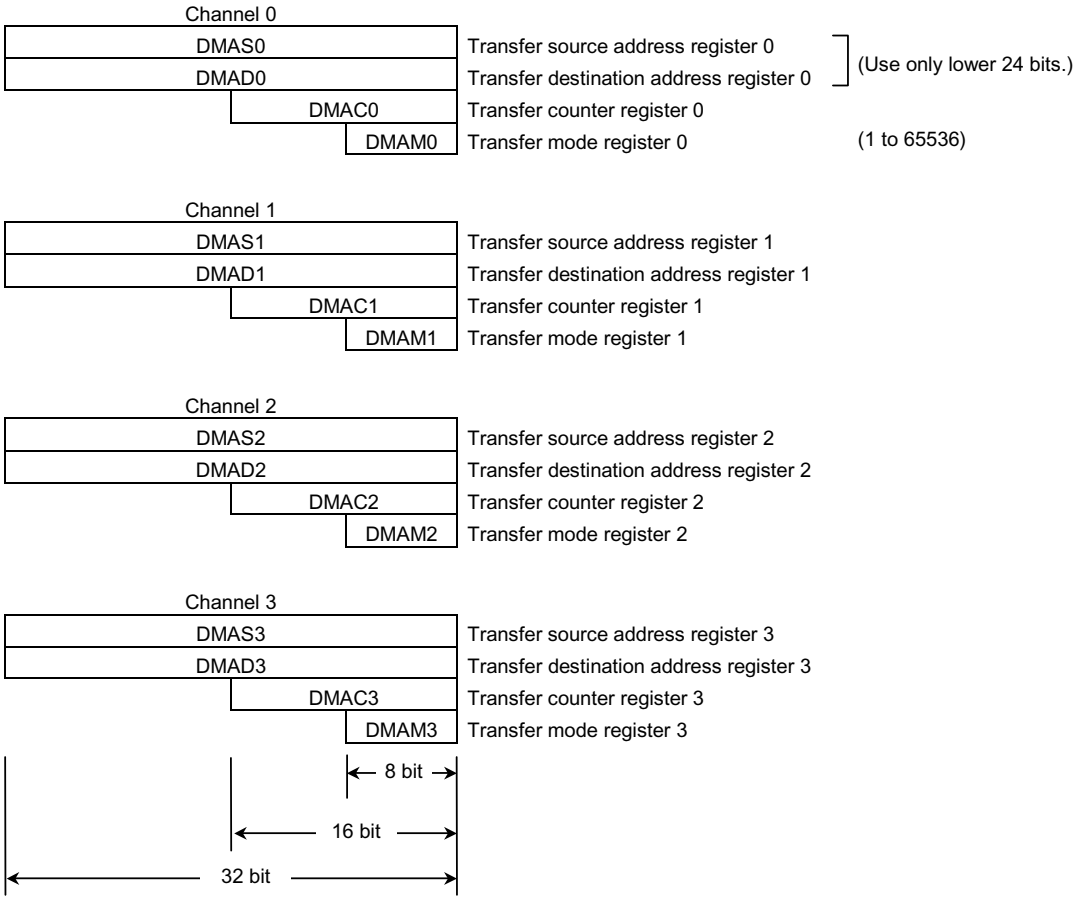


Figure 3.4.3 Micro DMA cycle (COUNT = 0)

(2) Register configuration (CPU control register)



These Control Registers can be set only "LDC cr, r" instruction.

```
Example: LD    XWA, 100H
         LDC   DMAS0, XWA
         LD    XWA, 50H
         LDC   DMAD0, XWA
         LD    WA, 40H
         LDC   DMAC0, WA
         LD    A, 05H
         LDC   DMAM0, A
```

(3) Transfer mode register DMA0 to 3

(DMAM0 to 3)

0	0	0	0	Mode

Note: When setting values for this register, set the upper 4 bits to 0

Z: 0 = Byte transfer, 1 = Word transfer

						<Execution time>
0	0	0	Z	Transfer destination address INC mode (DMADn +) ← (DMASn) DMACn←DMACn −1 if DMACn = 0 then INT.	(Peripheral to Memory)	16 states (2 μs)
0	0	1	Z	Transfer destination address DEC mode (DMADn −) ← (DMASn) DMACn←DMACn −1 if DMACn = 0 then INT.	(Peripheral to Memory)	16 states (2 μs)
0	1	0	Z	Transfer source address INC mode (DMADn) ← (DMASn +) DMACn←DMACn −1 if DMACn = 0 then INT.	(Memory to Peripheral)	16 states (2 μs)
0	1	1	Z	Transfer source address DEC mode (DMADn) ← (DMASn −) DMACn←DMACn −1 if DMACn = 0 then INT.	(Memory to Peripheral)	16 states (2 μs)
1	0	0	Z	Fixed address mode (DMADn) ← (DMASn) DMACn←DMACn −1 if DMACn = 0 then INT.	(Peripheral to Peripheral)	16 states (2 μs)
1	0	1	1	Counter mode DMASn ← DMASn + 1 DMACn←DMACn −1 if DMACn = 0 then INT.	(Interrupt counter)	11 states (1.375 μs)

(1 states = 125 ns at 16 MHz, High frequency mode)

Note 1: n; corresponds to micro DMA channels 0 to 3.

DMADn + / DMASn + : Post-increment(Increments register value after transfer.)

DMADn − / DMASn − : Post-decrement(Decrement register value after transfer.)

Note 2: Execution time: When setting source address/destination address area to ROM/RAM area.

Note 3: Do not use the codes other than the above mantioned codes for transfer mode register.

3.4.3 Interrupt Controller

Figure.3.4.4 shows a configuration of the interrupt controller.

The interrupt controller has an interrupt request flag, an interrupt priority setting register, and a micro-DMA start vector register for each interrupt channel (total 21 channels). The interrupt request flag latches an interrupt request from a peripheral device.

The interrupt request flag is cleared in the following cases:

(1) When the device is initialized (reset)

(2) When the CPU accepted an interrupt and its interrupt vector is read out

(3) When cleared by an instruction (by writing 0 to the Interrupt Priority Control Register's <IxxC> bit)

Example: To clear the INT0 interrupt request, set up the register after the "DI" instruction as shown below.

```
LD (INT0CP1), - - - - 0 - - - B
```

Also, the <IxxC> bit can be read as an interrupt request flag to see if the interrupt request is generated.

Interrupt priority can be set up to six levels using the Interrupt Priority Control Register. Setting the value in this register to 0 or 7 disables the relevant interrupt request. The nonmaskable interrupt (watchdog timer interrupt) has its priority fixed to the highest level (7). If interrupt requests with the same priority level occur simultaneously, they are accepted in order of default priority (which is set in hardware).

The interrupt controller resolves priority between the simultaneously generated interrupts and sends the interrupt request of the highest priority and its vector address to CPU. The CPU compares the priority of the received interrupt request with the values set in the Status Register (SR)'s interrupt mask bits <IFF2:0>. If priority is higher for the requested interrupt, the CPU accepts it and write the value of the accepted interrupt priority plus 1 to <IFF2:0>. When interrupt servicing is finished by RETI instruction, the interrupt priority, that has been saved to the stack, is restored back into <IFF2:0>.

The interrupt controller also handles micro-DMA processing for the interrupt sources used to initiate micro-DMA processing by writing their micro-DMA start vectors to the Micro-DMA Start Vector Register (4 channels). Parameters must be set in the Micro-DMA Control Registers (DMAS3 to 0, DMAD3 to 0, DMAC3 to 0 and DMAM3 to 0) before micro-DMA processing can be performed.

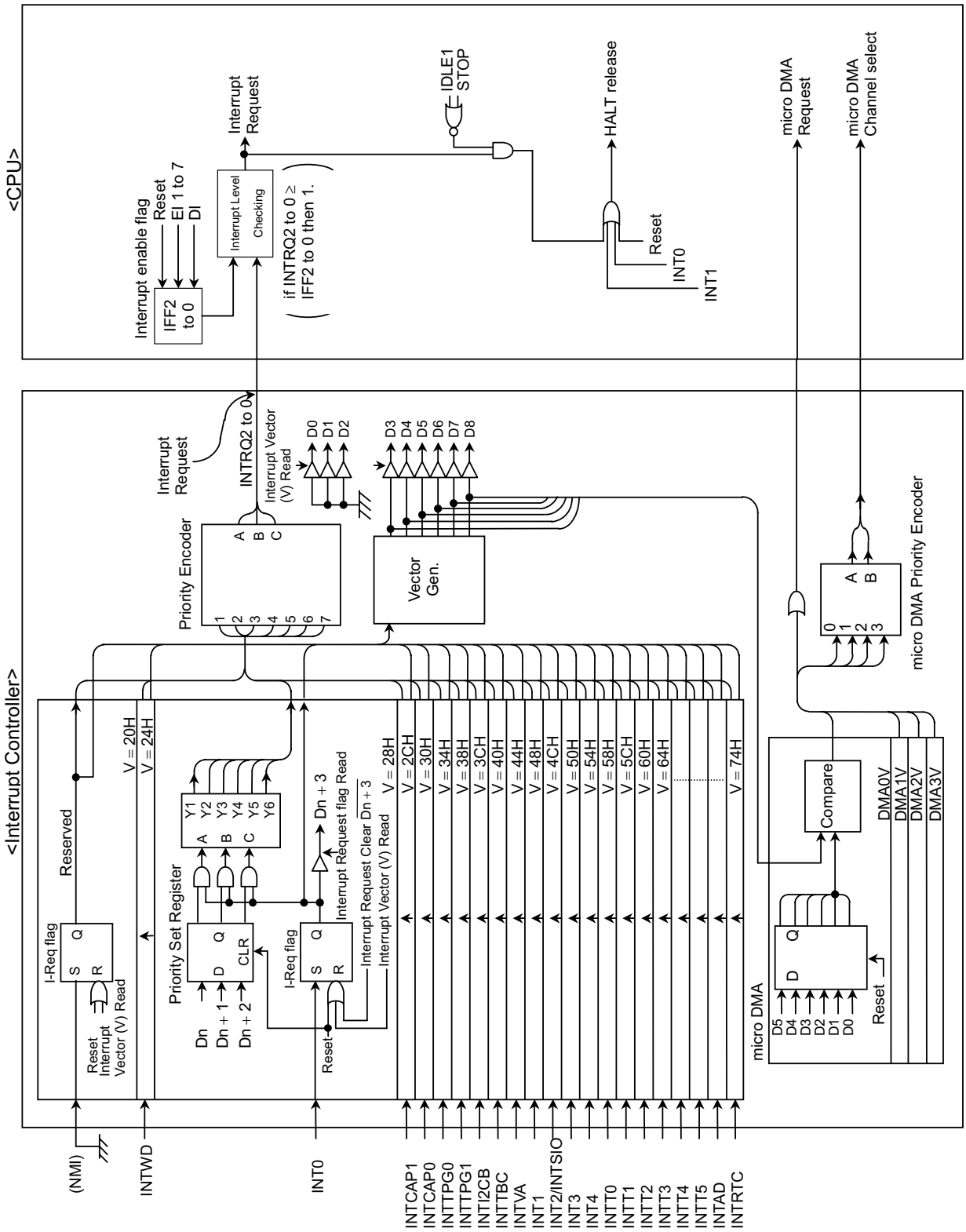


Figure.3.4.4 Block diagram of interrupt controller

(1) Interrupt priority setting register

INT0/CAP1 Interrupt Register

INT0CP1 (0070H)

7	6	5	4	3	2	1	0
ICAP1C	ICAP1M2	ICAP1M1	ICAP1M0	I0C	I0M2	I0M1	I0M0

(Initial Value: 0000 0000)

ICAP1C	CAP1 interrupt request flag	0:No interrupt request (read)/Clear interrupt flag (write) 1:Interrupt request (read)/- (write)	R/W
ICAP1M2 ICAP1M1 ICAP1M0	CAP1 interrupt request level	000: Interrupt request disable 001: Interrupt request level 1 010: Interrupt request level 2 011: Interrupt request level 3 100: Interrupt request level 4 101: Interrupt request level 5 110: Interrupt request level 6 111: Interrupt request disable	write only
I0C	INT0 interrupt request flag	0:No interrupt request (read)/Clear interrupt flag (write) 1:Interrupt request (read)/- (write)	R/W
I0M2 I0M1 I0M0	INT0 interrupt request level	000: Interrupt request disable 001: Interrupt request level 1 010: Interrupt request level 2 011: Interrupt request level 3 100: Interrupt request level 4 101: Interrupt request level 5 110: Interrupt request level 6 111: Interrupt request disable	write only

CAP0/TPG0 Interrupt Register

INTCP0TG0 (0071H)

7	6	5	4	3	2	1	0
ITPG0C	ITPG0M2	ITPG0M1	ITPG0M0	ICAP0C	ICAP0M2	ICAP0M1	ICAP0M0

(Initial Value: 0000 0000)

ITPG0C	TPG0 interrupt request flag	0: No interrupt request (read)/Clear interrupt flag (write) 1: Interrupt request (read)/- (write)	R/W
ITPG0M2 ITPG0M1 ITPG0M0	TPG0 interrupt request level	000: Interrupt request disable 001: Interrupt request level 1 010: Interrupt request level 2 011: Interrupt request level 3 100: Interrupt request level 4 101: Interrupt request level 5 110: Interrupt request level 6 111: Interrupt request disable	write only
ICAP0C	CAP0 interrupt request flag	0: No interrupt request (read)/Clear interrupt flag (write) 1: Interrupt request (read)/- (write)	R/W
ICAP0M2 ICAP0M1 ICAP0M0	CAP0 interrupt request level	000: Interrupt request disable 001: Interrupt request level 1 010: Interrupt request level 2 011: Interrupt request level 3 100: Interrupt request level 4 101: Interrupt request level 5 110: Interrupt request level 6 111: Interrupt request disable	write only

TPG1/I^{2}C bus Interrupt Register

INTTP1I2C (0072H)

7	6	5	4	3	2	1	0
II2CC	II2CM2	II2CM1	II2CM0	ITPG1C	ITPG1M2	ITPG1M1	ITPG1M0

(Initial Value: 0000 0000)

II2CC	I^{2}C bus interrupt request flag	0: No interrupt request (read)/Clear interrupt flag (write) 1: Interrupt request (read)/- (write)	R/W
II2CM2 II2CM1 II2CM0	I^{2}C bus interrupt request level	000: Interrupt request disable 001: Interrupt request level 1 010: Interrupt request level 2 011: Interrupt request level 3 100: Interrupt request level 4 101: Interrupt request level 5 110: Interrupt request level 6 111: Interrupt request disable	write only
ITPG1C	TPG1 interrupt request flag	0: No interrupt request (read)/Clear interrupt flag (write) 1: Interrupt request (read)/- (write)	R/W
ITPG1M2 ITPG1M1 ITPG1M0	TPG1 interrupt request level	000: Interrupt request disable 001: Interrupt request level 1 010: Interrupt request level 2 011: Interrupt request level 3 100: Interrupt request level 4 101: Interrupt request level 5 110: Interrupt request level 6 111: Interrupt request disable	write only

TBC/VA Interrupt Register

INTTBCVA (0073H)

7	6	5	4	3	2	1	0
IVAC	IVAM2	IVAM1	IVAM0	ITBCC	ITBCM2	ITBCM1	ITBCM0

(Initial Value: 0000 0000)

IVAC	VA interrupt request flag	0: No interrupt request (read)/Clear interrupt flag (write) 1: Interrupt request (read)/- (write)	R/W
IVAM2 IVAM1 IVAM0	VA interrupt request level	000: Interrupt request disable 001: Interrupt request level 1 010: Interrupt request level 2 011: Interrupt request level 3 100: Interrupt request level 4 101: Interrupt request level 5 110: Interrupt request level 6 111: Interrupt request disable	write only
ITBCC	TBC interrupt request flag	0: No interrupt request (read)/Clear interrupt flag (write) 1: Interrupt request (read)/- (write)	R/W
ITBCM2 ITBCM1 ITBCM0	TBC interrupt request level	000: Interrupt request disable 001: Interrupt request level 1 010: Interrupt request level 2 011: Interrupt request level 3 100: Interrupt request level 4 101: Interrupt request level 5 110: Interrupt request level 6 111: Interrupt request disable	write only

INT1/INT2/SIO Interrupt Register

INT12SIO (0074H)

7	6	5	4	3	2	1	0
I2C/ SIOC	I2M2/ SIOM2	I2M1/ SIOM1	I2M0/ SIOM0	I1C	I1M2	I1M1	I1M0

(Initial Value: 0000 0000)

I2C/SIOC	INT2/SIO interrupt request flag	0:No interrupt request (read)/Clear interrupt flag (write) 1:Interrupt request (read)/- (write)	R/W
I2M2/SIOM2 I2M1/SIOM1 I2M0/SIOM0	INT2/SIO interrupt request level	000: Interrupt request disable 001: Interrupt request level 1 010: Interrupt request level 2 011: Interrupt request level 3 100: Interrupt request level 4 101: Interrupt request level 5 110: Interrupt request level 6 111: Interrupt request disable	write only
I1C	INT1 interrupt request flag	0:No interrupt request (read)/Clear interrupt flag (write) 1:Interrupt request (read)/- (write)	R/W
I1M2 I1M1 I1M0	INT1 interrupt request level	000: Interrupt request disable 001: Interrupt request level 1 010: Interrupt request level 2 011: Interrupt request level 3 100: Interrupt request level 4 101: Interrupt request level 5 110: Interrupt request level 6 111: Interrupt request disable	write only

INT3/INT4 Interrupt Register

INT43 (0075H)

7	6	5	4	3	2	1	0
I4C	I4M2	I4M1	I4M0	I3C	I3M2	I3M1	I3M0

(Initial Value: 0000 0000)

I4C	INT4 interrupt request flag	0: No interrupt request (read)/Clear interrupt flag (write) 1: Interrupt request (read)/- (write)	R/W
I4M2 I4M1 I4M0	INT4 interrupt request level	000: Interrupt request disable 001: Interrupt request level 1 010: Interrupt request level 2 011: Interrupt request level 3 100: Interrupt request level 4 101: Interrupt request level 5 110: Interrupt request level 6 111: Interrupt request disable	write only
I3C	INT3 interrupt request flag	0: No interrupt request (read)/Clear interrupt flag (write) 1: Interrupt request (read)/- (write)	R/W
I3M2 I3M1 I3M0	INT3 interrupt request level	000: Interrupt request disable 001: Interrupt request level 1 010: Interrupt request level 2 011: Interrupt request level 3 100: Interrupt request level 4 101: Interrupt request level 5 110: Interrupt request level 6 111: Interrupt request disable	write only

Timer0/Timer1 Interrupt Register

INTT1T0 (0076H)

7	6	5	4	3	2	1	0
IT1C	IT1M2	IT1M1	IT1M0	IT0C	IT0M2	IT0M1	IT0M0

(Initial Value: 0000 0000)

IT1C	Timer1 interrupt request flag	0: No interrupt request (read)/Clear interrupt flag (write) 1: Interrupt request (read)/- (write)	R/W
IT1M2 IT1M1 IT1M0	Timer1 interrupt request level	000: Interrupt request disable 001: Interrupt request level 1 010: Interrupt request level 2 011: Interrupt request level 3 100: Interrupt request level 4 101: Interrupt request level 5 110: Interrupt request level 6 111: Interrupt request disable	write only
IT0C	Timer0 interrupt request flag	0: No interrupt request (read)/Clear interrupt flag (write) 1: Interrupt request (read)/- (write)	R/W
IT0M2 IT0M1 IT0M0	Timer0 interrupt request level	000: Interrupt request disable 001: Interrupt request level 1 010: Interrupt request level 2 011: Interrupt request level 3 100: Interrupt request level 4 101: Interrupt request level 5 110: Interrupt request level 6 111: Interrupt request disable	write only

Timer2/Timer3 Interrupt Register

INTT3T2 (0077H)

7	6	5	4	3	2	1	0
IT3C	IT3M2	IT3M1	IT3M0	IT2C	IT2M2	IT2M1	IT2M0

(Initial Value: 0000 0000)

IT3C	Timer3 interrupt request flag	0: No interrupt request (read)/Clear interrupt flag (write) 1: Interrupt request (read)/- (write)	R/W
IT3M2 IT3M1 IT3M0	Timer3 interrupt request level	000: Interrupt request disable 001: Interrupt request level 1 010: Interrupt request level 2 011: Interrupt request level 3 100: Interrupt request level 4 101: Interrupt request level 5 110: Interrupt request level 6 111: Interrupt request disable	write only
IT2C	Timer2 interrupt request flag	0: No interrupt request (read)/Clear interrupt flag (write) 1: Interrupt request (read)/- (write)	R/W
IT2M2 IT2M1 IT2M0	Timer2 interrupt request level	000: Interrupt request disable 001: Interrupt request level 1 010: Interrupt request level 2 011: Interrupt request level 3 100: Interrupt request level 4 101: Interrupt request level 5 110: Interrupt request level 6 111: Interrupt request disable	write only

Timer4/Timer5 Interrupt Register

INTT5T4 (0078H)

7	6	5	4	3	2	1	0
IT5C	IT5M2	IT5M1	IT5M0	IT4C	IT4M2	IT4M1	IT4M0

(Initial Value: 0000 0000)

IT5C	Timer5 interrupt request flag	0: No interrupt request (read)/Clear interrupt flag (write) 1: Interrupt request (read)/- (write)	R/W
IT5M2 IT5M1 IT5M0	Timer5 interrupt request level	000: Interrupt request disable 001: Interrupt request level 1 010: Interrupt request level 2 011: Interrupt request level 3 100: Interrupt request level 4 101: Interrupt request level 5 110: Interrupt request level 6 111: Interrupt request disable	write only
IT4C	Timer4 interrupt request flag	0: No interrupt request (read)/Clear interrupt flag (write) 1: Interrupt request (read)/- (write)	R/W
IT4M2 IT4M1 IT4M0	Timer4 interrupt request level	000: Interrupt request disable 001: Interrupt request level 1 010: Interrupt request level 2 011: Interrupt request level 3 100: Interrupt request level 4 101: Interrupt request level 5 110: Interrupt request level 6 111: Interrupt request disable	write only

AD/RTC Interrupt Register

INTADRTC (0079H)

7	6	5	4	3	2	1	0
IRTCC	IRTM2	IRTM1	IRTM0	IADC	IADM2	IADM1	IADM0

(Initial Value: 0000 0000)

IRTCC	RTC interrupt request flag	0: No interrupt request (read)/Clear interrupt flag (write) 1: Interrupt request (read)/- (write)	R/W
IRTM2 IRTM1 IRTM0	RTC interrupt request level	000: Interrupt request disable 001: Interrupt request level 1 010: Interrupt request level 2 011: Interrupt request level 3 100: Interrupt request level 4 101: Interrupt request level 5 110: Interrupt request level 6 111: Interrupt request disable	write only
IADC	AD interrupt request flag	0: No interrupt request (read)/Clear interrupt flag (write) 1: Interrupt request (read)/- (write)	R/W
IADM2 IADM1 IADM0	AD interrupt request level	000: Interrupt request disable 001: Interrupt request level 1 010: Interrupt request level 2 011: Interrupt request level 3 100: Interrupt request level 4 101: Interrupt request level 5 110: Interrupt request level 6 111: Interrupt request disable	write only

Figure 3.4.5 Interrupt priority setting register

Note 1: The interrupt priority setting register must not be used with read-modify-write instruction.

Note 2: The interrupt request signal and flag of the capture 0 interrupt (INTCAP0) is cleared by reading its data register.

Note 3: The interrupt request signal and flag of the capture 1 interrupt (INTCAP1) is cleared by reading its data register.

Note 4: The interrupt request signal and flag of the SIO interrupt (INTSIO) is cleared by reading its data buffer register.

Note 5: The interrupt request signal and flag of the AD conversion completion interrupt (INTAD) is cleared by reading AD conversion value register.

Note 6: When the timing pulse generator 0 interrupt (INTTPG0) is used as the FIFO empty interrupt, the interrupt request signal is cleared by writing timing data and output data, but the interrupt request flag is not cleared. It is necessary to clear the interrupt request flag by an instruction before executing RETI instruction.

(2) External interrupt control

External Interrupt Control Register 0

IIMC0 (005EH)	7	6	5	4	3	2	1	0
				I4IE (INT4)	I3IE (INT3)	I2IE (INT2)	I1IE (INT1)	I0IE (INT0)

(Initial Value: ***0 0000)

I4IE	External interrupt input	0: Disable 1: Enable	write only
I3IE			
I2IE			
I1IE			
I0IE			

External Interrupt Input Mode Control Register 1

IIMC1 (005FH)	7	6	5	4	3	2	1	0
	I4EG	I3EG	I2EG	I1EG	I0EG		INTTPG0E	INTTPG0S

(Initial Value: 0000 0*00)

I4EG	INT4 edge selection	0: Rising edge 1: Falling edge	write only
I3EG	INT3 edge selection	0: Rising edge 1: Falling edge	
I2EG	INT2 edge selection	0: Rising edge 1: Falling edge	
I1EG	INT1 edge/level selection	0: Rising edge 1: Level	
I0EG	INT0 edge selection	0: Rising edge 1: Falling edge	

Figure 3.4.6 Interrupt Input Mode Control Register

Note 1: The INT0 and INT1 pins can also be used for standby release. When these pins are not used for standby release, setting IIMC0<I1IE, I0IE> to 00 maintains the port function during standby mode.

Note 2: When the active edge is changed by the IIMC1<I4EG, I3EG, I2EG, I1EG, I0EG>, they must be changed after disabling interrupt.

Example:

```
LD    (INT0CP1)    , XXXX0000B  ; Disable the INT0 interrupt, clear the INT0 interrupt
                                  request flag.
LD    (IIMC0)      , XXXXXXX0B  ; Disable the INT0 input
LD    (IIMC1)      , XXXX1XXXB  ; Change the active edge to falling edge from rising
                                  edge.
LD    (INT0CP1)    , XXXX0nnnB  ; Set interrupt level “nnn” for INT0, clear the interrupt
                                  request flag.
```

Note 3: The minimum pulse width for external interrupt signal is $2/f_{SYS}$ [s] (250 ns at fc = 16 MHz).

Note 4: Prohibt read-modify-write.

Table 3.4.2 Setting of external interrupt pin functions

Interrupt	Shared Pin	Mode	Setting Method
INT0	P54	 Rising edge	IIMC1<I0EG> = 0,IIMC0<I0IE> = 1
		 Falling edge	IIMC1<I0EG> = 1,IIMC0<I0IE> = 1
INT1	P53	 Rising edge	IIMC1<I1EG> = 0,IIMC0<I1IE> = 1
		 Level	IIMC1<I1EG> = 1,IIMC0<I1IE> = 1
INT2	P52	 Rising edge	IIMC1<I2EG> = 0,IIMC0<I2IE> = 1
		 Falling edge	IIMC1<I2EG> = 1,IIMC0<I2IE> = 1
INT3	P51	 Rising edge	IIMC1<I3EG> = 0,IIMC0<I3IE> = 1
		 Falling edge	IIMC1<I3EG> = 1,IIMC0<I3IE> = 1
INT4	P50	 Rising edge	IIMC1<I4EG> = 0,IIMC0<I4IE> = 1
		 Falling edge	IIMC1<I4EG> = 1,IIMC0<I4IE> = 1

(3) Micro DMA start vector

When the CPU reads the interrupt vector after accepting an interrupt, it simultaneously compares the interrupt vector with each channel's Micro DMA start vector (bits 3 to 8 of the interrupt vector). When the two match up, the interrupt from the channel whose value matched is processed in Micro DMA mode.

If an interrupt vector matches up in more than two channels, the channel with the lower number has higher priority.

Micro DMA0 Start Vecter Register

DMA0V	7	6	5	4	3	2	1	0	
(007CH)			DMA0V5	DMA0V4	DMA0V3	DMA0V2	DMA0V1	DMA0V0	(Initial Value: **00 0000) Write only

Micro DMA1 Start Vecter Register

DMA1V	7	6	5	4	3	2	1	0	
(007DH)			DMA1V5	DMA1V4	DMA1V3	DMA1V2	DMA1V1	DMA1V0	(Initial Value: **00 0000) Write only

Micro DMA2 Start Register

DMA2V	7	6	5	4	3	2	1	0	
(007EH)			DMA2V5	DMA2V4	DMA2V3	DMA2V2	DMA2V1	DMA2V0	(Initial Value: **00 0000) Write only

Micro DMA3 Start Register

DMA3V	7	6	5	4	3	2	1	0	
(007FH)			DMA3V5	DMA3V4	DMA3V3	DMA3V2	DMA3V1	DMA3V0	(Initial Value: **00 0000) Write only

Note: Prohibt read-modify-write.

Figure 3.4.7 Micro DMA start vector

(4) Notice of the interrupt controller

When the CPU fetches an instruction to clear the interrupt request flag for the interrupt controller immediately before an interrupt is generated, the CPU may execute the instruction between receiving the interrupt and reading the interrupt vector. In such a case, the CPU reads default vector 0028H and the interrupt vector at address FFFF28H.

To avoid the above occurring, clear the interrupt request flag by entering the instruction to clear the flag after the DI instruction. In the case of setting an interrupt enable again by EI instruction after the execution of clearing instruction, execute EI instruction after clearing instruction and following more than one instruction are executed. When EI instruction is placed immediately after clearing instruction, an interrupt becomes enable before interrupt request flags are cleared.

In the case of changing the value of the interrupt mask register <IFF2: 0> by execution of POP SR instruction, disable an interrupt by DI instruction before execution of POP SR instruction

3.5 Functions of Ports

The TMP93CF76/CF77/CW76/CU76/CT76 have 67 bits for I/O ports, 8 bits for input ports and 10 bits for output ports. These port pins have I/O functions for the built-in CPU and internal I/Os as well as general-purpose I/O port functions. Table 3.5.1 lists the function of each port pin. Resetting makes the pins listed below function as general-purpose I/O ports.

Table 3.5.1 Functions of ports

Port Name	Pin Name	Pin No.	Direction	Output Mode	Direction/ Output Mode setting unit	Pin Name for Built-in Function
Port 0	P00 to P07	8	I/O	Push-pull	Bit	
Port 1	P10 to P17	8	I/O	Push-pull	Bit	
Port 2	P20 to P27	8	I/O	Push-pull	Bit	
Port 4	P40 to P47	8	Input	-	(fixed)	AIN2 to AIN9
Port 5	P50	1	I/O	Push-pull	Bit	INT4/TI3/TI5/SI
	P51	1	I/O	Push-pull	Bit	INT3/TI2/TI4/SO
	P52	1	I/O	Push-pull	Bit	INT2/TI1/TI0/SCK
	P53	1	I/O	Push-pull	Bit	INT1
	P54	1	I/O	Push-pull	Bit	INT0
Port 7	P73	1	I/O	Push-pull/Open-drain	Bit	SDA0
	P74	1	I/O	Push-pull/Open-drain	Bit	SCL0
	P75	1	I/O	Push-pull/Open-drain	Bit	SDA1/AIN0
	P76	1	I/O	Push-pull/Open-drain	Bit	SCL1/AIN1
Port 8	P80	1	I/O	Push-pull	Bit	CTLIN
	P81	1	I/O	Push-pull	Bit	DFGIN
	P82	1	I/O	Push-pull	Bit	RMTIN
	P83	1	I/O	Push-pull	Bit	EXT/TO1
	P84	1	I/O	Push-pull	Bit	DPGIN
	P85	1	I/O	Push-pull	Bit	CFGIN
	P86	1	I/O	Push-pull	Bit	CSYNCIN
	P87	1	I/O	Push-pull	Bit	COMPIN
Port 9	P90	1	I/O	Push-pull/Open-drain	Bit	TP0/TPG00
	P91	1	I/O	Push-pull/Open-drain	Bit	TPG01/VASWP
	P92	1	I/O	Push-pull/Open-drain	Bit	TP1
	P93	1	I/O	Push-pull/Open-drain	Bit	TPG03
	P94	1	I/O	Push-pull/Open-drain	Bit	CR
	P95	1	I/O	Push-pull/Open-drain	Bit	HA
	P96	1	I/O	Push-pull/Open-drain	Bit	TO1/TPG10
	P97	1	I/O	Push-pull/Open-drain	Bit	TPG11
Port A	PA0	1	I/O	Push-pull	Bit	PVPH/PWM3
	PA3	1	I/O	Push-pull/Open-drain	Bit	PWM2
Port B	PB0	1	I/O	Open-drain	Bit	XT1
	PB1	1	I/O	Open-drain	Bit	XT2
Port C	PC0 to PC7	8	Output	High break down voltage	(fixed)	G0 to G7
Port D	PD0, PD1	2	Output	High break down voltage	(fixed)	G8, G9
Port E	PE0 to PE7	8	I/O	High break down voltage /Open-drain	Bit	S0 to S7
Port F	PF0 to PF5	6	I/O	High break down voltage /Open-drain	Bit	S8 to S13

Note 1: Read signals from the port data register are switched according to the function of the port, when the port registers (P5, P6, P7, P8, P9, PA, PB, PE, PF) are read out (Refer to Figure 3.5.2 to Figure 3.5.31).
Output data is written to output latch by writing operation to the port.

Note 2: Due to “Read-Modify & Write” instruction, 1 byte data including specified 1 bit data are read out once and the 1 byte are modified, and then the modified 1 byte are written to output latches.

Note 3: The port status during STOP mode, except PWM0 and PWM1, can be selected from no-change or high impedance. When WDMOD<DRVE> is 1, the port status remains. And when it is 0, the port status becomes high impedance. This function is controlled upon the structure shown below.

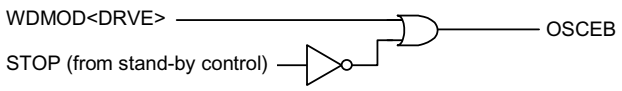


Figure 3.5.1 Port status control circuit for STOP mode

3.5.1 Port 0 (P00 to P07)

Port 0 is an 8-bit general purpose I/O port which can be set to input or output mode to each bit. I/O mode is set by Port 0 control register (P0CR). Reset operation clears Port 0 data register (P0) and P0CR to 0 and initializes port 0 to the input mode.

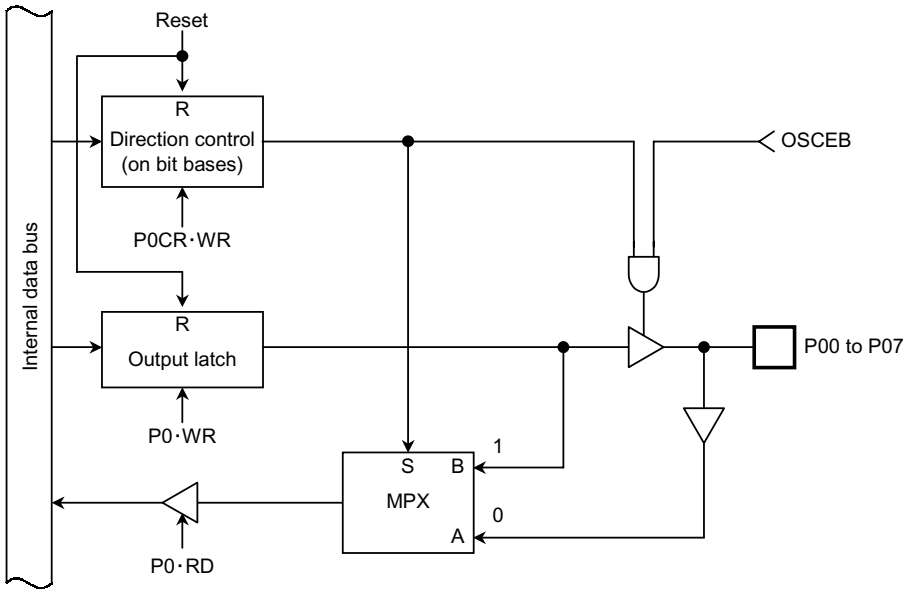


Figure 3.5.2 Port 0 (P00 to P07)

Port 0 Data Register

	7	6	5	4	3	2	1	0	
P0									(Initial Value: 0000 0000)
(0000H)	P07	P06	P05	P04	P03	P02	P01	P00	Read/Write

Port 0 Control Register

	7	6	5	4	3	2	1	0	
P0CR									
(0002H)	P07C	P06C	P05C	P04C	P03C	P02C	P01C	P00C	(Initial Value: 0000 0000)

P07C to P00C	P0 input/output control	0: Input mode 1: Output mode	write only

Prohibit read-modify-write.

Figure 3.5.3 Registers for Port 0

3.5.2 Port 1 (P10 to P17)

Port 1 is an 8-bit general purpose I/O port which can be set to input or output mode to each bit. I/O mode is set by Port 1 control register (P1CR). Reset operation clears Port 1 data register (P1) and control register P1CR to 0 and initializes port 1 to the input mode.

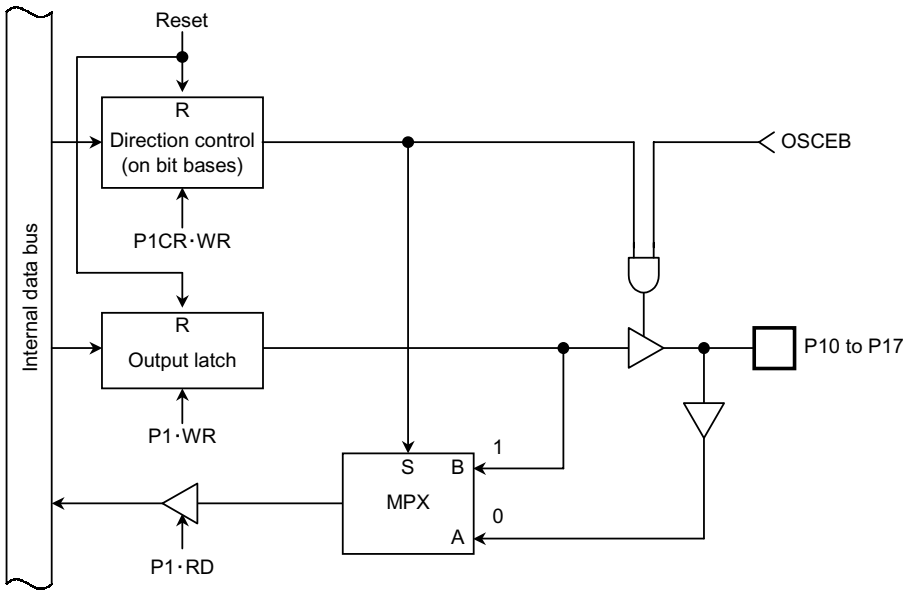


Figure 3.5.4 Port 1 (P10 to P17)

Port 1 Data Register

	7	6	5	4	3	2	1	0	
P1									(Initial Value: 0000 0000)
(0001H)	P17	P16	P15	P14	P13	P12	P11	P10	Read/Write

Port 1 Control Register

	7	6	5	4	3	2	1	0	
P1CR									
(0004H)	P17C	P16C	P15C	P14C	P13C	P12C	P11C	P10C	(Initial Value: 0000 0000)

P17C to P10C	P1 input/output control	0: Input mode 1: Output mode	Write only

Prohibit read-modify-write.

Figure 3.5.5 Registers for Port 1

3.5.3 Port 2 (P20 to P27)

Port 2 is an 8-bit general purpose I/O port which can be set to input or output mode to each bit. I/O mode is set by Port 2 control register (P2CR). Reset operation sets Port 2 data register (P2) to 1 and clears P2CR to 0 and initializes port 2 to the input mode.

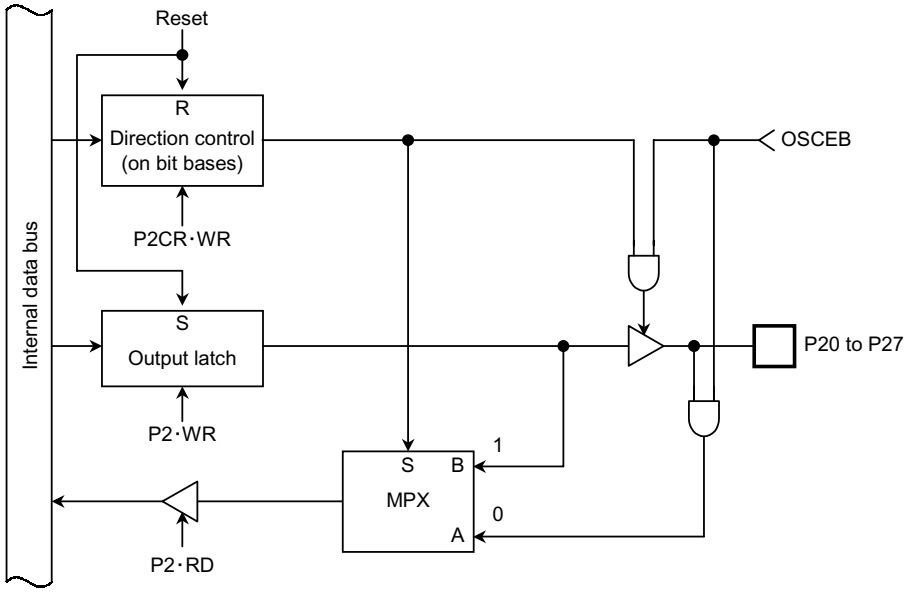


Figure 3.5.6 Port 2 (P20 to P27)

Port 2 Data Register

P2	7	6	5	4	3	2	1	0	(Initial Value: 1111 1111)
(0006H)	P27	P26	P25	P24	P23	P22	P21	P20	Read/Write

Port 2 Control Register

P2CR	7	6	5	4	3	2	1	0	
(0008H)	P27C	P26C	P25C	P24C	P23C	P22C	P21C	P20C	(Initial Value: 0000 0000)

P27C to P20C	P2 input/output control	0: Input mode 1: Output mode	Write only

Prohibit read-modify-write.

Figure 3.5.7 Registers for Port 2

3.5.4 Port 4 (P40 to P47)

Port 4 is an 8-bit general purpose input port. Port 4 is also used for analog input ports (AIN2 to AIN9) of 8-bit AD conversion circuit (AD).

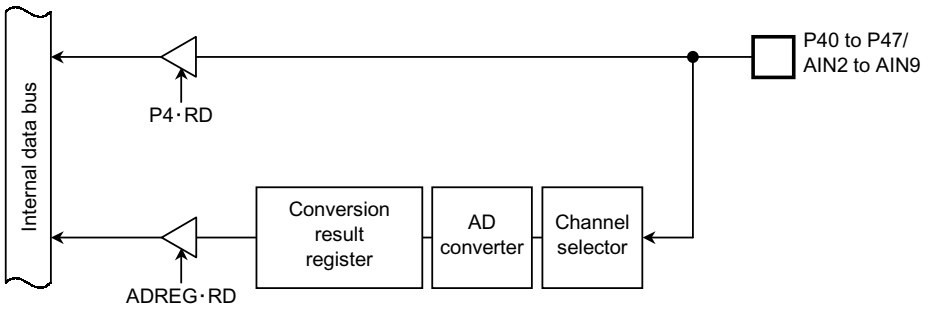


Figure 3.5.8 Port 4

Port 4 Data Register

P4	7	6	5	4	3	2	1	0	(Initial Value: *** ****)
(000AH)	P47	P46	P45	P44	P43	P42	P41	P40	Read only

Figure 3.5.9 Register for Port 4

Note: The input channel selection of AD converter is set by AD converter mode register (ADMOD).

3.5.5 Port 5 (P50 to P54)

Port 5 is a 5-bit general purpose I/O port which can be set to input or output mode to each bit. I/O mode is set by Port 5 control register (P5CR). Reset operation sets Port 5 data register (P5) to 1 and clears control register P5CR to 0 and initializes port 5 to the input mode.

(1) P50/INT4/TI3/TI5/SI

P50 is also used as external interrupt input (INT4), timer counter input (TI3, TI5), or serial data input (SI).

When P50 is used as INT4, TI3, TI5 or SI, clear P5CR<P50C> to 0 and it is set to input mode.

INT4 interrupt input is permitted by <I4IE> of external interrupt control register 0 (IIMC0), and can choose input edge by <I4EG> of external interrupt control register 1 (IIMC1).

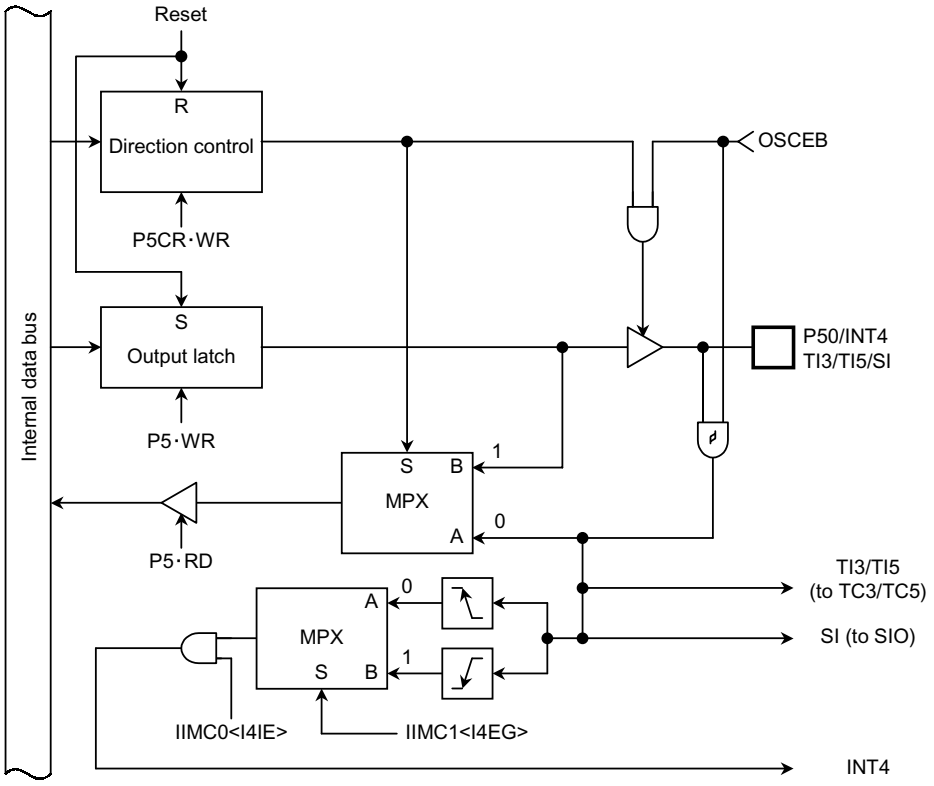


Figure 3.5.10 Port 5 (P50)

(2) P51/INT3/TI2/TI4/SO

P51 is also used as external interrupt input (INT3), timer counter input (TI2, TI4) or serial data output (SO).

When P51 is used as INT3, TI2 or TI4, clear P5CR<P51C> to 0 and it is set to input mode.

INT3 interrupt input is permitted by <I3IE> of IIMC0, and can choose input edge by <I3EG> of IIMC1.

When P51 is used as SO, set P5CR<P51F> and <P51C> to 1 respectively.

(3) P52/INT2/TI1/TI0/SCK

P52 is also used as external interrupt input (INT2), timer counter input (TI1, TI0) or serial clock (SCK).

When P52 is used as INT2, TI1, TI0 or SCK input, clear P5CR<P52C> to 0 and it is set to input mode.

INT2 interrupt input is permitted by <I2IE> of IIMC0, and can choose input edge by <I2EG> of IIMC1.

When P52 is used as SCK output, set P5CR<P52F> and <P52C> to 1 respectively.

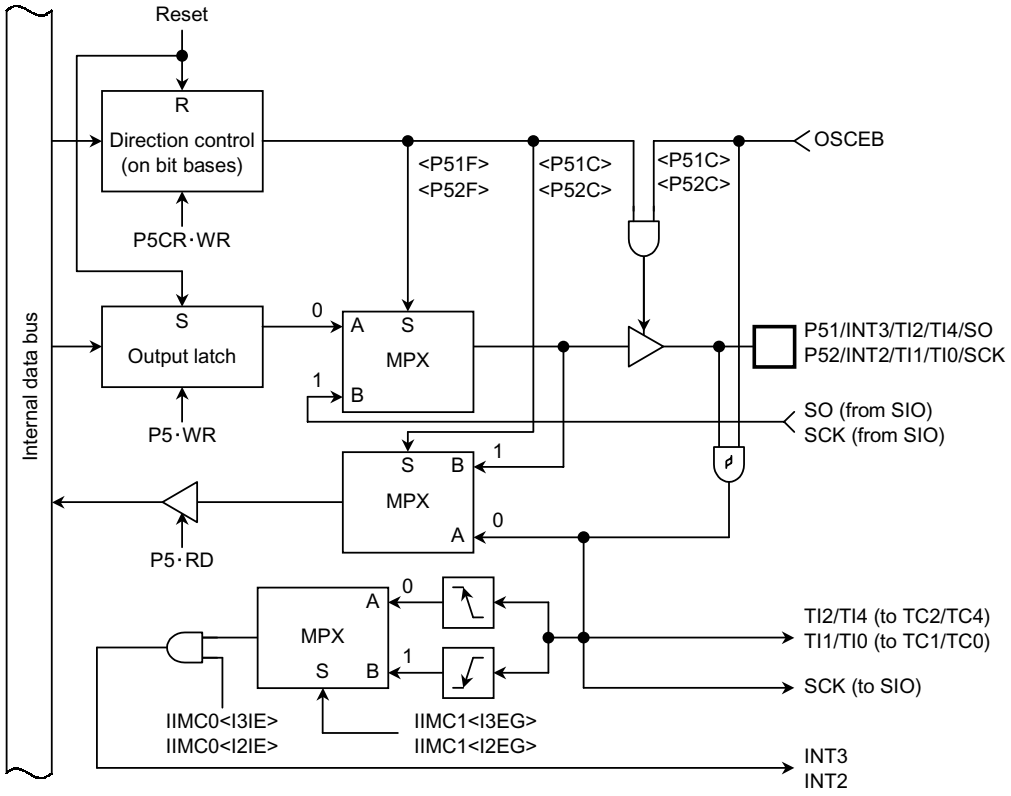


Figure 3.5.11 Port 5 (P51, P52)

(4) P53/INT1

P53 is also used as external interrupt input (INT1).

When P53 is used as INT1, clear P5CR<P53C> to 0 and it is set to input mode.

INT1 interrupt input is permitted by <I1IE> of IIMC0, and can choose input edge by <I1EG> of IIMC1.

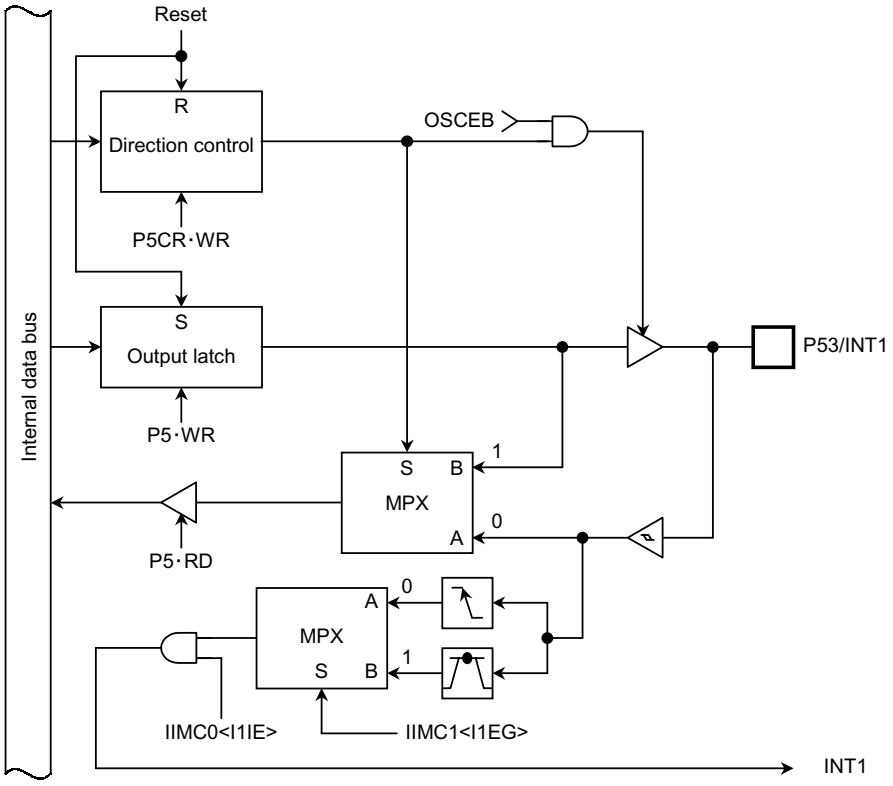


Figure 3.5.12 Port 5 (P53)

(5) P54/INT0

P54 is also used as external interrupt input (INT0).

When P54 is used as INT0, clear P5CR<P54C> to 0 and it is set to input mode.

INT0 interrupt input is permitted by <I0IE> of IIMC0, and can choose input edge by <I0EG> of IIMC1.

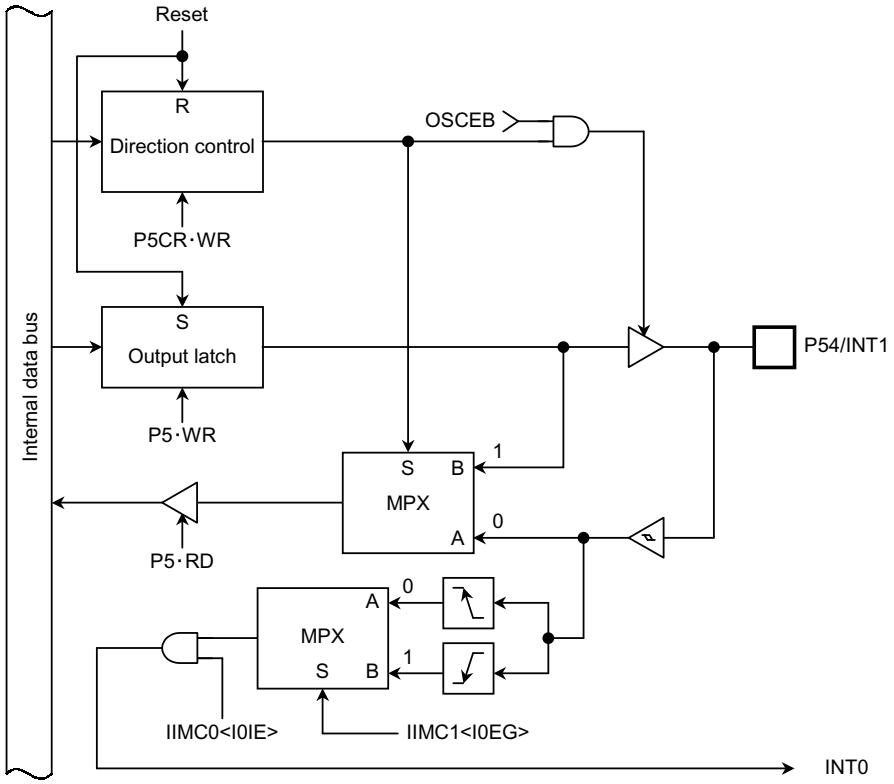


Figure 3.5.13 Port 5 (P54)

Port 5 Data Register

	7	6	5	4	3	2	1	0	
P5				P54	P53	P52	P51	P50	(Initial Value: ***1 1111)
(000BH)									Read/Write

Port 5 Control Register

	7	6	5	4	3	2	1	0	
P5CR	P52F	P51F		P54C	P53C	P52C	P51C	P50C	(Initial Value: 00*0 0000)
(000CH)									

P52F	P52 output selection	0: P52 1: SCK	write only
P51F	P51 output selection	0: P51 1: SO	
P54C to P50C	P5 input/output control	0: Input mode 1: Output mode	

Access by Read-Modify and Write instruction is prohibited.

External Interrupt Control Register 0

	7	6	5	4	3	2	1	0	
IIMC0				I4IE	I3IE	I2IE	I1IE	I0IE	
(005EH)				(INT4)	(INT3)	(INT2)	(INT1)	(INT0)	(Initial Value: ***0 0000)

I4IE to I0IE	External interrupt input Enable/Disable	0: Disable 1: Enable	write only

Access by Read-Modify and Write instruction is prohibited.

External Interrupt Control Register 1

	7	6	5	4	3	2	1	0	
IIMC1	I4EG	I3EG	I2EG	I1EG	I0EG		INTTPG0E	INTTPG0S	(Initial Value: 000 0*00)
(005FH)									

I4EG	INT4 edge selection	0: Rising edge 1: Falling edge	write only
I3EG	INT3 edge selection	0: Rising edge 1: Falling edge	
I2EG	INT2 edge selection	0: Rising edge 1: Falling edge	
I1EG	INT1 edge/level selection	0: Rising edge 1: Level	
I0EG	INT0 edge selection	0: Rising edge 1: Falling edge	

Access by Read-Modify and Write instruction is prohibited.

Figure 3.5.14 Registers for Port 5

Note 1: Do not write the data to <P51F> and <P51C> of Port 5 control register at the same time, <P52F> and <P52C> as well.

Note 2: INT0 and INT1 pin are applicable also to standby release.
<I0IE> and <I1IE> are set to “0” when not using it an object for standby release, a port function can be maintained also during standby.

Note 3: When change effective edge by IIMC1 register, change after carrying out interrupt prohibition.

```
LD   (INT0TP1),     - - - - 0000B   ; Disabled INT0、Clear the request flag.
LD   (IIMC0),       - - - - - - - 0B   ; INT0 input disable.
LD   (IIMC1),       - - - - 1 - - - B   ; Change from a rising edge to level detection.
LD   (INT0CP1),     - - - - 0nnnB   ; INT0 is set to a level n and a request flag is cleared.
```

Note 4: “H” level and “L” level of the external interrupt minimum input pulse width are $2/f_{SYS}$[s] (250 ns at 16 MHz operation).

3.5.6 Port 7 (P73 to P76)

Port 7 is a 4-bit general purpose I/O port which can be set to input or output mode to each bit. I/O mode is set by Port 7 control register (P7CR). Reset operation sets Port 7 data register (P7) to 1 and clears P7CR to 0 and initializes port 7 to the input mode. In the case of the output mode, Port 7 can be set to either push-pull output or N-ch open-drain output per bit by open-drain output control register 1 (ODCR1).

(1) P73/SDA0, P74/SCL0

P73 and P74 are also used as serial data (SDA0) or serial clock (SCL0) of serial bus interface (I^2C bus).

When outputting SDA0 or SCL0, set Port 7 function register (P7FC)<P73F><P74F>, ODCR1<POD73><POD74> and P7CR<P73C><P74C> to 1 respectively. When inputting, clear P7CR<P73C><P74C> to 0.

Input source of P73 and P74 can be chosen by <PR73><PR74> of Port 7 input control register (P7ICR).

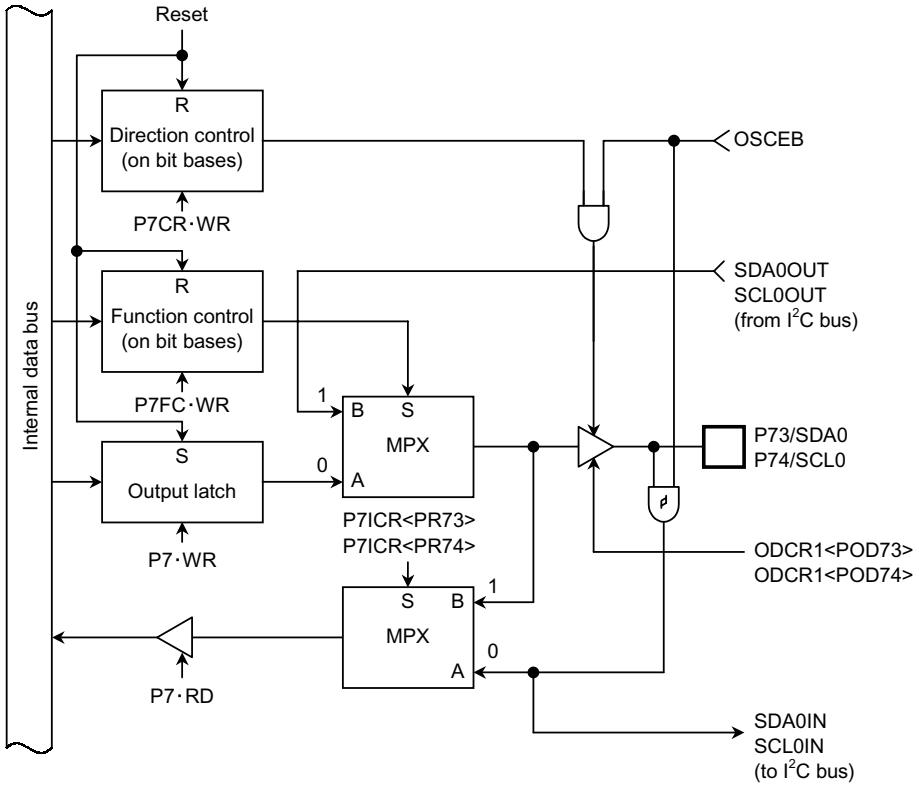


Figure 3.5.15 Port 7 (P73, P74)

(2) P75/SDA1/AIN0, P76/SCL1/AIN1

P75 and P76 are also used as serial data/address (SDA1), serial clock (SCL1) of I^2C bus or analog input ports (AIN0, AIN1) of 8-bit AD conversion circuit (AD).

When outputting SDA1 or SCL1, set P7FC<P75F><P76F>, ODCR1<POD75><POD76> and P7CR<P75C><P76C> to 1 respectively. When inputting SDA1, SCL1, AIN0, or AIN1, clear F7CR<P75C><P76C> to 0 respectively.

Input source of P75 and P76 can be chosen by <PR75><PR76> of P7ICR.

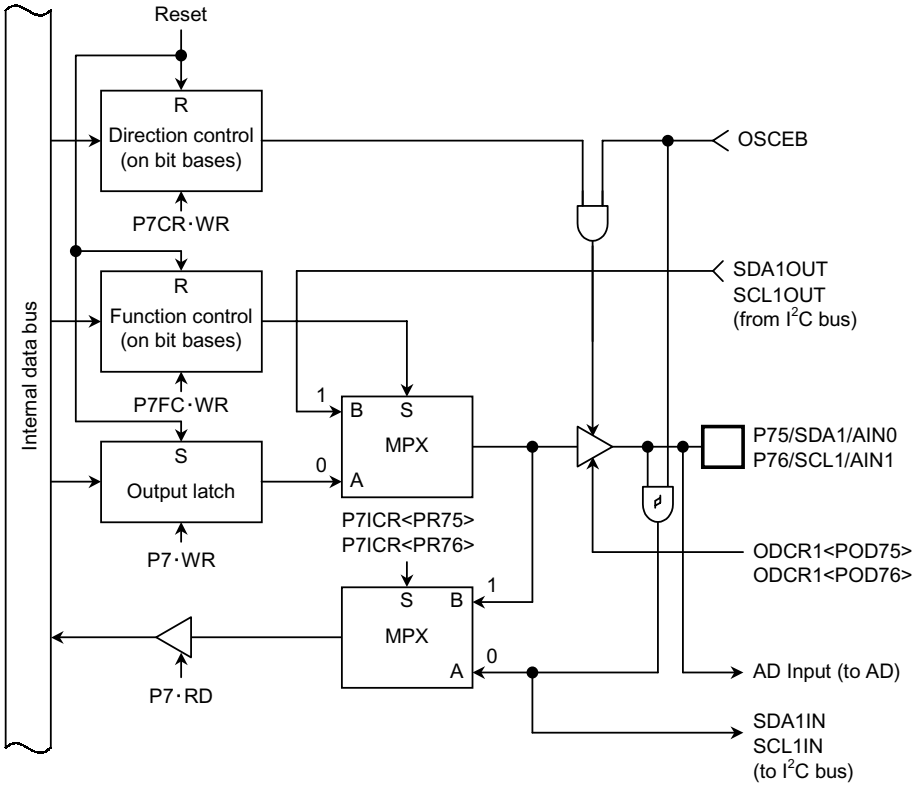


Figure 3.5.16 Port 7 (P75,P76)

Port 7 Data Register

	7	6	5	4	3	2	1	0	
P7									(Initial Value: *111 1***)
(000FH)		P76	P75	P74	P73				Read/Write

Port 7 Control Register

	7	6	5	4	3	2	1	0	
P7CR									
(0011H)		P76C	P75C	P74C	P73C				(Initial Value: *000 0***)

P76C to P73C	P7 input/output control	0: Input mode 1: Output mode	write only

Access by Read-Modify and Write instruction is prohibited.

Port 7 Function Register

	7	6	5	4	3	2	1	0	
P7FC									
(0013H)		P76F	P75F	P74F	P73F				(Initial Value: *000 0***)

P76F	P76 output selection	0: P76 1: SCL1	write only
P75F	P75 output selection	0: P75 1: SDA1	
P74F	P74 output selection	0: P74 1: SCL0	
P73F	P73 output selection	0: P73 1: SDA0	

Access by Read-Modify and Write instruction is prohibited.

Open-drain Output Control Register 1

	7	6	5	4	3	2	1	0	
ODCR1									
(0015H)		POD76	POD75	POD74	POD73				(Initial Value: *000 0***)

POD76 to POD73	P7 open-drain control	0: Push-pull Output 1: Open-drain Output	write only

Access by Read-Modify and Write instruction is prohibited.

Port 7 Input Control Register

	7	6	5	4	3	2	1	0	
P7ICR									
(000DH)		PR76	PR75	PR74	PR73				(Initial Value: *000 0***)

PR76 to PR73	P7 input selection	0: Pin 1: Output latch	write only

Access by Read-Modify and Write instruction is prohibited.

Figure 3.5.17 Registers for Port 7

3.5.7 Port 8 (P80 to P87)

Port 8 is an 8-bit general purpose I/O port which can be set to input or output mode to each bit. I/O mode is set by Port 8 control register (P8CR). Reset operation sets Port 8 data register P8 to 1 and clears P8CR to 0 and initializes port 8 to the input mode.

(1) P80/CTLIN, P81/DFGIN, P82/RMTIN, P84/DPGIN, P85/CFGIN, P86/CSYNCIN, P87/COMPIN

P80, P81, P84 and P85 are also used as capture trigger inputs (CTLIN, DFGIN, DPGIN, CFGIN).

P82, P86 and P87 are also used as remote-control signal input (RMTIN), composite synchronizing signal input (CSYNCIN) and head-amp.-switch comparison signal input (COMPIN) respectively.

When it is used as these functional inputs, clear P8CR<P80C, P81C, P82C, P84C, P85C, P86, P87C> to 0 respectively, and it is set to the input mode.

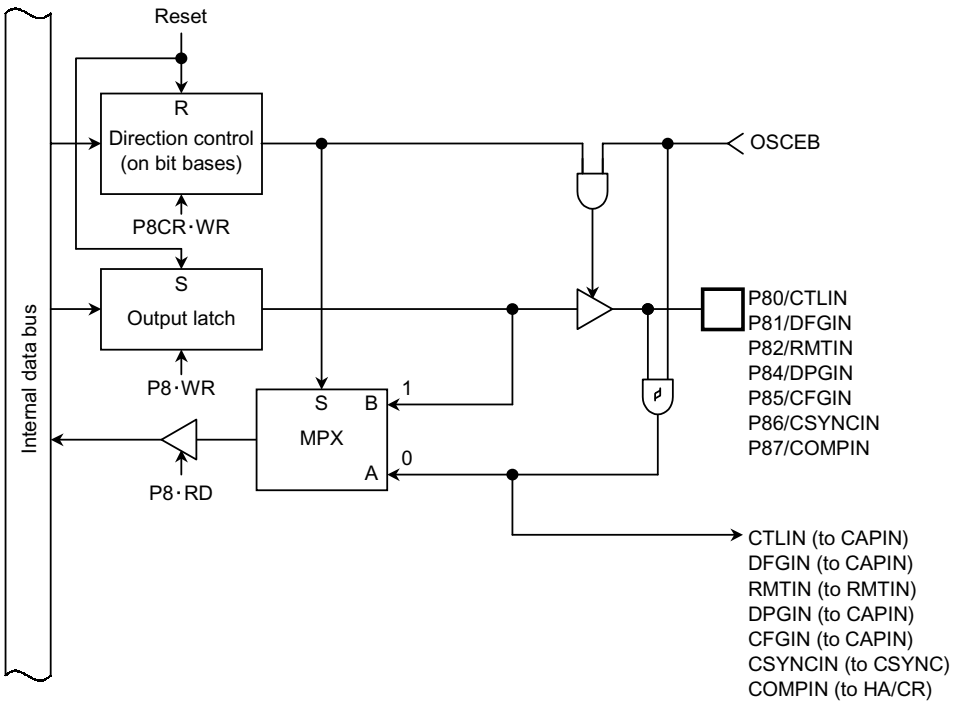


Figure 3.5.18 Port 8 (P80 to P87)

(2) P83/EXT/TO1

P83 is also used as capture trigger input (EXT) or timer counter output 1 (TO1).

When P83 is used as capture trigger input, clear P8CR<P83C> to 0 and it is set to the input mode.

When it is used as timer counter 1 output, set Port 8 function register (P8FC)<P83F> and P8CR<P83C> to 1 respectively.

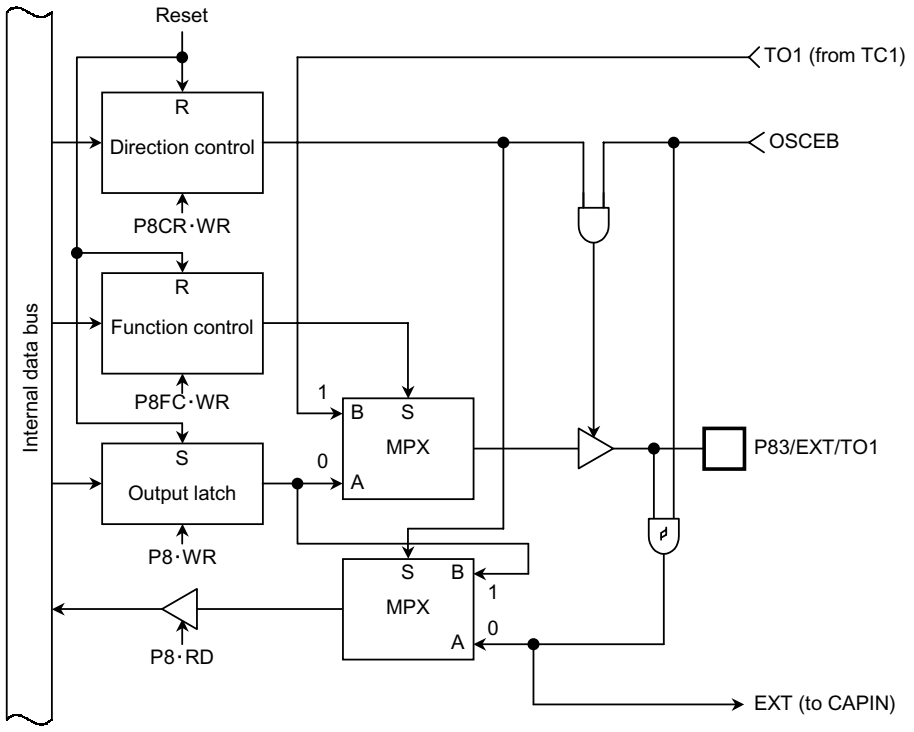


Figure 3.5.19 Port 8 (P83)

Port 8 Data Register

P8	7	6	5	4	3	2	1	0	(Initial Value: 1111 1111)
(0016H)	P87	P86	P85	P84	P83	P82	P81	P80	Read/Write

Port 8 Control Register

P8CR	7	6	5	4	3	2	1	0	
(0018H)	P87C	P86C	P85C	P84C	P83C	P82C	P81C	P80C	(Initial Value: 0000 0000)

P87C to P80C	P8 input/output control	0: Input mode 1: Output mode	write only

Access by Read-Modify and Write instruction is prohibited.

Port 8 Function Register

P8FC	7	6	5	4	3	2	1	0	
(0014H)					P83F				(Initial Value: **** 0***)

P83F	P83 output selection	0: P83 1: TO1	write only

Access by Read-Modify and Write instruction is prohibited.

Figure 3.5.20 Registers for Port 8

3.5.8 Port 9 (P90 to P97)

Port 9 is an 8-bit general purpose I/O port which can be set to input or output mode to each bit. I/O mode is set by Port 9 control register (P9CR). Reset operation sets Port 9 data register (P9) to 1 and clears P9CR to 0 and initializes port 9 to the input mode. In the case of the output mode, Port 9 can set to either push-pull output or N channel open-drain output per bit by open-drain output control register 2 (ODCR2).

(1) P90/TP0/TPG00

P90 is also used as timing pulse output 0 (TP0) or the timing pulse generator 0 (TPG00).

When P90 is used as TP0 output, set Port 9 function register (P9FC)<P90F> and P9CR<P90C> to 1 respectively. (Refer to chapter 3.8.3 Timing Pulse Output)

When it is used as TPG00 output, set P9<P90> and P9CR<P90C> to 1 respectively. TPG00 output is permitted by setting timing pulse control register (TPCR) <TPGOE0> to 1.

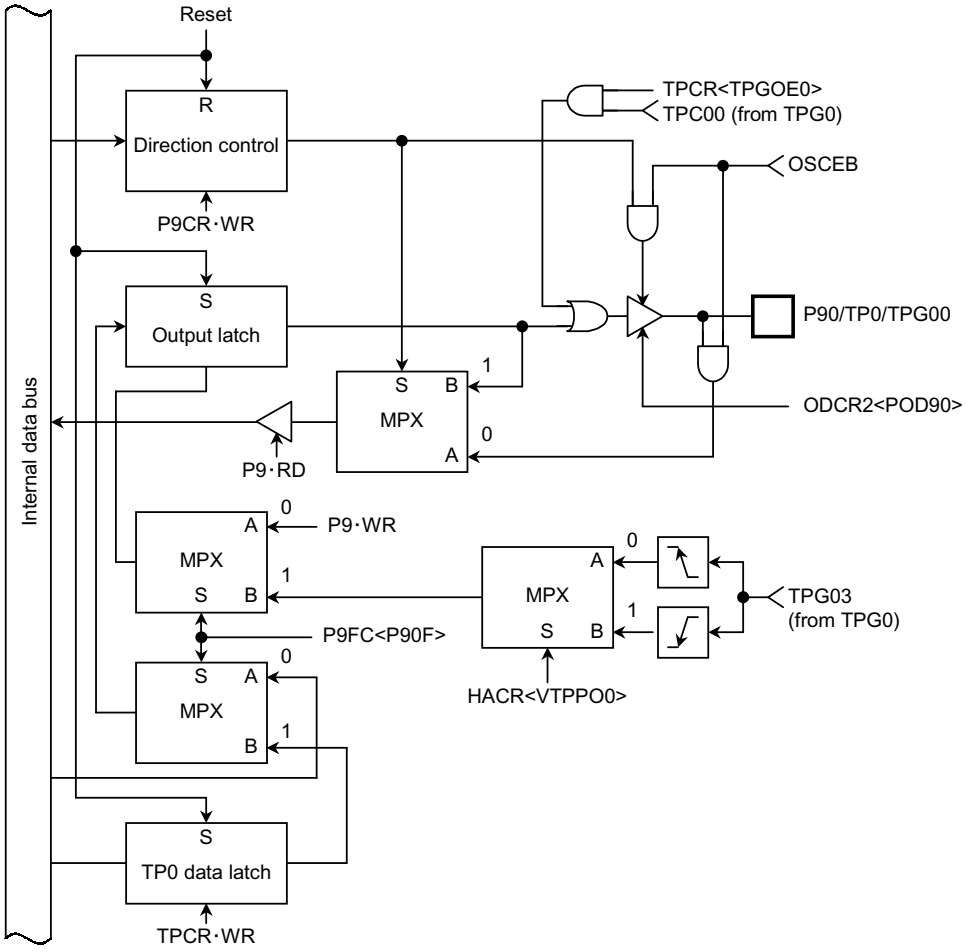


Figure 3.5.21 Port 9 (P90)

(2) P91/TPG01/VASWP

P91 is also used as timing pulse generator 0 (TPG0) output (TPG01) or Video/Audio Head switching control signal (VASWP).

When P91 is used as TPG01 output, clear Head Amp control register (HACR)<TPVASEL> to 0 and also set P9FC<P91F> and P9CR<P91C> to 1 respectively.

When it is used as VASWP output, set HACR<TPVASEL> to 1, set P9FC<P91F> to 1, and clear P9CR<P91C> to 0 respectively. (Refer to chapter 3.14.3 Control of VASMP Output)

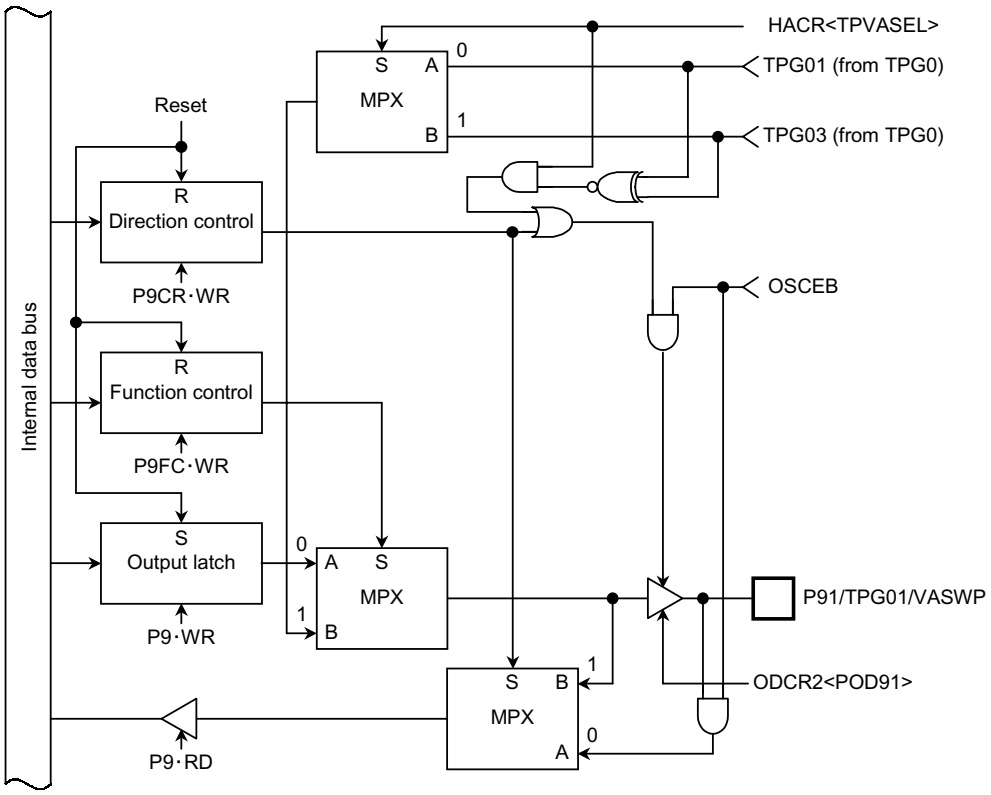


Figure 3.5.22 Port 9 (P91)

(3) P92/TP1

P92 is also used as timing pulse output (TP1). When P92 is used as TP1 output, set P9FC<P92F> and P9CR<P92C> to 1 respectively.

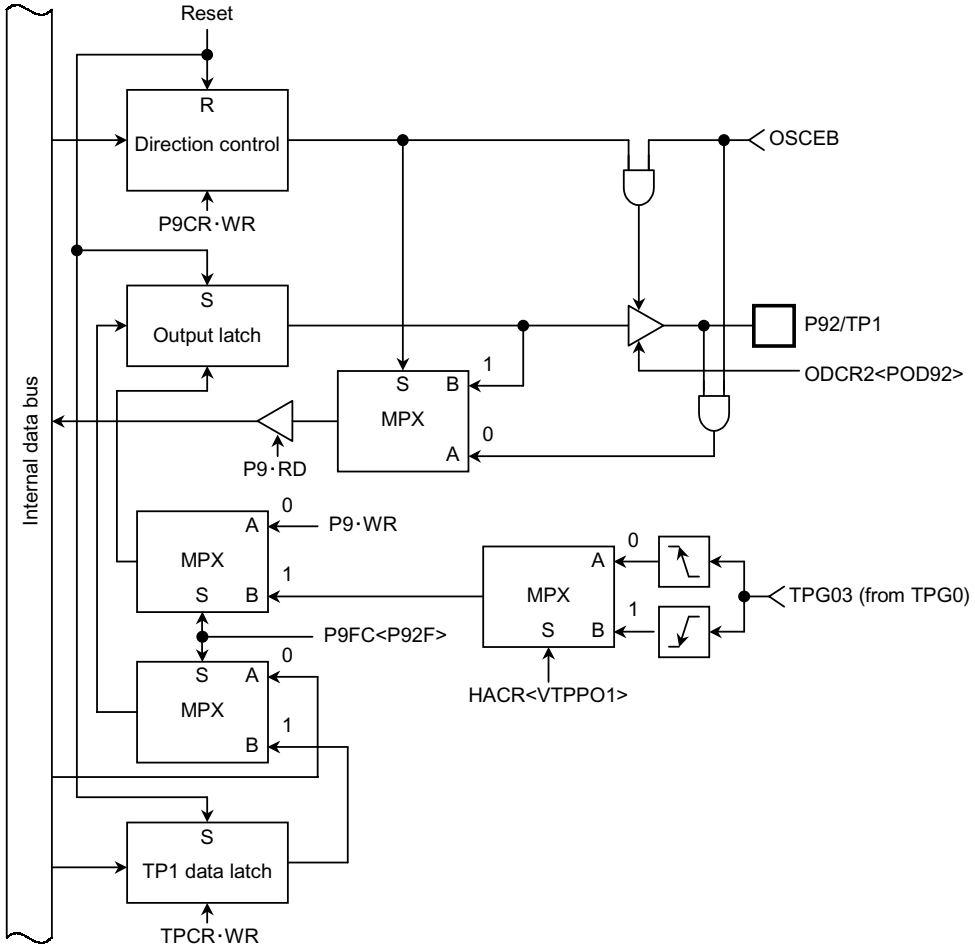


Figure 3.5.23 Port 9 (P92)

(4) P93/TPG03, P94/CR, P95/HA

P93, P94 and P95 are also used as timing pulse generator 0 (TPG0) output (TPG03), Color Rotary control output (CR), Head Amp switching control output (HA), respectively. When they are used as these function outputs, set P9FC<P93F, P94F, P95F> and P9CR<P93C, P94C, P95C> to 1 respectively.

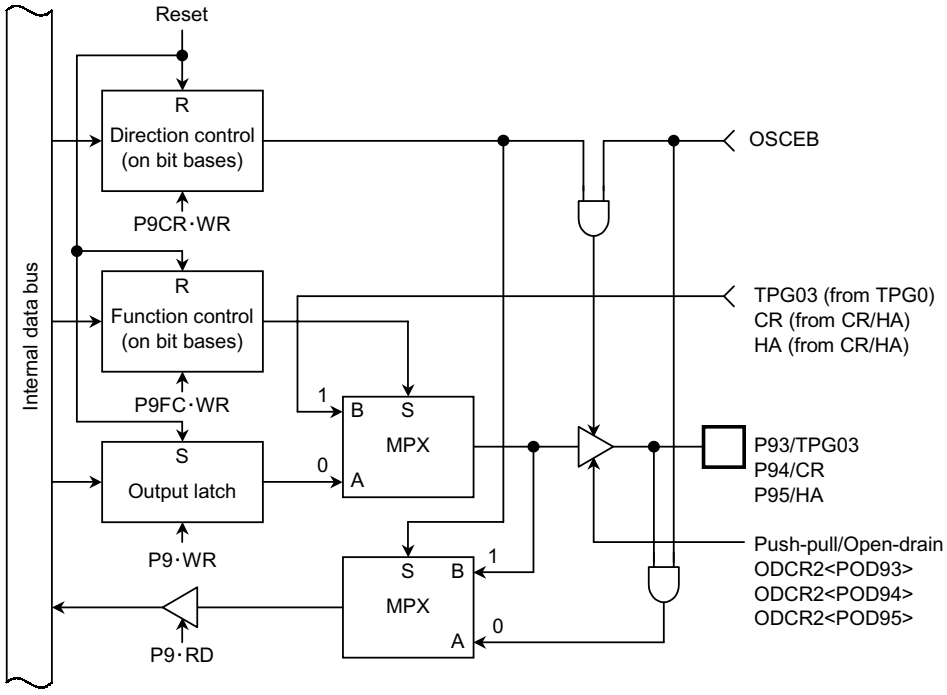


Figure 3.5.24 Port 9 (P93 to P95)

(5) P96/TO1/TPG10

P96 is also used as timer counter output 1 (TO1) and timing pulse generator 1 (TPG1) output (TPG10). When P96 is used as TO1 output, set P9FC<P96F> and P9CR<P96C> to 1 respectively, and clear TPCR<TPGOE1> to 0.

When P96 is used as TPG10 output, clear P9<P96> and P9FC<P96F> to 0, set P9CR<P96C> to 1 respectively, and set TPCR<TPGOE1> to 1.

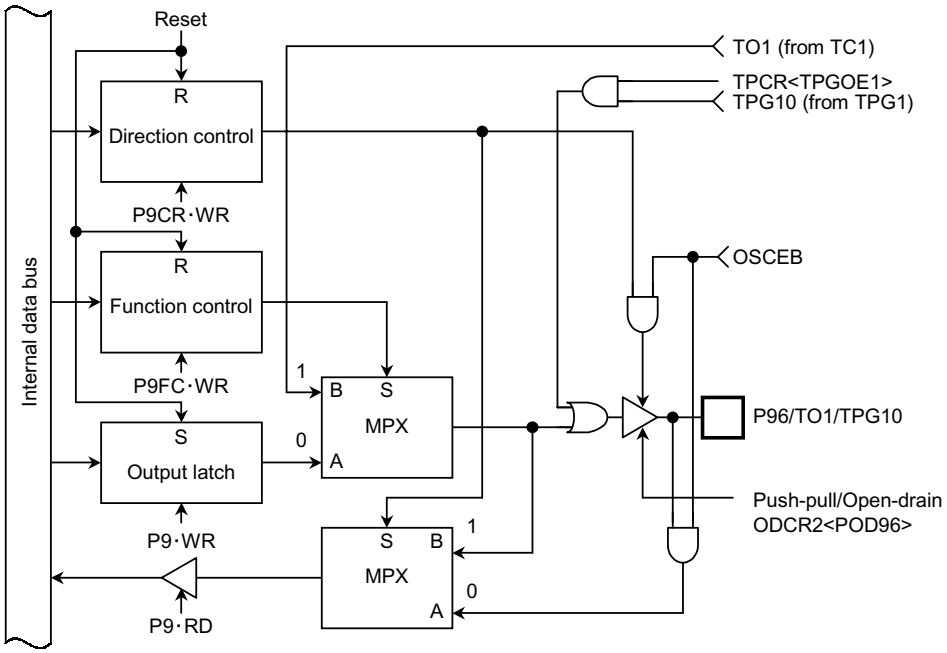


Figure 3.5.25 Port 9 (P96)

(6) P97/TPG11

P97 is also used as timing pulse generator 1 (TPG1) output (TPG11).

When P97 is used as TPG11 output, set P9FC<P97F> and P9CR<P97C> to 1 respectively.

P97 can be used as a logical-output syncronized with TPG10 as a below shown logical matrix.

This is enabled by setting TPCR<TPG1CNT> to 1.

TPG10	P97 output
H	TPG11
L	High-Z

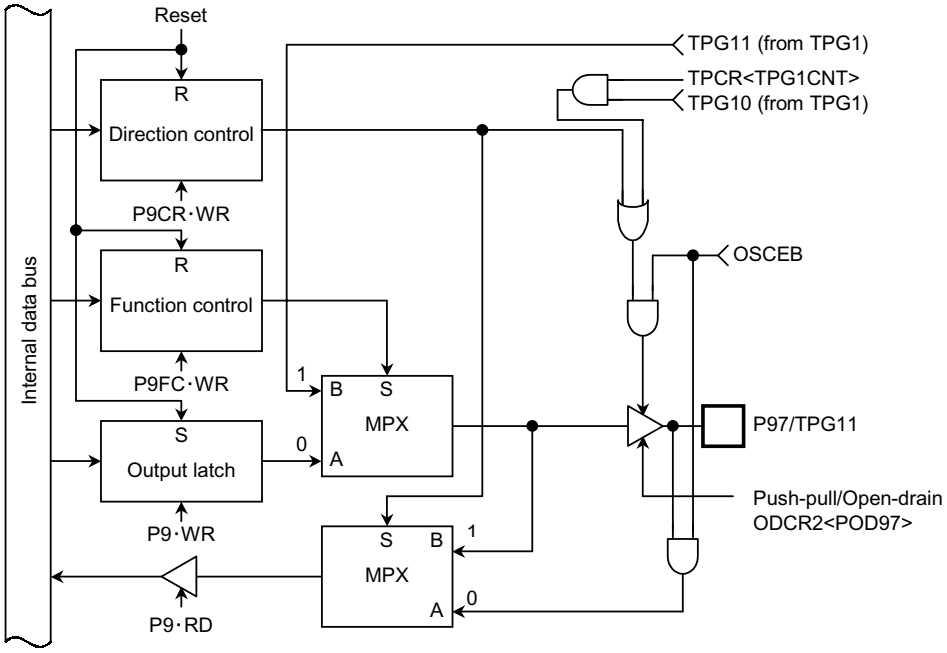


Figure 3.5.26 Port 9 (P97)

Port 9 Data Register

P9	7	6	5	4	3	2	1	0	(Initial Value: 1111 1111)
(0017H)	P97	P96	P95	P94	P93	P92	P91	P90	Read/Write

Port 9 Control Register

P9CR	7	6	5	4	3	2	1	0	
(0019H)	P97C	P96C	P95C	P94C	P93C	P92C	P91C	P90C	(Initial Value: 0000 0000)

P97C to P90C	P9 input/output control	0: Input mode 1: Output mode	write only

Access by Read-Modify and Write instruction is prohibited.

Port 9 Function Register

P9FC	7	6	5	4	3	2	1	0	
(001AH)	P97F	P96F	P95F	P94F	P93F	P92F	P91F	P90F	(Initial Value: 0000 0000)

P97F	P97 output selection	0: P97 1: TPG11	write only
P96F	P96 output selection	0: P96/TPG10 (P96 = 0) 1: TO1	
P95F	P95 output selection	0: P95 1: HA	
P94F	P94 output selection	0: P94 1: CR	
P93F	P93 output selection	0: P93 1: TPG03	
P92F	P92 output selection	0: P92 1: TP1	
P91F	P91 output selection	0: P91 1: TPG01/VASWP	
P90F	P90 output selection	0: P90 1: TP0/TPG00	

Access by Read-Modify and Write instruction is prohibited.

Open-drain Output control Register 2

ODCR2	7	6	5	4	3	2	1	0	
(001BH)	POD97	POD96	POD95	POD94	POD93	POD92	POD91	POD90	(Initial Value: 0000 0000)

POD97 to POD90	P9 open-drain control	0: Push-pull Output 1: Open-drain Output	write only

Access by Read-Modify and Write instruction is prohibited.

Head Amp Control Register

HACR	7	6	5	4	3	2	1	0	
(008DH)	VTPPO1	VTPPO0	TPVASEL	DFFPO1	DFFPO0	COMPS	CRPO	HAPO	(Initial Value: 0000 0000)

TPE1	TPG03(P92) edge selection	0: Rising edge 1: Falling edge	R/W
TPE0	TPG03(P90) edge selection	0: Rising edge 1: Falling edge	
TPVASEL	P91 output selection	0: TPG01 1: VASWP	

Access by Read-Modify and Write instruction is prohibited.

Timing Pulse Control Register

TPCR (0086H)

7	6	5	4	3	2	1	0
TPGOE1	TPGOE0		TPG1CNT		TP1D		TP0D

(Initial Value: 00*0 *0*0)

TPGOE1	TPG10 output control	0: Disable 1: Enable	R/W
TPGOE0	TPG00 output control	0: Disable 1: Enable	
TPG1CNT	P97/TPG11 output control	0: Disable 1: TPG10 Enable	
TP1D	TP1 data latch	TP1 data	
TP0D	TP0 data latch	TP0 data	

Figure 3.5.27 Registers for Port 9

3.5.9 Port A (PA0, PA3)

Port A is a 2-bit general purpose I/O port which can be set to input or output mode to each bit. I/O mode is set by Port A control register (PACR). Reset operation sets Port A data register (PA) to 1 and PACR to 0 and initializes port A to the input mode.

(1) PA0/PVPH/PWM3

PA0 is also used as pseudo-synchronized signal output (PVPH) or 8-bit PWM output (PWM3).

When PA0 is used as general purpose I/O port, set <PA0F1> and <PA0F0> of port A function register (PAFC) to 0 and set the I/O mode by PACR<PA0C>.

When PA0 is used as PVPH output, set PAFC<PA0F0> to 1, clear PACR<PA0C> to 0 respectively.

When PA0 is used as PWM3 output, set PAFC<PA0F1><PA0F0> to 10, and set PACR<PA0C> to 1 respectively.

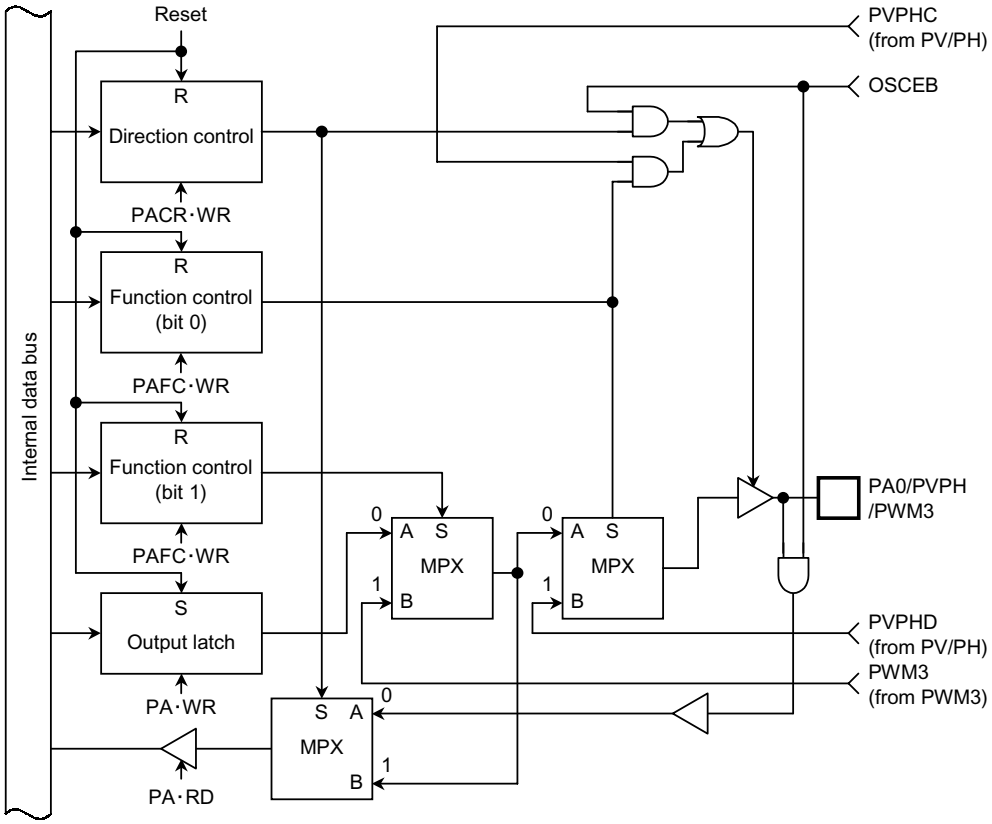


Figure 3.5.28 Port A (PA0)

(2) PA3/PWM2

PA3 is also used as 14-bit PWM output (PWM2). In the case of output mode, PA3 can be set to either push-pull output or N-ch open-drain output by open-drain output control register 3 (ODCR3)<PODA3>.

When PA3 is used as PWM2, set PAFC<PA3F> and PACR<PA3C> to 1 respectively.

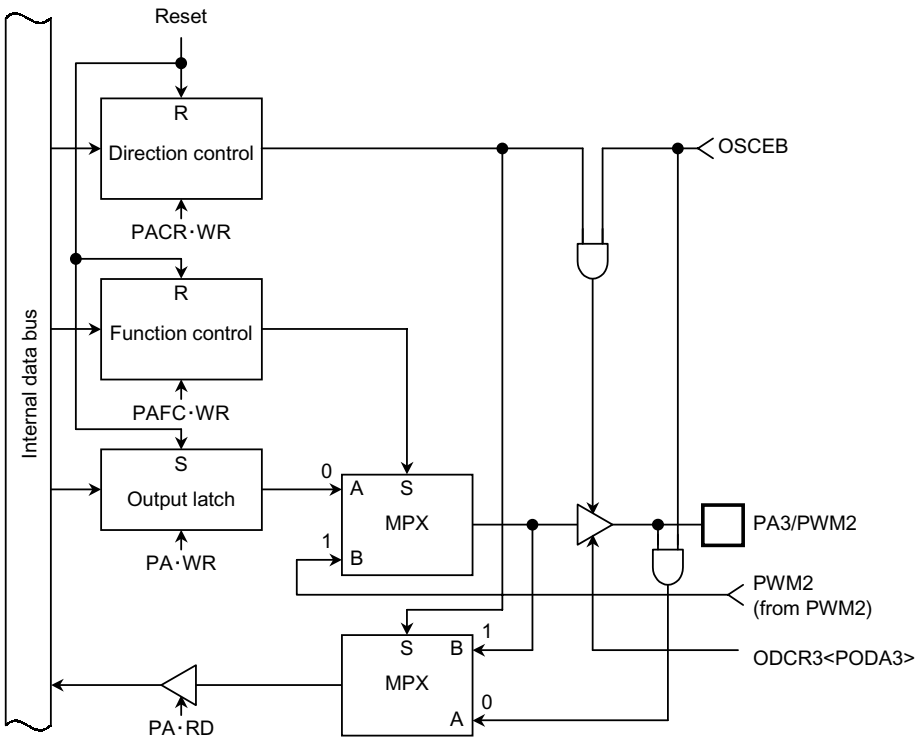


Figure 3.5.29 Port A (PA3)

Port A Data Register

	7	6	5	4	3	2	1	0	
PA					PA3			PA0	(Initial Value: **** 1**1)
(001CH)									Read/Write

Port A Control Register

	7	6	5	4	3	2	1	0	
PACR					PA3C			PA0C	(Initial Value: **** 0**0)
(001EH)									

PA3C, PA0C	PA input/output control	0: Input mode 1: Output mode	Write only

Access by Read-Modify and Write instruction is prohibited.

Port A Function Register

	7	6	5	4	3	2	1	0	
PAFC					PA3F		PA0F1	PA0F0	(Initial Value: **** 0*00)
(006BH)									

PA3F	PA3 output selection	0: PA3 1: PWM2	Write only
PA0F1	PA0 output selection	00: PA0 *1: PVPH 10: PWM3 11: Reserved	
PA0F0			

Access by Read-Modify and Write instruction is prohibited.

Open-drain Output Control Register 3

	7	6	5	4	3	2	1	0	
ODCR3				PWMOD1	PWMOD0			PODA3	(Initial Value: ***0 0**0)
(0021H)				(PWM1)	(PWM0)			(PA3)	

PODA3	PA3 open-drain control	0: Push-pull Output 1: Open-drain Output	Write only

Access by Read-Modify and Write instruction is prohibited.

Figure 3.5.30 Registers for Port A

3.5.10 Port B (PB0, PB1)

Port B is a 2-bit general purpose I/O port which can be set to input or output mode to each bit.

I/O mode is set by Port B control register (PBCR). Reset operation sets port B data register (PB) to 1 and PBCR to 0 and initializes port B to the input mode. Output buffer is constructed of N-channel open-drain.

(1) PB0/XT1,PB1/XT2

PB0 and PB1 are also used as a low-frequency oscillation circuit (XT1, XT2). A resonator is connected to XT1 and XT2. The low-frequency oscillation circuit goes active by setting system clock control register 0 (SYSCR0)<XTEN> to 1.

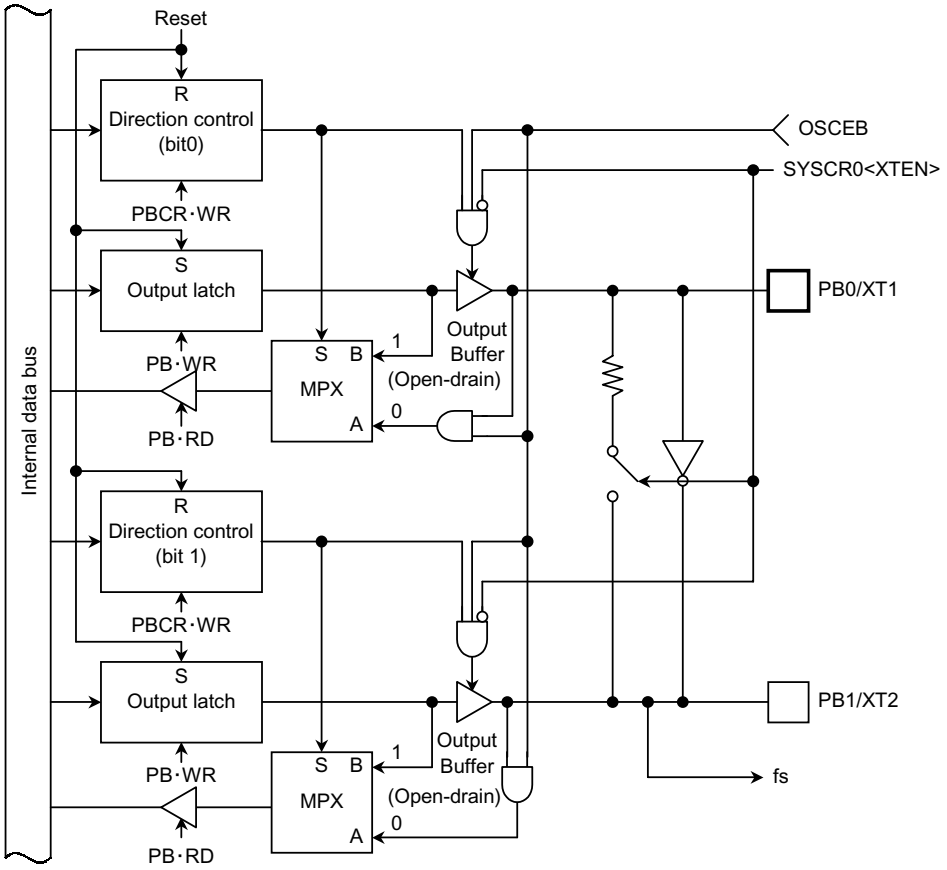


Figure 3.5.31 Port B (PB0, PB1)

Port B Data Register

	7	6	5	4	3	2	1	0	
PB									(Initial Value: **** **11)
(001DH)							PB1	PB0	Read/Write

Port B Control Register

	7	6	5	4	3	2	1	0	
PBCR									
(001FH)							PB1C	PB0C	(Initial Value: **** **00)

PB1C, PB0C	PB input/output control	0: Input mode 1: Output mode	Write only

Prohibit read-modify-write.

Figure 3.5.32 Registers for Port B

3.5.11 Port C (PC0/G0 to PC7/G7), Port D (PD0/G8 to PD1/G9)

Port C and port D are 8-bit and 2-bit P-channel high break-down voltage output port. PC and PD are also used grid-outputs and can drive vacuum fluorescent tube directly.

Reset operation clears port C data register (PC) and port D data register (PD) to 0 respectively.

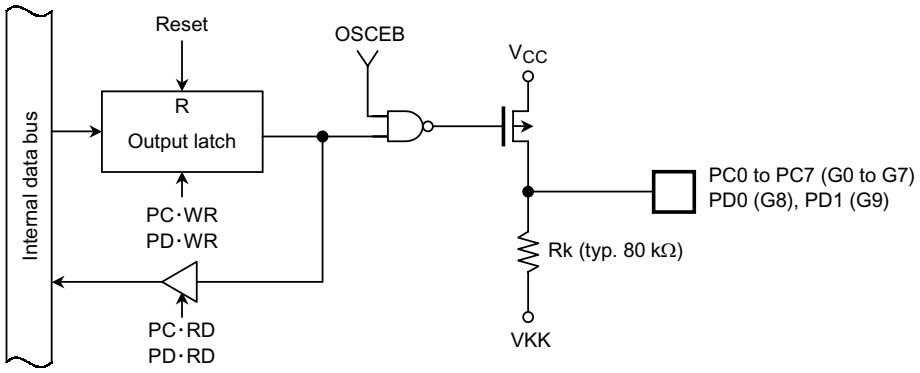


Figure 3.5.33 Port C (PC0 to PC7), Port D (PD0, PD1)

Port C Data Register

PC	7	6	5	4	3	2	1	0	(Initial Value: 0000 0000)
(0087H)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	Read/Write

Port D Data Register

PD	7	6	5	4	3	2	1	0	(Initial Value: **** **00)
(0088H)							PD1	PD0	Read/Write

Figure 3.5.34 Registers for Port C, Port D

3.5.12 Port E (PE0/S0 to PE7/S7), Port F (PF0/S8 to PF5/S13)

Port E and port F are 8-bit and 6-bit P-channel high break-down voltage output port. PE and PF are also used segment-outputs and can drive vacuum fluorescent tube directly. I/O mode is set by port E control register (PECR) and port F control register (PFCR).

Reset operation sets port E data register (PE), port F data register (PF), PECR, and PFCR to 0 respectively and initializes port E and port F to the input mode.

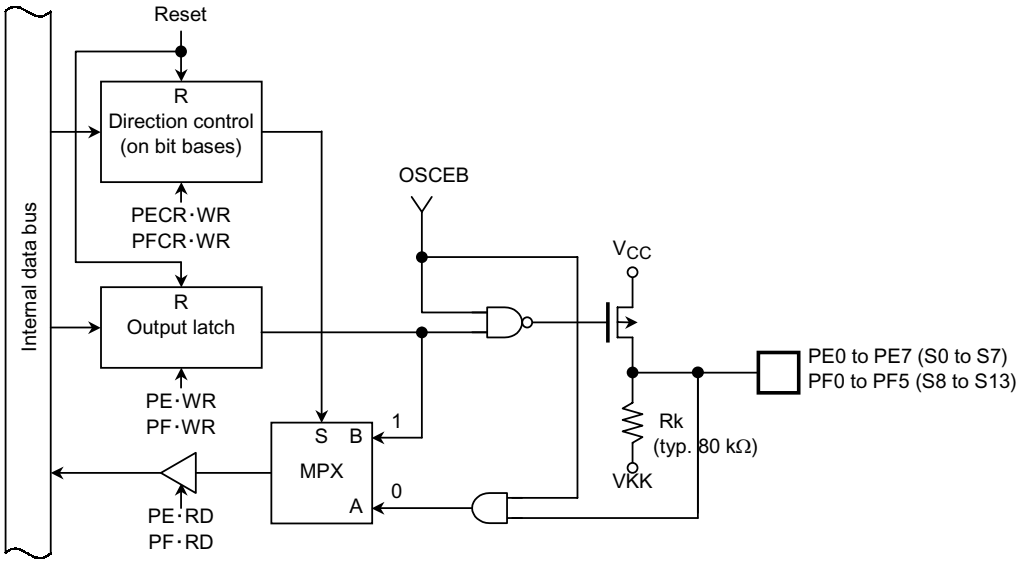


Figure 3.5.35 Port E (PE0 to PE7), Port F (PF0 to PF5)

Port E Data Register

	7	6	5	4	3	2	1	0	
PE									(Initial Value: 0000 0000)
(0089H)	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	Read/Write

Port E Control Register

	7	6	5	4	3	2	1	0	
PECR									
(008BH)	PE7C	PE6C	PE5C	PE4C	PE3C	PE2C	PE1C	PE0C	(Initial Value: 0000 0000)

PE7C to PE0C	PE input/output control	0: Input mode 1: Output mode	Write only

Prohibit read-modify-write.

Port F Data Register

	7	6	5	4	3	2	1	0	
PF									(Initial Value: **00 0000)
(008AH)			PF5	PF4	PF3	PF2	PF1	PF0	Read/Write

Port F Control Register

	7	6	5	4	3	2	1	0	
PFCR									
(008CH)			PF5C	PF4C	PF3C	PF2C	PF1C	PF0C	(Initial Value: **00 0000)

PF5C to PF0C	PF input/output control	0: Input mode 1: Output mode	Write only

Prohibit read-modify-write.

Figure 3.5.36 Registers for Port E, Port F

3.5.13 PWM0, PWM1

PWM0 and PWM1 output 14-bit pulse width modulation output (PWM0, PWM1).

The outputs are enabled by accessing PWM Start Regigter (PWMRUN) <PWM0RUN><PWM1RUN> and able to be set to N-channel open-drain output by Open-drain Output Control Register 3 (ODCR3).

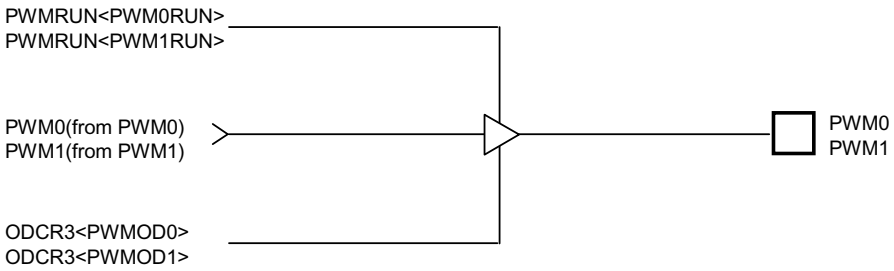


Figure 3.5.37 PWM0, PWM1

PWM Start Resister

PWMRUN (003DH)	7	6	5	4	3	2	1	0	(Initial Value: **** *000)
						PWM2RUN	PWM1RUN	PWM0RUN	

PWM1RUN	PWM1 start/stop	0: Stop 1: Start	Write only
PWM0RUN	PWM0 start/stop	0: Stop 1: Start	

Open Drain Output Control Resister 3

ODCR3 (0021H)	7	6	5	4	3	2	1	0	(Initial Value: ***0 0**0)
				PWMOD1 (PWM1)	PWMOD0 (PWM0)			PODA3 (PA3)	

PWMOD1	PWM1 Open Drain control	0: Push-Pull Output 1: Open Drain Output	Write only
PWMOD0	PWM0 Open Drain control	0: Push-Pull Output 1: Open Drain Output	

Figure 3.5.38 Registers for PWM0, PWM1

3.5.14 CLK

CLK can output fc/4 or fs/4 clock. The output is enabled by System Clock Control Register 3 (SYSCR3)<CLKEN>. The source clock can be selected from fc or fs by System Clock Control Register 1 (SYSCR1)<SYSCK> and System Clock Control Register 0 (SYSCR0)<RSYSCK>.

By the reset, <CLKEN> is initialized to 0 and CLK goes high-impedance.

During the reset, CLK is pulled internally up to V_{CC} level. (Refer to 6 Port Section Equivalent Circuit Diagram.)

When CLK is not enabled, the terminal should be pulled externally up to V_{CC}, in order to avoid some extra power consumption at the input gate.

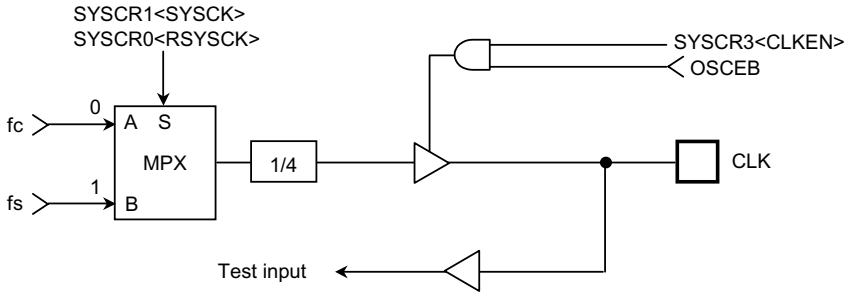


Figure 3.5.39 CLK

System Clock Control Resister 0

	7	6	5	4	3	2	1	0	
SYSCR0 (006EH)	XEN	XTEN	RXEN	RXTEN	RSYSCK	WUFF			(Reset Value: 1010 00**)

RSYSCK	Clock selection after released STOP mode	0: High frequency clock (fc) 1: Low frequency clock (fs)	R/W

System Clock Control Resister 1

	7	6	5	4	3	2	1	0	
SYSCR1 (006FH)	"0"				SYSCK	"0"	"0"	"0"	(Reset Value: 0*** 0000)

SYSCK	System clock selection	0: High frequency clock (fc) 1: Low frequency clock (fs)	R/W

System Clock Control Resister 3

	7	6	5	4	3	2	1	0	
SYSCR3 (006DH)	"1"	"1"	"1"	"1"	"0"	"0"		CLKEN	(Initial Value: 1111 00*0)

CLKEN	CLK output selection	0: High-inpidance output 1: Clock output	R/W

Figure 3.5.40 Register for CLK

3.6 Timer Counter

TMP93CF76/CF77/CW76/CU76/CT76F have an 8-bit timer counter and five 16-bit timer counters. They can be used as various event counters needed for VCR system control.

3.6.1 8-bit Timer Counter 0 (TC0)

(1) Block diagram

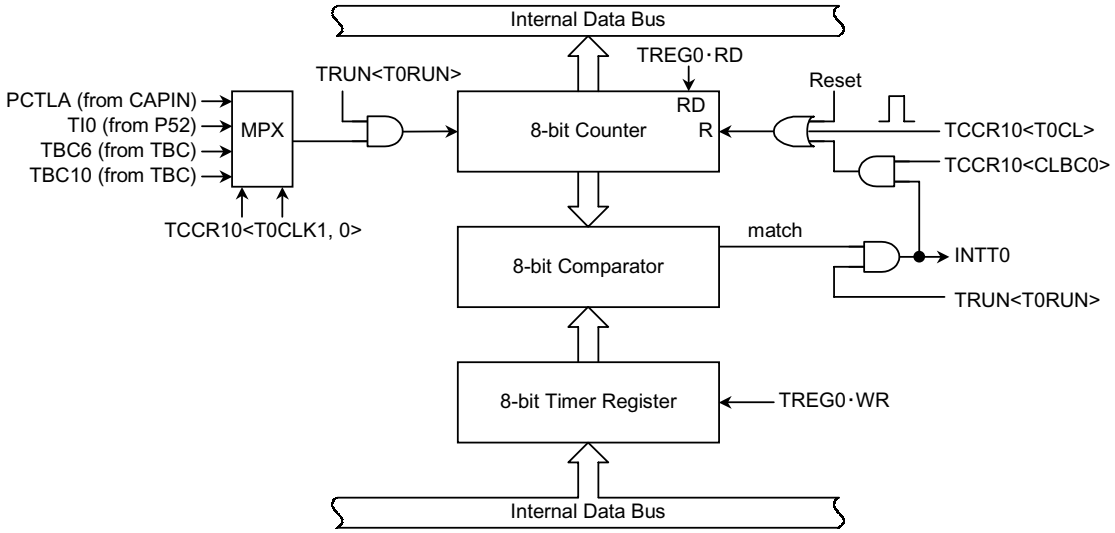


Figure 3.6.1 Composition of the Timer Counter 0

a. Up-counter

The 8-bit up-counter counts up with the input clock selected by Timer Counter Control Resister 10 (TCCR10)<T0CLK1,0>. The input clock can be selected from TBC6($2^6/f_{SYS}$), TBC10($2^{10}/f_{SYS}$) from Time Base Counter (TBC), PCTLA from Capture Input Control Circuit (CAPIN) and TI0(P52). The up-counter starts to count up when Timer Start Control Resister (TRUN)<T0RUN> is 1, and it stops to count up when TRUN<T0RUN> is 0. Reset operation clears the up-counter and TRUN<T0RUN>.

When TCCR10<CLBC0> is 1, the up-counter is cleared by the match signal from the comparator.

The up-counter is directly cleared by setting TCCR10<T0CL> to 1.

b. Timer register (TREG0)

The timer register is 8-bit register for setting the value of the interval time.

When the value of timer register coincides with the value of up-counter, a match signal is outputted from comparator. In case of setting "00H" to timer register, the match signal is outputted from comparator when up-counter overflows.

The set data is transferred to the comparator immediately after writting to TREG0. The real-time value of up-counter can be read out by reading TREG0.

TREG0 is not initialized when resetting.

c. Comparator

8-bit comparator compares the value of up-counter with the setting value of the timer register. When the value of timer register coincides with the value of up-counter, a match signal is outputted from comparator, and interrupt request (INTT0) occurs.

(2) Control Register

Timer Counter Control Register 10

TCCR10	7	6	5	4	3	2	1	0	
(0028H)	CLBC1	T1CL	T1CLK1	T1CLK0	CLBC0	T0CL	T0CLK1	T0CLK0	(Initial Value: 0000 0000)

CLBC0	TC0 counter clear by match	0: Disable 1: Enable	R/W
T0CL	TC0 counter clear	0: – 1: Clear (One-shot)	
T0CLK1 T0CLK0	TC0 source clock selection	00: PCTLA (from CAPIN) 01: TI0 (from P52) 10: TBC6 11: TBC10	

Timer Register 0

TREG0	7	6	5	4	3	2	1	0	
(0029H)	TC07	TC06	TC05	TC04	TC03	TC02	TC01	TC00	(Initial Value: 0000 0000) Read
	TR07	TR06	TR05	TR04	TR03	TR02	TR01	TR00	(Initial Value: **** ****) Write

Prohibit read-modify-write.

Timer Start Control Register

TRUN	7	6	5	4	3	2	1	0	
(0027H)			T5RUN	T4RUN	T3RUN	T2RUN	T1RUN	T0RUN	(Initial Value: *00 0000)

T0RUN	TC0 count start	0: Stop 1: Start	R/W

Figure 3.6.2 Registers for TC0

(3) Operation

a. Timer mode

In this mode, the up-counter counts up with TBC6 or TBC10.

Stop TC0 first, and select one input clock by TCCR10<T0CLK1,0> and set an interval time to TREG0. Then, enable TC0 interrupt (INTT0) and start TC0. The INTT0 interrupt request occurs when the value of the up-counter coincides with the value of TREG0.

Example : When generating TC0 interruption every 32μs by fc = 16MHz, set up each register in the order of the following.

	MSB LSB 7 6 5 4 3 2 1 0	
TRUN	– – – – – – – –	
	– – – – – – – 0	The count of the TC0 is stopped.
TCCR10	– – – – 1 * 1 0	The source clock is set to TBC6 (8 μs).
TREG0	0 0 0 0 0 1 0 0	32 μs ÷ 8 μs = 04H is set to the timer register.
INT1T0	0 n n n – – – –	INTT0 interrupt is enabled with Level “nnn”.
TRUN	– – – – – – – 1	The count of the TC0 is started.

Note: *; Don't care –; No change

Table 3.6.1 Interrupt Interval for the TC0

Interrupt Interval (at fc = 16 MHz)	Resolution	Input Clock
8.0 μs to 2.048 ms	8.0 μs	TBC6 $(2^6/f_{SYS})$
128 μs to 32.768 ms	128 μs	TBC10 $(2^{10}/f_{SYS})$

b. Event counter mode

In this mode, the up-counter counts up with the rising edge of TI0 (P52).

Stop TC0 first, and select TI0 as a source clock by TCCR10<T0CLK1,0> and set an interval time to TREG0. Then, enable TC0 interrupt (INTT0) and start TC0. The INTT0 interrupt request occurs when the value of the up-counter coincides with the value of TREG0.

The maximum input frequency is $f_{SYS}/2^3$ [Hz] (1 MHz at fc = 16 MHz). The minimum input pulse width (H level and L level) is each $2^2/f_{SYS}$ [s] (500 ns at fc = 16 MHz).

c. Playback control signal counter mode

In this mode, the up-counter counts up with the rising edge of PCTLA signal from Capture Input Control Circuit (CAPIN).

Stop TC0 first, and select PCTLA as a source clock by TCCR10<T0CLK1,0> and set an interval time to TREG0. Then, enable TC0 interrupt (INTT0) and start TC0. The INTT0 interrupt request is occurs when the value of the up-counter coincides with the value of TREG0.

3.6.2 16-Bit Timer Counter (TC1)

(1) Block diagram

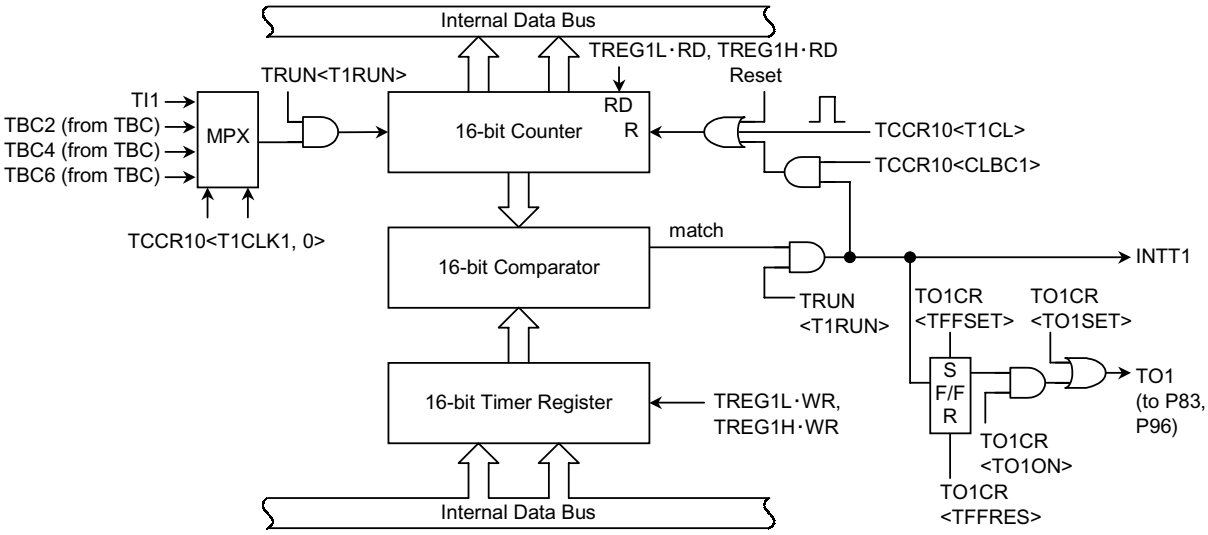


Figure 3.6.3 Composition of the timer counter 1

a. Up-counter

The 8-bit up-counter counts up with the input clock selected by Timer Counter Control Register 10 (TCCR10)<T1CLK1,0>. The input clock can be selected from TBC2($2^2/f_{SYS}$), TBC4($2^4/f_{SYS}$), TBC6($2^6/f_{SYS}$) from Time Base Counter (TBC) and TI1(P52). The up-counter starts to count up when Timer Start Cntrol Register (TRUN)<T1RUN> is 1, and it stops to count up when TRUN<T1RUN> is 0. Reset operation clears the up-counter and TRUN<T1RUN>.

When TCCR10<CLBC1> is 1, the up-counter is cleared by the match signal from the comparator.

The up-counter is directly cleared by setting TCCR10<T1CL> to 1.

b. Timer register (TREG1L/TREG1H)

The timer register is 16-bit register (8-bit register × 2) for setting the value of the interval time.

Set the lower 8-bit value to TREG1L first, and then, set the higher 8-bit value to TREG1H.

When the value of timer register coincides with the value of up-counter, a match signal is outputted from comparator. In case of setting "0000H" to timer register, the match signal is outputted from comparator when up-counter overflows.

The set data is transferred to the comparator immediately after writting to timer register. The real-time value of up-counter can be read out by reading TREG1L and TREG1H.

TREG1L and TREG1H is not initialized when resetting. TREG1H must be read after reading TREG1L. In case an overflow occurs immediately after reading TREG1L, the carry-over is added to the value of TREG1H.

Note: TREG1H must be written a data. Otherwise, the up-counter is not compared with the timer register.

c. Comparator

16-bit comparator compares the value of up-counter with the setting value of the timer register. When the value of timer register coincides with the value of up-counter, a match signal is outputted from comparator, and interrupt request (INTT1) occurs.

d. Output control circuit

The match signal from comparator is divided by 2 with a flip-flop (F/F) and can be outputted to TO1(P83 and P96).

When TO1CR<TO1SET> is 1, TO1 output is set to 1 and when <TO1SET> is 0, the divided signal is outputted from TO1.

When TO1CR<TFFSET> is 1, the flip-flop is set to 1 and when TO1CR <TFFRESET> is 1, the flip-flop is cleared to 0.

(2) Control register

Timer Counter Control Register 10

TCCR10	7	6	5	4	3	2	1	0	
(0028H)	CLBC1	T1CL	T1CLK1	T1CLK0	CLBC0	T0CL	T0CLK1	T0CLK0	(Initial Value: 0000 0000)

CLBC1	TC1 counter clear by match	0: Disable 1: Enable	R/W
T1CL	TC1 counter clear	0: – 1: Clear (One-shot)	
T1CLK1 T1CLK0	TC1 source clock selection	00: TI1 (from P52) 01: TBC2 10: TBC4 11: TBC6	

Timer Register 1 Lower order

TREG1L	7	6	5	4	3	2	1	0	
(002AH)	TC17	TC16	TC15	TC14	TC13	TC12	TC11	TC10	(Initial Value: 0000 0000) Read
	TR17	TR16	TR15	TR14	TR13	TR12	TR11	TR10	(Initial Value: **** ****) Write

Prohibit read-modify-write.

Timer Register 1 Higher order

TREG1H	7	6	5	4	3	2	1	0	
(002BH)	TC1F	TC1E	TC1D	TC1C	TC1B	TC1A	TC19	TC18	(Initial Value: 0000 0000) Read
	TR1F	TR1E	TR1D	TR1C	TR1B	TR1A	TR19	TR18	(Initial Value: **** ****) Write

Prohibit read-modify-write.

Note: Writing and reading in order of TREG1L → TREG1H are necessary.

Timer Start Control Register

TRUN	7	6	5	4	3	2	1	0	
(0027H)			T5RUN	T4RUN	T3RUN	T2RUN	T1RUN	T0RUN	(Initial Value: **00 0000)

T1RUN	TC1 count start	0: Stop 1: Start	R/W

TO1 Control Register

TO1CR (0062H)	7	6	5	4	3	2	1	0	(Initial Value: **** 0000)
					TFFRES	TFFSET	TO1ON	TO1SET	

TFFRES	Flip Flop reset	0: – 1: Reset (One-shot)	write only
TFFSET	Flip Flop reset	0: – 1: Set (One-shot)	
TO1ON	TO1 ON/OFF	0: OFF 1: ON	
TO1SET	TO1 output control	0: Divided signal is outputted from TO1. 1: Set TO1 to 1.	

Prohibit read-modify-write.

Figure 3.6.4 Registers for TC1

(3) Operation

a. Timer mode

In this mode, the up-counter counts up with TBC2, TBC4 or TBC6.

Stop TC1 first, and select one input clock by TCCR10<T1CLK1,0> and set an interval time to TREG1L and TREG1H. Then, enable TC1 interrupt (INTT1) and start TC1. The INTT1 interrupt request occurs when the value of the up-counter coincides with the value of TREG1L and TREG1H.

Table 3.6.2 Interrupt Interval or the TC1

Interrupt Interval (at fc = 16 MHz)			Resolution	Input Clock	
0.5 μs	to	32.768 ms	0.5 μs	TBC2	($2^2/f_{SYS}$)
2 μs	to	131.072 ms	2 μs	TBC4	($2^4/f_{SYS}$)
8 μs	to	524.288 ms	8 μs	TBC6	($2^6/f_{SYS}$)

b. Event counter mode

In this mode, the up-counter counts up with the rising edge of TI1 (P52).

Stop TC1 first, and select TI1 as a source clock by TCCR10<T1CLK1,0> and set an interval time to TREG1L and TREG1H. Then, enable TC1 interrupt (INTT1) and start TC1. The INTT1 interrupt request occurs when the value of the up-counter coincides with the value of TREG1L and TREG1H.

The maximum input frequency is $f_{SYS}/2^3$ [Hz] (1 MHz at fc = 16 MHz). The minimum input pulse width (H level and L level) is each $2^2/f_{SYS}$ [s] (500 ns at fc = 16 MHz).

c. Timer output 1 (TO1)

The match signal from comparator is divided by 2 with the flip-flop (F/F). The divided signal is outputted to TO1(P83 and P96).

Example: When outputing 40 [kHz] pulse at fc = 16 MHz (duty 50%), set up each register in order of the following.

	MSB 7	6	5	4	3	2	1	LSB 0	
TRUN	–	–	–	–	–	–	0	–	The count of the TC1 is stopped.
TO1CR	–	–	–	–	1	0	0	0	Reset the flip-flop.
TCCR10	0	1	0	1	–	–	–	–	Counter is cleared and the source clock is set to TBC2 (0.5 μs).
TREG1L	0	0	0	1	1	0	0	1	40 kHz, 0019H is set to timer register.
TREG1H	0	0	0	0	0	0	0	0	
INTT1T0	0	0	0	0	–	–	–	–	(INTT1 interrupt is disabled in this example.)
TO1CR	–	–	–	–	–	–	1	–	TO1 output is “ON”.
TRUN	–	–	–	–	0	0	1	0	TC1 starts counting.

Note: –; No change

3.6.3 16-Bit Timer Counter (TC2)

(1) Block diagram

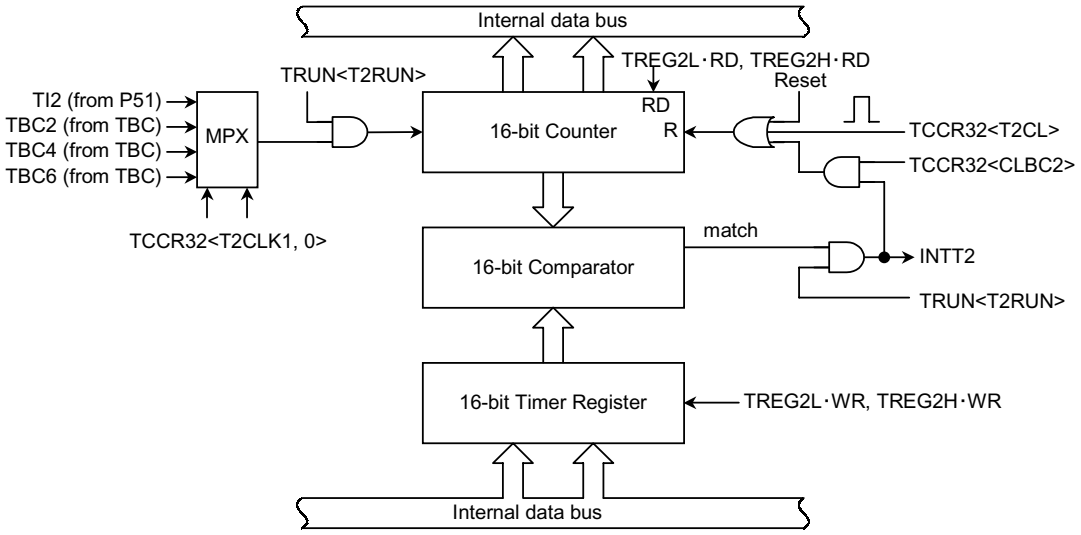


Figure 3.6.5 Composition of the Timer Counter 2

a. Up-counter

The 16-bit up-counter counts up with the input clock selected by Timer Counter Control Register 32 (TCCR32)<T2CLK1,0>. The input clock can be selected from TBC2(2^2/f_{SYS}), TBC4(2^4/f_{SYS}), TBC6(2^7/f_{SYS}) from Time Base Counter (TBC) and TI2(P51). The up-counter starts to count up when Timer Start Control Register (TRUN)<T2RUN> is 1, and it stops to count up when TRUN<T2RUN> is 0. Reset operation clears the up-counter and TRUN <T2RUN>.

When TCCR32<CLBC2> is 1, the up-counter is cleared by the match signal from the comparator.

The up-counter is directly cleared by setting TCCR32<T2CL> to 1.

b. Timer register (TREG2L/TREG2H)

The timer register is 16-bit register (8-bit register × 2) for setting the value of the interval time.

Set the lower 8-bit value to TREG2L first, and then, set the higher 8-bit value to TREG2H.

When the value of timer register coincides with the value of up-counter, a match signal is outputted from comparator. In case of setting "0000H" to timer register, the match signal is outputted from comparator when up-counter overflows.

The set data is transferred to the comparator immediately after writting to timer register. The real-time value of up-counter can be read out by reading TREG2L and TREG2H.

TREG2L and TREG2H is not initialized when resetting. TREG2H must be read after reading TREG2L. In case an overflow occurs immediately after reading TREG2L, the carry-over is added to the value of TREG2H.

Note: TREG2H must be written a data. Otherwise, the up-counter is not compared with the timer register.

c. Comparator

16-bit comparator compares the value of up-counter with the setting value of the timer register. When the value of timer register coincides with the value of up-counter, a match signal is outputted from comparator, and interrupt request (INTT2) occurs.

(2) Control register

Timer Counter Control Register 32

TCCR32	7	6	5	4	3	2	1	0	
(002CH)	CLBC3	T3CL	T3CLK1	T3CLK0	CLBC2	T2CL	T2CLK1	T2CLK0	(Initial Value: 0000 0000)

CLBC2	TC2 counter clear by match	0: Disable 1: Enable	R/W
T2CL	TC2 counter clear	0: – 1: Clear (One-shot)	
T2CLK1	TC2 source clock selection	00: TI2 (from P51) 01: TBC2 10: TBC4 11: TBC6	
T2CLK0			

Timer Register 2 Lower order

TREG2L	7	6	5	4	3	2	1	0	
(002EH)	TC27	TC26	TC25	TC24	TC23	TC22	TC21	TC20	(Initial Value: 0000 0000) Read
	TR27	TR26	TR25	TR24	TR23	TR22	TR21	TR20	(Initial Value: **** ****) Write

Prohibit read-modify-write.

Timer Register 2 Higher order

TREG2H	7	6	5	4	3	2	1	0	
(002FH)	TC2F	TC2E	TC2D	TC2C	TC2B	TC2A	TC29	TC28	(Initial Value: 0000 0000) Read
	TR2F	TR2E	TR2D	TR2C	TR2B	TR2A	TR29	TR28	(Initial Value: **** ****) Write

Prohibit read-modify-write.

Note: Writing and reading in order of TREG2L→TREG2H are necessary.

Timer Start Control Register

TRUN	7	6	5	4	3	2	1	0	
(0027H)			T5RUN	T4RUN	T3RUN	T2RUN	T1RUN	T0RUN	(Initial Value: **00 0000)

T2RUN	TC2 count start	0: Stop 1: Start	R/W

Figure 3.6.6 Registers for TC2

(3) Operation

a. Timer mode

In this mode, the up-counter counts up with TBC2, TBC4 or TBC6.

Stop TC2 first, and select one input clock by TCCR32<T2CLK1,0> and set an interval time to TREG2L and TREG2H. Then, enable TC2 interrupt (INTT2) and start TC2. The INTT2 interrupt request occurs when the value of the up-counter coincides with the value of TREG2L and TREG2H.

Table 3.6.3 Interrupt Interval for the TC2

Interrupt interval (at fc=16 MHz)	Resolution	Input Clock
0.5 μs to 32.768 ms	0.5 μs	TBC2 ($2^2/f_{SYS}$)
2 μs to 131.072 ms	2.0 μs	TBC4 ($2^4/f_{SYS}$)
8 μs to 524.288 ms	8.0 μs	TBC6 ($2^6/f_{SYS}$)

b. Event counter mode

In this mode, the up-counter counts up with the rising edge of TI2 (P51).

Stop TC2 first, and select TI2 as a source clock by TCCR32<T2CLK1,0> and set an interval time to TREG2L and TREG2H. Then, enable TC2 interrupt (INTT2) and start TC2. The INTT2 interrupt request occurs when the value of the up-counter coincides with the value of TREG2L and TREG2H.

The maximum input frequency is $f_{SYS}/2^3$ [Hz] (1 MHz at fc = 16 MHz). The minimum input pulse width (H level and L level) is each $2^2/f_{SYS}$ [s] (500 ns at fc = 16 MHz).

3.6.4 16-Bit Timer Counter (TC3)

(1) Block diagram

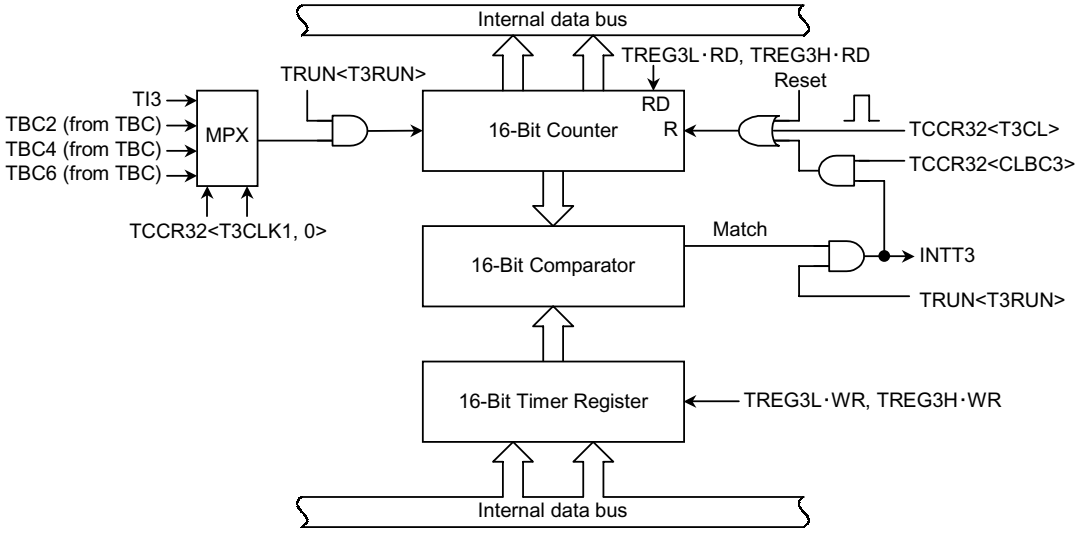


Figure 3.6.7 Composition of the timer counter 3

a. Up-counter

The 16-bit up-counter counts up with the input clock selected by Timer Counter Control Register 32 (TCCR32)<T3CLK1,0>. The input clock can be selected from TBC2(2^2/f_{SYS}), TBC4(2^4/f_{SYS}), TBC6(2^7/f_{SYS}) from Time Base Counter (TBC) and TI3(P50). The up-counter starts to count up when Timer Start Control Register (TRUN)<T3RUN> is 1, and it stops to count up when TRUN<T3RUN> is 0. Reset operation clears the up-counter and TRUN <T3RUN>.

When TCCR32<CLBC3> is 1, the up-counter is cleared by the match signal from the comparator.

The up-counter is directly cleared by setting TCCR32<T3CL> to 1.

b. Timer register (TREG3L/TREG3H)

The timer register is 16-bit register (8-bit register × 2) for setting the value of the interval time.

Set the lower 8-bit value to TREG3L first, and then, set the higher 8-bit value to TREG3H.

When the value of timer register coincides with the value of up-counter, a match signal is outputted from comparator. In case of setting "0000H" to timer register, the match signal is outputted from comparator when up-counter overflows.

The set data is transferred to the comparator immediately after writting to timer register. The real-time value of up-counter can be read out by reading TREG3L and TREG3H.

TREG3L and TREG3H is not initialized when resetting. TREG3H must be read after reading TREG3L. In case an overflow occurs immediately after reading TREG3L, the carry-over is added to the value of TREG3H.

Note: TREG3H must be written a data. Otherwise, the up-counter is not compared with the timer register.

c. Comparator

16-bit comparator compares the value of up-counter with the setting value of the timer register. When the value of timer register coincides with the value of up-counter, a match signal is outputted from comparator, and interrupt request (INTT3) occurrs.

(2) Control register

Timer Counter Control Register 32

TCCR32	7	6	5	4	3	2	1	0	
(002CH)	CLBC3	T3CL	T3CLK1	T3CLK0	CLBC2	T2CL	T2CLK1	T2CLK0	(Initial Value: 0000 0000)

CLBC3	TC3 counter clear by match	0: Disable 1: Enable	R/W
T3CL	TC3 counter clear	0: – 1: Clear (One-shot)	
T3CLK1	TC3 source clock selection	00: TI3 (from P50) 01: TBC2 10: TBC4 11: TBC6	
T3CLK0			

Timer Register 3 Lower order

TREG3L	7	6	5	4	3	2	1	0	
(0060H)	TC37	TC36	TC35	TC34	TC33	TC32	TC31	TC30	(Initial Value: 0000 0000) Read
	TR37	TR36	TR35	TR34	TR33	TR32	TR31	TR30	(Initial Value: **** ****) Write

Prohibit read-modify-write.

Timer Register 3 Higher order

TREG3H	7	6	5	4	3	2	1	0	
(0061H)	TC3F	TC3E	TC3D	TC3C	TC3B	TC3A	TC39	TC38	(Initial Value: 0000 0000) Read
	TR3F	TR3E	TR3D	TR3C	TR3B	TR3A	TR39	TR38	(Initial Value: **** ****) Write

Prohibit read-modify-write.

Note: Writing and reading in order of TREG3L→TREG3H are necessary.

Timer Start Control Register

TRUN	7	6	5	4	3	2	1	0	
(0027H)			T5RUN	T4RUN	T3RUN	T2RUN	T1RUN	T0RUN	(Initial Value: **00 0000)

T3RUN	TC3 count start	0: Stop 1: Start	R/W

Figure 3.6.8 Registers for TC3

(3) Operation

a. Timer mode

In this mode, the up-counter counts up with TBC2, TBC4 or TBC6.

Stop TC3 first, and select one input clock by TCCR32<T3CLK1,0> and set an interval time to TREG3L and TREG3H. Then, enable TC3 interrupt (INTT3) and start TC3. The INTT3 interrupt request occurs when the value of the up-counter coincides with the value of TREG3L and TREG3H.

Table 3.6.4 Interrupt interval for the TC3

Interrupt interval (at fc = 16 MHz)	Resolution	Input Clock
0.5 μs to 32.768 ms	0.5 μs	TBC2 ($2^2/f_{SYS}$)
2 μs to 131.072 ms	2.0 μs	TBC4 ($2^4/f_{SYS}$)
8 μs to 524.288 ms	8.0 μs	TBC6 ($2^6/f_{SYS}$)

b. Event counter mode

In this mode, the up-counter counts up with the rising edge of TI3 (P50).

Stop TC3 first, and select TI3 as a source clock by TCCR32<T3CLK1,0> and set an interval time to TREG3L and TREG3H. Then, enable TC3 interrupt (INTT3) and start TC3. The INTT3 interrupt request occurs when the value of the up-counter coincides with the value of the TREG3L and TREG3H.

The maximum input frequency is $f_{SYS}/2^3$ [Hz] (1 MHz at fc = 16 MHz). The minimum input pulse width (H level and L level) is each $2^2/f_{SYS}$ [s] (500 ns at fc = 16 MHz).

3.6.5 16-Bit Timer Counter (TC4)

(1) Block diagram

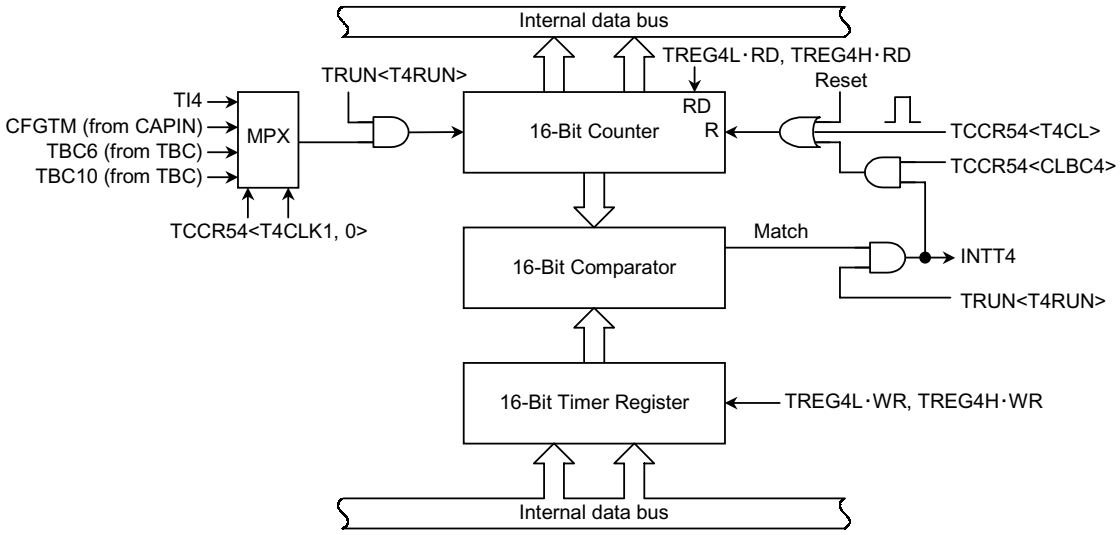


Figure 3.6.9 Composition of the timer counter 4

a. Up-counter

The 16-bit up-counter counts up with the input clock selected by Timer Counter Control Register 54 (TCCR54)<T4CLK1,0>. The input clock can be selected from TBC6(2^6/f_{SYS}), TBC10(2^{10}/f_{SYS}) from Time Base Counter (TBC), CFGTM signal from Capture Input Control Circuit (CAPIN) and TI4(P51). The up-counter starts to count up when Timer Start Control Register (TRUN)<T4RUN> is 1, and it stops to count up when TRUN<T4RUN> is 0. Reset operation clears the up-counter and TRUN<T4RUN>.

When TCCR54<CLBC4> is 1, the up-counter is cleared by the match signal from the comparator.

The up-counter is cleared by setting TCCR54<T4CL> to 1.

b. Timer register (TREG4L/TREG4H)

The timer register is 16-bit register (8-bit register × 2) for setting the value of the interval time.

Set the lower 8-bit value to TREG4L first, and then, set the higher 8-bit value to TREG4H.

When the value of timer register coincides with the value of up-counter, a match signal is outputted from comparator. In case of setting "0000H" to timer register, the match signal is outputted from comparator when up-counter overflows.

The set data is transferred to the comparator immediately after writting to timer register. The real-time value of up-counter can be read out by reading TREG4L and TREG4H.

TREG4L and TREG4H is not initialized when resetting. TREG4H must be read after reading TREG4L. In case an overflow occurs immediately after reading TREG4L, the carry-over is added to the value of TREG4H.

Note: TREG4H must be written a data. Otherwise, the up-counter is not compared with the timer register.

c. Comparator

16-bit comparator compares the value of up-counter with the setting value of the timer register. When the value of timer register coincides with the value of up-counter, a match signal is outputted from comparator, and interrupt request (INTT4) occurs.

(2) Control register

Timer Counter Control Register 54

TCCR54	7	6	5	4	3	2	1	0	
(002DH)	CLBC5	T5CL	T5CLK1	T5CLK0	CLBC4	T4CL	T4CLK1	T4CLK0	(Initial Value: 0000 0000)

CLBC4	TC4 counter clear by match	0: Disable 1: Enable	R/W
T4CL	TC4 counter clear	0: – 1: Clear (One-shot)	
T4CLK1	TC4 source clock selection	00: TI4 (from P51) 01: CFGTM (from CAPIN) 10: TBC6 11: TBC10	
T4CLK0			

Timer Register 4 Lower order

TREG4L	7	6	5	4	3	2	1	0	
(0032H)	TC47	TC46	TC45	TC44	TC43	TC42	TC41	TC40	(Initial Value: 0000 0000) Read
	TR47	TR46	TR45	TR44	TR43	TR42	TR41	TR40	(Initial Value: **** ****) Write

Prohibit read-modify-write.

Timer Register 4 Higher order

TREG4H	7	6	5	4	3	2	1	0	
(0033H)	TC4F	TC4E	TC4D	TC4C	TC4B	TC4A	TC49	TC48	(Initial Value: 0000 0000) Read
	TR4F	TR4E	TR4D	TR4C	TR4B	TR4A	TR49	TR48	(Initial Value: **** ****) Write

Prohibit read-modify-write.

Note: Writing and reading in order of TREG4L→TREG4H are necessary.

Timer Start Control Register

TRUN	7	6	5	4	3	2	1	0	
(0027H)			T5RUN	T4RUN	T3RUN	T2RUN	T1RUN	T0RUN	(Initial Value: **00 0000)

T4RUN	TC4 count start	0: Stop 1: Start	R/W

Figure 3.6.10 Registers for TC4

(3) Operation

a. Timer mode

In this mode, the up-counter counts up with TBC6 or TBC10.

Stop TC4 first, and select one input clock by TCCR54<T4CLK1,0> and set an interval time to TREG4L and TREG4H. Then, enable TC4 interrupt (INTT4) and start TC4. The INTT4 interrupt request occurs when the value of the up-counter coincides with the value of TREG4L and TREG4H.

Table 3.6.5 Interrupt Interval for the TC4

Interrupt interval (at fc = 16 MHz)	Resolution	Input Clock
8 μs to 524.288 ms	8.0 μs	TBC6 ($2^6/f_{SYS}$)
128 μs to 8388.608 ms	128 μs	TBC10 ($2^{10}/f_{SYS}$)

b. Event counter mode

In this mode, the up-counter counts up with the rising edge of TI4 (P51).

Stop TC4 first, and select TI4 as a source clock by TCCR54<T4CLK1,0> and set an interval time to TREG4L and TREG4H. Then, enable TC4 interrupt (INTT4) and start TC4. The INTT4 interrupt request occurs when the value of the up-counter coincides with the value of the TREG4L and TREG4H.

The maximum input frequency is $f_{SYS}/2^3$ [Hz] (1 MHz at fc = 16 MHz). The minimum input pulse width (H level and L level) is each $2^2/f_{SYS}$ [s] (500 ns at fc = 16 MHz).

c. Capstan FG signal counter mode

In this mode, the up-counter counts up with the rising edge of CFGTM signal from CAPIN.

Stop TC4 first, and select CFGTM as a source clock by TCCR54<T4CLK1,0> and set an interval time to TREG4L and TREG4H. Then, enable TC4 interrupt (INTT4) and start TC4. The INTT4 interrupt request occurs when the value of the up-counter coincides with the value of TREG4L and TREG4H.

3.6.6 16-Bit Timer Counter (TC5)

(1) Block diagram

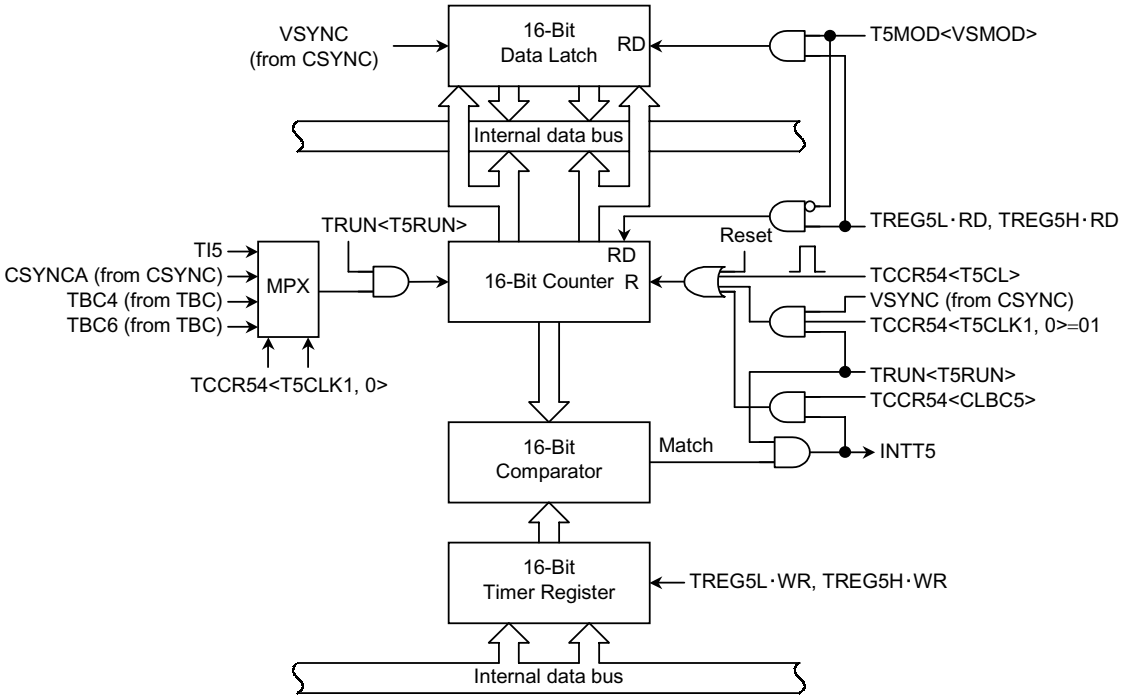


Figure 3.6.11 Composition of the timer counter 5

a. Up-counter

The 16-bit up-counter counts up with the input clock selected by Timer Counter Control Register 54 (TCCR54)<T5CLK1,0>. The input clock can be selected from TBC4(2^4/f_{SYS}), TBC6(2^6/f_{SYS}) from Time Base Counter (TBC), CSYNCA signal from Sync Signal Separator (CSYNC) and TI5(P50). The up-counter starts to count up when Timer Start Control Register (TRUN)<T5RUN> is 1, and it stops to count up when TRUN<T5RUN> is 0. Reset operation clears the up-counter and TRUN<T5RUN>.

When TCCR54<CLBC5> is 1, the up-counter is cleared by the match signal from the comparator.

The up-counter is cleared by setting TCCR54<T5CL> to 1.

b. Timer register (TREG5L/TREG5H)

The timer register is 16-bit register (8-bit register × 2) for setting the value of the interval time.

Set the lower 8-bit value to TREG5L first, and then, set the higher 8-bit value to TREG5H.

When the value of timer register coincides with the value of up-counter, a match signal is outputted from comparator. In case of setting "0000H" to timer register, the match signal is outputted from comparator when up-counter overflows.

The set data is transferred to the comparator immediately after writting to timer register. The real-time value of up-counter can be read out by reading TREG5L and TREG5H.

TREG5L and TREG5H is not initialized when resetting. TREG5H must be read after reading TREG5L. In case an overflow occurs immediately after reading TREG5L, the carry-over is added to the value of TREG5H.

Note : TREG5H must be written a data. Otherwise, the up-counter is not compared with the timer register.

c. Comparator

16-bit comparator compares the value of up-counter with the setting value of the timer register. When the value of timer register coincides with the value of up-counter, a match signal is outputted from comparator, and interrupt request (INTT5) occurs.

d. Data latch

The data latch latches the value of the up-counter at the rising edge of the vertical synchronizing signal VSYNC and read the value of this latch from TREG5L and TREG5H when T5MOD<VSMOD> is 1.

(2) Control register

Timer Counter Control Register 54

TCCR54	7	6	5	4	3	2	1	0	
(002DH)	CLBC5	T5CL	T5CLK1	T5CLK0	CLBC4	T4CL	T4CLK1	T4CLK0	(Initial Value: 0000 0000)

CLBC5	TC5 counter clear by match	0: Disable 1: Enable	R/W
T5CL	TC5 counter clear	0: – 1: Clear (One-shot)	
T5CLK1	TC5 source clock selection	00: TI5 (from P50) 01: CSYNCA (from CSYNC) 10: TBC4 11: TBC6	
T5CLK0			

Timer Register 5 Lower Order

TREG5L	7	6	5	4	3	2	1	0	
(0034H)	TC57	TC56	TC55	TC54	TC53	TC52	TC51	TC50	(Initial Value: 0000 0000) Read
	TR57	TR56	TR55	TR54	TR53	TR52	TR51	TR50	(Initial Value: **** ****) Write

Prohibit read-modify-write.

Timer Register 5 Higher Order

TREG5H	7	6	5	4	3	2	1	0	
(0035H)	TC5F	TC5E	TC5D	TC5C	TC5B	TC5A	TC59	TC58	(Initial Value: 0000 0000) Read
	TR5F	TR5E	TR5D	TR5C	TR5B	TR5A	TR59	TR58	(Initial Value: **** ****) Write

Prohibit read-modify-write.

Note: Setting and reading in order of TREG5L→TREG5H are necessary.

Timer Start Control Register

TRUN	7	6	5	4	3	2	1	0	
(0027H)			T5RUN	T4RUN	T3RUN	T2RUN	T1RUN	T0RUN	(Initial Value: **00 0000)

T5RUN	TC5 count start	0: Stop 1: Start	R/W

TC5 Mode Control Register

T5MOD (008EH)	7	6	5	4	3	2	1	0
								VSMOD

(Initial Value: **** ***0)

VSMOD	TC5 function selection	0: Timer/Event Counter 1: C.sync Counter	R/W

Figure 3.6.12 Registers for TC5

(3) Operation

a. Timer mode

In this mode, the up-counter counts up with TBC4 or TBC6.

Stop TC5 first, and select one input clock by TCCR54<T5CLK1,0> and set an interval time to TREG5L and TREG5H. Then, enable TC5 interrupt (INTT5) and start TC5. The INTT5 interrupt request occurs when the value of the up-counter coincides with the value of TREG5L and TREG5H.

Table 3.6.6 Interrupt interval for the TC5

Interrupt interval (at fc = 16 MHz)	Resolution	Input Clock
2 μs to 131.072 ms	2.0 μs	TBC4 ($2^4/f_{SYS}$)
8 μs to 524.288 ms	8.0 μs	TBC6 ($2^6/f_{SYS}$)

b. Event counter mode

In this mode, the up-counter counts up with the rising edge of TI5 (P50).

Stop TC5 first, and select TI5 as a source clock by TCCR54<T5CLK1,0> and set an interval time to TREG5L and TREG5H. Then, enable TC5 interrupt (INTT5) and start TC5. The INTT5 interrupt request occurs when the value of the up-counter coincides with the value of the TREG5L and TREG5H.

The maximum input frequency is $f_{SYS}/2^3$ [Hz] (1 MHz at fc = 16 MHz). The minimum input pulse width (H level and L level) is each $2^2/f_{SYS}$ [s] (500 ns at fc = 16 MHz).

c. Composite Sync. (C.Sync) signal counter mode

In this mode, the up-counter counts up with the rising edge of CSYNCA signal from CSYNC. Composite Sync. signal (C.sync) is inputted to CSYNCIN (P86) pin and its edge is selected by Sync Signal Separator (CSYNC). TC5 can measure the selected signal CSYNCA by synchronizing with the Vertical Synchronizing Signal (V.sync).

Stop TC5 first, and set T5MOD<VSMOD> to 1 and CSYNCA signal is selected as a source clock when TCCR54<T5CLK1,0>. Then, start TC5. The data latch latches the value of the up-counter at the rising edge of the VSYNC signal and the up-counter is cleared at the same time.

Composite Sync. signal can be measured by reading the data latch in Capture 0 interrupt (INTCAP0) service routine.

3.7 Capture

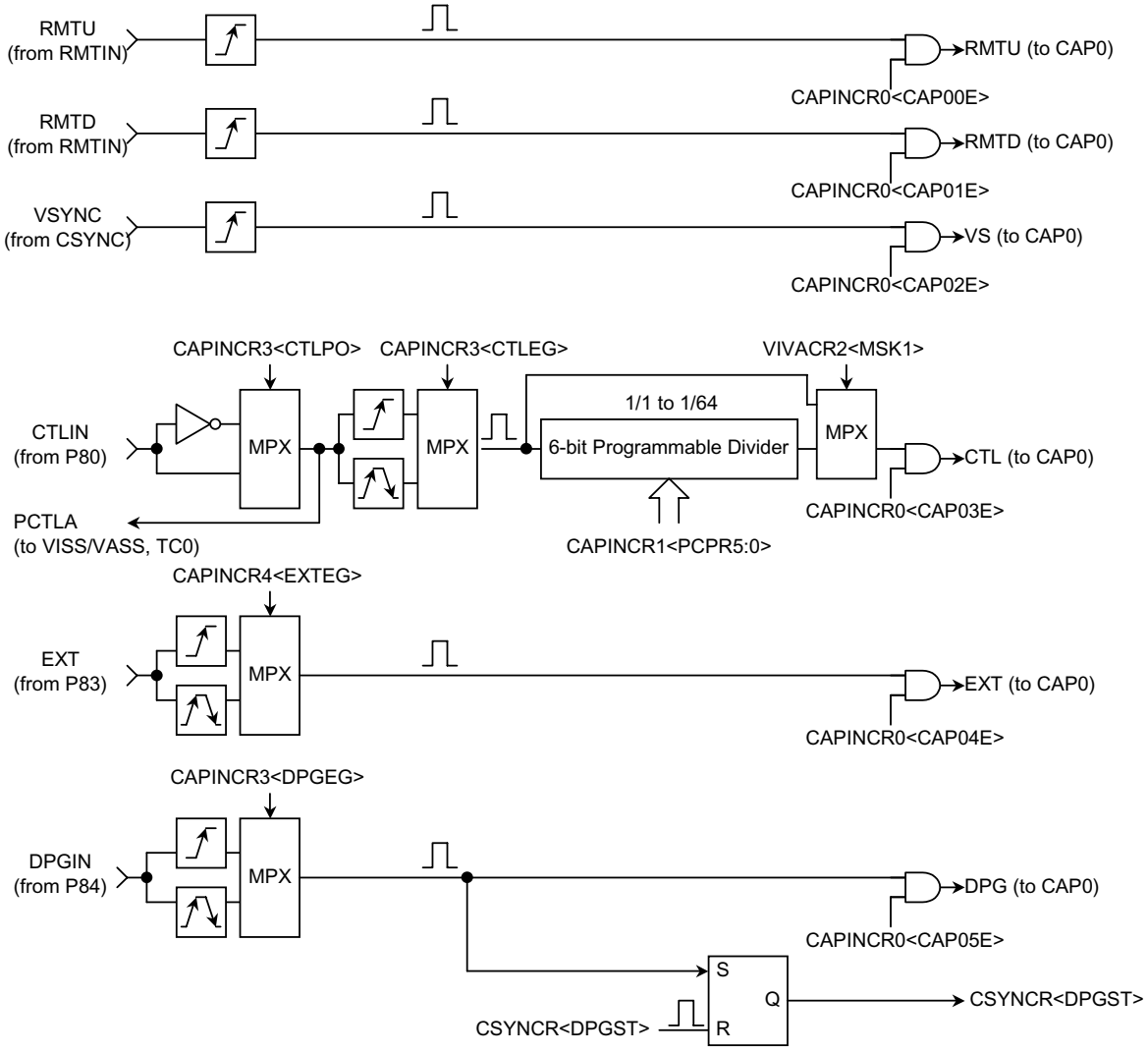
The capture circuit latches the time data of the time base counter (TBC) and the captures input status (trigger input signal). The data of TBC can be latched by the trigger input signal and the interrupt request is generated to CPU. By using the capture circuit, time measurement process for servo control can be done in high accuracy.

The capture circuit consists of the capture 0 (CAP0) with eight level of 24-bit FIFO (first-in first-out) data buffer, the capture 1 (CAP1) and the capture 2 (CAP2) with single level of 17-bit FIFO data buffers.

3.7.1 Capture Input Control Circuit (CAPIN)

Capture input control circuit (CAPIN) controls the trigger input signals for the three channels of capture circuits (CAP0, CAP1 and CAP2), and consists of the capture 0 input control circuit, capture 1 input control circuit and capture 2 input control circuit.

(1) Capture 0 (CAP0) input control circuit



Note: The minimum input pulse width (“H” level and “L” level) of CTLIN, EXT, DPGIN are $2/f_{SYS}$ (250 ns at fc = 16 MHz).

Figure 3.7.1 Capture 0 input control circuit

a. Remote control signal rising edge (RMTU)

This is the rising edge signal of the remote control signal detected by the remote control signal input circuit (RMTIN).

Enabling this trigger input to capture 0 (CAP0) is controlled by Capture Input Control Register 0 (CAPINCR0)<CAP00E>.

b. Remote control signal falling edge (RMTD)

This is the falling edge signal of the remote control signal detected by the remote control signal input circuit (RMTIN).

Enabling this trigger input to capture 0 (CAP0) is controlled by CAPINCR0<CAP01E>.

c. Sync. separation input (VS)

This is the vertical synchronizing signal (VSYNC) separated from Composite Sync.signal by Syncronizing signal separator (CSYNC).

Enabling this trigger input to capture 0 (CAP0) controlled by CAPINCR0 <CAP02E>.

d. Control signal input (CTL)

The CTLIN signal is a pulse formed with an external amplifier from the picture CTL signal and inputted to pin80 (CTLIN). The polarity of CTLIN can be selected by Capture Input Control Register 3 (CAPINCR3)<CTLPO>. The capturing timing can be selected from either rising edge of control signal or both rising and falling edges by CAPINCR3<CTLEG>. The detected edge signal can be divided by a 6-bit programmable frequency divider. The frequency division ratio can be set by Capture Input Control Register 1 (CAPINCR1)<PCPR5 to 0> from 1/1 to 1/64. It is selectable to skip the dividing process for CTLIN by VISS/VASS Control Resister 2 (VIVACR2)<MSK1>.

Enabling the trigger input to capture 0 (CAP0) is controlled by CAPINCR0 <CAP03E>.

e. EXT Input (EXT)

This is the trigger signal from EXT (P83) pin. Rising edge or rising/falling edge of EXT is selected by Capture Input Control Register 4 (CAPINCR4)<EXTEG>.

Enabling the trigger input to capture 0 (CAP0) is controlled by CAPINCR0 <CAP04E>.

f. Drum PG signal input (DPG)

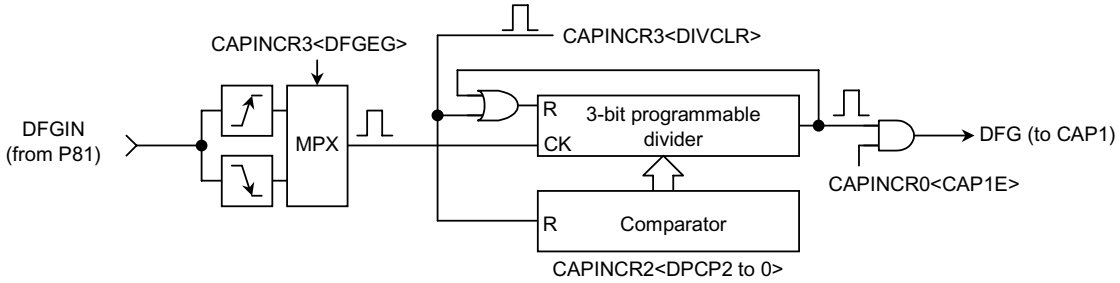
The external Drum PG signal is inputted to DPGIN (P84) pin.

Rising edge or rising/falling edge of DPGIN is selected by Capture Input Control Register 3 (CAPINCR3)<DFGEG>.

Enabling the trigger input to capture 0 (CAP0) is controlled by CAPINCR0 <CAP05E>.

A status F/F is also set by DPGIN. The status F/F can be read by CSYNC Control Register (CSYNCR)<DPGST>. By setting <DPGST> to 1, the status F/F is cleared.

(2) Capture 1 (CAP 1) Input Control



Note: The minimum input pulse width ("H" level and "L" level) of DFGIN is $f_{SYS}/2$ (250 ns at fc = 16 MHz).

Capture 1 input control circuit

The trigger of capture 1 (CAP1) is the external Drum FG signal (DPGIN). Rising edge or falling edge of DFGIN is selected by CAPINCR3<DFGED>. The detected edge signal is divided by a 3-bit programmable frequency divider from 1/1 (CAPINCR2<DPCP2 to 0 = 0H>) to 1/8 (<DPCP2 to 0> = 7H). 3-bit programmable divider and <DPCP2:0> can be cleared to 0 by setting CAPINCR3<DIVCLR>. Enabling trigger input to Capture1 (CAP1) is controlled by CAPINCR0<CAP1E>.

Figure 3.7.2 shows a timing chart of the Capture 1 Control Circuit.

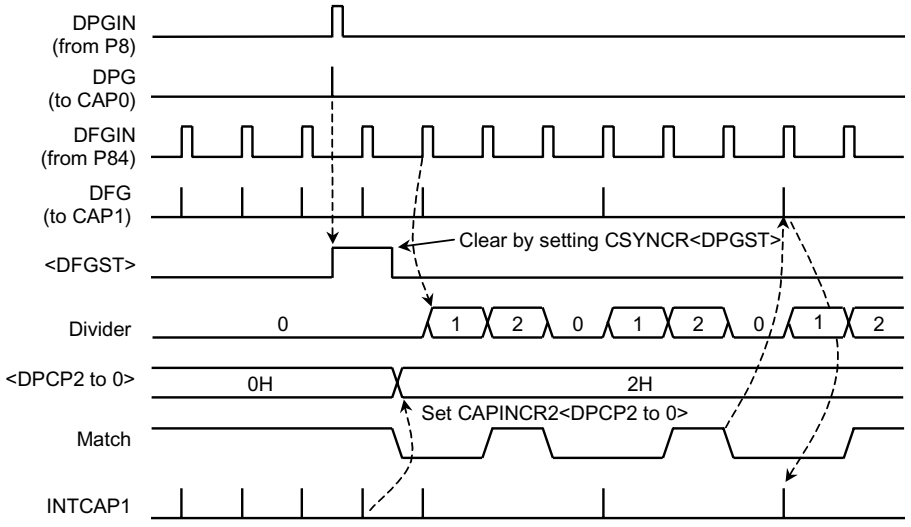
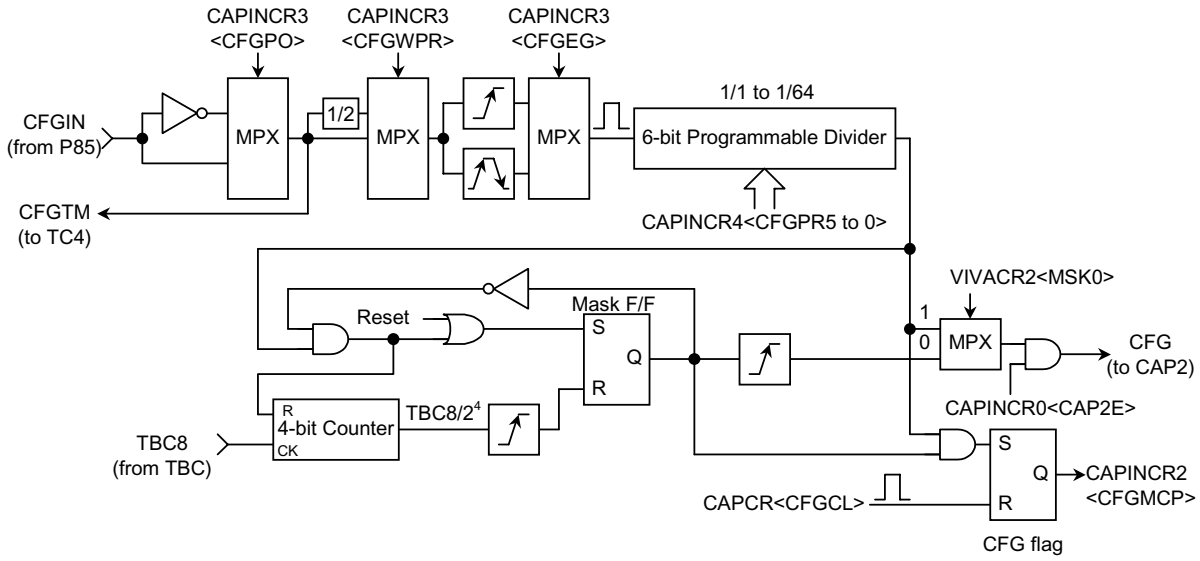


Figure 3.7.2 Capture 1 input control timing chart

(3) Capture 2 (CAP2) Input Control



Note: The minimum input pulse width ("H" level and "L" level) of CFGIN is $2/f_{SYS}$ (250 ns at fc = 16 MHz).

Figure 3.7.3 Capture 2 input control circuit

The trigger of capture 2 (CAP2) is the external capstan FG signal (CFGIN). The polarity of CFGIN can be selected by CAPINCR3 <CFGPO>. The input signal can be divided 1/1 or 1/2 by using CAPINCR3<CFGWPR>. Either rising edge or both rising and falling edges of CFGIN signal can be selected by CAPINCR3<CFGEG>. The detected edge signal can be divided by a 6-bit programmable frequency divider. The frequency division ratio can be set by Capture Input Control Register 4 (CAPINCR4)<CFGPR5 to 0>. The divided CFGIN signal can be masked during an interval of TBC8 $(2^9/fc) \times 8$ [s] by a 4-bit mask counter. The CFGIN signal during the interval is not inputted to CAP2, but sets CAPINCR2<CFGMCP> to 1. The CFG flag <CFGMCP> can be reset to 0 by CAPCR<CFGCL>. CFGIN signal to mask processing or by-passing can be selected by VIVACR2<MSK0>.

Enabling the trigger input to capture 2 (CAP2) is controlled by CAPINCR0<CAP2E>.

Figure 3.7.4 shows the timing chart for Capture 2 Input Control.

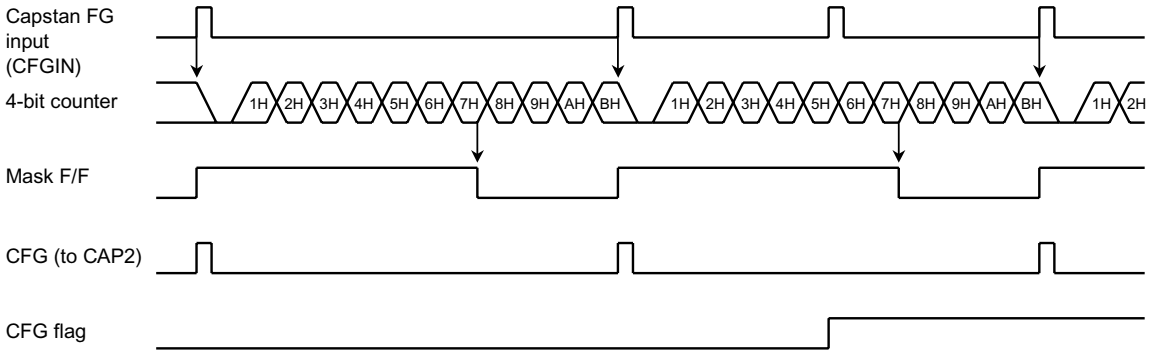


Figure 3.7.4 Capture 2 input control timing chart (VIVACR2<MSK0> = 0)

(4) Capture Input Control Register

Capture Input Control Register 0

CAPINCR0 (0046H)

7	6	5	4	3	2	1	0	(Initial Value: 0000 0000)
CAP2E (CFG)	CAP1E (DFG)	CAP05E (DPG)	CAP04E (EXT)	CAP03E (CTL)	CAP02E (VS)	CAP01E (RMTD)	CAP00E (RMTU)	

CAP2E	Capture 2 input Enable/Disable	0: Disable 1: Enable	R/W
CAP1E	Capture 1 input Enable/Disable	0: Disable 1: Enable	
CAP05E to CAP00E	Capture 0 input Enable/Disable	0: Disable 1: Enable	

Capture Input Control Register 1

CAPINCR1 (0047H)

7	6	5	4	3	2	1	0	(Initial Value: 0000 0000)
PCTLCK1	PCTLCK0	PCPR5	PCPR4	PCPR3	PCPR2	PCPR1	PCPR0	

PCPR5 to PCPR0	CTL signal (CTLIN) freqency division ratio (1/1 to 1/64)	000000: 1/1 000001: 1/2 to 111111: 1/64	R/W

Capture Input Control Register 2

CAPINCR2 (0048H)

7	6	5	4	3	2	1	0	(Initial Value: 0000 0000)
0	RMTST	RMTP0	RMTBP	CFGMCP	DPCP2	DPCP1	DPCP0	

CFGMCP	CFG flag	0: Normal 1: Error	read only
DPCP2 to DPCP0	DFG signal (DFGIN) frequency division ratio (1/1 to 1/8)	000: 1/1 001: 1/2 to 111: 1/8	R/W

Note: The bit 7 should be cleared to 0.

Capture Input Control Register 3

CAPINCR3 (0049H)	7	6	5	4	3	2	1	0	(Initial Value: 0000 0000)
	DIVCLR	CTLPO	CFGPO	DPGEG	DFGEG	CFGWPR	CFGEG	CTLEG	

DIVCLR	DFG divider division ratio clear	0: – 1: Clear (One-shot)	R/W
CTLPO	CTL input polarity selection	0: Positive 1: Negative	
CFGPO	CFG input polarity selection	0: Positive 1: Negative	
DPGEG	DFG input edge selection	0: Rising edge 1: Both edge	
DFGEG	DFG input edge selection	0: Rising edge 1: Falling edge	
CFGWPR	CFG input division ratio	0: 1/1 1: 1/2	
CFGEG	CFG input edge selection	0: Both edge 1: Rising edges	
CTLEG	CTL input edge selection	0: Rising edge 1: Both edges	

Capture Input Control Register 4

CAPINCR4 (0068H)	7	6	5	4	3	2	1	0	(Initial Value: 0*00 0000)
	EXTEG		CFGPR5	CFGPR4	CFGPR3	CFGPR2	CFGPR1	CFGPR0	

EXTEG	EXT input edge selection	0: Rising edge 1: Both edges	R/W
CFGPR5 to CFGPR0	CFG signal (CFGIN) Frequency division ratio (1/1 to 1/64)	000000: 1/1 to 111111: 1/64	

CSYNC Control Register

CSYNCR (0057H)	7	6	5	4	3	2	1	0	(Initial Value: 0*00 0000)
	0		DPGST	CSYNCPO	SEPMOD	CSYNBP	0	MASK	

DPGST	DPG detection monitor	(Read) 0: – 1: DPG input detected (Write) 0: – 1: Reset (One-shot)	R/W

Note: The bit 7 and 1 should be cleared to 0.

VISS/VASS Control Register 2

VIVACR2 (0055H)	7	6	5	4	3	2	1	0	(Initial Value: 0*00 0000)
	PCTLPO	PCTLCKS	MSK1	MSK0	VISS3	VISS2	VISS1	VISS0	

MSK1	CTLIN input division control	0: Divide 1: Bypass	R/W
MSK0	CFG input masking control	0: Mask 1: Bypass	

Capture Control Register

CAPCR (0052H)	7	6	5	4	3	2	1	0	(Initial Value: 0000 0000)
	CAP2T (CFG)	CAP1T (DFG)	CAPCL	VISFRS	VASFRS	TPRS0	CFGCL	CAFRS	

CFGCL	CFG flag clear	0: – 1: Clear (One-shot)	R/W

Prohibit read-modify-write.

Figure 3.7.5 Register for CAPIN

3.7.2 Capture 0 (CAP0)

(1) Block diagram

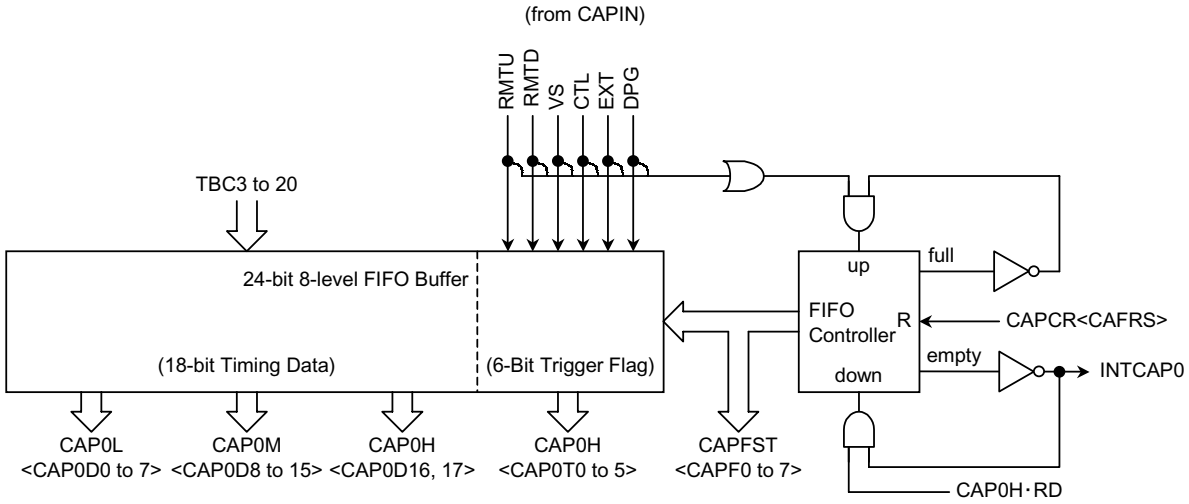


Figure 3.7.6 Composition of the Capture 0

(2) Operation

a. Capture

The trigger signals for capture 0 (CAP0) are the six signals outputted from capture 0 input control circuit: RMTU, RMTD, VS, CTL, EXT and DPG. The CAP0 latches 18-bit timing data (Outputs from Time Base Counter: TBC3 to TBC20) and 6-bit trigger data in 3-byte Capture Data Register (CAP0L, CAP0M, CAP0H).

The 24 bits latched data can be obtained by reading CAP0L → CAP0M → CAP0H in order. The address of FIFO buffer is shifted by reading CAP0H.

Note: CAP0M and CAP0H need to be read serially. Therefore, CAP0M and CAP0H need to be read by word operation, or CAPFST, CAP0L,CAP0M and CAP0H need to be read by long-word read operation.

```
ex1) LDB   reg. (CAP0L)
     LDW   reg. (CAP0M)     ; CAP0M/CAP0H word read operation
ex2) LDL   reg. (CAPFST)    ; CAPFST/CAP0L/CAP0M/CAP0H long-word
                              read operation
```

b. FIFO Status Register

The 24-bit 8-level data buffer features FIFO (First In First Out) function, allowing the data latched first to be read first. Capture 0 FIFO status register (CAPFST) indicates the status of FIFO shifting, and the status bits that correspond to the level being latched are set to 1. When the 8-level FIFO buffer becomes full, capture operations are disabled and the FIFO status register shows "FFH".

When the FIFO status register shows "00H", meaning empty, "FFH" is read out from the capture data register. The capture data can be read out when INTCAP0 interruption is generated or FIFO status register doesn't show "00H."

c. Capture Reset

In addition to a system reset function (initialization by resetting), capture 0 also has a software reset function. Software reset is performed by writing 1 at <CAFRS> of capture control register (CAPCR). In performing a software reset, the following circuits are initialized.

a. The FIFO address counter indicates the first level of the 8-stage FIFO buffer.
b. The FIFO status register (CAPFST) is initialized to "00H."

d. INTCAP0 Interruption

When a latch operation is performed by the trigger input, INTCAP0 interruption request is generated. The INTCAP0 interruption request signal is held in the active state until the FIFO status register reaches "00H" (empty).

When INTCAP0 interruption is accepted, read out the capture data from CAP0L, CAP0M and CAP0H <CAP0D16 to 17> and trigger data from CAP0H<CAP0T0 to 5> to verify the time data and interrupt sources.

INTCAP0 interruption request is available until reading out the FIFO buffer until the FIFO status register reaches "00H" or writing 1 to CAPCR<CAFRS>.

e. Data Processing

The upper 6 bits of the FIFO buffer show the status of the trigger input. As the data corresponding to the trigger input is set to 1, the trigger input can be identified by reading out the data.

Restore the latched data to RAM, and by subtracting the data from the data latched by the next trigger input, highly precise time measurement can be performed. Detection precision is 500 ns at 16 MHz operation, and quantum error is extremely small.

(3) Control Register

Capture 0 FIFO Status Register

CAPFST (004AH)

7	6	5	4	3	2	1	0	
CAPF7 (FIFO8)	CAPF6 (FIFO7)	CAPF5 (FIFO6)	CAPF4 (FIFO5)	CAPF3 (FIFO4)	CAPF2 (FIFO3)	CAPF1 (FIFO2)	CAPF0 (FIFO1)	(Initial Value: 0000 0000)

CAPF7 to CAPF0	FIFO status	0: No capture data 1: Capture data present in FIFO	read only

Capture 0 Data Register - Low order

CAP0L (004BH)

7	6	5	4	3	2	1	0	
CAP0D7 (TBC10)	CAP0D6 (TBC9)	CAP0D5 (TBC8)	CAP0D4 (TBC7)	CAP0D3 (TBC6)	CAP0D2 (TBC5)	CAP0D1 (TBC4)	CAP0D0 (TBC3)	(Initial Value: **** ****) Read only

Capture 0 Data Register - Middle order

CAP0M (004CH)

7	6	5	4	3	2	1	0	
CAP0D15 (TBC18)	CAP0D14 (TBC17)	CAP0D13 (TBC16)	CAP0D12 (TBC15)	CAP0D11 (TBC14)	CAP0D10 (TBC13)	CAP0D9 (TBC12)	CAP0D8 (TBC11)	(Initial Value: **** ****) Read only

Capture 0 Data Register - High order

CAP0H (004DH)

7	6	5	4	3	2	1	0	
CAP0T5 (DPG)	CAP0T4 (EXT)	CAP0T3 (CTL)	CAP0T2 (VS)	CAP0T1 (RMTD)	CAP0T0 (RMTU)	CAP0D17 (TBC20)	CAP0D16 (TBC19)	(Initial Value: **** ****)

CAP0T5 to CAP0T0	Trigger input status	0: No trigger input 1: Trigger input accepted in FIFO	read only

Capture Control Register

CAPCR (0052H)

7	6	5	4	3	2	1	0	
CAP2T (CFG)	CAP1T (DFG)	CAPCL	VISFRS	VASFRS	TPRS0	CFGCL	CAFRS	(Initial Value: 0000 0000)

CAFRS	CAP0 FIFO counter/status clear	0: – 1: Clear (One-shot)	R/W

Prohibit read-modify-write.

Figure 3.7.7 Registers for Capture 0

3.7.3 Capture 1/Capture 2 (CAP1/CAP2)

(1) Block diagram

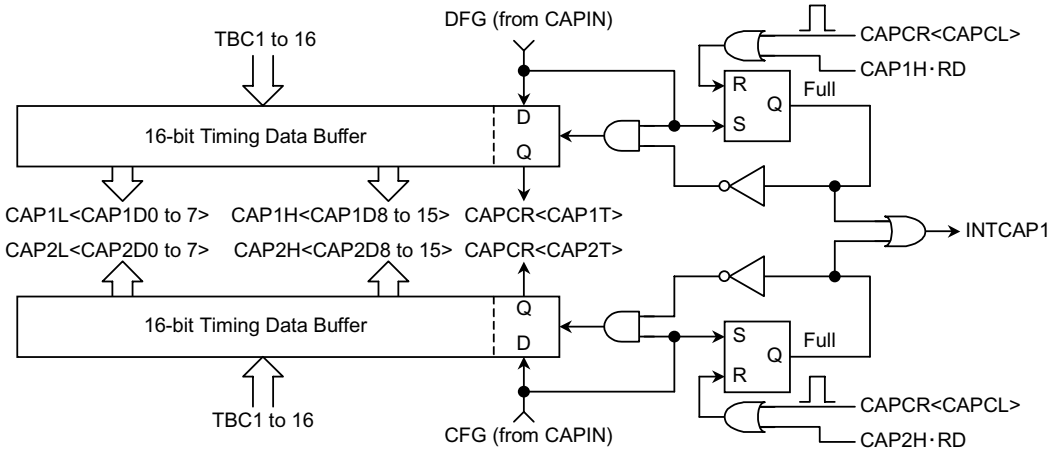


Figure 3.7.8 Composition of the Capture 1/Capture 2

(2) Operation

a. Capture

The trigger input signals are DFG and CFG signals for capture 1 and capture 2 respectively.

The outputs of time base counters (TBC1 to TBC16) are latched into the 2 bytes of capture data register (CAP1L and CAP1H for Capture1, CAP2L and CAP2H for Capture2) at the edge of the trigger input signal.

The trigger input signal is also latched into <CAP1T> or <CAP2T> of capture control register (CAPCR).

When the CAPCR<CAP1T> is 1, capture 1 data can be obtained by reading out the lower data from capture 1 data register (CAP1L) and the higher data from capture 1 data register (CAP1H) in this order. By reading out CAP1H, the trigger input status <CAP1T> is cleared. When <CAP1T> is 0, "FFH" is read out from CAP1L and CAP1H each.

When the CAPCR<CAP2T> is 1, capture 2 data can be obtained by reading out the lower data from capture 2 data register (CAP2L) and higher data from capture 2 data register (CAP2H) in this order. By reading out CAP2H, the trigger input status <CAP2T> is cleared. When <CAP2T> is 0, "FFH" is read out from CAP2L and CAP2H each.

b. Capture Reset

In capture 1 and 2, trigger input status <CAP1T> and <CAP2T> can be cleared by writing 1 to CAPR <CAPCL> .

c. INTCAP1 Interruption

When the trigger input signal is latched by the edge of DFG or CFG signal, an INTCAP1 interruption request is generated.

INTCAP1 is common interruption for both Capture 1 and Capture 2, and read out <CAP1T> and <CAP2T> to identify the trigger input.

INTCAP1 interruption request is kept available until <CAP1T> <CAP2T> is cleared to 0.

INTCAP1 interruption request is released by reading out either CAP1H or CAP2H and clearing <CAP1T> <CAP2T> to 0, or by writing CAPCR <CAPCL> to 1.

(3) Control Register

a. Control Register for Capture 1

Capture 1 Data Register - Low order

CAP1L	7	6	5	4	3	2	1	0	(Initial Value:
(004EH)	CAP1D7 (TBC8)	CAP1D6 (TBC7)	CAP1D5 (TBC6)	CAP1D4 (TBC5)	CAP1D3 (TBC4)	CAP1D2 (TBC3)	CAP1D1 (TBC2)	CAP1D0 (TBC1)	**** ****)
									Read only

Capture 1 Data Register - High order

CAP1H	7	6	5	4	3	2	1	0	(Initial Value:
(004FH)	CAP1D15 (TBC16)	CAP1D14 (TBC15)	CAP1D13 (TBC14)	CAP1D12 (TBC13)	CAP1D11 (TBC12)	CAP1D10 (TBC11)	CAP1D9 (TBC10)	CAP1D8 (TBC9)	**** ****)
									Read only

Capture Control Register

CAPCR	7	6	5	4	3	2	1	0	
(0052H)	CAP2T (CFG)	CAP1T (DFG)	CAPCL	VISFRS	VASFRS	TPRS0	CFGCL	CAFRS	(Initial Value: 0000 0000)

CAP1T	CAP1 trigger (DFG) input status	0: No trigger input 1: Trigger input	read only
CAPCL	CAP1/CAP2 status clear	0: – 1: Clear (One-shot)	R/W

Prohibit read-modify-write.

Figure 3.7.9 Registers for Capture 1

b. Control Register for Capture 2

Capture 2 Data Register - Low order

CAP2L	7	6	5	4	3	2	1	0	(Initial Value:
(0050H)	CAP2D7 (TBC8)	CAP2D6 (TBC7)	CAP2D5 (TBC6)	CAP2D4 (TBC5)	CAP2D3 (TBC4)	CAP2D2 (TBC3)	CAP2D1 (TBC2)	CAP2D0 (TBC1)	**** ****) Read only

Capture 2 Data Register – High order

CAP2H	7	6	5	4	3	2	1	0	(Initial Value:
(0051H)	CAP2D15 (TBC16)	CAP2D14 (TBC15)	CAP2D13 (TBC14)	CAP2D12 (TBC13)	CAP2D11 (TBC12)	CAP2D10 (TBC11)	CAP2D9 (TBC10)	CAP2D8 (TBC9)	**** ****) Read only

Capture Control Register

CAPCR	7	6	5	4	3	2	1	0	
(0052H)	CAP2T (CFG)	CAP1T (DFG)	CAPCL	VISFRS	VASFRS	TPRS0	CFGCL	CAFRS	(Initial Value: 0000 0000)

CAP2T	CAP2 trigger (CFG) input status	0: No trigger input 1: Trigger input	read only
CAPCL	CAP1/CAP2 status clear	0: – 1: Clear (One-shot)	R/W

Prohibit read-modify-write.

Figure 3.7.10 Registers for Capture 2

3.8 Timing Pulse Generator (TPG)

To generate the various kinds of timing pulse necessary for VTR system control, the TMP93CF76/CF77/CW76/CU76/CT76 has timing pulse generator 0 (TPG0) with 22-bit 8-stage FIFO buffer and 20-bit timing pulse generator 1 (TPG1).

The TPG0 and TPG1 can output the timing pulse synchronized with time base counter (TBC). The accuracy for both TPG0 and TPG1 is 500 ns (when operating at 16 MHz).

3.8.1 Timing Pulse Generator 0 (TPG0)

(1) Block diagram

The TPG0 is composed of 22-bit 8-stage FIFO data register (16-bit timing data + 6-bit output data), 16-bit comparator, 6-bit output data buffer and FIFO control circuit.

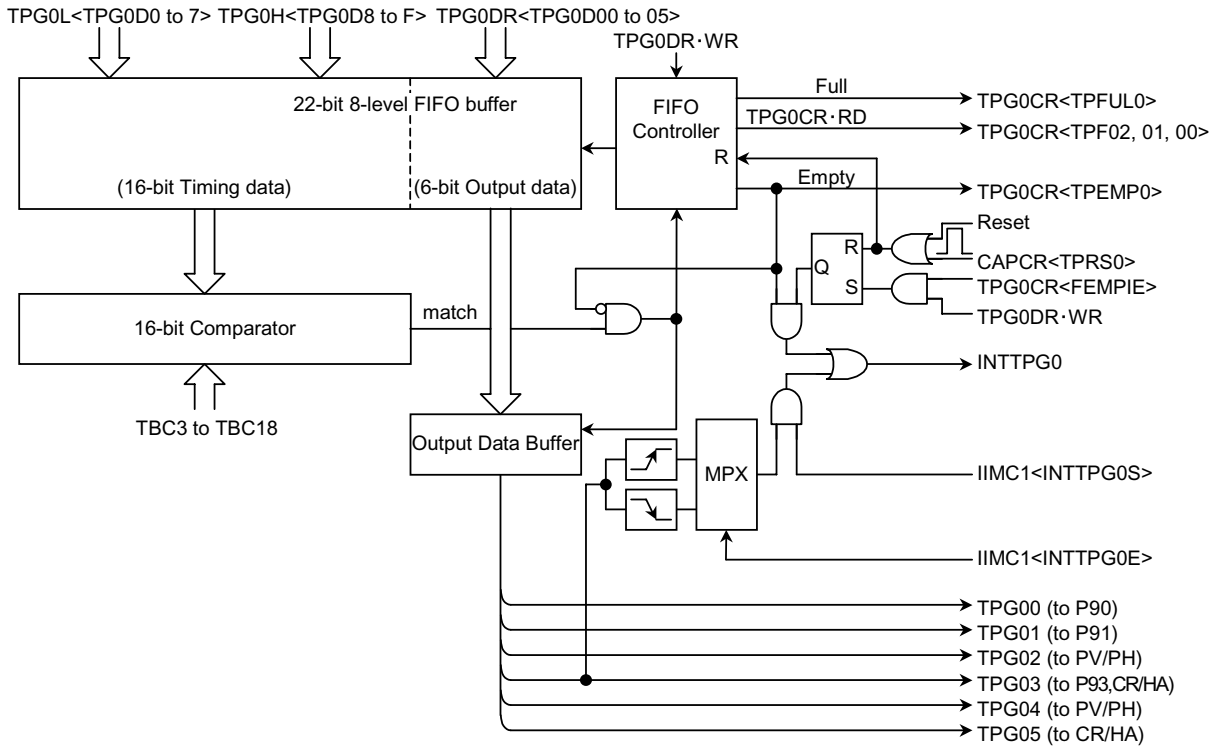


Figure 3.8.1 Composition of timing pulse generator 0 (TPG0)

(2) Operation

a. 22-bit 8-stage FIFO buffer

This is a 22-bit data register which is composed of 16-bit timing data and 6-bit output data. As this register has a 8-stage FIFO structure, the first written timing data and output data are transferred first to the comparator and output data register. Set the data to the lower timing data register (TPG0L), the higher timing data register (TPG0H) and the output data register (TPG0DR) in this order. The FIFO address is incremented by writing of TPG0DR. 6-bit output data is transferred to the output data buffer when 16-bit timing data matches the value of TBC3 to TBC18. And they become the TPG00 to TPG05.

b. 16-bit comparator

When the set data of the TPG0L and TPG0H matches the value of TBC3 to TBC18, the comparator outputs a match signal. The value of TPG0DR is transferred to output data buffer and the FIFO address is incremented by the match signal.

c. Output data buffer

The data set in the output data register (TPG0DR) is latched by the match signal from the 16-bit comparator, and TPG00 to TPG05 outputs are changed. When resetting, this buffer is cleared to 0 and TPG00 to TPG05 outputs become 0.

d. FIFO control circuit

The FIFO control circuit controls the 22-bit 8-stage FIFO buffer and has a status flag to monitor the FIFO address.

The current number of retained data can be verified by reading out the FIFO status flags <TPF02, TPF01, TPF00> of the TPG0 control register (TPG0CR). When the value of the FIFO status flag is 000, the FIFO empty flag<TPEMP0> is set to 1 in case the retained data is nothing. While <TPEMP0> is 1, transferring the output data to output data buffer is disabled. When the value of the FIFO status flag is 000, the FIFO full flag <TPFUL0> is set to 1 in case the retained data are 8 words. While <TPFUL0> is 1, writing a data to the FIFO buffer is disabled. The FIFO status flags updates the status each time the match signal is outputted from the comparator. The contents of the FIFO status flags is cleared to 000 by resetting. In addition, the FIFO address can be cleared directly by writing 1 to <TPRS0> of the capture control register (CAPCR).

e. Timing pulse generator 0 interrupt (INTTPG0)

When the contents of the FIFO buffer becomes empty, INTTPG0 (empty) interrupt to request the writing of the next data is generated. INTTPG0 (empty) interrupt request can be controlled by TPG0CR <FEMPIE> and CAPCR <TPRS0>. When TPG0CR <FEMPIE> is 1, INTTPG0 (empty) interrupt request is enabled by writing of TPG0 output data register (TPG0DR). And by writing 1 to CAPCR <TPRS0>, it can be disabled (the FIFO address is also cleared).

In addition, INTTPG0 (TPG03) interrupt request can be generated at the rising or falling edge of TPG03. Either rising or falling edge of TPG03 can be selected by <INTTPG0E> of Interrupt Input Mode Control Register (IIMC1). To enable or disable INTTPG0 (TPG03) interrupt request can be selected using IIMC1 <INTTPG0S>.

INTTPG0 interrupt request is generated through the logical-OR with INTTPG0 (empty) interrupt request and INTTPG0 (TPG03) interrupt request.

(3) Control Register

TPG0 Control Register

TPG0CR	7	6	5	4	3	2	1	0	
(0036H)	0		FEMPIE	TPFUL0	TPEMP0	TPF02	TPF01	TPF00	(Initial Value: 0*00 1000)

FEMPIE	Enable INTTPG0 FIFO interrupt	0: Disable 1: Enable	write only
TPFUL0	TPG0 FIFO full flag	0: – 1: FIFO full	read only
TPEMP0	TPG0 FIFO empty flag	0: – 1: FIFO empty	
TPF02 TPF01 TPF00	TPG0 FIFO status flag	000: Empty or Full 001: Retained data is 1 word 010: Retained data are 2 words 011: Retained data are 3 words 100: Retained data are 4 words 101: Retained data are 5 words 110: Retained data are 6 words 111: Retained data are 7 words	

Note 1: The bit 7 of TPG0CR should be written 0.

Note 2: Prohibit read-modify-write.

TPG0 Timing Data Register – Low order

TPG0L	7	6	5	4	3	2	1	0	
(0037H)	TPG0D7 (TBC10)	TPG0D6 (TBC9)	TPG0D5 (TBC8)	TPG0D4 (TBC7)	TPG0D3 (TBC6)	TPG0D2 (TBC5)	TPG0D1 (TBC4)	TPG0D0 (TBC3)	(Initial Value: **** ****) Write only

Prohibit read-modify-write.

TPG0 Timing Data Register – High order

TPG0H	7	6	5	4	3	2	1	0	
(0038H)	TPG0DF (TBC18)	TPG0DE (TBC17)	TPG0DD (TBC16)	TPG0DC (TBC15)	TPG0DB (TBC14)	TPG0DA (TBC13)	TPG0D9 (TBC12)	TPG0D8 (TBC11)	(Initial Value: **** ****) Write only

Prohibit read-modify-write.

TPG0 Output Data Register

TPG0DR (0039H)	7	6	5	4	3	2	1	0	
			TPGD05 (TPG05)	TPGD04 (TPG04)	TPGD03 (TPG03)	TPGD02 (TPG02)	TPGD01 (TPG01)	TPGD00 (TPG00)	(Initial Value: **** ****) Write only

Prohibit read-modify-write.

Capture Control Register

CAPCR (0052H)	7	6	5	4	3	2	1	0	
	CAP2T (CFG)	CAP1T (DFG)	CAPCL	VISFRS	VASFRS	TPRS0	CFGCL	CAFRS	(Initial Value: 0000 0000)

TPRS0	TPG0 FIFO counter clear	0: – 1: Clear (One-shot)	R/W

Note 1: TPRS0 should be set to 1 before setting STOP mode.

Note 2: Prohibit read-modify-write.

Interrupy Input Mode Control Register 1

IIMC1 (005FH)	7	6	5	4	3	2	1	0	
	I4EG	I3EG	I2EG	I1EG	I0EG		INTTPG0E	INTTPG0S	(Initial Value: 0000 0*00)

INTTPG0E	INTTPG0 (TPG03) edge selection	0: Rising edge 1: Falling edge	R/W
INTTPG0S	INTTPG0 source selection	0: FIFO empty 1: FIFO empty or TPG03	

Prohibit read-modify-write.

Figure 3.8.2 Registers for TPG0

(4) Outputs of timing pulse generator 0

a. TPG00

TPG00 outputs from TPG00 (P90) pin

b. TPG01

TPG01 can be used as AFF (Audio-head switching) signal. It outputs from TPG01 (P91) pin. It controls output of Video/Audio head switching control signal (VASWP).

c. TPG02

TPG02 controls the pseudo synchronizing signal output (PV/PH).

d. TPG03

TPG03 can be used as DFF (Video-head switching) signal. It outputs from TPG03 (P93) pin. It controls Head Amplifier (HA) /Color Rotary (CR) output, Video/Audio-head switching control signal (VASWP) output, and Timing pulse output (TP0, TP1).

e. TPG04

TPG04 controls the pseudo synchronizing signal output (PV/PH).

f. TPG05

TPG05 controls the Head Amplifier/Color Rotary (HA/CR) output.

3.8.2 Timing Pulse Generator 1 (TPG1)

(1) Block diagram

TPG1 is composed of 20-bit data register (16-bit timing data + 4-bit output data), 16-bit comparator and 4-bit output data buffer.

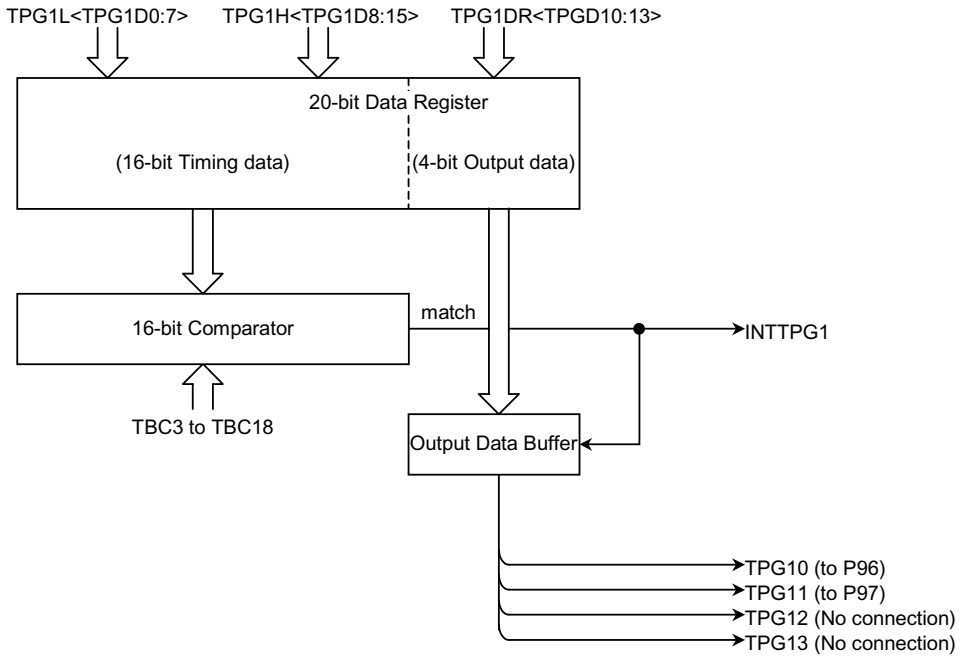


Figure 3.8.3 Composition of timing pulse generator 1 (TPG1)

(2) Operation

a. 20-bit data register

This is a 20-bit data register which is composed of 16-bit timing data and 4-bit output data. Set the data to the lower timing data register (TPG1L), higher timing data register (TPG1H), and the output data register (TPG0DR) in this order. 4-bit output data is transferred to the output data buffer when 16-bit timing data matches the value of TBC3 to TBC18. And they become the TPG10 to TPG13.

b. 16-bit comparator

When the set data of the TPG1L and TPG1H matches the value of TBC3 to TBC18, the comparator outputs a match signal. The data of TPG1DR is transferred to output data buffer and INTTPG1 interrupt request is generated by the match signal.

c. Output data buffer

The data set in the output data register (TPG1DR) is latched by the match signal from the 16-bit comparator, and TPG10 to TPG13 are outputted. By resetting, this buffer is cleared to 0 and TPG10 to TPG13 output become 0.

(3) Control register

TPG1 Timing Data Register – Low order

TPG1L	7	6	5	4	3	2	1	0	
(003AH)	TPG1D7 (TBC10)	TPG1D6 (TBC9)	TPG1D5 (TBC8)	TPG1D4 (TBC7)	TPG1D3 (TBC6)	TPG1D2 (TBC5)	TPG1D1 (TBC4)	TPG1D0 (TBC3)	(Initial Value: 0000 0000) Write only

Prohibit read-modify-write.

TPG1 Timing Data Register – High order

TPG1H	7	6	5	4	3	2	1	0	
(003BH)	TPG1DF (TBC18)	TPG1DE (TBC17)	TPG1DD (TBC16)	TPG1DC (TBC15)	TPG1DB (TBC14)	TPG1DA (TBC13)	TPG1D9 (TBC12)	TPG1D8 (TBC11)	(Initial Value: 0000 0000) Write only

Prohibit read-modify-write.

TPG1 Output Data Register

TPG1DR	7	6	5	4	3	2	1	0	
(003CH)					TPGD13 (TPG13)	TPGD12 (TPG12)	TPGD11 (TPG11)	TPGD10 (TPG10)	(Initial Value: **** 0000) Write only

Prohibit read-modify-write.

Figure 3.8.4 Registers for TPG1

(4) Output of timing pulse generator 1

a. TPG10

TPG10 outputs from TPG10 (P96) pin.

(Refer to 3.5.8 Port 9)

b. TPG11

TPG11 outputs from TPG11 (P97) pin.

(Refer to 3.5.8 Port 9)

3.8.3 Timing Pulse Output (P90, TP0, P92, TP1)

The timing pulse synchronized with DFF (cylinder head switching) signal can output from TO0 (P90) and TP1 (P92).

a. TP0

The data written in <TP0D> of Timing Pulse Control Register (TPCR) outputs at the rising edge or falling edge of TPG03. Either rising edge or falling edge of TPG03 can be selected by <VTPPO0> of head amp control register (HACR). Please refer to 3.5.8 port9 (1) P90/TP0/TPG00 section.

b. TP1

The data written in <TP1D> of Timing Pulse Control Register (TPCR) outputs at the rising edge or falling edge of TPG03. Either rising edge or falling edge of TPG03 can be selected by <VTPPO1> of head amp control register. Please refer to 3.5.8 Port9 (3) P92/TP1 section.

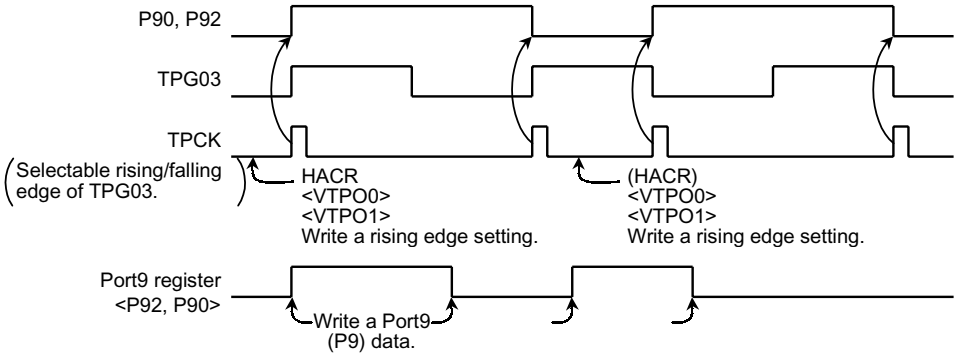


Figure 3.8.5 Timing Pulse output

3.9 Pulse Width Modulation Output (PWM)

TMP93CF76/CF77/CW76/CU76/CT76 have 3 channels of the pulse width modulation output with 14-bit resolution (PWM0, PWM1, PWM2) and another 1 channel with 8-bit resolution (PWM3). PWM can be used for some applications, such as D.C. conversion for the frequency/phase error of a drum and capstan servo system, tuner control (voltage synthesizing system), etc. by attaching a low path filter outside.

3.9.1 8-bit PWM (PWM3)

(1) Block diagram

PWM3 is composed of 8-bit data register (PWMDBR), a data latch, and a comparator.

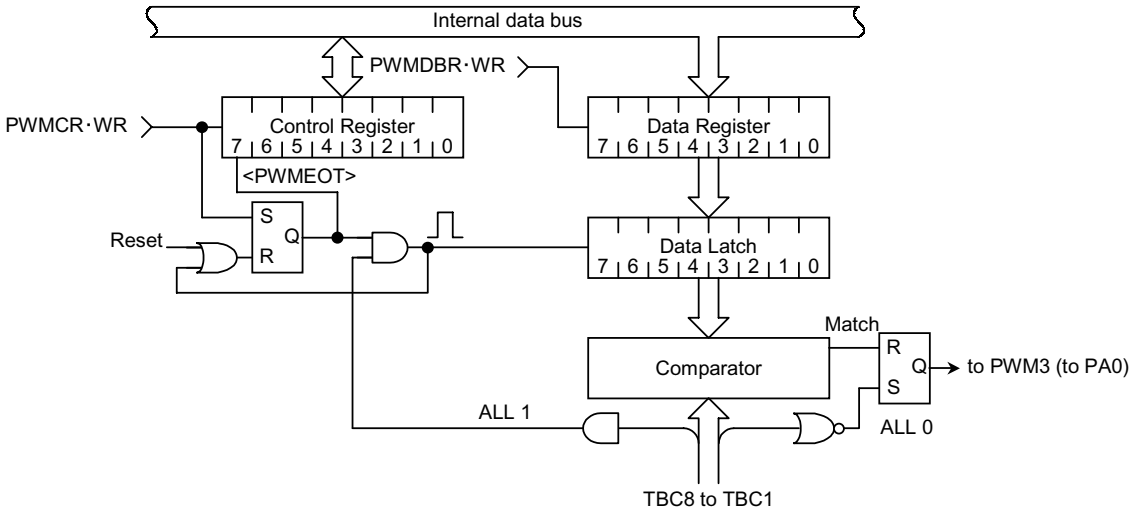


Figure 3.9.1 Composition of the 8-bit PWM output(PWM3)

(2) Control of PWM3 output

PWM3 is the pulse width modulation output with 8-bit resolution and the carrier frequency is $1/T_M = f_{SYS}/2^8$ [Hz] (32 us/31.25 kHz at 16 MHz operation). When the value of the 8-bit data latch is "n", pulse width (active "H") is n×t0 (t0 = 1/ f_{SYS} [s]).

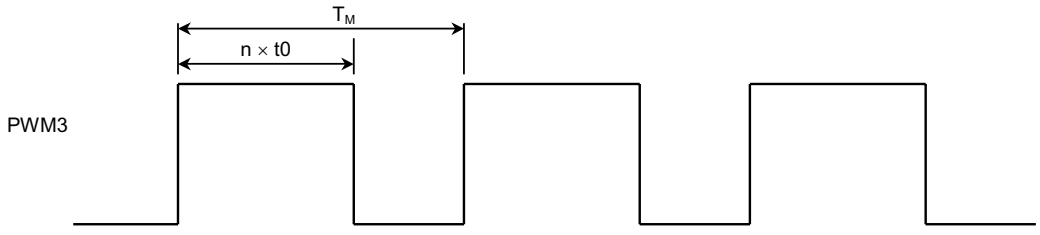


Figure 3.9.2 PWM3 output timing chart

PWM3 Data Register

PWMDBR	7	6	5	4	3	2	1	0	(Initial Value: **** ****)
(0044H)	PWM3DR7	PWM3DR6	PWM3DR5	PWM3DR4	PWM3DR3	PWM3DR2	PWM3DR1	PWM3DR0	Write only

Prohibit read-modify-write.

PWM3 Control Register

PWMCR	7	6	5	4	3	2	1	0	
(0045H)	PWMEOT				PWMC3	PWMC2	PWMC1	PWMC0	(Initial Value: 0*** 0000)

PWMEOT	PWM3 status flag	0: no inhibition 1: busy	Read only
PWMC3 to PWMC0	PWM3 data transfer request	write 0000	Write only

Prohibit read-modify-write.

Figure 3.9.3 Registers for the 8-bit PWM

PWM3 output is controlled by the data transmission to the data latch. When PWM3 status flag (PWMCR<PWMEOT> is 0, and the data can be written in PWMDBR.

By writing 0000 in PWMCR <PWMC3:0>, a data transmission request from PWMDBR to the data latch occurs, and the output data is transmitted at the timing that TBC8 to TBC1 of Time Base Counter (TBC) becomes "FFH", and the output switches.

Note: When PWMCR <PWMEOT> is 1, do not write the data in PWMDBR.

3.9.2 14-Bit PWM(PWM0 to PWM2)

(1) Block diagram

PWM0, PWM1 and PWM2 are composed of 14-bit data registers (PWM0DRL/PWM0DRH, PWM1DRL/PWM1DRH, PWM2DRL/PWM2DRH), data latches and comparators.

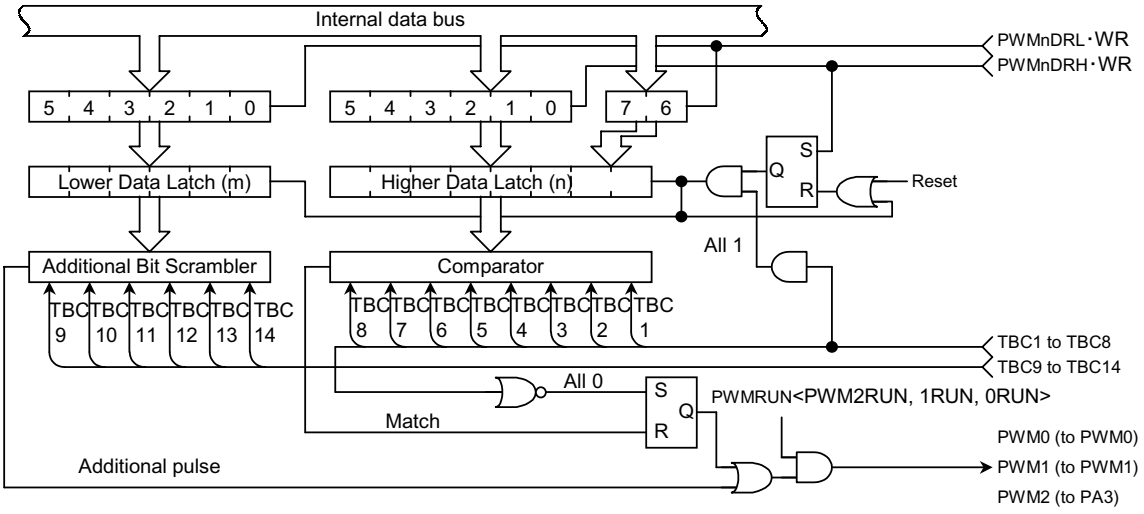


Figure 3.9.4 Composition of the 14-bit PWM output (PWM0 to PWM2)

(2) Control of PWM0 to PWM2 output

PWM0 to PWM2 are the pulse width modulation output with 14-bit resolution and the one cycle time $T_M = 2^{14}/f_{SYS}$ [s] (2.048ms at 16 MHz operation). The carrier frequency $1/T_S = 64/T_M$ [Hz] (32 μs/31.25 kHz at 16 MHz operation). The data registers are assigned as PWM0DRL/PWM0DRH, PWM1DRL/PWM1DRH, PWM2DRL/PWM2DRH. Write the 8-bits data to PWMnDRL first, and then write the 6-bits data to PWMnDRH. After writing the data to PWMnDRH, Lower Data Latch (m) and Higher Data Latch (n) latch the data written in PWMnDRL and PWMnDRH at the next T_S cycle. When the value of the higher data latch is "n" and the value of the lower data latch is "m", pulse width (active "H") of T_S is n × t0 ($t0 = 1/f_{SYS}$) [s], and the pulse with t0 is added at the "m" points into 64 T_S cycle. The PWM output is enabled when the PWM start register (PWMRUN)<PWM0RUN, PWM1RUN, PWM2RUN> is set to 1.

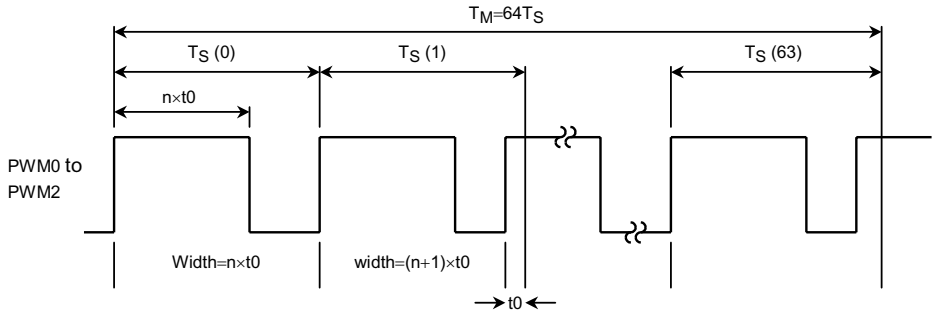


Figure 3.9.5 Wave form of the 14-bit PWM output

PWM Start Register

PWMRUN (003DH)

7	6	5	4	3	2	1	0
					PWM2RUN	PWM1RUN	PWM0RUN

(Initial Value: **** *000)

PWM2RUN	PWM2 start/stop	0: Stop 1: Start	R/W
PWM1RUN	PWM1 start/stop	0: Stop 1: Start	
PWM0RUN	PWM0 start/stop	0: Stop 1: Start	

PWM0 Register – Low order

PWM0DRL (003EH)

7	6	5	4	3	2	1	0
PWM0D7	PWM0D6	PWM0D5	PWM0D4	PWM0D3	PWM0D2	PWM0D1	PWM0D0

(Initial Value: **** ****) Write only

Prohibit read-modify-write.

PWM0 Register – High order

PWM0DRH (003FH)

7	6	5	4	3	2	1	0
		PWM0DD	PWM0DC	PWM0DB	PWM0DA	PWM0D9	PWM0D8

(Initial Value: **** ****) Write only

Prohibit read-modify-write.

PWM1 Register – Low order

PWM1DRL (0040H)

7	6	5	4	3	2	1	0
PWM1D7	PWM1D6	PWM1D5	PWM1D4	PWM1D3	PWM1D2	PWM1D1	PWM1D0

(Initial Value: **** ****) Write only

Prohibit read-modify-write.

PWM1 Register – High order

PWM1DRH (0041H)

7	6	5	4	3	2	1	0
		PWM1DD	PWM1DC	PWM1DB	PWM1DA	PWM1D9	PWM1D8

(Initial Value: **** ****) Write only

Prohibit read-modify-write.

PWM2 Register – Low order

PWM2DRL (0042H)

7	6	5	4	3	2	1	0
PWM2D7	PWM2D6	PWM2D5	PWM2D4	PWM2D3	PWM2D2	PWM2D1	PWM2D0

(Initial Value: **** ****) Write only

Prohibit read-modify-write.

PWM2 Register – High order

PWM2DRH (0043H)

7	6	5	4	3	2	1	0
		PWM2DD	PWM2DC	PWM2DB	PWM2DA	PWM2D9	PWM2D8

(Initial Value: **** ****) Write only

Prohibit read-modify-write.

Open-drain Output Control Register 3

ODCR3 (0021H)

7	6	5	4	3	2	1	0
			PWMOD1 (PWM1)	PWMOD0 (PWM0)			PODA3 (Port A3)

(Initial Value: ***0 0**0)

PWMOD1	PWM1 Open-drain control	0: Push-pull Output 1: Open-drain Output	write only
PWMOD0	PWM0 Open-drain control	0: Push-pull Output 1: Open-drain Output	
PODA3	PA3/PWM2 Open-drain control	0: Push-pull Output 1: Open-drain Output	

Prohibit read-modify-write.

Figure 3.9.6 Registers for 14-bit PWM

3.10 Sync Signal Separator (CSYNC)

The Sync Signal Separator (CSYNC) separates Vertical Synchronizing signal (V.sync) from composite synchronizing signal (C.sync).

3.10.1 Block Diagram

The Sync Signal Separator is composed of Synchronizing signal separator and H-pulse generator.

The configuration of the Sync Signal Separator is shown in Figure 3.10.1.

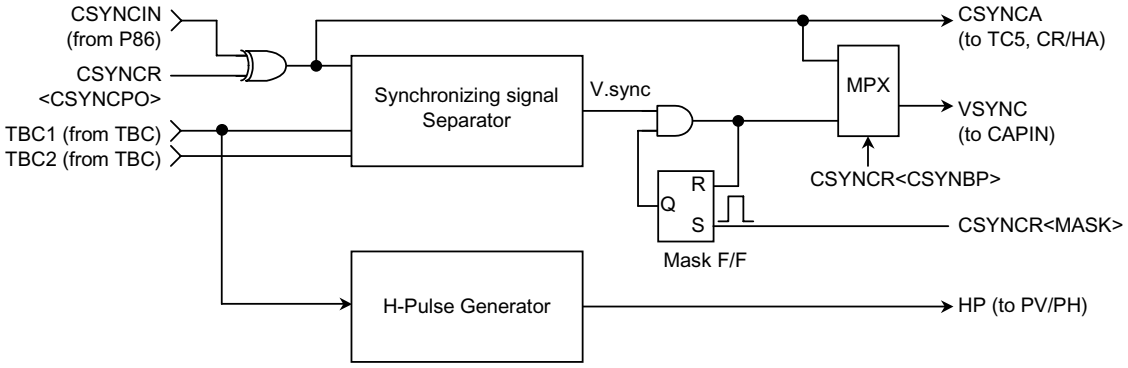


Figure 3.10.1 Composition of the sync signal separator

(1) Synchronizing signal separator

The Synchronizing Signal Separator separates V.sync signal from the C.sync inputted from CSYNCIN (P86) pin. A separated V.sync signal (VSYNC) is transferred to Capture 0 (CAP0) via Capture input control circuit (CAPIN). And it is used as a reference signal in the servo processing routine.

(2) H-Pulse Generator

The H-pulse generator generates a serrated-pulse (HP signal). The HP signal is transferred to the Pseudo-sync signal output circuit (PV/PH), and it is superimposed on the pseudo-V.sync signal as a serrated-pulse.

(Figure 3.11.1 Pseudo-sync signal output circuit.)

3.10.2 Control Registers

CSYNC Control Register

CSYNCR	7	6	5	4	3	2	1	0	
(0057H)			DPGST	CSYNCPO	SEPMOD	CSYNBP	0	MASK	(Initial Value: **00 00*0)

CSYNCPO	C.sync input polarity selection	0: Positive 1: Negative	R/W
SEPMOD	7-bit counter source clock selection (during counting down)	0: TBC1 1: TBC2	
CSYNBP	C.sync bypass control	0: V.sync 1: Bypass	
MASK	VSYNC (to CAPIN) mask control	0: – 1: Release masking (One-shot)	

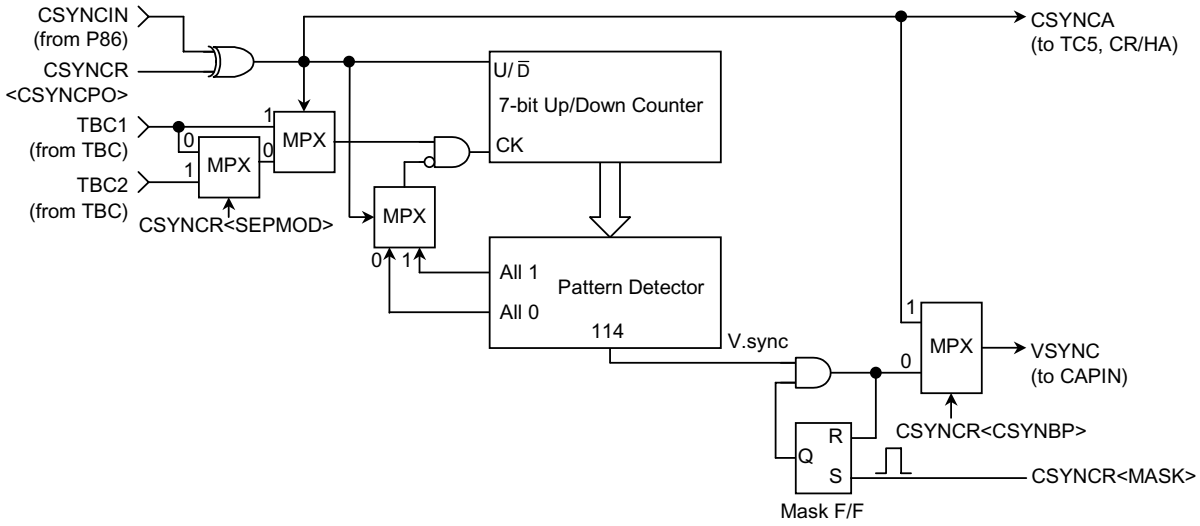
Note: The bit 1 of CSYNCR should be set to 0.

Figure 3.10.2 Register for CSYNC

3.10.3 Synchronizing signal Separator

The synchronizing signal separator separtes the vertical synchronizing signal (V.sync) from the composite synchronizing signal inputted from CSYNCIN (P86) pin. The synchronizing signal separator is composed of a 7-bit up/down counter and a pattern detector (comparison circuit).

The 7-bit up/down counter counts TBC1 ($2/f_{SYS}$) or TBC2 ($2^2/f_{SYS}$) output from Time Base Counter (TBC). And its direction for counting is controlled by input polarity of CSYNCIN pin (when CSYNCA is 1, the counter is counting up, when CSYNCA is 0, the counter is counting down). The source clock for counting up is TBC1 (0.25 μs: fc = 16 MHz). The source clock for counting down is selected from either TBC1 or TBC2 (0.5 μs: fc = 16 MHz) by CSYNCR <SEPMOD>. The input polarity of CSYNCIN pin (CSYNCA signal) is selected by setting CSYNCR<CSYNCPO> and it controls the direction for counting. In case that CSYNCA is 1 and the counter becomes all 1, the counter stops. Also in case that CSYNCA is 0 and the counter becomes all 0 the counter stops as well. When CSYNCR <CSYNBP> is set to 1, CSYNCA instead of V.sync is inputted to capture input control circuit (CAPIN).



Vertical synchronizing signal separation

When the pattern detector (comparison circuit) detects "114 (72H)" (TBC1 = 250 [ns] at fc = 16 [MHz]. Therefore, threshold is 250 [ns] × 114 = 28.5 [μs]), it outputs the V.sync signal. V.sync signal is inputted to capture input control circuit (CAPIN) and resets a flip-flop (Mask F/F) for masking. The flip-flop is reset once, the following V.sync signals are not accepted until masking is released. The flip-flop is released from masking when CSYNCR<MASK> is set to 1. Timing chart of vertical synchronizing signal separation is show in Figure 3.10.3.

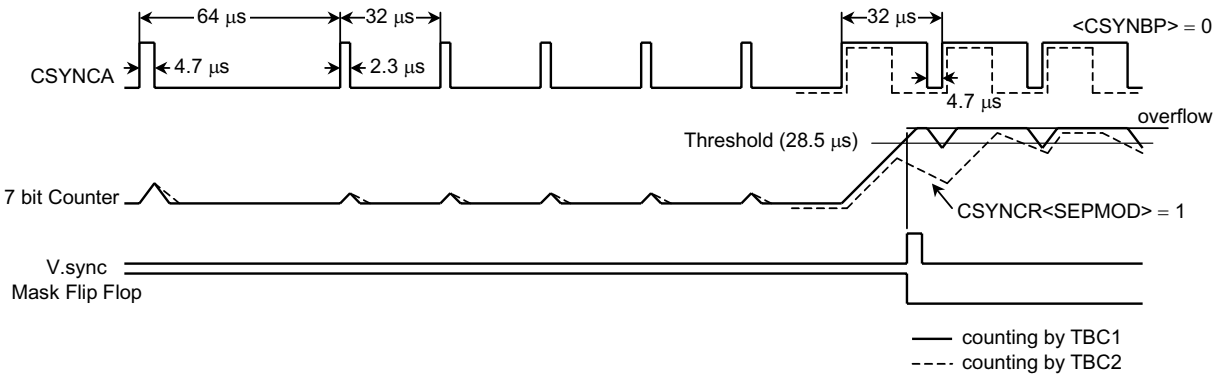


Figure 3.10.3 Timing Chart for Vertical synchronizing signal separation

3.10.4 H-Pulse Generator

H-Pulse generator generates a serrated pulse inserted into V.sync signal. This pulse (HP signal) is transferred to Pseudo-sync signal output circuit (PV/PH), and it can be mixed into pseudo-V.sync signal. Configuration of the H-Pulse generator is shown in Figure 3.10.4.

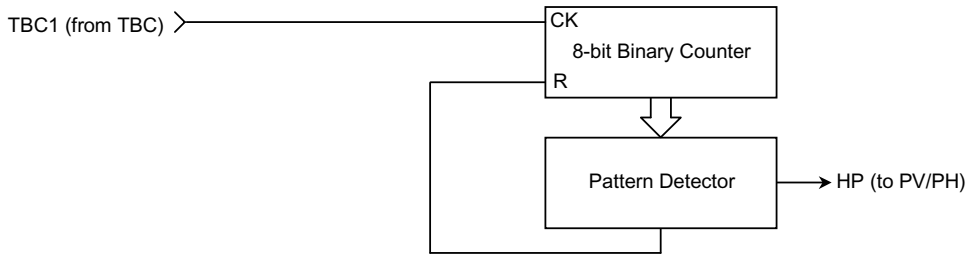


Figure 3.10.4 H-Pulse generator

H.Pulse Generator generates a serrated pulse (HP signal) to be mixed into pseudo-V.sync signal. The timing to mix HP signal into pseudo-V.sync signal is controlled by TPG02 from the timing pulse generator 0 (TPG0) (Refer to section 3.11 Pseudo-sync signal output circuit). HP signal is not synchronized with Composite sync. signal input.

The wave form of the HP signal is shown in Figure 3.10.5.

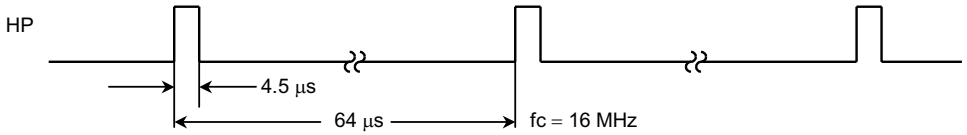


Figure 3.10.5 Wave form of HP signal output

3.11 Pseudo-sync Signal Output Circuit (PV/PH)

The TMP93CF76/CF77/CW76/CU76/CT76 have a function to output a pseudo-sync signal (PV) in place of the playback sync signal during special effect reproduction. The PV output is controlled by the timing pulse generator 0 (TPG0)'s TPG02 and TPG04 outputs and the PV control register (PVCR).

3.11.1 Block Diagram

The pseudo-sync signal output circuit consists of a sync signal mixing circuit and a 3-level output circuit. The sync signal mixing circuit is used to superimpose the serrated pulse (HP) that is generated by the H pulse generator of the sync signal separation circuit (CSYNC) on a pseudo-V.sync signal.

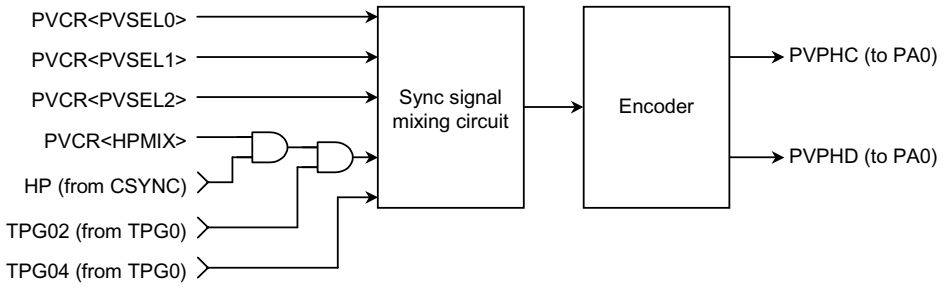


Figure 3.11.1 Composition of the pseudo-sync signal output circuit

3.11.2 Control Register

PV/PH Control Register

PVCR (0058H)	7	6	5	4	3	2	1	0
					HPMIX	PVSEL2	PVSEL1	PVSEL0

(Initial Value: **** 0000)

HPMIX	Insert HP to pseudo-V.sync	0: Disable 1: Enable	R/W
PVSEL2 to PVSEL0	PV/PH output format selection	Select output format 0H to 7H	

Figure 3.11.2 Register for PV/PH

3.11.3 Control of Pseudo-V.sync. Signal Output

Output of the pseudo-sync signal (PVPH) is controlled by TPG02 and TPG04 outputs of Timing Pulse Generator 0 (TPG0) and PV control register (PVCR).

The pseudo-V.sync. signal is patterned by the TPG0, and it is outputted while TPG04 is high-level. The TPG02 output is used to set a period at which time HP signal is inserted (HP signal is inserted into the pseudo-V.sync. signal while TPG02 is high-level). The serration (HP signal) is generated by the H.Pulse generator of the sync signal separation circuit (CSYNC). The HP signal is inserted into pseudo V.sync by setting the PVCR <HPMIX> to 1.

The pseudo-sync signal has six output formats which can be selected by PVCR <PVSEL2:0>. Figure 3.11.3 shows the output formats of the pseudo-V.sync signal.

<PVSEL 2:0>			
2	1	0	TPG02 TPG04 (<HPMIX> = 1)
0	0	0	HP Vcc level High-Z output Vss level
0	0	1	HP
0	1	0	HP
0	1	1	HP
1	*	0	HP
1	*	1	HP

Note: *; Don't care

Figure 3.11.3 Pseudo-V.sync output format

3.12 VISS/VASS Detector (VIVA)

VISS/VASS detector is a control circuit specific to VISS (Video Index Search System)/VASS (Video Address Search System) of VHS. Duty of CTL signal recorded on the control track can be discriminated and VISS code can be detected. Also the address code of VASS can be read out.

3.12.1 Block Diagram

VISS/VASS detector is composed of a CTL duty discrimination circuit, a VISS detection circuit, a VASS head detection circuit and a 16-bit address code register.

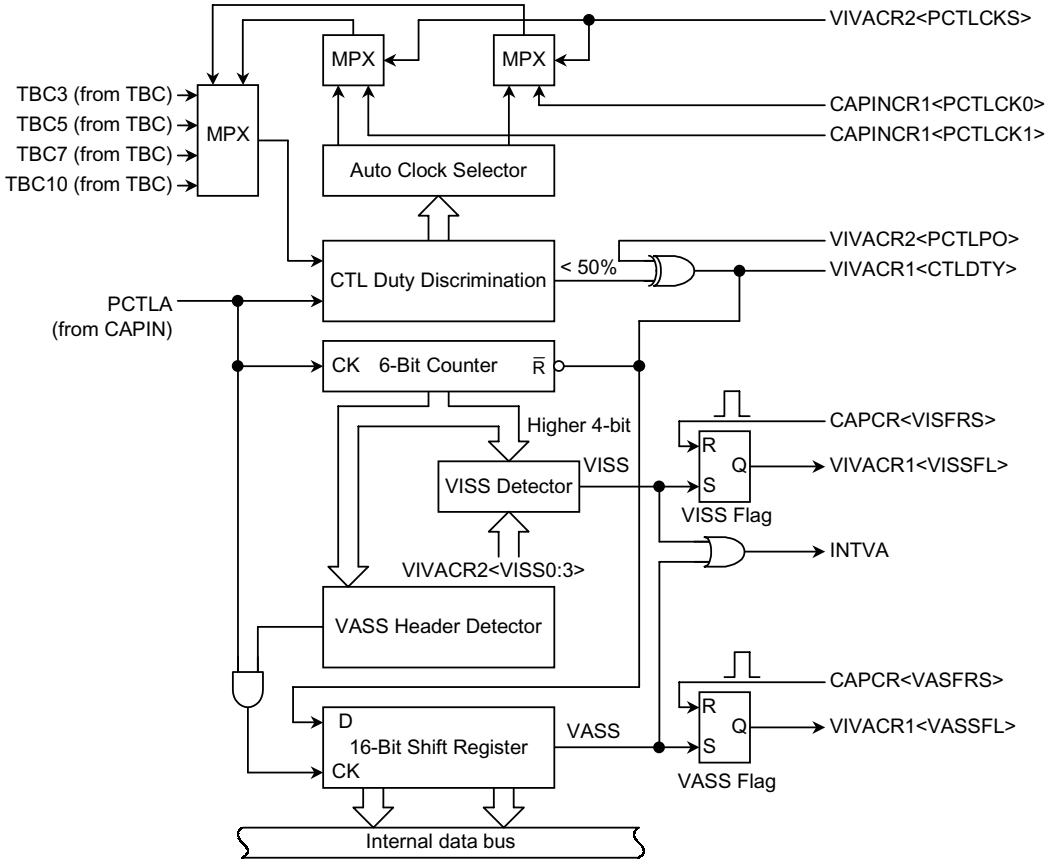


Figure 3.12.1 Composition of the VISS/VASS detector

3.12.2 Control Registers

VISS/VASS Control Register 1

VIVACR1	7	6	5	4	3	2	1	0	
(0054H)	0					CTLDTY	VISSFL	VASSFL	(Initial Value: 0*** *100)

CTLDTY	CLT duty detect monitor flag	0: CTL duty ≥ 50% (when<PCTLP0> = 0) 1: CTL duty < 50% (when<PCTLP0> = 0)	read only
VISSFL	VISS detect flag	0: – 1: VISS detected	
VASSFL	VASS detect flag	0: – 1: VASS detected	

Note: The bit 7 of VIVACR1 should be cleared to 0.

VISS/VASS Control Register 2

VIVACR2	7	6	5	4	3	2	1	0	
(0055H)	PCTLPO	PCTLCKS	MSK1	MSK0	VISS3	VISS2	VISS1	VISS0	(Initial Value: 0*00 0000)

PCTLPO	CTL duty discrimination polarity selection	0: Positive (CTL duty ≤ 50% when <CTLDTY> = 1) 1: Negative (CTL duty > 50% when <CTLDTY> = 1)	R/W
PCTLCKS	CTL duty discrimination sampling clock selector	0: Selected by CAPINCR1<PCTLCK0, 1> 1: Selected automatically	
VISS3 to VISS0	VISS discrimination comparison data	4-bit data “0H” to “FH” (compared with higher 4-bit data of 6-bit counter)	

Capture Input Control Register 1

CAPINCR1	7	6	5	4	3	2	1	0	
(0047H)	PCTLCK1	PCTLCK0	PCPR5	PCPR4	PCPR3	PCPR2	PCPR1	PCPR0	(Initial Value: 0000 0000)

PCTLCK1 PCTLCK0	CTL duty discrimination sampling clock selection in case <PCTCKS>= 0	00: TBC3 01: TBC5 10: TBC7 11: TBC10	R/W

Capture Control Register

CAPCR	7	6	5	4	3	2	1	0	
(0052H)	CAP2T (CFG)	CAP1T (DFG)	CAPCL	VISFRS	VASFRS	TPRS0	CFGCL	CAFRS	(Initial Value: 0000 0000)

VISFRS	Reset VISS flag	0: – 1: Reset (One-shot)	R/W
VASFRS	Reset VASS flag	0: – 1: Reset (One-shot)	

Prohibit read-modify-write.

VASS Data Register

VASSDR	7	6	5	4	3	2	1	0	
(0056H)	VASS7	VASS6	VASS5	VASS4	VASS3	VASS2	VASS1	VASS0	(Initial Value: **** ****)
	VASS15	VASS14	VASS13	VASS12	VASS11	VASS10	VASS9	VASS8	

VASS7 to VASS0	VASS data lower 8 bits	Twice reading from VASSDR. The first is lower 8-bit, the second is higher 8-bit.	read only
VASS15 to VASS8	VASS data higher 8 bits		

Figure 3.12.2 Registers for VISS/VASS

3.12.3 Control of the CTL Duty Discrimination Circuit

The clock source can be selected automatically or a command by VIVACR2 <PCTLCKS>. When VIVACR2<PCTLCKS> is 0, the clock source is selected by CAPINCR1 <PCTLCK1, 0>. When <PCTLCKS> is 1, according to the cycle of CTL signal, clock source is automatically selected by hardware (it applies to Table 3.12.1).

(1) Control of CTL duty discrimination circuit

The polarity of picture-play CTL signal inputted from CTLIN (P80) pin, which is named PCTLA signal, is selected of Capture Input Control Circuit (CAPIN) and PCTLA signal is transferred to VISS/VASS detector (VIVA). The CTL duty discrimination circuit discriminates the duty of PCTLA signal. If the duty is more than 50%, VIVACR1<CTLDTY> is cleared to 0. When it is less than 50%, <CTLDTY> is set to 1. The polarity of discrimination can be reversed by VIVACR2<PCTLPO>.

(2) Clock selection control

The clock source for CTL duty discrimination is selected by CAPINCR1<PCTLCK1, 0>.

When VIVACR2<PCTLCKS> is 0, the clock source for CTL duty discrimination is selected by CAPINCR1<PCTLKC1, 0>. When VIVACR2<PCTKCKS> is 1, it is selected automatically by hardware.

The clock source for CTL duty discrimination is selected from Table 3.12.1.

Table 3.12.1 Correspondence of the cycle of CTL signal and the clock source for duty discrimination

<PCTLCK1> <PCTLCK0>	Clock source for CTL duty discrimination (at fc = 16 MHz)	Cycle of CTL signal		
00	TBC3 (1 μs)		to	512 μs
01	TBC5 (4 μs)	512 μs	to	2048μs
10	TBC7 (16 μs)	2048 μs	to	8192 μs
11	TBC10 (128 μs)	8192 μs	to	

3.12.4 Control of VISS Detector

VISS detector is composed of a 6-bit up-counter which counts PCTLA signal, a 4-bit comparison circuit which detects VISS code, and a R/S flip-flop (VISS flag).

The output of the CTL duty discrimination circuit is inputted to a reset-input (active-low) of the 6-bit up-counter. When VIVACR2<PCTLPO> is 0, the 6-bit up-counter counts up while the output of the CTL duty discrimination circuit is high.

The higher 4-bit of the 6-bit up-counter are connected to 4-bit comparison circuit for detection of VISS code and are compared with VIVACR2<VISS3 to 0>. When the higher 4-bit of the 6-bit up-counter matches VIVACR2<VISS3 to 0>, VIVACR1<VISSFL> is set to 1 and INTVA occurs at the same time. VIVACR1<VISSFL> can be cleared to 0 by setting CAPCR<VISFRS> to 1.

The relation between the count value of the PCTLA signal and VIVACR2<VISS3 to 0> are shown in Table 3.12.2.

Clear VIVACR2<PCTLPO> to 0 when a tape runs forward, set <PCTLPO> to 1 when it runs reversed.

Table 3.12.2 Relation between the value of <VISS3> to <VISS0> and count value of the PCTLA signal

<VISS3> to <VISS0>				The count value for detecting VISS index code
3	2	1	0	
0	0	0	0	Don't use
0	0	0	1	4
0	0	1	0	8
0	0	1	1	12
0	1	0	0	16
0	1	0	1	20
0	1	1	0	24
0	1	1	1	28
1	0	0	0	32
1	0	0	1	36
1	0	1	0	40
1	0	1	1	44
1	1	0	0	48
1	1	0	1	52
1	1	1	0	56
1	1	1	1	60

3.12.5 Control of VASS Detector

VASS detector consists of a header detection circuit and address code register (16-bit shift register).

If a header detection circuit detects that the output of the CTL duty discrimination circuit is 1, 9 times continuously after it detects that the output of the CTL duty discrimination circuit is 0, a header of VASS is detected. The output of the CTL duty discrimination circuit is shifted into 16-bit shift register 16 times, as address code, following the output of the CTL duty discrimination circuit is 0 after a header of VASS. When a shift register latched all 16-bit data, VIVACR1<VASSFL> is set to 1 and INTVA occurred.

It recognizes which an interrupt is occurred by reading VIVACR1<VISSFL> and VAVACR1<VASSFL> is cleared to 0 by setting VAVACR1<VASFRS> to 1.

In order to read a 16-bit address code, a data is read from VASDR twice. The first data is read as lower 8-bit (VASS7 to 0), and the second data is read as higher 8-bit (VASS15 to 8).

Clear VIVACR<PCTLPO> to 0 when a tape operates forward, set VIVACR2<PCTLPO> to 1 when it operates backward. However, when a tape operates backward, a LSB and MSB of an address code is exchanged.

Note 1: Since an address code has 4 headers, an INTVA is occurred 4 times each an address code. But 4th data is dummy data. It is necessary that an address code should be read before beginning to shift a next address code into a shift register after INTVA is occurred.

Note 2: After a data is written to VASDR, lower 8-bit of an address code can be read from VASDR.

3.13 Remote Control Signal Input Circuit (RMTIN)

The remote control signal input circuit (RMTIN) rejects noise from remote control signal. It detects the rising edge and the falling edge from RMTIN signal (P82) without the noise. The detected rising edge signal (RMTU) and the falling edge signal (RMTD) are inputted into capture 0 (CAP0) via capture input circuit (CAPIN). The pulse width of a remote control signal can be measured by CAP0.

(1) Block diagram

The remote control signal input circuit is composed of H-level noise canceller and L-level noise canceller, which each consists of a 4-bit up-counter and a comparator.

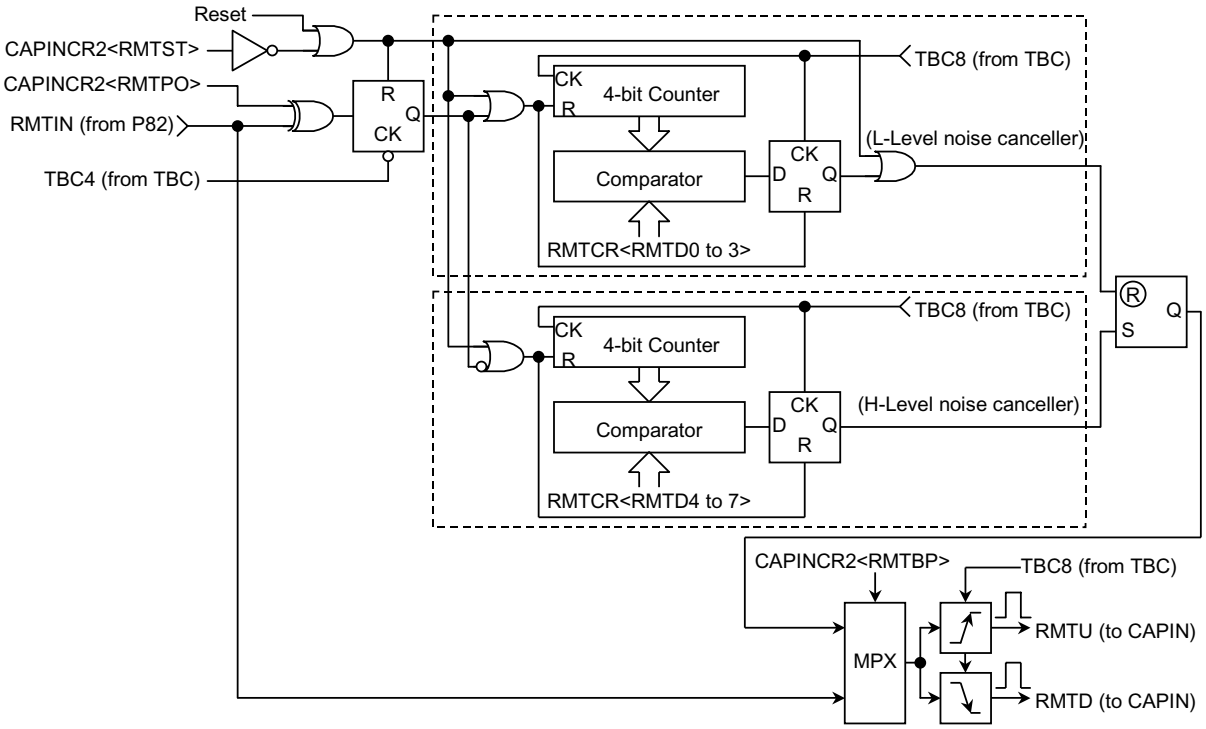


Figure 3.13.1 Composition of the remote control signal input circuit (RMTIN)

(2) Control register

Remote Control signal input Control Register

RMTCR (0053H)

7	6	5	4	3	2	1	0
RMTD7	RMTD6	RMTD5	RMTD4	RMTD3	RMTD2	RMTD1	RMTD0

(Initial Value: 0000 0000)

RMTD7 to RMTD4	Width of H noise cancellation	Setting of comparative value of 4-bit counter (H-level noise canceller)	R/W
RMTD3 to RMTD0	Width of L noise cancellation	Setting of comparative value of 4-bit counter (L-level noise canceller)	

Capture Input Control Register 2

CAPINCR2 (0048H)

7	6	5	4	3	2	1	0
0	RMTST	RMTP0	RMTBP	CFGMCP	DPCP2	DPCP1	DPCP0

(Initial Value: 0000 0000)

RMTST	Start/Stop remote control signal input control	0: Stop & Counter clear 1: Start	R/W
RMTP0	Switching polarity of remote control signal input	0: Positive 1: Negative	
RMTBP	RMTIN noise canceller control	0: Active 1: Bypass	

Note: The bit 7 should be cleared to 0.

Figure 3.13.2 Register for RMTIN

(3) Operation of the remote control signal input circuit

The remote control signal input circuit starts operation by setting CAPIN2<RMTST> to 1. In advance, the input polarity of a remote control signal and noise removal width need to be set up.

a. Control of remote control signal input

By CAPIN2 <RMTPO>, the polarity of the remote control signal inputted from RMTIN (P82) pin can be changed accordingly. The inputted remote control signal is sampled with the falling edge of TBC4 and is inputted to a noise canceller.

b. Operation of the noise canceller (in case CAPIN2<RMTPO> is 0)

"H" level noise removal width and "L" level noise removal width are set up by RMTCR <RMTD7:0> and <RMTD3:0> each. When the width of "H" level pulse or "L" level pulse of the remote control signal is less than the removal width set to RMTCR<RTMD7:4> and RMTCR<RTMD3:0>, the pulse is rejected as a noise.

i) "H" level noise canceller

While the remote control signal is high, a 4-bit counter counts up by TBC8. And while the remote control signal is low, the 4-bit counter is reset. When the count of the counter matches the value of RMTCR<RMTD7:4>, a flip-flop is set to 1 as a rising edge of remote control signal.

ii) "L" level noise canceller

While the remote control signal is low, a 4-bit counter counts up by TBC8. And while the remote control signal is high, the 4-bit counter is reset. When the count of the counter matchs the value of RMTCR<RMTD3:0>, a flip-flop is cleared to 0 as a falling edge of remoto control signal.

iii) Measurement of remote control signal pulse width

The rising edge of the flip-flop output (RMTU) and the falling edge of the flip-flop output (RMTD) are inputted into Capture 0 (CAP0) via Capture Input Control Circuit (CAPIN). The time gap between RMTU and RMTD can be measured in INTCAP0 interrupt routine.

When RMTCR<RMTD7:4> or RMTCR<RMTD3:0> is cleared to 0, "H" or "L" level cancellation is not performed. Also when CAPINCR2<RMTBP> is set 1, it is not performed.

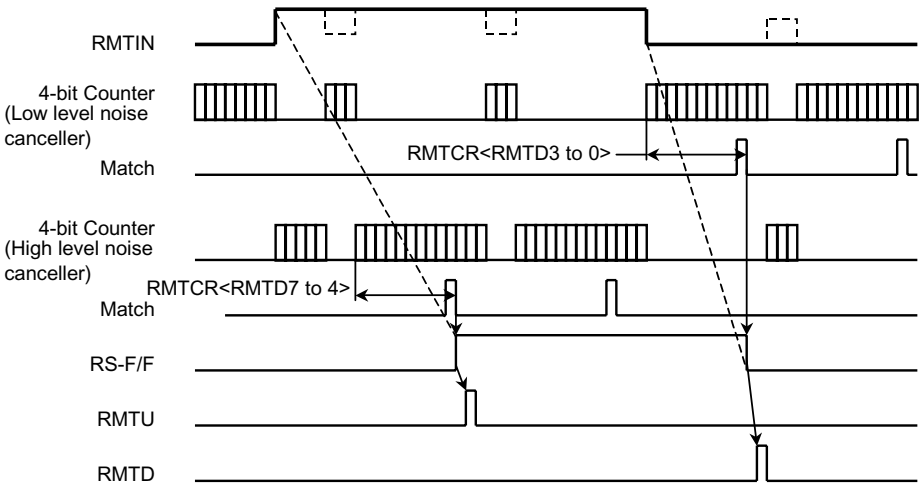


Figure 3.13.3 Timing chart of the remote control signal input circuit (CAPINCR2<RMTPO> = 0)

3.14 Head Amp Switch/Color Rotary Control Circuit (HA/CR)

TMP93CF76/CF77/CW76/CU76/CT76 have the head amp switch (HA)/color rotary (CR) control output circuit. HA output/CR output can control Video-head amplifier switching with the logical combination pattern by TPG03, TPG05 of Timing Pulse Generator 0 (TPG0) and setting value of head amp control register (HACR).

3.14.1 Block Diagram

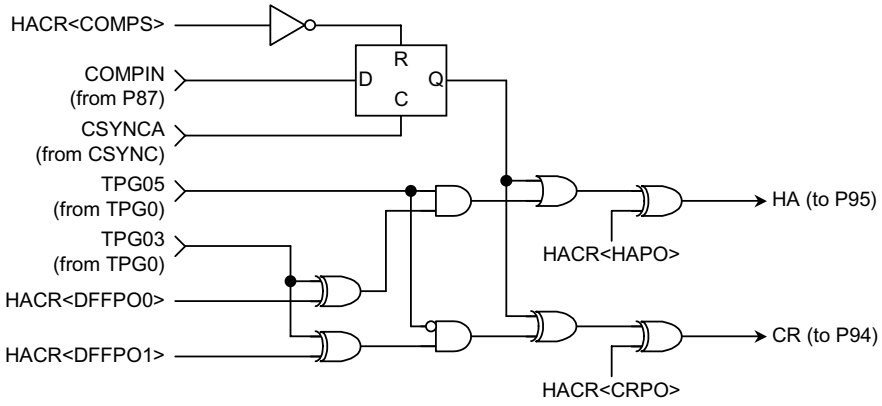


Figure 3.14.1 Composition of the head amp/color rotary control circuit

3.14.2 Control Register

Head Amp Control Register

HACR	7	6	5	4	3	2	1	0	
(008DH)	VTPPO1	VTPPO0	TPVASEL	DFFPO1	DFFPO0	COMPS	CRPO	HAPO	(Initial Value: 0000 0000)

TPVASEL	P91 output selection	0: TPG01 1: VASWP	R/W
DFFPO1	CR control TPG03 input polarity selector	0: Positive 1: Negative	
DFFPO0	HA control TPG03 input polarity selector	0: Positive 1: Negative	
COMPS	HR/CR control Enable COMPIN	0: Disable 1: Enable	
CRPO	CR control CR output polarity selector	0: Positive 1: Negative	
HAPO	HA control HA output polarity selector	0: Positive 1: Negative	

Figure 3.14.2 Register for HA/CR

(1) Logic architecture and operation mode

Controlling HA (Head Amp)/CR (Color Rotary) output is performed by TPG03 and TPG05 of Timing Pulse Generator 0 (TPG0) and Head Amp Control Register (HACR) as shown in Figure 3.14.2.

$$HA = \langle HAPO \rangle \oplus [(COMPIN \cdot \langle COMPS \rangle + (TPG05 \cdot (TPG03 \oplus \langle DFFPO0 \rangle))]$$
$$CR = \langle CRPO \rangle \oplus [(COMPIN \cdot \langle COMPS \rangle \oplus (\overline{TPG05} \cdot (TPG03 \oplus \langle DFFPO1 \rangle))]$$

Generally, for controlling a head amplifier switching, HA output and CR output are provided with three basic modes as shown below.

Table 3.14.1 HA/CR output operate mode

Mode	<COMPS>	TPG05	HA output	CR output
mode1	0	0	<HAPO>	<CRPO> ⊕ (TPG03 ⊕ <DFFPO1>)
mode2	0	1	<HAPO> ⊕ (TPG03 ⊕ <DFFPO0>)	<CRPO>
mode3	1	0	<HAPO> ⊕ COMPIN	<CRPO> ⊕ COMPIN ⊕ (TPG03 ⊕ <DFFPO1>)

In this case, TPG03 can be used as a cylinder head switching signal (DFF). The polarity of TPG03 input is selected by HACR <DFFPO1, 0>. And TPG05 can be used for switching mode 1 to 3. HACR <COMPS> controls the input of COMPIN (P87) signal (emvelop detection and camparison of FM signal of SP/EP head).

(2) Example

SP/EP mode is set by HACR <HAPO> = HACR <CRPO>. HA and CR output frequence is shown in Figure 3.14.4 in case of <DFFPO0> = <DFFPO1> (In case with an example of a Rec/Pre amplifier device to Figure 3.14.3).

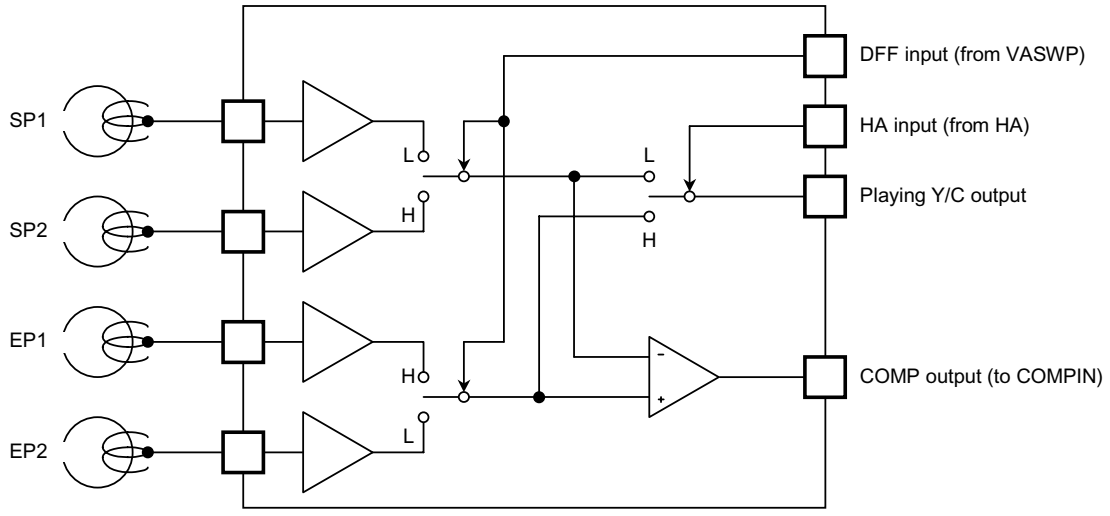


Figure 3.14.3 Example for the interface with Rec/Pre amplifier

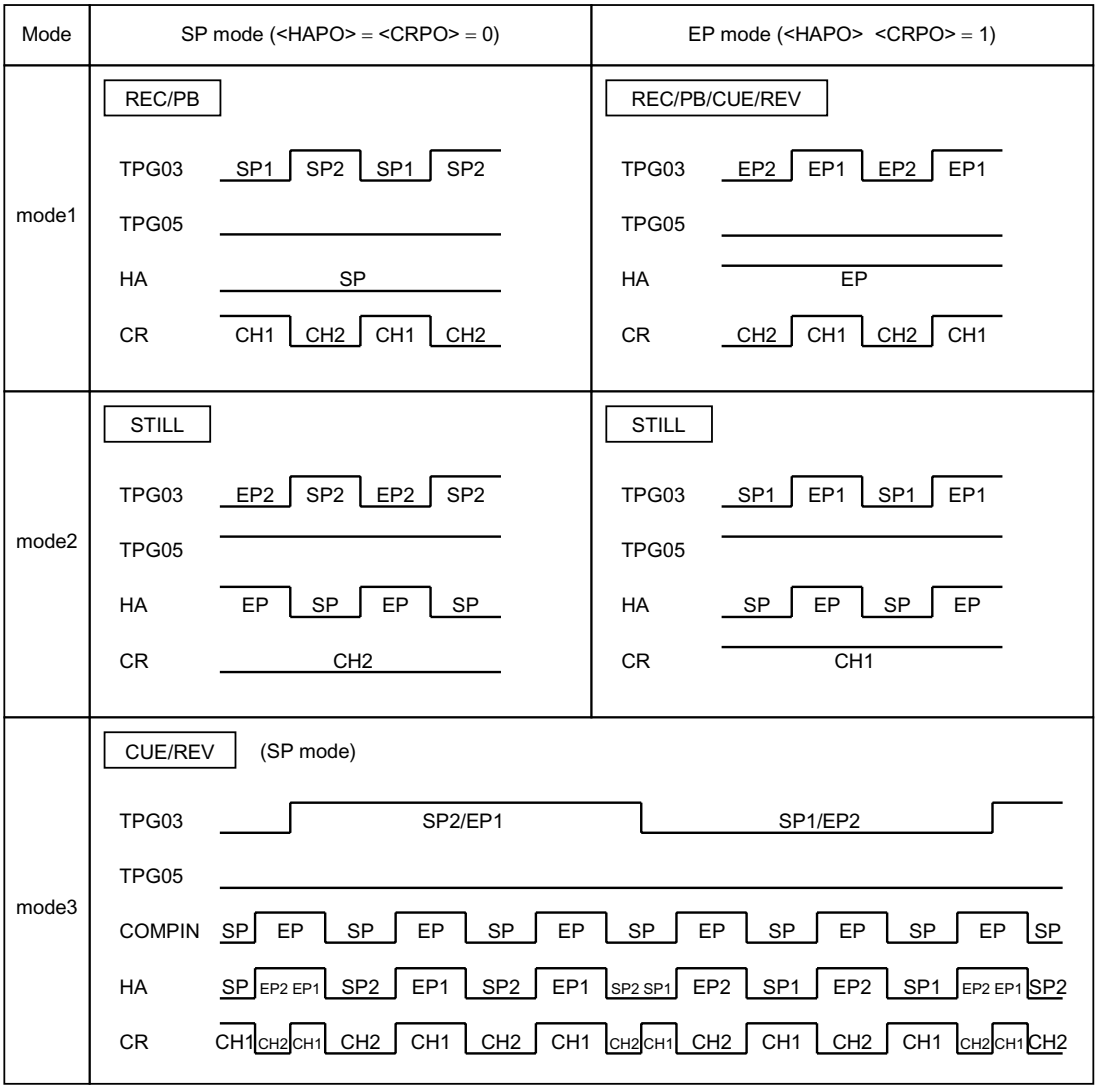


Figure 3.14.4 HA/CA output frequence

As shown in Figure 3.14.4, the control for each operation, such as REC/PB, STILL and CUE/REV, can be performed by setting the modes. Moreover, SLOW operation can be controlled by using sequentially mode 1 and 2.

3.14.3 Control of VASWP Output

TPG03 and TPG01 are used as DFF signal (cylinder head switching) and AFF signal (audio head change) for head switching control each.

DFF signal is outputted to TPG03 (P93) pin and AFF signal is outputted to TPG01 (P91) pin respectively. The signal multiplexed with these signals can also be outputted to VASWP (P91) pin.

(1) Circuit composition

The circuit construction of VASWP output is shown in Figure 3.14.5, also refer to figure 3.5.21 (P91).

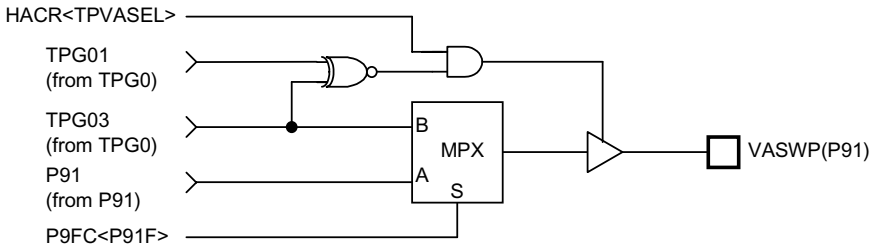


Figure 3.14.5 Composition of the VASWP circuit

(2) VASWP output

P9FC <P91F> is set to 1, and VASWP output is enabled by HACR <TPVASEL>. 3-state output maltiprexed with DFF signal (TPG03) and AFF signal (TPG01) is outputted to VASWP pin. The timing chart, an example of VASWP output is shown in Figure 3.14.6.

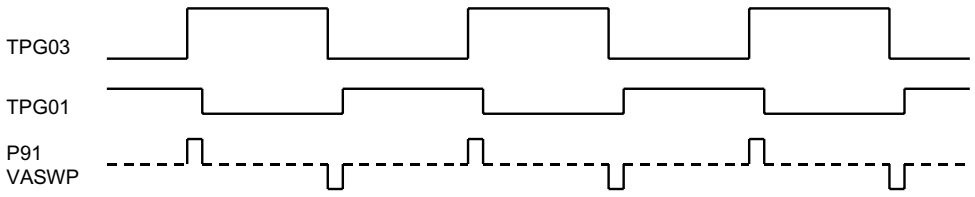


Figure 3.14.6 VASWP output timing chart

Note: When P91 terminal is used as VASWP output, set P9CR <P91C> to 0.

3.15 Serial Channels (SIO)

The TMP93CF76/CF77/CW76/CU76/CT76 have one built-in 8-bit synchronous serial channel. Serial channel (SIO) is connected to an external circuit via P52 (SCK), P51 (SO), P50 (SI).

3.15.1 Block Diagram

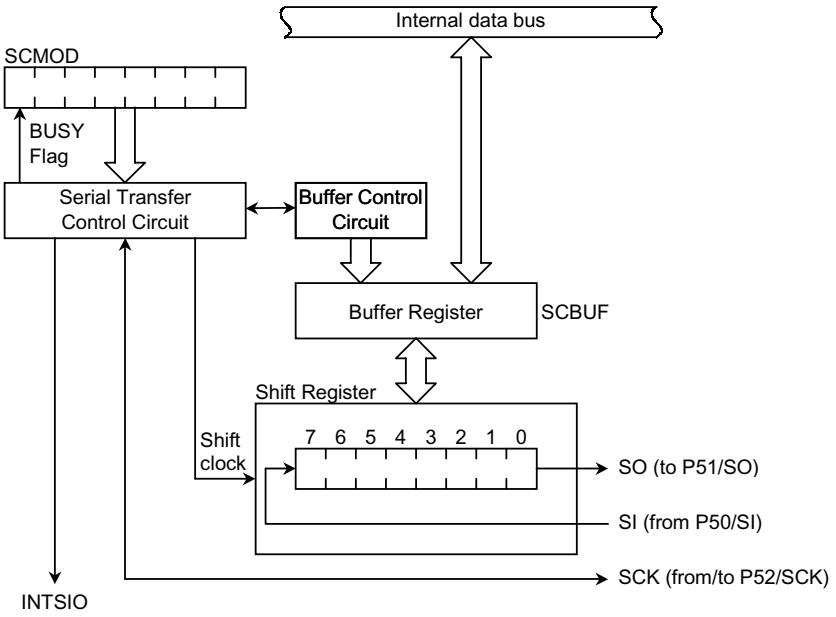


Figure 3.15.1 Configuration of the serial channel

3.15.2 Control Registers

The serial channel are controlled by serial channel control register (SCMOD) and serial channel buffer register(SCBUF). To use serial channel, set the port 5 control register to serial channel pin function.

Serial Channel Control Register

SCMOD (0067H)

7	6	5	4	3	2	1	0
FFSI	SRES	SMD1	SMD0	SIFT	CLKSI	SCKS	SIOE

(Initial Value: 1000 0000)

FFSI	Serial transfer monitor flag	0: Transfer in progress 1: Transfer stop	Read only
SRES	Serial transfer termination	0: – 1: Terminate (One-shot)	R/W
SMD1 SMD0	Serial transfer mode selection	00: Transmit mode 01: Receive mode 10: reserved 11: Transmit/receive mode	
SIFT	Serial transfer shift edge selection	0: Leading edge 1: Trailing edge	
CLKSI	Serial transfer internal clock rate selection	0: $f_{SYS}/2^3$ 1: $f_{SYS}/2^7$	
SCKS	Serial transfer clock selection	0: Internal clock 1: External clock	
SIOE	Serial transfer start	0: Stop 1: Start	

Serial Channel Buffer Register

SCBUF (0066H)

7	6	5	4	3	2	1	0
TRB7	TRB6	TRB5	TRB4	TRB3	TRB2	TRB1	TRB0

(Initial Value: **** ****)
Read/Write

Prohibit read-modify-write.

Interrupt Source Control Register

ISCR (008FH)

7	6	5	4	3	2	1	0
SELINT							

(Initial Value: 0*** ****)

SELINT	Interrupt source select	0: INT2 1: INTSIO	R/W

Note: It is necessary to select from either serial channel interrupt (INTSIO) or external interrupt 2 (INT2) by <SELINT> of interrupt source control register (ISCR) because an interrupt request flag is used both as a INTSIO and INT2.

3.15.3 Operation

(1) Shift Clock

a. Clock Source Selection

The clock of SIO can be selected from either internal clock or external clock by setting SCMOD <SCKS>.

i) Internal clock

The clock rate can be selected from either TBC3($f_{SYS}/2^3$) or TBC7($f_{SYS}/2^7$) by setting SCMOD <CLKSI>.

Figure 3.15.1 shows the maximum transfer rate using the internal clock.

The shift clock automatically stops after the end of one-frame transfer operation and waits for the next transfer operation. The SCK pin holds high-level in no transferring.

Table 3.15.1 The maximum transfer rate by internal clock

Internal Clock	Maximum Transfer Rate (at fc = 16 MHz)
TBC3 ($f_{SYS}/2^3$)	1 Mbps
TBC7 ($f_{SYS}/2^7$)	62500 bps

ii) External clock

The clock input to the SCK pin is used as the shift clock. Before starting serial transfer, set SCMOD <SCKS> to 1. To make certain shift operation, it is necessary to input more than 8/fc at both high-level and low-level of the shift clock width.

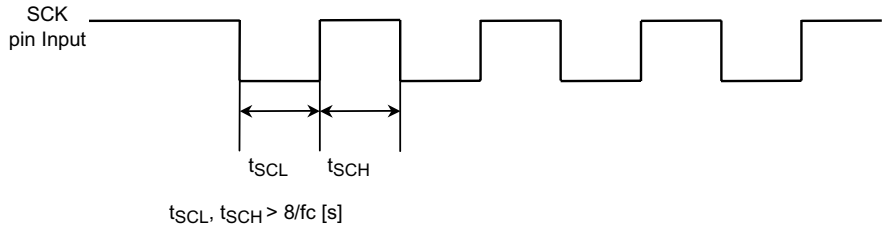


Figure 3.15.2 External clock input

b. Shift Edge Selection

The leading or trailing edge shift can be selected by setting SCMOD <SIFT> .

i) Leading edge

The serial data are shifted on the leading edge of the shift clock (falling edge of SCK pin input/output).

ii) Trailing edge

The serial data are shifted on the trailing edge of the shift clock (rising edge of SCK pin input/output).

In the transmit mode, trailing edge mode can not be operating.

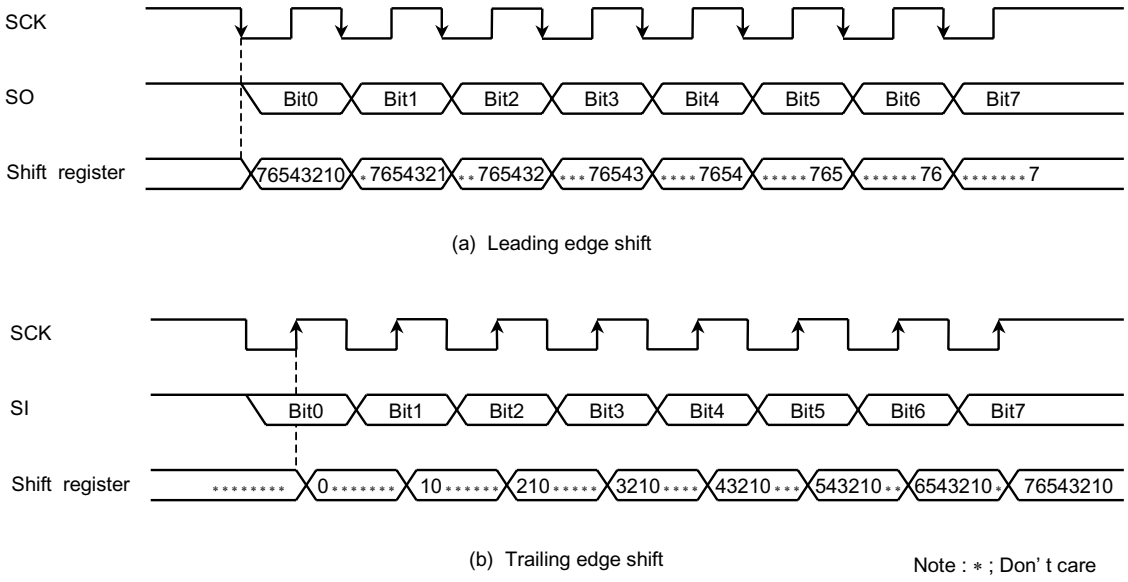


Figure 3.15.3 Shift edge

(2) Serial Operation

Three transfer mode such as transmit, receive and simultaneous transmit-receive modes for serial channel are selected by SCMOD<SMD1, 0>. After reset, SMOD<SMD1, 0> are cleared to 0, and transmit mode is selected. The following explains the operation in each transfer mode.

a. Transmit mode

After setting transmit mode 00 to SMOD<SMD1, 0>, the first transmit data is written into a buffer registers SCMOD. When transmit mode is not set, a transmit data can not be written into a buffer registers. Next, set SCMOD <SIOE> to 1 to start transmission. After starting transmission, a transmit data is transferred from a buffer register to a shift register, the transmit data is output from the SO pin synchronous with the falling edge of shift clock (leading edge shift), starting from the least significant bit (LSB). When LSB of written data is output to SO pin, the buffer register is empty and the serial channel interrupt to request a new data is generated. When the next transmit data is written into the buffer register in the interrupt service program, the interrupt request signal is cleared.

Note: After SCMOD<SIOE> is set to 1, undefined data is output from SO pin till the first falling edge of the shift clock

i) Internal clock mode

In the internal clock mode, when all data are finished to transmit, if a new data is not set in the buffer register, the shift clock stops and a wait function starts.

Figure 3.15.4 (a) shows the timing chart of internal clock operation in transmit mode (with wait function).

ii) External clock mode

In the external clock mode, data must be set in the buffer registers before the next data shift operation begins. Therefore the transfer rate is determined by the maximum delay time from interrupt request generation to writing the transmit data into the buffer register in the interrupt service program.

Figure 3.15.4 (b) shows the timing chart of external clock operation in transmit mode.

iii) Finish to transmit

In order to end the transmit operation, set SCMOD<SIOE> to 0 instead of writing the next transmit data into the buffer register in the interrupt service program. When <SIOE> is cleared to 0, the transmit operation stops when all data is output. And when SCMOD<SRES> is set to 1, the transmit operation stops immediately and SCMOD<SIOE> is cleared to 0 automatically.

The end of transmit operation can be confirmed by reading out the serial transfer monitor flag SCMOD<FFSI>. When the transmit operation is finished, the serial transfer monitor flag is set to 1.

In the external clock mode, <SIOE> must be cleared to 0 before starting the next transmit data shift operation. If <SIOE> is not cleared to 0 before the shift operation begins; otherwise, dummy data is transmitted and operation ends.

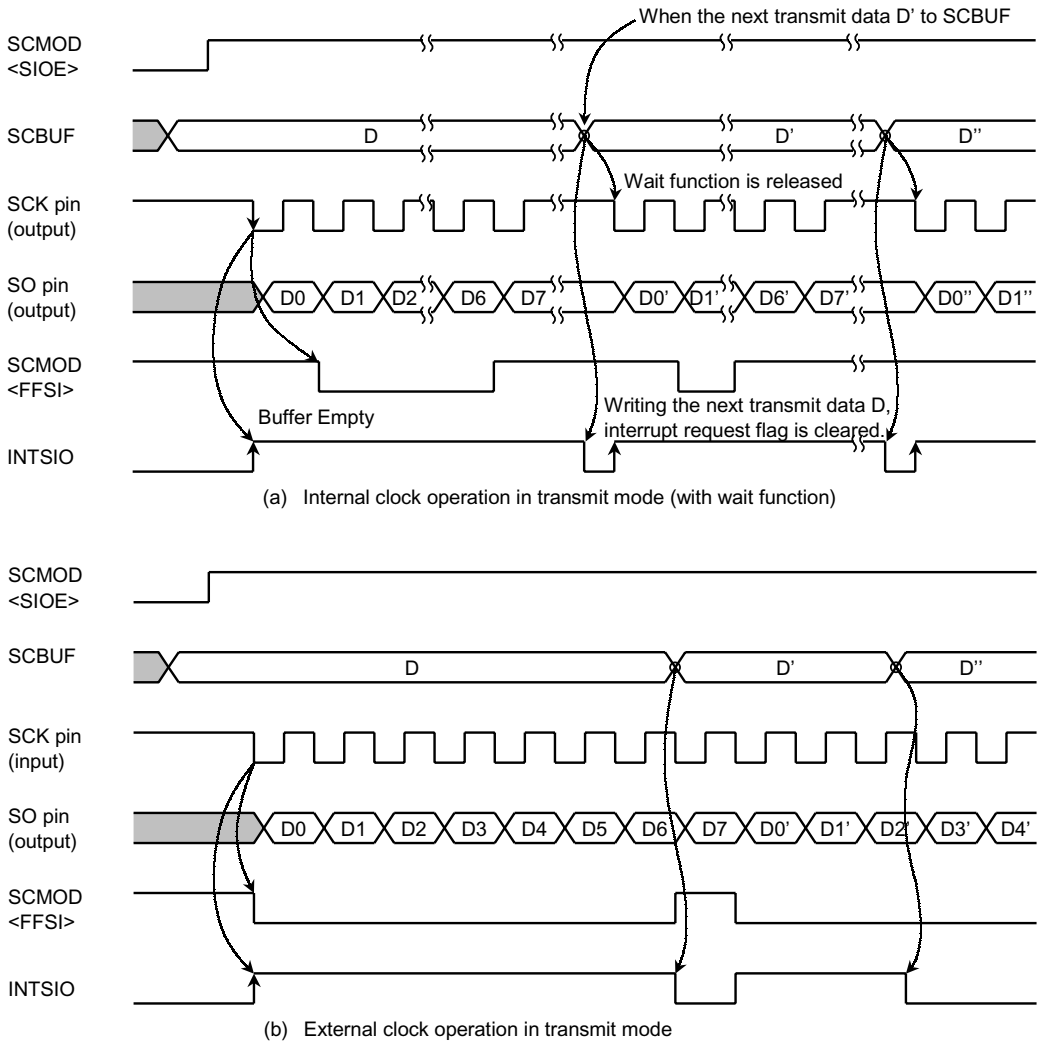


Figure 3.15.4 Serial channel timing chart in transmit mode

b. Receive Mode

After setting receive mode 01 to SCMOD <SMD1, 0> and 1 to SCMOD <SIOE>, receive mode is enabled. Data is received from SI pin to the shift register synchronous with the shift clock, starting from the least significant bit (LSB). When 8-bit data is received, the data is transferred from the shift register to the buffer register, the buffer register is full and the serial channel interrupt to read a received data is generated. When the received data is read from the buffer register in the interrupt service program, the interrupt request signal is cleared.

i) Internal clock mode

In the internal clock mode, if the previous receive data has not been read from the buffer register after the next data is received, the shift clock stops and a wait function starts until the previous data is read.

Figure 3.15.5 (a) shows the timing chart of internal clock operation in receive mode (leading edge shift with wait function).

Figure 3.15.6 (a) shows the timing chart of internal clock operation in receive mode (trailing edge shift with wait function).

ii) External clock mode

In the external clock mode, because the shift operation synchronizes with external supplied clock, it is necessary to read from the buffer register before transferring the next receive data to the buffer register. If the previous data has not read, the receive data will not be transferred to the buffer register, and next receive data will be canceled.

The maximum transfer rate of the external clock operation is determined by the maximum delay time from the generation of interrupt requests to reading received data.

Figure 3.15.5 (b) shows the timing chart of external clock operation in receive mode (leading edge shift).

Figure 3.15.6 (b) shows the timing chart of external clock operation in receive mode (trailing edge shift).

iii) Shift edge

In the receive mode, either leading edge shift or trailing edge shift can be selected. Because data is received at the leading edge of the serial clock, the first shift data must already be input to the SI pin when the initial serial clock pulses are applied at transfer start.

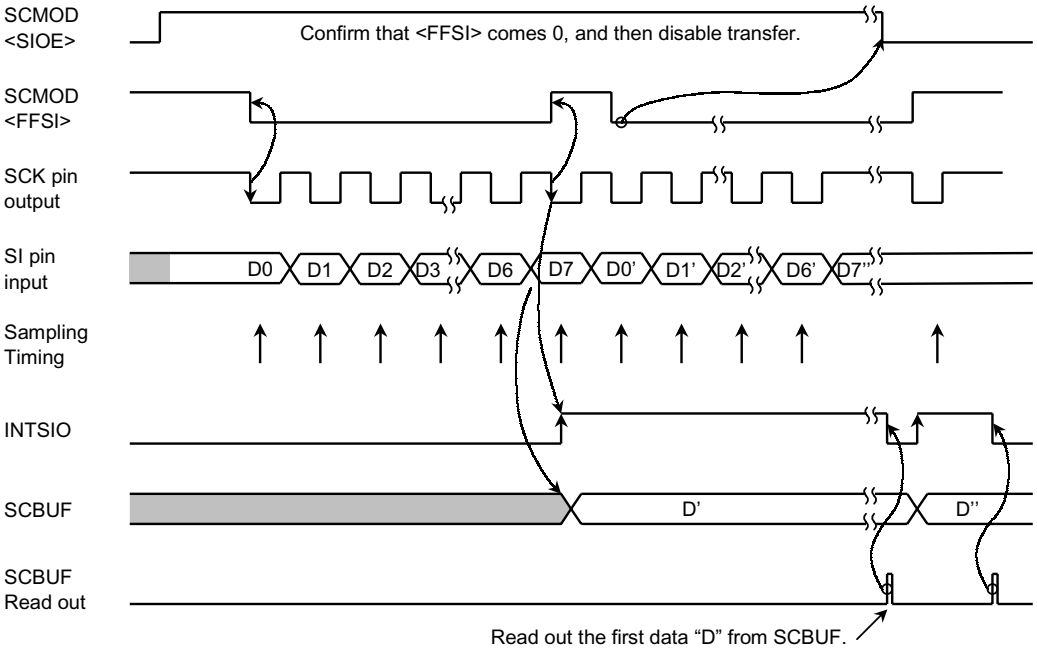
iv) Finish to receive

To end the receive operation, clear SCMOD <SIOE> to 0. When <SIOE> is cleared to 0, the receive operation stops after all data are received and transferred to the buffer register.

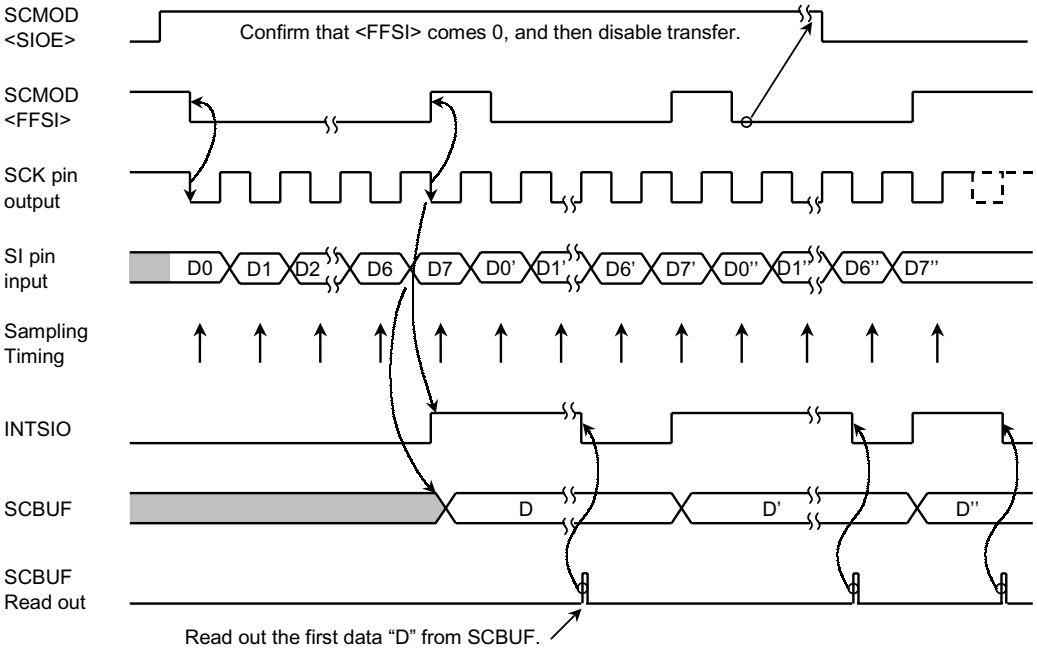
Setting SCMOD <SRES> is set to 1, the receive operation stops immediately and SCMOD <SIOE> is cleared to 0 automatically.

Note: If the transfer mode is switched, the contents of the buffer register is lost. In case that the mode needs to be switched, switch the mode after clearing <SIOE> to 0 and reading out the last received data. Undefined data is output from SO pin.

An end of receive operation can be confirmed by reading the serial transfer monitor flag SCMOD<FFSI>.

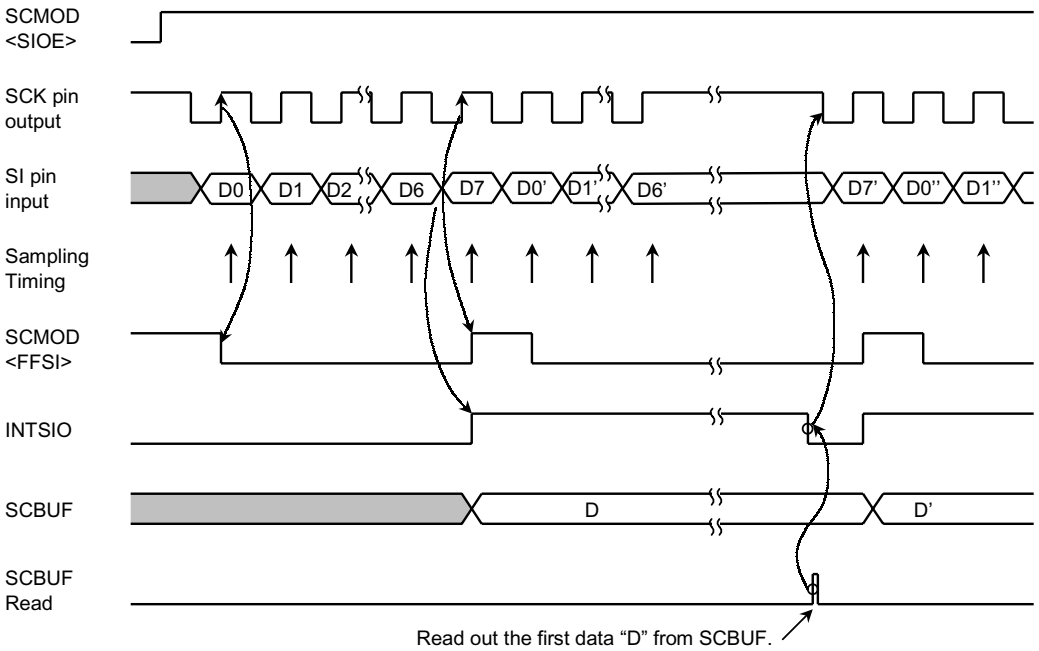


(a) Internal clock operation in receive mode (Shifted by leading edge with wait function)

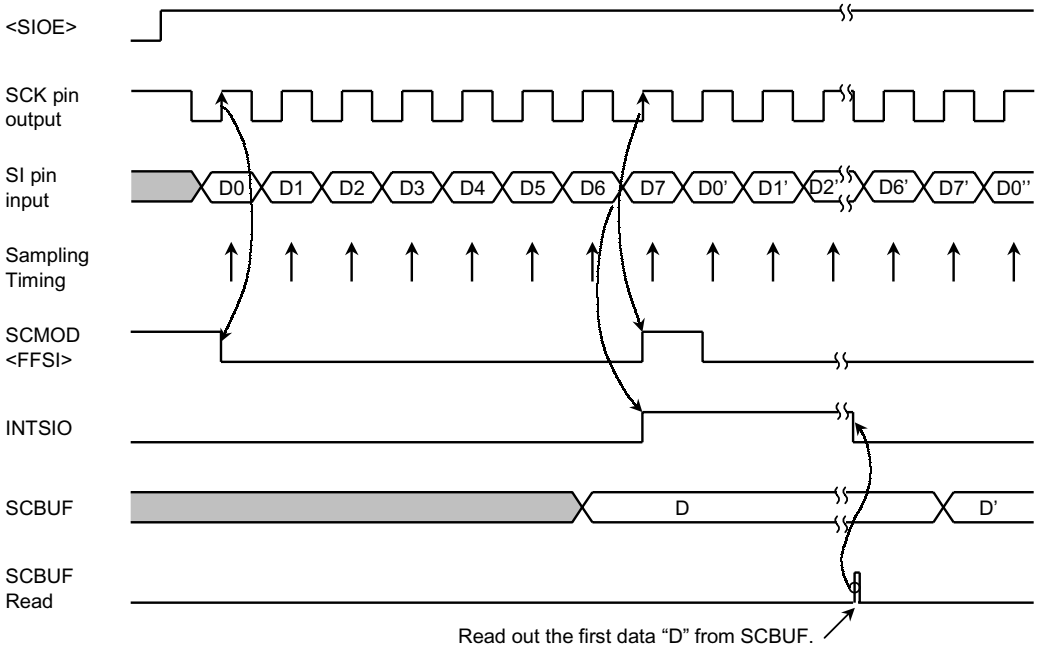


(b) External clock operation in receive mode (shifted by leading edge)

Figure 3.15.5 Serial channel timing chart in receive mode (Leading edge)



(a) Internal clock operation in receive mode (Shifted by trailing edge with wait operation)



(b) External clock operation in receive mode (shifted by trailing edge)

Figure 3.15.6 Serial channel timing chart in receive mode (Trailing edge)

c. Transmit/Receive mode

After setting transmit/receive mode 11 to SMOD <SMD1, 0>, the first transmit data is written into a buffer registers SCMOD. And then set SCMOD <SIOE> to 1, transmit/receive mode is enabled. The transmit data is output from SO pin synchronous with the falling edge of shift clock (leading edge shift), data is received from SI pin to the shift register synchronous with the rising edge of shift clock (trailing edge shift), starting from the least significant bit (LSB).

When 8-bit data is received, the data is transferred from the shift register to the buffer register, the buffer register is full and the serial channel interrupt to read a received data is generated. When the received data is read from the buffer register in the interrupt service program, the interrupt request signal is cleared. And then a next data is written into buffer register.

Note: After SCMOD<SIOE> is set to 1, undifined data is output from SO pin till the first falling edge of the shift clock.

i) Internal clock mode

In the internal clock mode, a wait function starts until the receive data is read and the next transmit data is written into the buffer register.

ii) External clock mode

In the external clock mode, the receive data must be read and the next transmit data written before the next shift operation, because the shift operation is synchronized with external supplied clock. The maximum transfer rate of the external clock operation is detemined by the maximum delay time from interrupt request generation to reading received data and writing transmit data.

Figure 3.15.7 (b) shows the timing chart of external clock operation in transmit/receive mode.

Since the buffer registers are used for both transmit and receive data, transmit data must be written after 8 receive data is read.

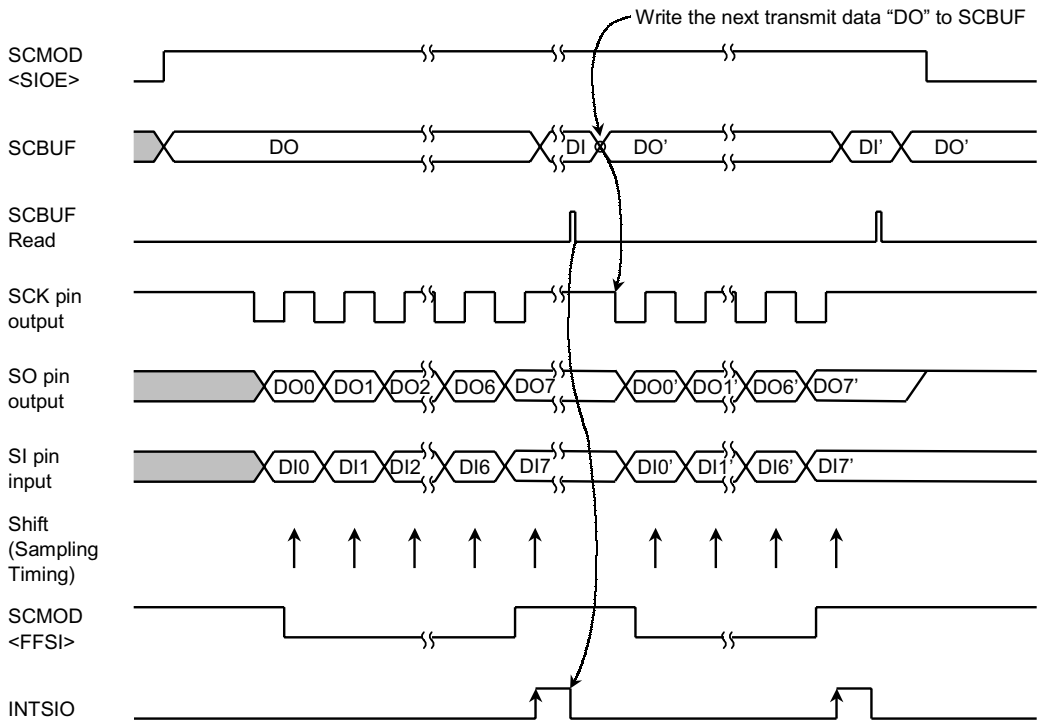
iii) Finish to transmit

To end the transmit/receive operation, clear SCMOD <SIOE> to 0.

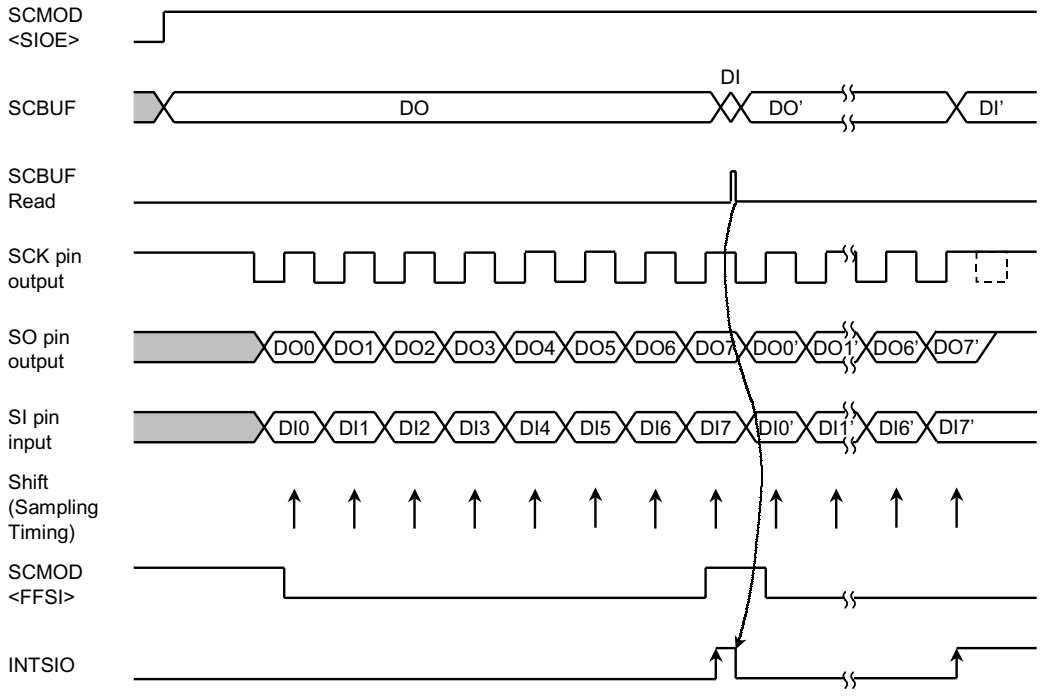
When SCMOD <SIOE> is cleared to 0, the transmit/receive operation ends after all data are received and transferred to the buffer register.

In the transmit/receive mode, the serial transfer operation ends just after setting SCMOD <SRES> to 1, and SCMOD <SIOE> is cleared to 0 auto matically.

The end of transmit/receive operation can be confirmed by reading the serial transfer monitor flag SCMOD <FFSI>.



(a) Internal clock operation in transmit/receive mode (with wait function)



(b) External clock operation in transmit/receive mode

Figure 3.15.7 Serial channel timing chart in transmit/receive mode

3.16 Serial Bus Interface (I^2C bus)

TMP93CF76/CF77/CW76/CU76/CT76 have one channel serial bus interface (I^2C bus). The interface terminals for communication are multiplexed and named channel 0 and 1. These sets of terminals can be switched by software. (I^2C bus is the bus system by Philips.)

The interface terminals can be selected from two channels.

- Channel 0; P73 (SDA0), P74 (SCL0)
- Channel 1; P75 (SDA1), P76 (SCL1)

The terminals for I^2C bus are multiplexed with P7 port and these are used as normal port when not to use as I^2C bus. When used for I^2C bus pins, control registers are set to 1 for output mode and function registers are set to 1 for I^2C bus.

I^2C bus Function

- Master/Slave Switching
- Single Master System without BUS arbitration
- High Speed Capability with 8-level FIFO in Master mode
- 9-bit data (8-bit data and 1-bit acknowledge)

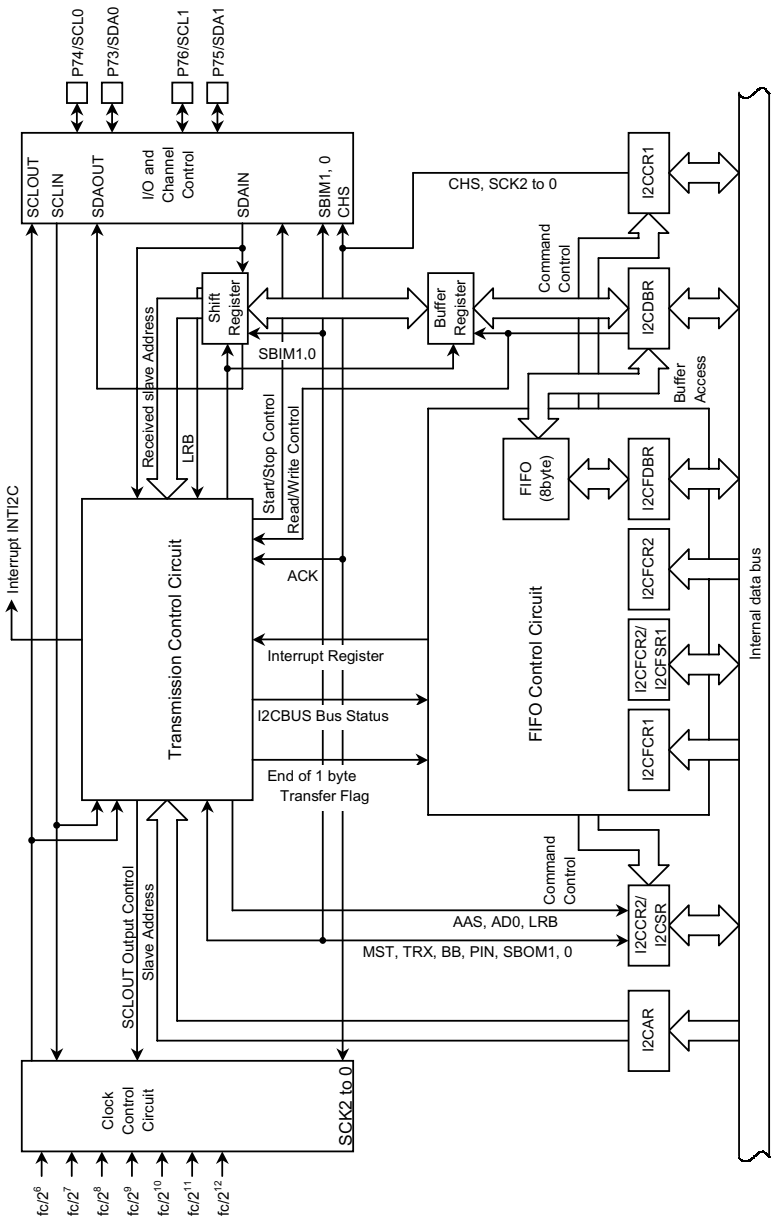


Figure 3.16.1 Configuration of serial bus interface

3.16.1 Control

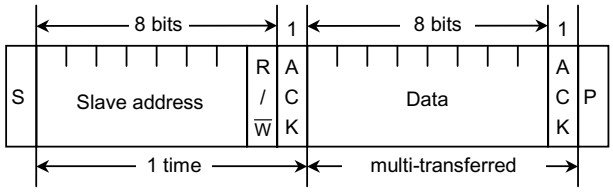
The following registers are used for control and monitor the serial bus interface.

- Serial BUS Interface Control Register 1 (I2CCR1)
- Serial BUS Interface Control Register 2 (I2CCR2)
- Serial BUS Interface Data Buffer Register (I2CDBR)
- I²C bus Address Register (I2CAR)
- Serial BUS Interface Status Register (I2CSR)

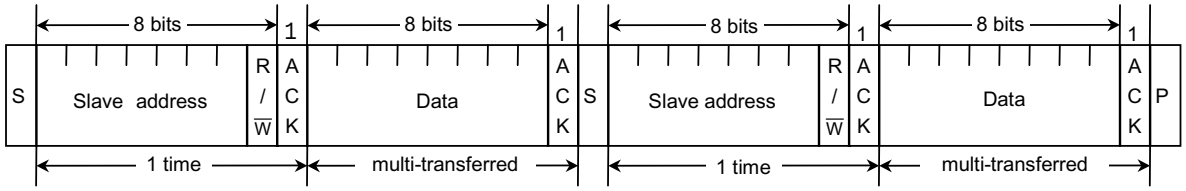
3.16.2 Data Format in I²C bus Mode

The followings shows the data format in I²C bus.

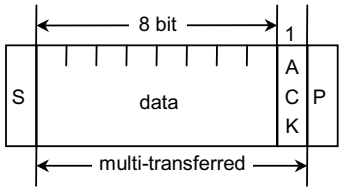
(a) Addressing format: transferring between master and slave



(b) Addressing format (restart): in case the direction for transfer



(c) Free data format: transferring format for data only; transferring neither involving slave address and direction bit



Note: S ; start condition: Output timing pulse which indicates start transmitting.
R/$\overline{W}$; direction bit: Indicate the direction for transferring against slave.
0: slave receives (master transfers)
1: slave transfers (master receives)
ACK ; acknowledge bit: Receiver response to transmitting as a confirmation for data receiving
0: receiving completed
1: not accepting data transferred, or in case master receiver instructs slave transmitter to terminate transferring
P ; stop condition: Output timing pulse which indicates terminate transmitting

Figure 3.16.2 Data Format for I²C bus

3.16.3 Control in I²C Bus

The following registers are used for control and monitor the serial BUS interface.

Serial BUS Interface Control Register 1

I2CCR1	7	6	5	4	3	2	1	0	
(0081H)	0	0	0	ACK	CHS	SCK			(Initial Value: 0000 0000)

ACK	Acknowledge bit select	0: Acknowledge not returned to transmitter. 1: Acknowledge returned to transmitter.	R/W
CHS	Input/Output channel select	0: Channel 0 (SCL0, SDA0) 1: Channel 1 (SCL1, SDA1)	
SCK	Serial clock frequency select (available in master mode)	000: fc/2^6 (250 kHz) 001: fc/2^7 (125 kHz) 010: fc/2^8 (62.5 kHz) 011: fc/2^9 (31.2 kHz) 100: fc/2^{10} (15.6 kHz) 101: fc/2^{11} (7.8 kHz) 110: fc/2^{12} (3.9 kHz) 111: reserved at fc=16 [MHz]	write only

Note 1: The bit 7 to 5 should be cleared to 0.

Note 2: Prohibit read-modify-write.

Serial BUS Interface Data Buffer Register

I2CDBR	7	6	5	4	3	2	1	0	
(0082H)	I2DBR7	I2DBR6	I2DBR5	I2DBR4	I2DBR3	I2DBR2	I2DBR1	I2DBR0	(Initial Value: **** ****) Read/Write

Prohibit read-modify-write.

I²C bus Address Register

I2CAR	7	6	5	4	3	2	1	0	
(0083H)	SA6	SA5	SA4	SA3	SA2	SA1	SA0	ALS	(Initial Value: 0000 0000)

SA	Slave address for a serial bus interface		write only
ALS	Address confirm	0: Confirm slave address(addressing format) 1: Not confirm slave address(free data format)	

Prohibit read-modify-write.

Serial BUS Interface Control Register 2

I2CCR2	7	6	5	4	3	2	1	0	
(0084H)	MST	TRX	BB	PIN	SBIM		0	0	(Initial Value: 0001 0000)

MST	Master/slave selection	0: Slave 1: master	write only
TRX	Transmission/Receive selection	0: Receiver 1: Transmitter	
BB	Start/stop condition control	0: Generate the stop condition when MST, TRX and Pin are 1. 1: Generate the start condition when MST, TRX and PIN are 1.	
PIN	Interrupt request reset	0: – 1: Cancel interrupt service request	
SBIM	Serial BUS interface Operating mode selection	00: Port mode 01: reserved 10: I²C bus mode 11: reserved	

Note 1: The bit 1 and 0 should be cleared to 0.

Note 2: Prohibit read-modify-write.

Serial BUS Interface Status Register

I2CSR (0084H)

7	6	5	4	3	2	1	0
MST	TRX	BB	PIN		AAS	AD0	LRB

(Initial Value: 0001 *000)

MTS	Master/slave selection mode monitor	0: Slave 1: Master	Read only
TRX	Transmission/Receive selection status monitor	0: Receiver 1: Transmitter	
BB	I^2C bus status monitor	0: BUS free 1: BUS busy	
PIN	Interrupt request moniter	0: Interrupt service requested 1: interrupt service released	
AAS	Slave address match detection monitor	0: Slave address match or "GENERAL CALL" not detected 1: Slave address match or "GENERAL CALL" detected	
AD0	"GENERAL CALL" detection monitor	0: "GENERAL CALL" not detected 1: "GENERALCALL" detected	
LRB	Last receive bit monitor	0: Last receive bit is 0 (Acknowledge) 1: Last receive bit is 1 (No-Acknowledge)	

(1) Acknowledge mode specification

Set the I2CCR1 <ACK> to 1 for operation in the acknowledge mode.

In the receive mode during the clock pulse cycle, the SDA pin is set to the low-level in order to generate the acknowledge signal. When I2CCR1 <ACK> is cleared to 0, the SDA pin released high-level in the acknowledge timing.

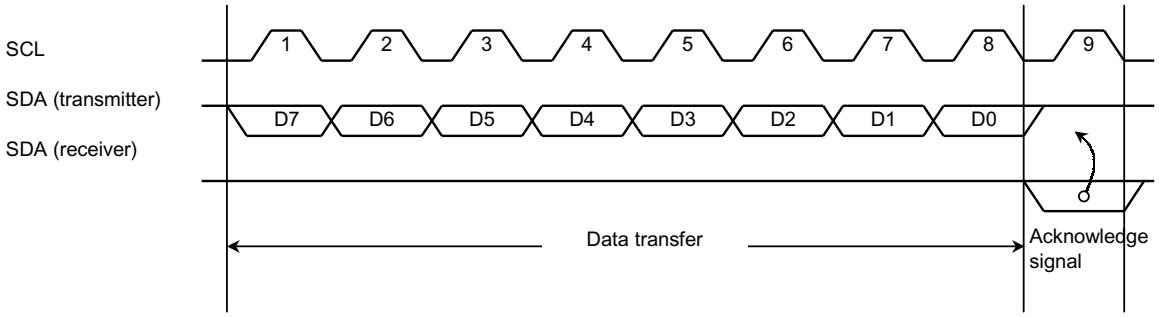


Figure 3.16.3 Acknowledge signal output timing

(2) Input/Output channel setting

The channel can be selected by setting I2CCR1 <CHS>.

Channel 1 (pair of SCL1 and SDA1) is selected by setting 1 to I2CCR1 <CHS> and Channel 0 (pair of SCL0 and SDA0) is selected by setting 0 to I2CCR1 <CHS>.

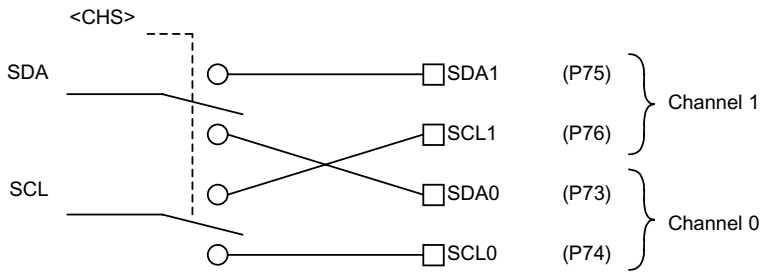


Figure 3.16.4 Input/output channel

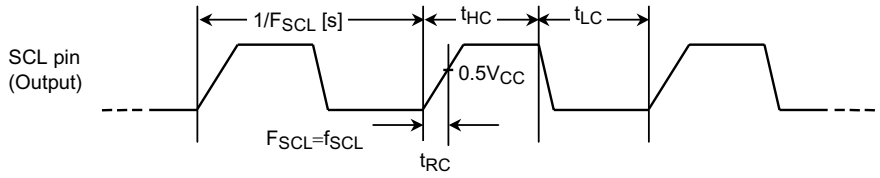
(3) Serial Clock

The I2CCR1 <SCK 2:0> are used to select a maximum transfer frequency directed from the SCL pin in the master mode. When rising time of the output clock (t_{RC}) is at least 8/fc [s], a high-level time of the output clock (t_{HC}) is t_{SCL}.

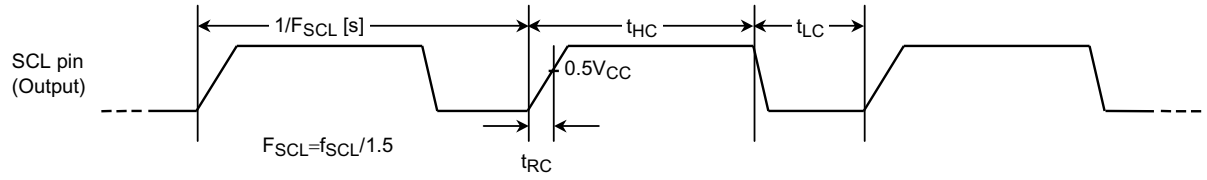
While the SCL line is fixed to low-level by a slave device,the output clock stops.

The first clock (t_{HC} [s]) after restart is ($t_{SCL}/2$) ≤ t_{HC} ≤ t_{SCL}.

(a) In case of t_{RC} < (8/fc) [s] $t_{HC} = t_{LC} = t_{SCL}/2$ [s] ($t_{SCL} = 1/f_{SCL}$ [s])



(b) In case of $t_{RC} \geq$ (8/fc) [s] $t_{HC} = t_{SCL}$ [s], $t_{LC} = t_{SCL}/2$ [s]



SCK (Bit 2 to 0 of I2CCR1)	F_{SCL} (at fc = 16 MHz)	
	t_{RC} < 500 [ns]	500 [ns] ≤ t_{RC}
000	250 kHz	166.7 kHz
001	125 kHz	83.3 kHz
010	62.5 kHz	41.7 kHz
011	31.2 kHz	20.8 kHz
100	15.6 kHz	10.4 kHz
101	7.8 kHz	5.2 kHz
110	3.9 kHz	2.6 kHz
	In case of (a)	In case of (b)

Figure 3.16.5 Serial clock

(4) Slave Address and Address Comfirm

When TMP93CF76/CF77/CW76/CU76/CT76 is used as a slave device, set the slave address <SA6:0> and <ALS> to I2CAR register. Set I2CAR2 <ALS> 0 to the for the addressing format mode.

(5) Master/Slave Selection

Set the I2CCR2 <MST> to 1 for operating the serial bus interface as a master device. I2CCR2 <MST> is cleared to 0 by the handware after a stop condition on the bus is detected.

(6) Transmitter/Receiver Selection

Set the I2CCR2 <TXR> to 1 for operating the serial bus interface as a transmitter. Clear I2CCR2 <TRX> for operation as a reciver. When the serial bus interface receive a slave address setted in I2CAR or a GENERAL CALL from the master device in the addressing format is transferred in the slave mode, I2CCR2 <TRX> is set to 1 if the direction bit (R/W) sent from the master device is 1, and is cleared to 0 if the bit is 0.

In the master mode, after an acknowledge signal is returned from the slave device, I2CCR2 <TRX> is set to 0 if a transmitted direction bit is 1, and set to 1 if it is 0.

When an acknowledge signal is not returned, the current condition is maintained.

I2CCR2 <TRX> is cleared to 0 by the hardware after a stop condition on a bus is detected.

The following shows I2CCR2 <TRX> change conditions in each mode and I2CCR2 <TRX> after changing.

Mode	Direction bit	Change condition	I2CCR2 <TRX> after changing
Slave mode	0	A received slave address is the same as a value set to I2CAR.	0
	1		1
Master mode	0	ACK signal is returned.	1
	1		0

When the serial bus interface circuit operates in the free data format, the slave address and the direction bit are not recognized. They are handled as data just after generating a start condigion. I2CCR2 <TRX> was not changed by the hardware.

(7) Start/Stop Condition Generation (for Master Mode)

When I2CSR <BB> is 0, the slave address and the direction bit which are set to the I2CDBR are output on a bus after generation a start condition be writing 1 the I2CCR2 <MST>, I2CCR2 <TRX>, I2CCR2 <BB> and I2CCR2 <PIN>. It is necessary to set transmitted data to I2CDBR and set 1 to <ACK> beforehand.

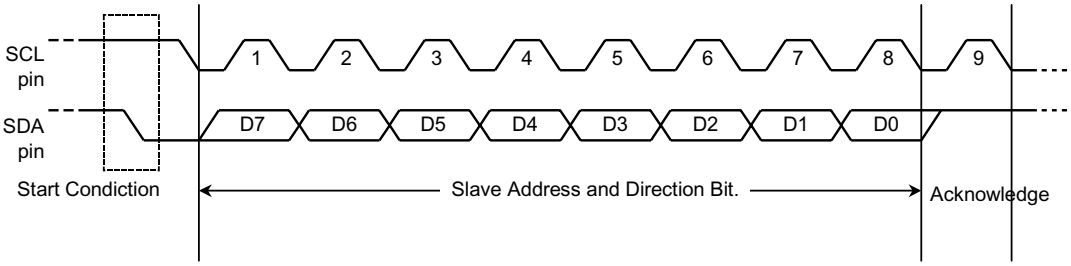


Figure 3.16.6 Start condition and slave address generation

When I2CSR <BB> is 1, a sequence of generating a shop condition is started by writing 1 to I2CCR2 <MST>, I2CCR2 <TRX>, and I2CCR2 <PIN>, and 0 to I2CCR2 <BB>. Do not modify the contents of I2CCR2 <MST>, I2CCR2 <TRX>, I2CCR2 <BB>, and I2CCR2 <PIN> until a stop condition is generated on a bus.

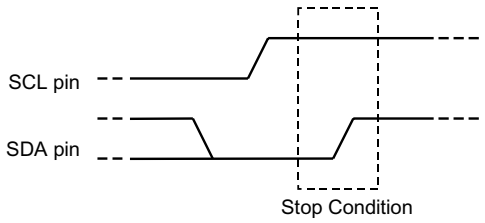


Figure 3.16.7 Stop Condition Generation

The bus condition can be indicated by reading I2CSR <BB>. The I2CSR <BB> is set to 1 when start condition is detected and is cleated to 0 when stop condition is detected on a bus.

(8) Interrupt Service Request and Cancel

When a serial bus interface interrupt request (INTI2C) occurs, the I2CSR <PIN> is cleared to 0. During the time that <PIN> is 0, the SCL pin is pulled down to the low level.

<PIN> is cleared to 0 when 1-byte of data is transmitted or received. Either writing/reading data to/from the I2CDBR sets <PIN> to 1.

The time from <PIN> being set to 1 until the SCL pin is released takes t_{LOW}.

In the address recognition mode (ALS = 0), <PIN> is cleared to 0 when the received slave address is the same as the value set to the I2CAR or when a "GENERAL CALL" is received (all 8-bit data are 0 after a start condition). Although I2CCR2 <PIN> can be set to 1 by the program, <PIN> is not cleared to 0 when it is written 0.

(9) Serial Bus Interface Operation Mode Selection

The I2CCR2 <SBIM1:0> is used to specify the serial bus interface operation mode. Set the I2CCR2 <SBIM1:0> to 10 when used in the I^2C bus Mode after confirming that input signal via port is high level. Switch a mode to port after confirming sure that the bus is free.

(10) Slave Address Match Detection Monitor

I2CSR <AAS> is set to 1 in the slave mode, in the address recognition mode (<ALS> = 0), or when receiving "GENERAL CALL" or a slave address with the same value that is set to the I2CAR. When I2CAR2 <ALS> is 1, I2CSR2 <AAS> is set to 1 after receiving the first 1byte of data. <AAS> is cleared to 0 by writing/reading data to/from a data buffer register.

(11) GENERAL CALL Detection Monitor

I2CSR <AD0> is set to 1 in the slave mode, when all 8-bit data received after a start condition are 0. I2CSR <AD0> is cleared to 0 when a start or stop condition is detected on a bus.

(12) Last Received Bit Monitor

The SDA line value stored at the rising edge of the SCL line is sent to I2CSR <LRB>. In the acknowledge mode, immediately after an INTI2C interrupt request is generated an acknowledge signal is read by reading contents of I2CSR <LRB>.

3.16.4 Data Transfer in I^2C bus Mode

(1) Device Initialization

Set I2CCR1 <ACK>, <CHS>, <SCK 2:0>. Clear 0 to bits 7 to 5.

Set a slave address and I2CAR <ALS> <ALS> = 0 when an addressing format. After confirming that input signals via port are high level, for specifying the default setting to slave receiver mode, clear 0 to I2CCR2 <MST>, <TRX>, <BB> and set 1 to I2CCR2 <PIN>, 10 to I2CCR1 <SBIM 1:0>; and 0 to bit 0 and 1.

(2) Start condition and Slave address Generation.

Confirm that I2CSR <BB> is 0.

Set I2CCR2 <ACK> to 1 and specify a slave address and a direction bit to the I2CDBR.

When I2CSR <BB> is 0, the start condition is generated and the slave address and the direction bit which were set to the I2CDBR are output on a bus by setting 1 to I2CCR2 <MST>,<TRX>, <BB> and <PIN>. A slave device receives these data and pulls down the SDA line to the low level at the acknowledge signal timing. An INTI2C interrupt request occurs at the 9th falling edge of the SCL clock cycle, and the I2CSR <PIN> is cleared to 0.

The SCL pin is pulled down to the low level while <PIN> is 0. When an interrupt request occurs, I2CCR2 <TRX> changes by the according to the direction bit only when an acknowledge signal is returned from the slave device.

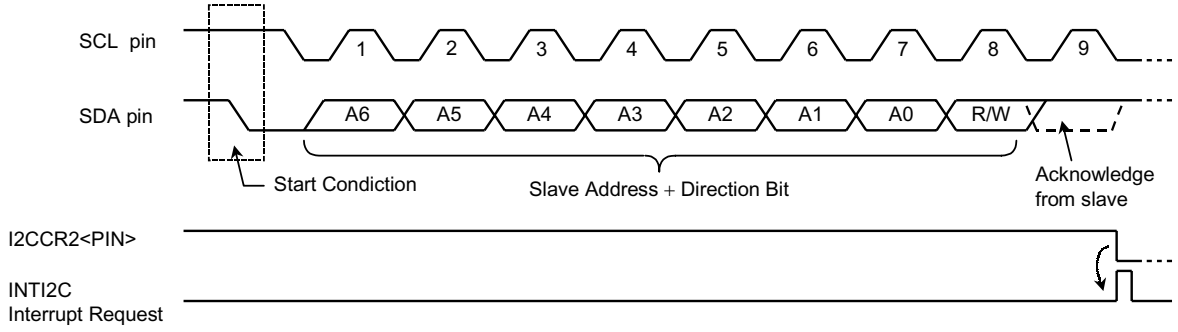


Figure 3.16.8 Start condition and slave address generation

(3) 1-byte Data Transfer

Check I2CRS <MST> by the INTI2C interrupt process after a 1-byte data transfer is completed, and determine whether the mode is a master or slave.

a. When I2CSR <MST> is 1 (Master mode)

Check <TRX> and determine whether the mode is a transmitter or receiver.

i) When I2CSR <TRX> is 1 (Transmitter mode)

Check I2CSR < LRB>. When the <LRB> is 1, a receiver does not request data. Implement the process to generate a stop condition (described later) and terminate data transfer.

When <LRB> is 0, the receiver requests new data. Write the transmitted data to the I2CDBR. After writing the data, <PIN> becomes 1, a serial clock pulse is generated for transferring a new 1-byte of data from the SCL pin, and then the 1-byte data is transmitted from SDA pin. After the data is transmitted, an INTI2C interrupt request occurs. <PIN> becomes 0 and the SCL pin is pulled down to the low level. If the data to be transferred is more than one byte in length, repeat the procedure from <LRB> checking above.

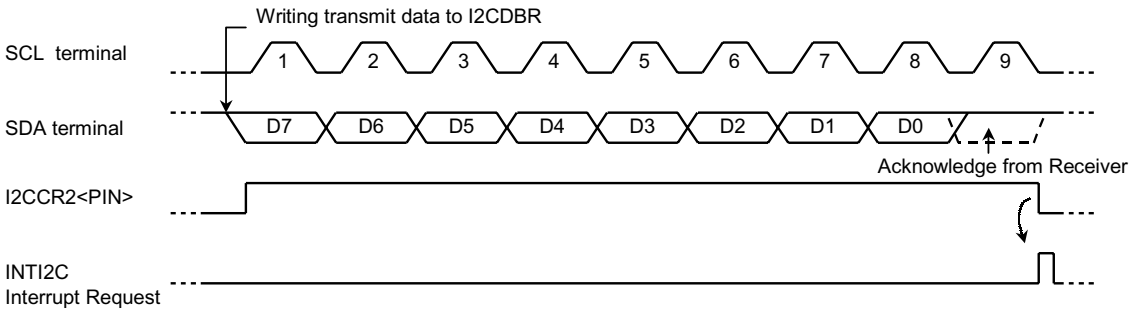


Figure 3.16.9 1-byte transmission

ii) When I2CSR <TRX> is 0 (Receiver mode)

Set I2CCR1 <ACK> to 1 and read the received data from the I2CDBR (data which is read immediately after a slave address is sent is undefined). After the data is read, <PIN> becomes 1. The serial bus interface output a serial clock pulse to the SCL pin to transfer new 1-byte of data and set the SDA pin to 0 at the acknowledge signal timing.

An INTI2C interrupt request occurs, < PIN> becomes 0 and the SCL pin pulled down to the low level. The serial bus interface output a clock pulse for 1-byte of data transfer and the acknowledge signal each time that received data is read from the I2CDBR.

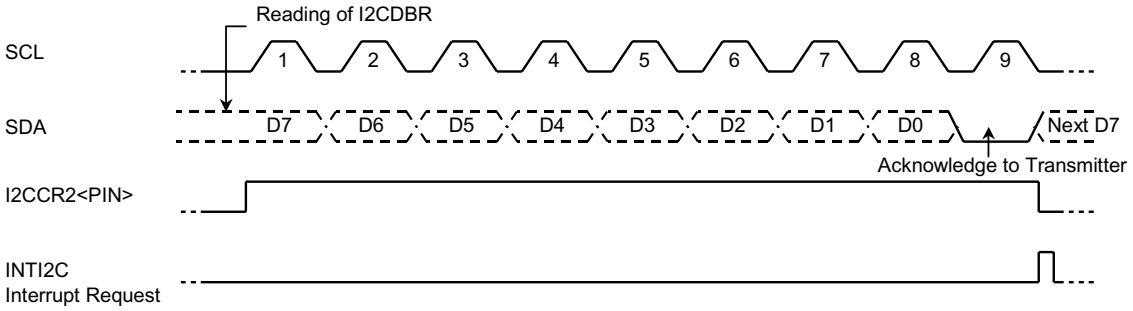


Figure 3.16.10 1-byte receive

In order to terminate transmitting data to a transmitter, clear <ACK> to 0 before reading data which is 1-byte before the last data to be received. The SDA pin released high-level in an acknowledge timing of last received byte. The receiver indicates to the transmitter that data transfer is complete. After data is received and an interrupt request has occurred, the serial bus interface generates a stop condition and terminate data transfer. When reading data from I2CDBR in the last received byte, the serial clock and acknowledge signal don't output because <ACK> is 0.

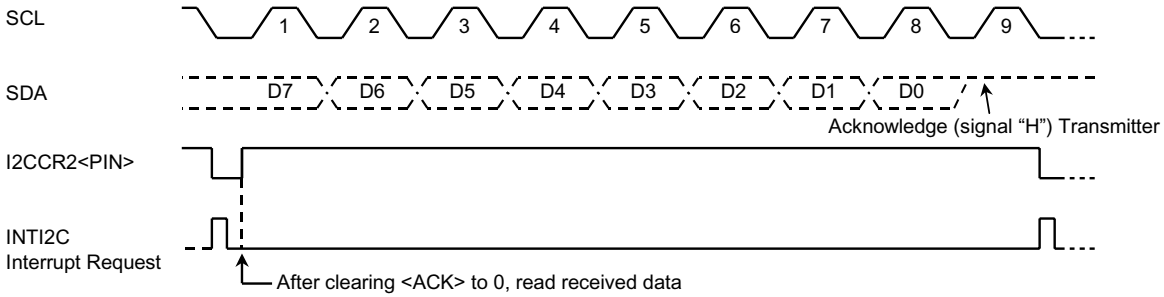


Figure 3.16.11 Data Transmission of final data in master/receiver mode

b. When < MST> is 0 (Slave mode)

In the slave mode, an INTI2C interrupt request occurs when the serial bus interface receive a slave address or a "GENERAL CALL" from the master device, or when a "GENERAL CALL" is received and data transfer is complete after matching a received slave address. When an INTI2C interrupt request occurs, I2CCR2 <PIN> is cleared, and the SCL pin is pulled down to the low level. Either reading/writing from to the I2CDBR or setting <PIN> to 1 releases the SCL pin after taking t_{LOW} time.

In the slave mode, the serial bus interface operates either in normal slave mode.

Check the I2CSR <TRX>, <AAS> and <AD0> and implement processes according to conditions listed in the next table.

Table 3.16.1 Status and service in slave mode

TRX	AAS	AD0	Status	Service
1	1	0	In Slave/Receiver mode, received the slave address of serial bus interface with direction bit 1. This condition is slave transmit mode by transfer request from master device.	Write transmit data into I2CDBR register.
	0	0	In slave transmitter mode, 1-byte transmission has completed.	In case of <LRB> = 1 (no further data request), set <PIN> 1 and <TRX> 0 for BUS release. In case of <LRB> = 0 (further data request), write transmit data to I2CDBR register.
0	1	1/0	In slave receiver mode, received address of the serial bus interface with direction bit 0 or "GENERAL CALL". This condition is slave receive mode by receive request from master device.	Read I2CDBR register in order to set <PIN> 1 (dummy read).
	0	1/0	In slave receiver mode, 1-byte receive has completed.	Read received data from I2CDBR register.

(4) Stop Condition Generation

When I2CSR <BB> is 1, a sequence of generating a stop condition is started by writing 1 to I2CCR2<MST>, <TRX>, and <PIN>, and 0 to I2CCR2<BB>. Do not modify the contents of I2CCR2<MST>, <TRX>, <BB>, <PIN> until stop condition is generated on a bus.

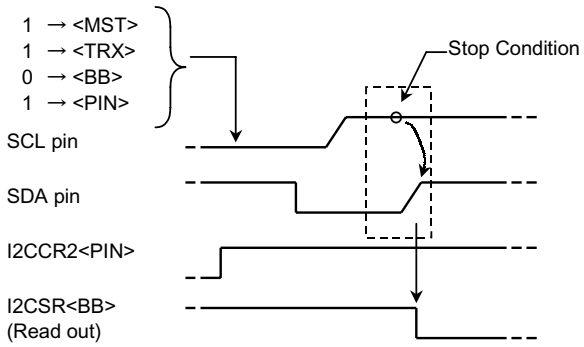


Figure 3.16.12 Stop condition generation

(5) Restart

Restart is used to change the direction of data transfer between a master device and a slave device during transferring data. The following explains how to restart when the serail bus interface is in the master mode.

Clear 0 to I2CCR2<MST>, <TRX>, and <BB> and set 1 to I2CCR2<PIN> and release the bus. The SDA pin retains the high level and the SCL pin is released. Since a stop condition is not generated on the bus, the bus is assumed to be in a busy state from other devices. Check I2CSR<BB> until it becomes 1 to check that the SCL pin of the serial bus interface are released. Check the I2CSR<LRB> until it becomes 1 to check that the SCL line of the bus is not pulled down to the low level by other devices. After confirming that the bus stays in a free state, generate a start condition with procedure (2).

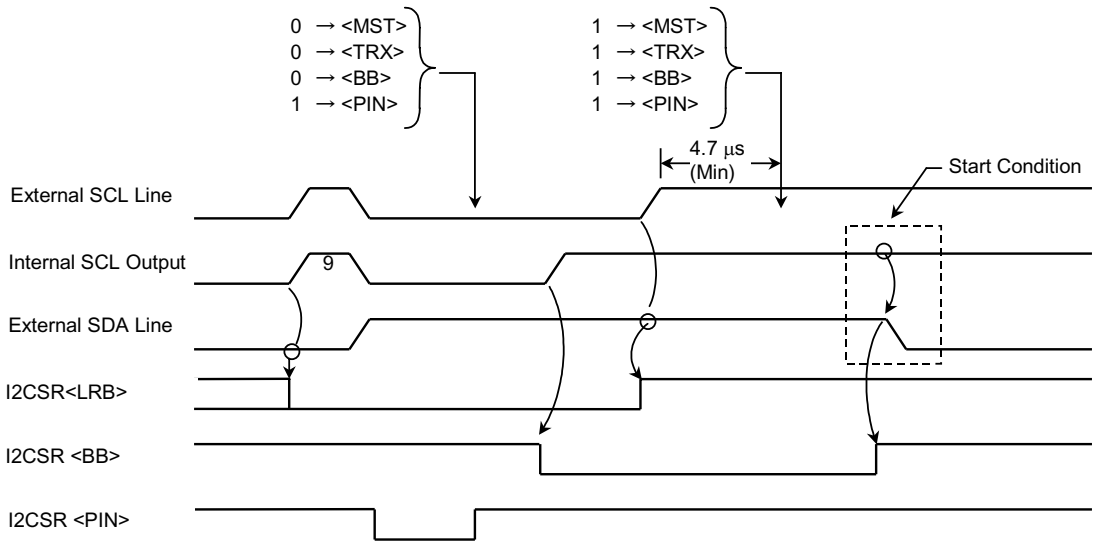


Figure 3.16.13 Restart timing chart

3.16.5 FIFO Controling

In I²C bus/Master mode, 8-byte continuous data transfer can be done with FIFO control.

I²C bus control registers are accessed from FIFO control circuit instead of CPU. Before starting FIFO control circuit, I²C bus should be set in slave mode (initialized condition). FIFO control circuit is controlled by following registers,

I²C bus FIFO Control Register 1

I2CFCR1 (0063H)

7	6	5	4	3	2	1	0
T/$\overline{R}$		FSCK		CONT		BYTE	

(Initial Value: 0000 0000)

T/$\overline{R}$	FIFO transfer mode selection	0: Receiver mode 1: Transmitter mode	write only
FSCK	Serial clock frequency (fscl) selection	000: fc/2^6 (250 kHz) 001: fc/2^7 (125 kHz) 010: fc/2^8 (62.5 kHz) 011: fc/2^9 (31.2 kHz) 100: fc/2^{10} (15.6 kHz) 101: fc/2^{11} (7.8 kHz) 110: fc/2^{12} (3.9 kHz) 111: – at fc = 16 [MHz]	
CONT	Data transfer mode selection	0: 8 to 1-byte data transfer 1: Continuous transfer	
BYTE	Number of transfer data byte (Data is valid when <CONT> = 0)	000: 1-byte 001: 2-byte 010: 3-byte 011: 4-byte 100: 5-byte 101: 6-byte 110: 7-byte 111: 8-byte	

Prohibit read-modify-write.

I²C bus FIFO Control Register 2

I2CFCR2 (0064H)

7	6	5	4	3	2	1	0
$\overline{START}$	$\overline{STOP}$	CHS	$\overline{INT}$			$\overline{RST}$	

(Initial Value: 1101 **1*)

$\overline{START}$	Start FIFO buffer transfer	0: Start or restart 1: –	write only
$\overline{STOP}$	Stop FIFO buffer transfer	0: Stop 1: –	
CHS	Input/Output Channel selection	0: Channel 0 (SCL0, SDA0) 1: Channel 1 (SCL1, SDA1)	
$\overline{INT}$	Restart in continuous mode	0: Start continuous transfer 1: –	
$\overline{RST}$	Reset for I²C bus and FIFO control circuit (Note)	0: Reset 1: –	

Note 1: Since 4.5-state width system reset is executed after writing to this register, Do not access with I²C bus or FIFO controller during the period.

Note 2: Prohibit read-modify-write.

I²C bus FIFO Data Buffer Register

I2CFDBR	7	6	5	4	3	2	1	0	(Initial Value: **** ****)
(0065H)	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0	Read/Write

Prohibit read-modify-write.

I²C bus FIFO Status Register 1

I2CFSR1	7	6	5	4	3	2	1	0	
(0064H)	SDA	END	CHS	BUSY	FULL	EMPTY	SCERR	AKERR	(Initial Value: *000 0000)

SDA	SDA line monitor	0: SDA line low 1: SDA line high	read only
END	FIFO buffer status flag	1: End of transfer cleared by setting <STOP> to 0	
CHS	Input/Output channel monitor	0: Channel 0 1: Channel 1	
BUSY	FIFO buffer transfer status	1: FIFO buffer data in transfer cleared by setting <STOP> to 0	
FULL	FIFO buffer full/Receive end	0: – 1: FIFO buffer full/receive end	
EMPTY	FIFO buffer empty/Transmit end	0: – 1: FIFO buffer empty/Transmit end	
SCERR	Start condition error	0: – 1: Start condition error	
AKERR	Acknowledge error	0: – 1: Acknowledge error	

I²C bus FIFO Status Register 2

I2CFSR2	7	6	5	4	3	2	1	0	
(0069H)	NOMAT	LRBM							(Initial Value: 01** ****)

NOMAT	Matching monitor between SCL line and SCL terminal	0: – 1: SCL line pulled down by slave device	read only
LRBM	Last received bit monitor (acknowledge signal monitor)	0: Last receive bit 0 (acknowledge) 1: Last receive bit 1 (no-acknowledge)	

(1) Transmit Operation

Set the number of byte transferred and select transfer clock by setting I2CFCR1 register. Set FIFO controller in transmitter mode by setting 1 to I2CFCR1 <T/$\overline{R}$>. The number of byte for transfer at start time includes slave address. This can be set up to 8 bytes. By setting I2CFCR1 <CONT>, the number of byte is set to 8bytes and continuous data transfer becomes available. After setting I2CFCR1 register, write data into I2CFDBR in order of transmission. When number of data written becomes the number of byte set, I2CFSR1 <FULL> register is set 1. It's ignored if data is written during <FULL> is 1. For starting transmission, slave address and <R/$\overline{W}$> bit should be set as the first data.

Then set I2CFCR2 <CHS> and <START>, the FIFO controller becomes active.

The FIFO controller sets I2CFSR <BUSY> to 1 and accesses I2CFCR1, I2CFDBR and I2CFCR2 registers to start transmission. At this time, if BUS is busy, <SCERR> bit in I2CFSR1 register is set 1 and generate the interrupt request INTI2C. If this happens, set I2CFCR2 <$\overline{RST}$> to 1 and reset FIFO controller by software.

If there is no acknowledge return for each byte, the interrupt request INTI2C is generated and I2CFSR1 <AKERR> is set 1.

When all data byte has been transferred, I2CFSR1 <EMPTY> is set 1 and the interrupt request INTI2C is generated. And if I2CFCR1 <CONT> is 0, I2CFSR1 <END> register is set 1 to terminate all data transfer. In case that <CONT> bit is 1, <END> bit is not set because of continuous mode. This is the reason why the rest of data should be transferred by restarting after setting the number of data remained and data into I2CFCR1 and I2CFDBR registers. If an interrupt request is no needed when data transfer completes, set <$\overline{INT}$> to 0 before restart.

(2) Receive Operation

The procedure is almost same as transmit operation except that the number of data byte does not include slave address. Set the FIFO controller in Receiver mode by setting I2CFCR1 <T/$\overline{R}$>. Following that, set slave address and I2CFDBR <R/$\overline{W}$> and set FIFO controller active by setting I2CFCR2 <START> to 0. When the number of data, which was set in I2CFCR1 register, has been received, I2CFSR <FULL> is set 1 and the interrupt request INTI2C is generated. The status can be monitored in I2CFSR1 <CONT> and <$\overline{INT}$> as same as in transmit operation.

The content of dummy read, which is executed right after the slave address, is not set into FIFO buffer.

(3) Restart Operation

When <END> bit is 1, to provide the following procedure can be recognized as restart operation,

Start preparation as same as (1) or (2)

Start by setting <$\overline{START}$> bit 0

The FIFO controller does restart operation then data is transferred.

(4) Stop Operation

By setting I2CFCR2 <$\overline{STOP}$> to 0 when I2CFCR1 <END> is 1, FIFO controller stops data transfer after generate stop condition on to BUS and clearing I2CFSR1 <BUSY> is 0.

3.17 8-Bit AD Conversion Circuit (AD)

The TMP93CF76/CF77/CW76/CU76/CT76 have an 8-bit AD conversion circuit of high precision, the successive comparison type with 10-channels analog input. The 8-cannels (AIN2 to AIN9) of 10-channels analog input pin are also used as general purpose input ports (P40 to P47). The other 2-channels (AIN0, AIN1) are also used as I/O port (P75, P76).

The AD conversion ends in 11.9 μs (at 16 MHz).

3.17.1 Block diagram

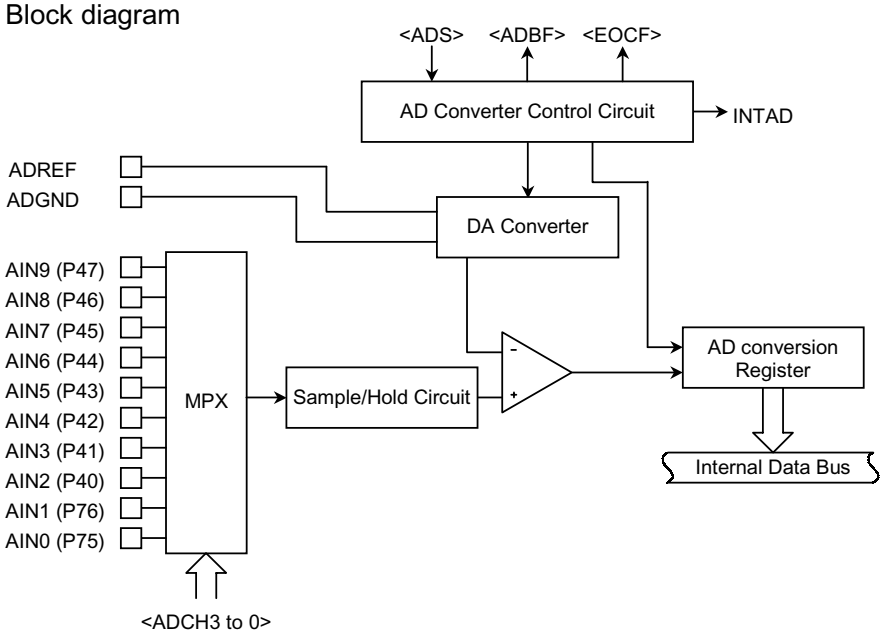


Figure 3.17.1 Composition of the 8-bit AD conversion circuit

3.17.2 Operation of AD Conversion Circuit

(1) AD conversion reference voltage

The positive electrode of AD conversion reference voltage connects to ADREF pin, and the negative electrode of AD conversion reference voltage connects to ADGND pin.

The AD conversion is carried out by splitting reference voltage between ADREF pin and ADGND pin to bit divided by 256 by ladder resistor in DA converter and making a judgment by comparing it with analog input voltage.

(2) Analog input channels

One of the 10-channels analog input (AIN0 to AIN9) is selected by the AD conversion control register ADMOD <ADCH3 to 0>.

The analog input channel selection register ADMOD <ADCH3 to 0> are initialized to 0 by reset operation, then the AIN0 (P75) is selected. When these ports are not used as the analog input port, they can be used as general purpose input ports (Port 4), input/output ports (P75, P76).

During conversion, do not change output level. (The AD conversion value may be in fluenced)

(3) AD conversion time

The result of AD conversion is stored into ADREG after the passage of 95 states (11.9 μs at fc = 16 MHz) from setting ADMOD <ADS> to 1.

(4) Start AD conversion start

AD conversion is started by setting ADMOD <ADS> to 1. After AD conversion starts, ADCR <ADBF> is set to 1.

Note : If AD conversion is restarted when <ADBF> is 1, AD conversion will be stopped. Set ADMOD <ADS> to 1 after confirming <ADBF> to 0.

(5) AD conversion end

After the end of AD conversion ADMOD <EOCF> is set to 1, and the interrupt request signal (INTAD) is generated, and the <ADBF> is cleared to 0.

(6) AD conversion interruption (INTAD)

After the end of AD conversion, the interrupt request signal (INTAD) is generated, and the AD circuit requests CPU to interrupt. The interrupt request signal (INTAD) is cleared to 0 by reading out the ADREG in program.

Note : When interrupt is accepted and the vector address is read, the interrupt request flag is not cleared to 0 because interrupt request signal(INTAD) remains 1 until the content of ADREG is read. Accordingly, the interrupt request flag must be cleared to 0 by program after the content of ADREG is read. (Refer to 3.4 Interrupts.)

(7) Reading of AD conversion values

The result of AD conversion is put into the AD conversion register (ADREG).

The AD conversion end flag ADMOD <EOCF> is cleared to 0 by reading the ADREG.

The value of the ADREG is an undefined data durring AD conversion.

Figure 3.17.2 shows the timing chart of AD conversion operation.

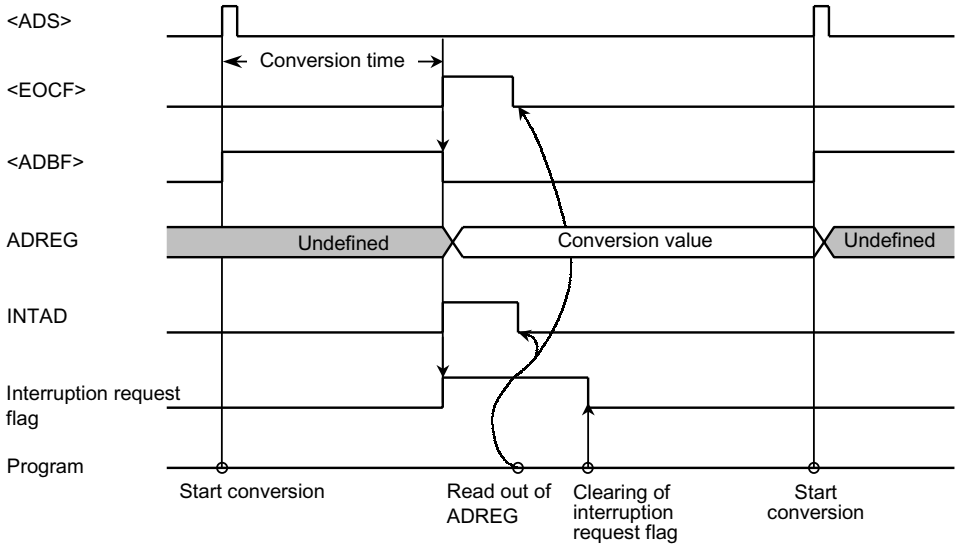


Figure 3.17.2 Shown in timingchart of AD conversion operation.

Note: When executing the HALT instruction during AD conversion, AD conversion is stopped and the value of ADREG is undefined. At the same time, AD control register (ADMOD) is initialized.

3.17.3 Control Register

AD Converter Control Register

ADMOD (005AH)	7	6	5	4	3	2	1	0
	1	EOCF	ADBF	ADS	ADCH3	ADCH2	ADCH1	ADCH0

(Initial Value: 1000 0000)

EOCF	AD conversion completed flag	0: AD conversion in progress or before conversion 1: AD conversion completed	read only
ADBF	AD conversion busy flag	0: AD conversion stopped 1: AD conversion in progress	
ADS	AD conversion start	0: – 1: Start	R/W
ADCH3 to ADCH0	Analog input channel selection	0000: AIN0 0110: AIN6 0001: AIN1 0111: AIN7 0010: AIN2 1000: AIN8 0011: AIN3 1001: AIN9 0100: AIN4 1010 to 111: Reserved 0101: AIN5	

Note: Bit 7 of ADCR must be set to 1.

AD Conversion Register

ADREG (005BH)	7	6	5	4	3	2	1	0
	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0

(Initial Value: **** ****)
Read only

Figure 3.17.3 Registers for AD converter

3.18 Watchdog Timer (Runaway Detecting Timer)

TMP93CF76/CF77/CW76/CU76/CT76 contain a watchdog timer of Runaway detecting.

The watchdog timer (WDT) is used to return the CPU to the normal state when it detects that the CPU has started to malfunction (runaway) due to causes such as noise. When the watchdog timer detects a malfunction, it generates a non-maskable interrupt INTWD to notify the CPU of the malfunction.

Connecting the watchdog timer output to the reset pin internally forces a reset.

This watchdog timer consists of 22-stage binary counters.

These binary counters are also used as a warm-up timer for the internal oscillator stabilization. This is used for releasing the STOP and before changing system clock.

3.18.1 Block Diagram

Figure 3.18.1 shows the block diagram of the watchdog timer (WDT).

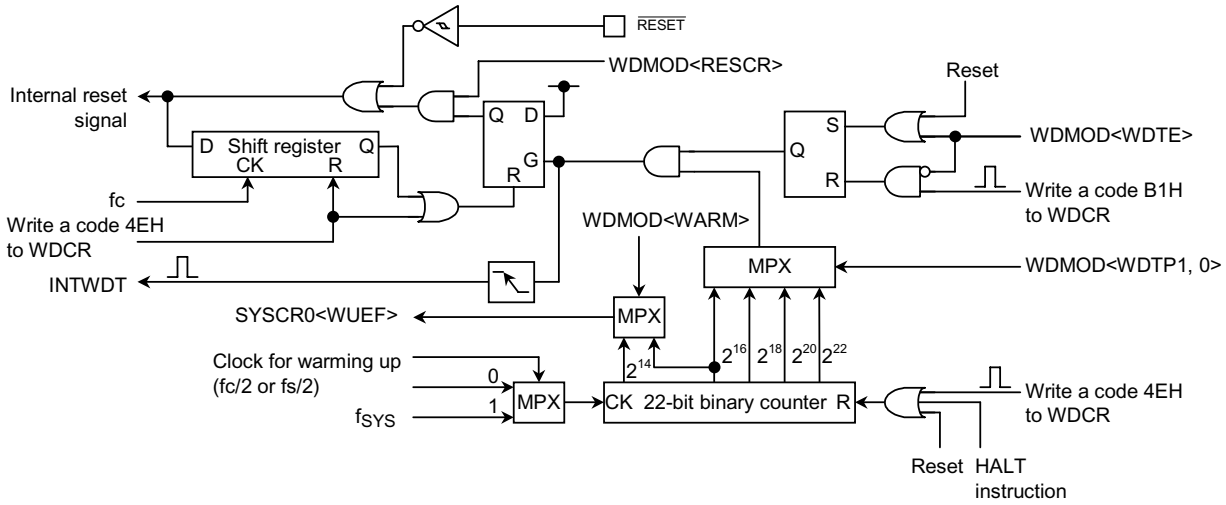


Figure 3.18.1 Composition of the Watchdog Timer/Warm-up Timer

The watchdog timer consists of 22-stage binary counters which use System clock (f_{SYS}) as the input clock. The 22-stage binary counter has $f_{SYS}/2^{16}$, $f_{SYS}/2^{18}$, $f_{SYS}/2^{20}$, and $f_{SYS}/2^{22}$ output. Selecting one of the outputs with the WDMOD<WDTP1, 0> register generates a watchdog interrupt and outputs watchdog timer out when an overflow occurs. The binary counter for the watchdog timer should be cleared to 0 with runaway detecting result software (instruction) before an interrupt occurs.

Example:

```
LDW     (WDMOD), 0B100H ;   disable
LD      (WDCR), 4EH     ;   write clear code
SET     7, (WDMOD)      ;   enable again
```

The runaway detecting result can also be connected to the reset pin internally. In this case, the watchdog timer resets itself.

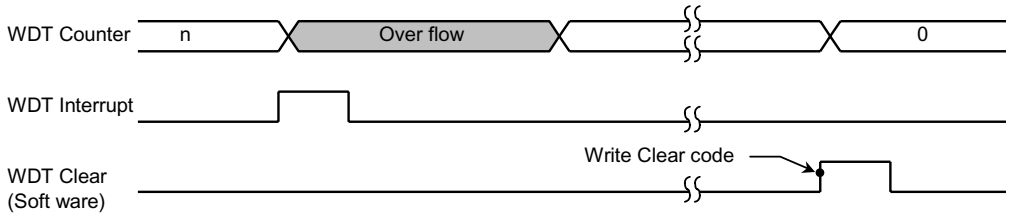


Figure 3.18.2 Normal Mode

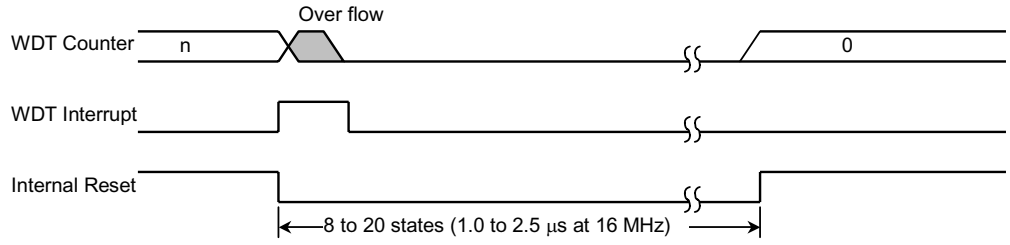


Figure 3.18.3 Reset mode

For warm-up counter, 2^{14} and 2^{16} output of 22-stage binary counter can be selected using WDMOD<WARM> register.

3.18.2 Control Registers

Watchdog timer WDT is controlled by two control registers WDMOD and WDCR.

(1) Watchdog Timer Mode Register (WDMOD)

a. Setting the detecting time of watchdog timer <WDTP>

This 2-bit register is used to set the watchdog timer interrupt time for detecting the runaway. This register is initialized to WDMOD<WDTP1, 0> = 00 when reset.

The detecting time of WDT is shown Table 3.18.1.

b. Watchdog timer enable/disable control register <WDTE>

When reset, WDMOD<WDTE> is initialized to 1 enable the watchdog timer.

To disable, it is necessary to set this bit to 0 and write the disable code (B1H) in the watchdog timer control register WDCR. This makes it difficult for the watchdog timer to be disabled by runaway.

However, it is possible to return from the disable state to enable state by merely setting <WDTE> to 1.

c. Watchdog timer out reset connection<RESCR>

This register is used to connect the output of the watchdog timer with $\overline{\text{RESET}}$ terminal, internally. Since WDMOD<RESCR>is initialized to 0 at reset, a reset by the watchdog timer will not be performed.

(2) Watchdog Timer Control Register (WDCR)

This register is used to disable and clear of binary counter the watchdog timer function.

- Disable control

By writting the disable code (B1H) in this WDCR register after clearing WDMOD<WDTE> to 0, the watchdog timer can be disabled.

```
WDMOD   ← 0 - - - - - X X   Clear WDMOD <WDTE> to 0.
WDCR    ← 1 0 1 1 0 0 0 1   Write the disable code (B1H).
```

Note: X:Don't care -: No change

- Enable control

Set WDMOD<WDTE>to 1.

- Watchdog timer clear control

The binary counter can be cleared and resume counting by writing clear code (4EH) into the WDCR register.

```
WDCR    ← 0 1 0 0 1 1 1 0   Write the clear code (4EH).
```

Watchdog Timer Mode Control Register

WDMOD (005CH)

7	6	5	4	3	2	1	0
WDTE	WDTP1	WDTP0	WARM	HALTM1	HALTM0	RESCR	DRVE

(Initial Value: 1000 0000)

WDTE	Watchdog timer Enable/Disable control	0: Disable 1: Enable	R/W
WDTP1, 0	WDT detection time	00: $2^{15}/f_{SYS}$ 01: $2^{17}/f_{SYS}$ 10: $2^{19}/f_{SYS}$ 11: $2^{21}/f_{SYS}$	
WARM	Warm-up timer source clock selection	0: 2^{14}/input frequency 0: 2^{17}/input frequency	
HALTM1, 0	HALT mode selection	00: RUN mode 01: STOP mode 10: IDLE1 11: IDLE2	
RESCR	Watchdog timeout control	0: Don't care 1: Connects WDT output to RESET internaly	
DRVE	Pin control of STOP mode	0: I/O off 1: Remains the state before HALT	

Watchdog Timer Control Register

WDCR (005DH)

7	6	5	4	3	2	1	0
WDCR7	WDCR6	WDCR5	WDCR4	WDCR3	WDCR2	WDCR1	WDCR0

(Initial Value: **** ****)

WDCR	Watchdog timer control	B1H: Disable code 4EH: Clear code Others: Don't care	Write only

Prohibit read-modify-write.

Figure 3.18.4 Watchdog timer control register

Table 3.18.1 Watchdog timer detecting time

at fc = 16 MHz, fs = 32.768 kHz

System clock selection <SYSCK>	Watchdog Timer Detecting Time WDMOD<WDTP1,0>			
	00	01	10	11
1(fs)	2.000 s	8.000 s	32.000 s	128.000 s
0(fc)	4.097 ms	16.384 ms	65.536 ms	262.144 ms

3.18.3 Operation

The watchdog timer generates interrupt INTWD after the detecting time set in the WDMOD<WDTP1, 0>. The watchdog timer must be zero-cleared by software before an INTWD interrupt is generated. If the CPU malfunctions (runaway) due to causes such as noise, but does not execute the instruction used to clear the binary counter, the binary counter overflows and an INTWD interrupt is generated. The CPU detects malfunction (runaway) due to the INTWD Interrupt and it is possible to return to normal operation by an anti-mulfunction program.

The watchdog timer restarts operation immediately after resetting is released.

The watchdog timer stops its operation in the IDLE1 and STOP modes.

Example 1: Clear the binary counter

```
WDCR    ← 0 1 0 0 1 1 1 0    Write clear code (4EH).
```

Example 2: Set the watchdog timer detecting time to $2^{17}/f_{SYS}$

```
WDMOD   ← 1 0 1 - - - X X
```

Example 3: Disable the watchdog timer

```
WDMOD   ← 0 - - - - - X X    Clear WDTE to 0.
WDCR    ← 1 0 1 1 0 0 0 1    Write disable code (B1H).
```

Example 4: Set the STOP mode (warming up time: $2^{16}/f_{SYS}$)

```
WDMOD   ← - - - 1 0 1 X X    Set the STOP mode.
Execute HALT command.        Set the HALT mode.
```

Note : X : Don't care -: No change

4. Electrical Characteristics

4.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Power Supply Voltage	Vcc	−0.5 to 6.5	V
Input Voltage	V_{IN}	−0.5 to Vcc+0.5	
Output Voltage (except PC, PD, PE, PF)	V_{OUT1}	−0.5 to Vcc+0.5	
Output Voltage (PC, PD, PE, PF)	V_{OUT2}	Vcc−40	
Output Current (except PC, PD, PE, PF) (per 1 pin)	I_{OH1}	−3.2	mA
Output Current (PC, PD) (per 1 pin)	I_{OH2}	−25	
Output Current (PE, PF) (per 1 pin)	I_{OH3}	−15	
Output Current (per 1 pin)	I_{OL}	3.2	
Output Current (total except PC, PD, PE, PF)	ΣI_{OH1}	−40	
Output Current (total of PC, PD, PE, PF)	ΣI_{OH2}	−120	
Output Current (total)	ΣI_{OL}	120	
Power Dissipation (Ta = 70°C)	PD	600	mW
Soldering Temperature	Tsolder	260	°C
Storage Temperature	Tstg	−65 to 150	
Operating Temperrature	Topr	−20 to 70	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2)

Ta = −20 to 70°C

Parameter		Symbol	Condition	Min	Typ.	Max	Unit
Power Supply Voltage		Vcc	fc = 4 to 16 MHz	4.5		5.5	V
			fs = 30 to 34 kHz	2.7			
Input Low Voltage	P0, P1, P2, P4, P9, PA, PB, PE, PF	V_{IL1} (CMOS)	Vcc = 2.7 to 5.5 V	−0.3		0.3 Vcc	V
	$\overline{RESET}$, P5, P7, P8	V_{IL2} (Schmitt)				0.25 Vcc	
	$\overline{TEST}$	V_{IL3} (Fixed)				0.3	
	X1	V_{IL4} (Xtal)				0.2 Vcc	
Input High Voltage	P0, P1, P2, P4, P9, PA, PB, PE, PF	V_{IH1} (CMOS)		0.7 Vcc		Vcc + 0.3	
	$\overline{RESET}$, P5, P7, P8	V_{IH2} (Schmitt)		0.75 Vcc			
	$\overline{TEST}$	V_{IH3} (Fixed)		Vcc − 0.3			
	X1	V_{IH4} (Xtal)		0.8 Vcc			

4.2 DC Characteristics (2/2)

Ta = −20 to 70°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Output Low Voltage	V_{OL}	IOL = 1.6 mA (Vcc = 2.7 to 5.5 V)			0.45	V
Output High Voltage	V_{OH}	IOH = −400 μA (Vcc = 2.7 to 5.5 V)	2.4			V
	V_{OH1}	IOH = −700 μA (Vcc = 4.5 to 5.5 V)	4.1			
PE, PF	I_{OH}	Vcc = 4.5 V VOH = 2.4 V	−5			mA
PC, PD			−15			
Input Leakage Current	I_{LI}	0.0 ≦ Vin ≦ V_{CC}		0.02	±5	μA
Output Leakage Current	I_{LO}	0.2 ≦ Vin ≦ V_{CC} -0.2		0.05	±10	
Power Down Voltage	V_{STOP}	VIL2 = 0.2 V_{CC}, VIH2 = 0.8 V_{CC}	2.0		6.0	V
$\overline{RESET}$ Pull Up Resistor	R_{RST}	Vcc = 5 V ± 10%	50		150	kΩ
		Vcc = 3 V ± 10%	80		200	
Pin Capacitance	C_{IO}	osc = 1 MHz/100 mVp-p			10	pF
Schmitt Width $\overline{RESET}$, P5,P7,P8	V_{TH}			1.0		V
NORMAL	Icc	Vcc = 5 V ± 10% fc = 16 MHz		30	50	mA
RUN				18	28	
IDLE2				15	25	
IDLE1				5	8	
SLOW		Vcc = 3 V ± 10% fs = 32.768 kHz (typ: V_{CC} = 3.0 V)		50	80	μA
RUN				30	45	
IDLE2				25	40	
IDLE1				12	25	
STOP		Vcc = 2.7 to 5.5 V		0.2	10	

Note 1: Typical value are for Ta = 25°C and Vcc = 5 V unless otherwise noted.

Note 2: Icc measurement conditions (NORMAL,SLOW).
Only CPU is operational;output pins are open and input pins are fixed.

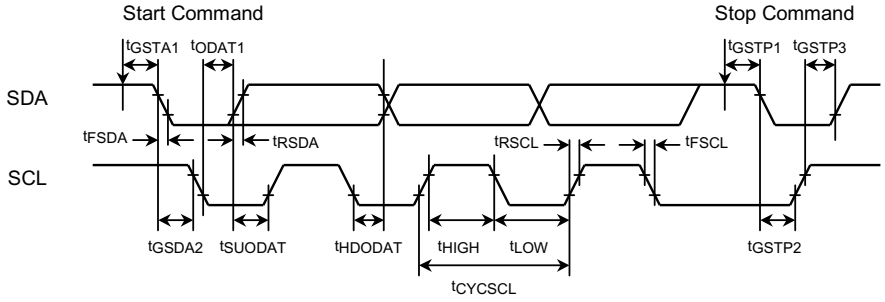
4.3 AD Conversion Characteristics

Ta = −20 to 70°C, V_{CC} = 4.5 to 5.5 V

Parameter	Symbol	Min	Typ.	Max	Unit
Analog Reference Voltage Supply	ADREF	Vcc − 1.5	Vcc	Vcc	V
	ADGND	Vss	Vss	Vss	V
Analog Input Voltage Range	V_{AIN}	ADGND	—	ADREF	V
Analog Current for ADREF	I_{REF}	—	1.0	1.5	mA
Total tolerance (excludes quantization error) (Ta = 25°C, Vcc = ADREF = 5 V)	E_T	—	—	±3	LSB

4.4 Serial Bus Interface Timing

(1) I²C bus Logic Timing



Parameter	Symbol	Min	Typ.	Max	Unit
SCL cycle	t_{CYCSCL}	2^N/fc	—	—	s
SCL low pulse width	t_{LOW}	—	2^{N-1}/fc	—	s
SCL High pulse width	t_{HIGH}	2^{N-1}/fc	—	—	s
SDA Rising Time (Note 1)	t_{RSDA}	—	—	—	s
SDA Falling Time (Note 1)	t_{FSDA}	—	—	—	s
SCL Rising Time (Note 1)	t_{RSCL}	—	—		s
SCL Falling Time (Note 1)	t_{FSCL}	—	—		s
The time from start command write to start sheecense	t_{GSTA1}	—	—	2^N/fc	s
Start condition hold time, start generation of the first clock after this	t_{GSTA2}	—	2^{N-1}/fc		s
Delay time from SCL falling to data output (Note 2)	t_{ODAT1}	—	—	5/fc	s
Set up time of data output for SCL rising (Note 2)	t_{SUODAT}	0	—	—	s
The time of holding data for SCL rising (Note 3)	t_{HODAT}	4/fc	—	—	s
The time from stop command write to starting stop sheecense	t_{GSTP1}	—	—	2^{N-1}/fc	s
The time from SDA falling to SCL rising (during stop sheecense)	t_{GSTP2}	2^{N-2}/fc	—	—	s
Stop condition set up time	t_{GSTP3}	2^{N-1}/fc	—	—	s

Note 1: The time of rising/falling depend on the feature of bus interface.

Note 2: The worst case is at the first bit of slave address.

Note 3: The worst case is at the acknowledge bit.

Note 4: N: dividing value set by I2CCR1 <SCK 2:0>.

SCK	N
000	6
001	7
010	8
011	9
100	10
101	11
110	12
111	reserved

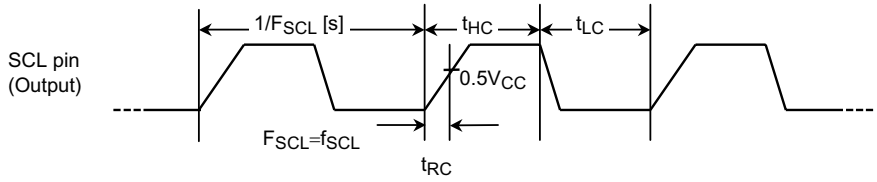
(2) Master SCL output timing

The I2CCR1 <SCK 2:0> are used to select a maximum transfer frequency directed from the SCL pin in the master mode.When rising time of the output clock (t_{RC}) is at least 8/fc [s], a high-level time of the output clock (t_{HC}) is t_{SCL}.

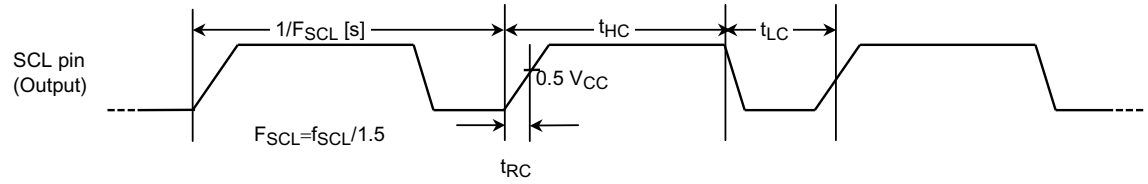
While the SCL line is fixed to low-level by a slave device,the output clock stops.

The first clock (t_{HC} [s]) after restart is $(t_{SCL}/2) \leq t_{HC} \leq t_{SCL}$.

(a) In case of $t_{RC} < (8/fc)$ [s] $t_{HC} = t_{LC} = t_{SCL}/2$ [s] ($t_{SCL} = 1/f_{SCL}$ [s])



(b) In case of $t_{RC} \geq (8/fc)$ [s] $t_{HC} = t_{SCL}$ [s] , $t_{LC} = t_{SCL}/2$ [s]



(3) Clock Syncro 8 bit SIO mode

1. SCK Input mode

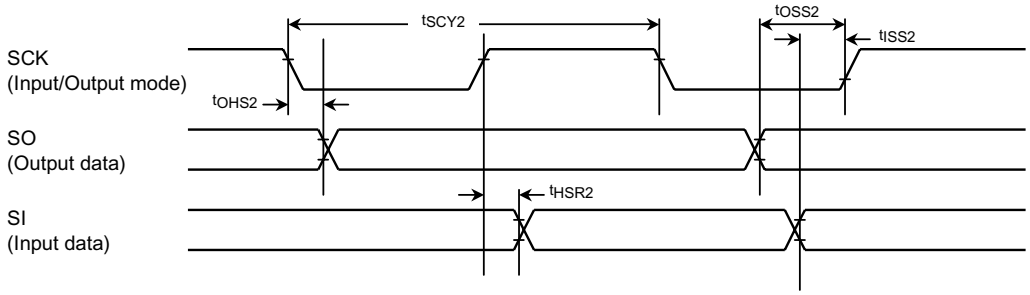
Parameter	Symbol	Expression		Unit
		Min	Max	
SCK cycle	t_{SCY2}	2^5X		s
SCK falling→Latch output data	t_{OHS2}	6X		s
Enable output data→SCK raising	t_{OSS2}		$t_{SCY2} - 16X$	s
SCK raising→Latch input data	t_{HSR2}	6X		ns
Enable input data→SCK raising	t_{ISS2}	0		ns

Note: $X=1/f_c$

2. SCK Output mode

Parameter	Symbol	Expression		Unit
		Min	Max	
SCK cycle	t_{SCY2}	2^5X	$2^{11}X$	s
SCK falling→Latch output data	t_{OHS2}	2X		s
Enable output data→SCK raising	t_{OSS2}		$t_{SCY2} - 2X$	s
SCK raising→Latch input data	t_{HSR2}	2X		s
Enable input data→SCK raising	t_{ISS2}	0		ns

Note: $X=1/f_c$



5. Table of Special Function Registers (SFR; Special Function Register)

The special function registers (SFRs) include the I/O ports and peripheral control registers allocated to the 144-byte addresses from 000000H to 00008FH.

Configuration of the table

Symbol	Name	Address	7	6	5	4	3	2	1	0
			Bit symbol							
			Read/Write							
			Value after Reset							
			Function							

Note: “Prohibit RMW” in the table means that you cannot use RMW instructions on these registers. The “LD” (transfer) instruction must be used to write for “Prohibit RMW” registers.

R/W : Read/Write
R : Read-only
W : Write-only
Prohibit RMW : Prohibit read-modify-write
(cannot be used the instruction such as RES,SET,TEST,CHG,STCF,ANDCF,ORCF,XORCF)

Don’t access (Reserved) addresses.

Table 5.1 I/O register address map

Address	Name	Address	Name	Address	Name	Address	Name	Address	Name
000000H	P0	20H	(Reserved)	40H	PWM1DRL	60H	TREG3L	80H	(Reserved)
1H	P1	21H	ODCR3	41H	PWM1DRH	61H	TREG3H	81H	I2CCR1
2H	P0CR	22H	(Reserved)	42H	PWM2DRL	62H	T1MOD	82H	I2CDBR
3H	(Reserved)	23H	TBCMOD	43H	PWM2DRH	63H	I2CFCR1	83H	I2CAR
4H	P1CR	24H	TBCDR0	44H	PWMDBR	64H	I2CFCR2	84H	I2CCR2
5H	(Reserved)	25H	TBCDR1	45H	PWMCR	65H	I2CFDBR	85H	(Reserved)
6H	P2	26H	TBCIF	46H	CAPINCR0	66H	SCBUF	86H	TPCR
7H	(Reserved)	27H	TRUN	47H	CAPINCR1	67H	SCMOD	87H	PC
8H	P2CR	28H	TCCR10	48H	CAPINCR2	68H	CAPINCR4	88H	PD
9H	(Reserved)	29H	TREG0	49H	CAPINCR3	69H	I2CFSR2	89H	PE
AH	P4	2AH	TREG1L	4AH	CAPFST	6AH	(Reserved)	8AH	PF
BH	P5	2BH	TREG1H	4BH	CAP0L	6BH	PAFC	8BH	PECR
CH	P5CR	2CH	TCCR32	4CH	CAP0M	6CH	SYSCR2	8CH	PFCR
DH	P7ICR	2DH	TCCR54	4DH	CAP0H	6DH	SYSCR3	8DH	HACR
EH	(Reserved)	2EH	TREG2L	4EH	CAP1L	6EH	SYSCR0	8EH	T5MOD
FH	P7	2FH	TREG2H	4FH	CAP1H	6FH	SYSCR1	8FH	ISCR
10H	(Reserved)	30H	(Reserved)	50H	CAP2L	70H	INT0CP1		
11H	P7CR	31H	(Reserved)	51H	CAP2H	71H	INTCP0TG0		
12H	(Reserved)	32H	TREG4L	52H	CAPCR	72H	INTTP1I2C		
13H	P7FC	33H	TREG4H	53H	RMTCR	73H	INTTBCVA		
14H	P8FC	34H	TREG5L	54H	VIVACR1	74H	INT12SIO		
15H	ODCR1	35H	TREG5H	55H	VIVACR2	75H	INT43		
16H	P8	36H	TPG0CR	56H	VASSDR	76H	INTT1T0		
17H	P9	37H	TPG0L	57H	CSYNCR	77H	INTT3T2		
18H	P8CR	38H	TPG0H	58H	PVCR	78H	INTT5T4		
19H	P9CR	39H	TPG0DR	59H	(Reserved)	79H	INTADRTC		
1AH	P9FC	3AH	TPG1L	5AH	ADMOD	7AH	(Reserved)		
1BH	ODCR2	3BH	TPG1H	5BH	ADREG	7BH	(Reserved)		
1CH	PA	3CH	TPG1DR	5CH	WDMOD	7CH	DMA0V		
1DH	PB	3DH	PWMRUN	5DH	WDCR	7DH	DMA1V		
1EH	PACR	3EH	PWM0DRL	5EH	IIMC0	7EH	DMA2V		
1FH	PBCR	3FH	PWM0DRH	5FH	IIMC1	7FH	DMA3V		

(1) System Control/RTC

Symbol	Name	Address	7	6	5	4	3	2	1	0
SYSCR0	System Clock Control Register0	00006EH	XEN	XTEN	RXEN	RXTEN	RSYSCK	WUEF	—	—
			R/W	R/W	R/W	R/W	R/W	R/W	(R/W)	(R/W)
			1	0	1	0	0	0	(0)	(0)
			High frequency oscillator (fc: 16 MHz) 0: Stop 1: Oscillation	Low frequency oscillator (fs: 32 kHz) 0: Stop 1: Oscillation	High frequency oscillator (fc) after released STOP mode 0: Stop 1: Oscillation	Low frequency oscillator (fs) after released STOP mode 0: Stop 1: Oscillation	System clock after releasing STOP mode 0: fc (Normal) 1: fs (Slow)	Warming up timer (Write) 0: Don't care 1: Start timer (Read) 0: End of warming up 1: Under warming up	Fix to 0.	Fix to 0.
SYSCR1	System Clock Control Register1	00006FH	—	—	—	—	SYSCK	—	—	—
			(R/W)				R/W	(R/W)	(R/W)	(R/W)
			(0)				(0)	(0)	(0)	(0)
			Fix to 0.				System clock 0: fc (Normal) 1: fs (Slow)	Fix to 0.	Fix to 0.	Fix to 0.
SYSCR2	System Clock Control Register2	00006CH	—	—		RTCCK	RTCST	RTCIS1	RTCIS0	
			(R/W)	(R/W)		R/W	R/W	R/W		
			(0)	(0)		0	0	0		
			Fix to 0.	Fix to 0.		RTC input clock source select 0: fs 1: fc/4 or fs/4	RTC count control 0: Stop& Clear 1: Start	Interval time control of RTC interrupt 00: $f_{SYS}/2^{16}$ or $fs/2^{15}$ 01: $f_{SYS}/2^{17}$ or $fs/2^{16}$ 10: $f_{SYS}/2^{15}$ or $fs/2^{14}$ 11: Reserved		

(2) Watch Dog Timer

Symbol	Name	Address	7	6	5	4	3	2	1	0
WDMOD	Watch Dog Timer Mode Register	00005CH	WDTE	WDTP1	WDTP0	WARM	HALTM1	HALTM0	RESCR	DRVE
			R/W	R/W		R/W	R/W		R/W	R/W
			1	0		0	0		0	0
			WDT timer Enable/ Disable control 0: Disable 1: Enable	WDT detection time 00: $2^{15}/f_{SYS}$ 01: $2^{17}/f_{SYS}$ 10: $2^{19}/f_{SYS}$ 11: $2^{21}/f_{SYS}$		Warming up timer source clock selection 0: 2^{14}/ selected clock frequency 1: 2^{16}/ selected clock frequency	HALT mode selection 00: RUN 01: STOP 10: IDLE1 11: IDLE2		WDT interal reset control 0: — 1: Connects WDT output to RESET internaly	Pin control of STOP mode 0: I/O off 1: Remains the state before HALT
WDCR	Watch Dog Timer Control Register	00005DH (Prohibit RMW)	—							
			Write-only							
			—							
			B1H: WDT disable code 4EH: WDT clear code							

(3) Time Base Counter (TBC) (1/2)

Symbol	Name	Address	7	6	5	4	3	2	1	0
TBCMOD	TBC Mode Register	000023H (Prohibit RMW)	—	—	TBC1E	TBC0E	INTTBC11	INTTBC10	INTTBC01	INTTBC00
			(R/W)	(R/W)	R/W		R/W		R/W	
			(0)	(0)	0		0		0	
			Fix to 0.	Fix to 0.	INTTBC interrupt enable/disable 00: Disable 01: INTTBC0 enable 10: INTTBC1 enable 11: INTTBC0/1 enable		TBC1 interrupt source clock selection 00: TBC12 01: TBC14 10: TBC16 11: TBC18		TBC0 interrupt source clock selection 00: TBC11 01: TBC13 10: TBC15 11: TBC17	
TBCDR0	TBC Data Register0	000024H	TBCD7 (TBC12)	TBCD6 (TBC11)	TBCD5 (TBC10)	TBCD4 (TBC9)	TBCD3 (TBC8)	TBCD2 (TBC7)	TBCD1 (TBC6)	TBCD0 (TBC5)
			Read-only							
			0							
			TBC12 to 5							
TBCDR1	TBC Data Register1	000025H	TBCD15 (TBC20)	TBCD14 (TBC19)	TBCD13 (TBC18)	TBCD12 (TBC17)	TBCD11 (TBC16)	TBCD10 (TBC15)	TBCD9 (TBC14)	TBCD8 (TBC13)
			Read-only							
			0							
			TBC20 to 13							

(3) Time Base Counter (TBC) (2/2)

Symbol	Name	Address	7	6	5	4	3	2	1	0
TBCIF	TBC Interrupt Flag Register	000026H (Prohibit RMW)	—	—	TBC1F	TBC0F		—		
			(R/W)	(R/W)	R/W			(R/W)		
			(0)	(0)	0			(0)		
			Fix to 0. Note: This bit is read as 1 always.	Fix to 0. Note: This bit is read as 1 always.	TBC1 interrupt request flag Write 0: Clear request flag 1: Don't set to 1. Read 0: – 1: Interrupt request	TBC0 interrupt request flag Write 0: Clear request flag 1: Don't set to 1. Read 0: – 1: Interrupt request		Fix to 0. Note: This bit is read as 1 always.		

(4) Timer Counter 0,1

Symbol	Name	Address	7	6	5	4	3	2	1	0
TRUN	Timer Start Control Register	000027H	—	—	T5RUN	T4RUN	T3RUN	T2RUN	T1RUN	T0RUN
					R/W					
					0					
							0:Stop	1:Run		
TCCR10	Timer Counter Control Register10	000028H (Prohibit RMW)	CLBC1	T1CL	T1CLK1	T1CLK0	CLBC0	T0CL	T0CLK1	T0CLK0
			R/W	R/W	R/W		R/W	R/W	R/W	
			0	0	0		0	0	0	
			TC1 counter clear by match 0: Disable 1: Enable	TC1 counter clear 0: — 1: Clear (One-shot)	TC1 source clock selection 00: TI1 (from P52) 01: TBC2 10: TBC4 11: TBC6		TC0 counter clear by match 0: Disable 1: Enable	TC0 counter clear 0: — 1: Clear (One-shot)	TC0 source clock selection 00: PCTLA (from CAPIN) 01: TI0 (from P52) 10: TBC6 11: TBC10	
TREG0	Timer Counter Register0	000029H (Prohibit RMW)	TC/TR07	TC/TR06	TC/TR05	TC/TR04	TC/TR03	TC/TR02	TC/TR01	TC/TR00
			R/W							
			0/*							
			W: Writing TREG0 register R: Reading TC0 counter							
TREG1L	Timer Counter Register1L	00002AH (Prohibit RMW)	TC/TR17	TC/TR16	TC/TR15	TC/TR14	TC/TR13	TC/TR12	TC/TR11	TC/TR10
			R/W							
			0/*							
			W: Writing TREG1L register R: Reading TC1L counter							
TREG1H	Timer Counter Register1H	00002BH (Prohibit RMW)	TC/TR1F	TC/TR1E	TC/TR1D	TC/TR1C	TC/TR1B	TC/TR1A	TC/TR19	TC/TR18
			R/W							
			0/*							
			W: Writing TREG1H register R: Reading TC1H counter							
T1MOD	Timer1 Mode Register	000062H (Prohibit RMW)					TFFRES	TFFSET	TO1ON	TO1SET
							W	W	W	W
							0	0	0	0
							TFF Reset 0: — 1: TFF reset (One-shot)	TFF set 0: — 1: TFF set (One-shot)	TO1 ON/OFF 0: TO1OFF 1: TO1ON	TO1 Set/Reset 0: Divided signal is passed TO1 1: TO1 set

*: Unknown after reset

(5) Timer Counter 2, 3

Symbol	Name	Address	7	6	5	4	3	2	1	0
TCCR32	Timer Counter Control Register32	00002CH (Prohibit RMW)	CLBC3	T3CL	T3CLK1	T3CLK0	CLBC2	T2CL	T2CLK1	T2CLK0
			R/W	R/W	R/W		R/W	R/W	R/W	
			0	0	0		0	0	0	
			TC3 counter clear by match 0: Disable 1: Enable	TC3 counter clear 0: — 1: Clear (One-shot)	TC3 source clock selection 00: TI3 (from P50) 01: TBC2 10: TBC4 11: TBC6		TC2 counter clear by match 0: Disable 1: Enable	TC2 counter clear 0: — 1: Clear (One-shot)	TC2 source clock selection 00: TI2 (from P51) 01: TBC2 10: TBC4 11: TBC6	
TREG2L	Timer Counter Register2L	00002EH (Prohibit RMW)	TC/TR27	TC/TR26	TC/TR25	TC/TR24	TC/TR23	TC/TR22	TC/TR21	TC/TR20
			R/W							
			0/*							
			W: Writing TREG2L register R: Reading TC2L counter							
TREG2H	Timer Counter Register2H	00002FH (Prohibit RMW)	TC/TR2F	TC/TR2E	TC/TR2D	TC/TR2C	TC/TR2B	TC/TR2A	TC/TR29	TC/TR28
			R/W							
			0/*							
			W: Writing TREG2H register R: Reading TC2H counter							
TREG3L	Timer Counter Register3L	000060H (Prohibit RMW)	TC/TR37	TC/TR36	TC/TR35	TC/TR34	TC/TR33	TC/TR32	TC/TR31	TC/TR30
			R/W							
			0/*							
			W: Writing TREG3L register R: Reading TC3L counter							
TREG3H	Timer Counter Register3H	000061H (Prohibit RMW)	TC/TR3F	TC/TR3E	TC/TR3D	TC/TR3C	TC/TR3B	TC/TR3A	TC/TR39	TC/TR38
			R/W							
			0/*							
			W: Writing TREG3H register R: Reading TC3H counter							

*: Unknown after reset

(6) Timer Counter 4, 5

Symbol	Name	Address	7	6	5	4	3	2	1	0
TCCR54	Timer Counter Control Register54	00002DH (Prohibit RMW)	CLBC5	T5CL	T5CLK1	T5CLK0	CLBC4	T4CL	T4CLK1	T4CLK0
			R/W	R/W	R/W		R/W	R/W	R/W	
			0	0	0		0	0	0	
			TC5 counter clear by match 0: Disable 1: Enable	TC5 counter clear 0: — 1: Clear (One-shot)	TC5 source clock selection 00: TI5 (from P50) 01: CSYNCA (from CSYNC) 10: TBC4 11: TBC6		TC4 counter clear by match 0: Disable 1: Enable	TC4 counter clear 0: — 1: Clear (One-shot)	TC4 source clock selection 00: TI4 (from P51) 01: CFGTM (from CAPIN) 10: TBC6 11: TBC10	
TREG4L	Timer Counter Register4L	000032H (Prohibit RMW)	TC/TR47	TC/TR46	TC/TR45	TC/TR44	TC/TR43	TC/TR42	TC/TR41	TC/TR40
			R/W							
			0/*							
			W: Writing TREG4L register R: Reading TC4L counter							
TREG4H	Timer Counter Register4H	000033H (Prohibit RMW)	TC/TR4F	TC/TR4E	TC/TR4D	TC/TR4C	TC/TR4B	TC/TR4A	TC/TR49	TC/TR48
			R/W							
			0/*							
			W: Writing TREG4H register R: Reading TC4H counter							
TREG5L	Timer Counter Register5L	000034H (Prohibit RMW)	TC/TR57	TC/TR56	TC/TR55	TC/TR54	TC/TR53	TC/TR52	TC/TR51	TC/TR50
			R/W							
			0/*							
			W: Writing TREG5L register R: Reading TC5L counter							
TREG5H	Timer Counter Register4H	000035H (Prohibit RMW)	TC/TR5F	TC/TR5E	TC/TR5D	TC/TR5C	TC/TR5B	TC/TR5A	TC/TR59	TC/TR58
			R/W							
			0/*							
			W: Writing TREG5H register R: Reading TC5H counter							
T5MOD	Timer5 Mode Register	00008EH								VSMOD
										R/W
										0
										TC5 function selection 0: Timer/ Event Counter 1: C.sync counter

*: Unknown after reset

(7) Capture Control (1/2)

Symbol	Name	Address	7	6	5	4	3	2	1	0
CAPINCR0	Capture Input Control Register0	000046H	CAP2E (CFG)	CAP1E (DFG)	CAP05E (DPG)	CAP04E (EXT)	CAP03E (CTL)	CAP02E (VS)	CAP01E (RMTD)	CAP00E (RMTU)
			R/W							
			0	0	0	0	0	0	0	0
			Capture 0,1, 2 input source enable/disable control 0: Disable 1: Enable							
CAPINCR1	Capture Input Control Register1	000047H	PCTLCK1	PCTLCK0	PCPR5	PCPR4	PCPR3	PCPR2	PCPR1	PCPR0
			R/W		R/W					
			0		0					
			CTL duty discrimination sampling clock selction (VIVACR2<PCTLCKS> = 0) 00: TBC3 01: TBC5 10: TBC7 11: TBC10		CTL signal (CTLIN) frequency division ratio 000000: 1/1 000001: 1/2 000010: 1/4 to 111111: 1/64					
CAPINCR2	Capture Input Control Register2	000048H	—	RMTST	RMTP0	RMTBP	CFGMCP	DPCP2	DPCP1	DPCP0
			(R/W)	R/W	R/W	R/W	R	R/W		
			(0)	0	0	0	0	0		
			Fix to 0.	RMTIN start/stop control 0: Stop& counter clear 1: Start	RMTIN input polarity selection 0: Positive 1: Negative	RMTIN noise chancellor control 0: Active 1: Bypass	CFG status flag 0: Normal 1: Error	DFG signal (DFGIN) frequency division ratio 000: 1/1 001: 1/2 to 111: 1/8		
CAPINCR3	Capture Input Control Register3	000049H	DIVCLR	CTLPO	CFGPO	DPGEG	DFGEG	CFGWPR	CFGEG	CTLEG
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	0	0	0	0	0
			DFG divider division ratio clear 0: — 1: Clear (One-shot)	CTL input polarity selection 0: Positive 1: Negative	CFG input polarity selection 0: Positive 1: Negative	DPG input edge selection 0: Rising edge 1: Both edges	DFG input edge selection 0: Rising edge 1: Falling edge	CFG input division ratio selection 0: 1/1 1: 1/2	CFG input edge selection 0: Both edges 1: Rising edge	CTLIN input edge selection 0: Rising edge 1: Both edges
CAPINCR4	Capture Input Control Register4	000068H	EXTEG		CFGPR5	CFGPR4	CFGPR3	CFGPR2	CFGPR1	CFGPR0
			R/W		R/W					
			0		0					
			EXT input edge selection 0: Rising edge 1: Both edges		CFG division ratio signal (CFGIN) frequency 000000: 1/1 000001: 1/2 000010: 1/4 to 111111: 1/64					

(7) Capture Control (2/2)

Symbol	Name	Address	7	6	5	4	3	2	1	0
CSYNCR	CSYNC Control Register	000057H	—		DPGST	CSYNCPO	SEPMOD	CSYNBP	—	MASK
			(R/W)		R/W	R/W	R/W	R/W	(R/W)	R/W
			(0)		0	0	0	0	(0)	0
			Fix to 0.		DPG detect monitor (Read) 0: — 1: DPG input detected (Write) 0: — 1: Reset (One-shot)	CSYNC input signal polarity selection 0: Positive 1: Negative	7-bit counter down count selection 0: TBC1 1: TBC2	C.sync bypass control 0: V.sync 1: Bypass	Fix to 0.	VSYNC mask control 0: — 1: Release masking (One-shot)
VIVACR2	VISS/ VASS Control Register2	000055H	PCTLPO	PCTLCKS	MSK1	MSK0	VISS3	VISS2	VISS1	VISS0
			R/W	R/W	R/W	R/W	R/W			
			0	0	0	0	0			
			CTL signal polarity selection 0: Positive (when duty < 50%, VIVACR1 <CTLDTY> = 1 1: Negative (when duty > 50%, VIVACR1 <CTLDTY> = 1	CTL duty measuring clock selection 0: Selected by CAPINCR1 <PCTLCK1, 2> 1: Automatic selection	CTLIN input division control 0: Divide 1: Bypass	CFG input masking control 0: Mask 1: Bypass	VISS compare data These 4-bit data are compared with higher 4-bit of the 6-bit CTL counter			

(8) Capture 0

Symbol	Name	Address	7	6	5	4	3	2	1	0
CAPFST	Capture0 FIFO Status Register	00004AH	CAPF7 (FIFO8)	CAPF6 (FIFO7)	CAPF5 (FIFO6)	CAPF4 (FIFO5)	CAPF3 (FIFO4)	CAPF2 (FIFO3)	CAPF1 (FIFO2)	CAPF0 (FIFO1)
			Read-only							
			0							
			Capture0 FIFO status 0: No capture data, 1: Capture data present in FIFO							
CAP0L	Capture0 Data Register – Low order	00004BH	CAP0D7	CAP0D6	CAP0D5	CAP0D4	CAP0D3	CAP0D2	CAP0D1	CAP0D0
			Read-only							
			*	*	*	*	*	*	*	*
CAP0M	Capture0 Data Register – Middle order	00004CH	CAP0D15	CAP0D14	CAP0D13	CAP0D12	CAP0D11	CAP0D10	CAP0D9	CAP0D8
			Read-only							
			*	*	*	*	*	*	*	*
CAP0H	Capture0 Data Register – High order	00004DH	CAP0T5	CAP0T4	CAP0T3	CAP0T2	CAP0T1	CAP0T0	CAP0D17	CAP0D16
			Read-only						Read-only	
			*	*	*	*	*	*	*	*
			Trigger input status 0: No trigger input 1: Trigger input accepted in FIFO						Capture0 higher data register	

*: Unknown after reset

(9) Capture 1, 2

Symbol	Name	Address	7	6	5	4	3	2	1	0
CAP1L	Capture1 Data Register – Low order	00004EH	CAP1D7	CAP1D6	CAP1D5	CAP1D4	CAP1D3	CAP1D2	CAP1D1	CAP1D0
			Read-only							
			*	*	*	*	*	*	*	*
CAP1H	Capture1 Data Register – High order	00004FH	CAP1D15	CAP1D14	CAP1D13	CAP1D12	CAP1D11	CAP1D10	CAP1D9	CAP1D8
			Read-only							
			*	*	*	*	*	*	*	*
CAP2L	Capture2 Data Register – Low order	000050H	CAP2D7	CAP2D6	CAP2D5	CAP2D4	CAP2D3	CAP2D2	CAP2D1	CAP2D0
			Read-only							
			*	*	*	*	*	*	*	*
CAP2H	Capture2 Data Register – High order	000051H	CAP2D15	CAP2D14	CAP2D13	CAP2D12	CAP2D11	CAP2D10	CAP2D9	CAP2D8
			Read-only							
			*	*	*	*	*	*	*	*

*: Unknown after reset

(10) Timing Pulse Generator 0 (TPG 0)

Symbol	Name	Address	7	6	5	4	3	2	1	0
TPG0CR	TPG0 Control Register	000036H (Prohibit RMW)	—		FEMPIE	TPFUL0	TPEMP0	TPF02	TPF01	TPF00
			(W)		W	R	R	R		
			(0)		0	0	1	0		
			Fix to 0.		INTTPG0 FIFO empty interrupt 0: Disable 1: Enable	TPG0 FIFO full flag 0: — 1: FIFO full	TPG0 FIFO empty flag 0: — 1: FIFO empty	TPG0 FIFO status flag 000: Empty or Full 001: 1 word 010: 2 word 011: 3 word 100: 4 word 101: 5 word 110: 6 word 111: 7 word		
TPG0L	TPG0 Lower Timing Data Register	000037H (Prohibit RMW)	TPG0D7	TPG0D6	TPG0D5	TPG0D4	TPG0D3	TPG0D2	TPG0D1	TPG0D0
			Write-only							
			*	*	*	*	*	*	*	*
TPG0H	TPG0 Higher Timing Data Register	000038H (Prohibit RMW)	TPG0DF	TPG0DE	TPG0DD	TPG0DC	TPG0DB	TPG0DA	TPG0D9	TPG0D8
			Write-only							
			*	*	*	*	*	*	*	*
TPG0DR	TPG0 Output Data Register	000039H (Prohibit RMW)			TPGD05	TPGD04	TPGD03	TPGD02	TPGD01	TPGD00
					Write-only					
					*	*	*	*	*	*
CAPCR	Capture Control Register	000052H (Prohibit RMW)	CAP2T (CFG)	CAP1T (DFG)	CAPCL	VISFRS	VASFRS	TPRS0	CFGCL	CAFRS
			R	R	R/W					
			0	0	0	0	0	0	0	0
			CAP2 trigger input status 0: No trigger input 1: Trigger input	CAP1 trigger input status 0: No trigger input 1: Trigger input	CAP1/ CAP2 status clear 0: — 1: Clear (One-shot)	VISS detect flag clear 0: — 1: Clear (One-shot)	VASS detect flag clear 0: — 1: Clear (One-shot)	TPG0 FIFO counter clear 0: — 1: Clear (One-shot)	CFG flag clear 0: — 1: Clear (One-shot)	Capture0 FIFO counter/ status clear 0: — 1: Clear (One-shot)

*: Unknown after reset

(11) Timing Pulse Generator 1(TPG1)

Symbol	Name	Address	7	6	5	4	3	2	1	0
TPG1L	TPG1 Lower Timing Data Register	00003AH (Prohibit RMW)	TPG1D7 (TBC10)	TPG1D6 (TBC9)	TPG1D5 (TBC8)	TPG1D4 (TBC7)	TPG1D3 (TBC6)	TPG1D2 (TBC5)	TPG1D1 (TBC4)	TPG1D0 (TBC3)
			Write-only							
			0	0	0	0	0	0	0	0
			TPG1 lower data register							
TPG1H	TPG1 Higher Timing Data Register	00003BH (Prohibit RMW)	TPG1DF (TBC18)	TPG1DE (TBC17)	TPG1DD (TBC16)	TPG1DC (TBC15)	TPG1DB (TBC14)	TPG1DA (TBC13)	TPG1D9 (TBC12)	TPG1D8 (TBC11)
			Write-only							
			0	0	0	0	0	0	0	0
			TPG1 higher data register							
TPG1DR	TPG1 Output Data Register	00003CH (Prohibit RMW)					TPGD13 (TPG13)	TPGD12 (TPG12)	TPGD11 (TPG11)	TPGD10 (TPG10)
							Write			
							0	0	0	0
							TPG1 output data register			

(12) 8-bit PWM

Symbol	Name	Address	7	6	5	4	3	2	1	0
PWMDBR	8-bit PWM Data Buffer Register	000044H (Prohibit RMW)	PWM3DBR7	PWM3DBR6	PWM3DBR5	PWM3DBR4	PWM3DBR3	PWM3DBR2	PWM3DBR1	PWM3DBR0
			Write-only							
			*	*	*	*	*	*	*	*
PWMCR	8-bit PWM Control Register	000045H (Prohibit RMW)	PWMEOT				PWMC3	PWMC2	PWMC1	PWMC0
			R				Write-only			
			0				0			
			End of data Transfer PWM data transfer 0:End of transfer 1:Under transfer				PWM data transfer request These bits must be cleared to 0.			

*: Unknown after reset

(13) 14-bit PWM 0,1, 2

Symbol	Name	Address	7	6	5	4	3	2	1	0
PWMRUN	PWM Start Control Register	00003DH						PWM2RUN	PWM1RUN	PWM0RUN
								R/W		
								0	0	0
								0: Stop 1: Start		
PWM0DRL	PWM0 lower Data Register	00003EH (Prohibit RMW)	PWM0D7	PWM0D6	PWM0D5	PWM0D4	PWM0D3	PWM0D2	PWM0D1	PWM0D0
			Write-only							
			*	*	*	*	*	*	*	*
PWM0DRH	PWM0 Higher Data Register	00003FH (Prohibit RMW)			PWM0DD	PWM0DC	PWM0DB	PWM0DA	PWM0D9	PWM0D8
					Write-only					
					*	*	*	*	*	*
PWM1DRL	PWM1 Lower Data Register	000040H (Prohibit RMW)	PWM1D7	PWM1D6	PWM1D5	PWM1D4	PWM1D3	PWM1D2	PWM1D1	PWM1D0
			Write-only							
			*	*	*	*	*	*	*	*
PWM1DRH	PWM1 Higher Data Register	000041H (Prohibit RMW)			PWM1DD	PWM1DC	PWM1DB	PWM1DA	PWM1D9	PWM1D8
					Write-only					
					*	*	*	*	*	*
PWM2DRL	PWM2 Lower Data Register	000042H (Prohibit RMW)	PWM2D7	PWM2D6	PWM2D5	PWM2D4	PWM2D3	PWM2D2	PWM2D1	PWM2D0
			Write-only							
			*	*	*	*	*	*	*	*
PWM2DRH	PWM2 Higher Data Register	000043H (Prohibit RMW)			PWM2DD	PWM2DC	PWM2DB	PWM2DA	PWM2D9	PWM2D8
					Write-only					
					*	*	*	*	*	*

*: Unknown after reset

(14) CSYNC

Symbol	Name	Address	7	6	5	4	3	2	1	0
CSYNCR	CSYNC Control Register	000057H	—		DPGST	CSYNCPO	SEPMOD	CSYNBP	—	MASK
			(R/W)		R/W	R/W	R/W	R/W	(R/W)	R/W
			(0)		0	0	0	0	(0)	0
			Fix to 0.		DPG detect monitor (Read) 0: — 1: DPG input detected (Write) 0: — 1: Reset (One-shot)	CSYNC input signal polarity selection 0: Positive 1: Negative	7-bit counter down count selection 0: TBC1 1: TBC2	C.sync bypass control 0: V.sync 1: Bypass	Fix to 0.	VSYNC mask control 0: — 1: Release masking (One-shot)

(15) PV

Symbol	Name	Address	7	6	5	4	3	2	1	0
PVCR	PV Control Register	000058H					HPMIX	PVSEL2	PVSEL1	PVSEL0
							R/W	R/W		
							0	0		
							Insert HP to pseudo V.sync 0: Disable 1: Enable	PV/PH output format control		

(16) VISS/VASS

Symbol	Name	Address	7	6	5	4	3	2	1	0
VIVACR1	VISS/ VASS Control Register1	000054H (Prohibit RMW)	—					CTLDTY	VISSFL	VASSFL
			(W)					R	R	R
			(0)					1	0	0
			Fix to 0.					CTL signal duty detector monitor flag 0:CTL duty ≥ 50% (VIVACR2 <PCTLPO> = 0) 1: CTL duty < 50% (VIVACR2 <PCTLPO> = 0)	VISS detect flag 0: — 1: VISS detected	VASS detect flag 0: — 1: VASS detected
VIVACR2	VISS/ VASS Control Register2	000055H	PCTLPO	PCTLCKS	MSK1	MSK0	VISS3	VISS2	VISS1	VISS0
			R/W	R/W	R/W	R/W	R/W			
			0	0	0	0	0			
			CTL signal polarity selection 0: Positive (when duty < 50%, VIVACR1 <CTLDTY> = 1 1: Negative (when duty > 50%, VIVACR1 <CTLDTY> = 1	CTL duty measuring clock selection 0: Selected by CAPINCR1 <PCTLCK1, 2> 1: Automatic selection	CTLIN input division control 0: Divide 1: Bypass	CFG input masking control 0: Mask 1: Bypass	VISS compare data These 4-bit data are compared with higher 4-bit of the 6-bit CTL counter			
VASSDR	VASS Data Register	000056H	VASS7	VASS6	VASS5	VASS4	VASS3	VASS2	VASS1	VASS0
			VASS lower 8-bit data							
			VASS15	VASS14	VASS13	VASS12	VASS11	VASS10	VASS9	VASS8
			VASS higher 8-bit data							
			Read-only							
			*	*	*	*	*	*	*	*
			Twice reading from VASSDR The First is lower 8-bit, the second is higher 8-bit							

*: Unknown after reset

(17) Remote Control Input (RMTIN)

Symbol	Name	Address	7	6	5	4	3	2	1	0
RMTCR	RMTIN Signal Input Control Register	000053H	RMTD7	RMTD6	RMTD5	RMTD4	RMTD3	RMTD2	RMTD1	RMTD0
			R/W				R/W			
			0				0			
			Width of H noise cancellation 4-bit data (TBC8:32 µs)				Width of L noise cancellation 4-bit data (TBC8:32 µs)			

(18) HA/CR

Symbol	Name	Address	7	6	5	4	3	2	1	0
HACR	Head Amp Control Register	00008DH	VTPPO1	VTPPO0	TPVASEL	DFFPO1	DFFPO0	COMPS	CRPO	HAPO
			R/W							
			0	0	0	0	0	0	0	0
			TPG03 (P92) edge selection 0: Rising edge 1: Falling edge	TPG03 (P90) edge selection 0: Rising edge 1: Falling edge	P91 output selection 0: TPG01 1: VASWP	TPG03 input polarity selector 0: Positive 1: Negative	TPG03 input polarity selector 0: Positive 1: Negative	Enable COMPIN 0: Disable 1: Enable	CR output polarity selector 0: Positive 1: Negative	HA output polarity selector 0: Positive 1: Negative

(19) 8-bit AD Converter

Symbol	Name	Address	7	6	5	4	3	2	1	0
ADMOD	AD Converter Control Register	00005AH	—	EOCF	ADBF	ADS	ADCH3	ADCH2	ADCH1	ADCH0
			(R/W)	R	R	R/W	R/W			
			(1)	0	0	0	0			
			Fix to 1.	AD conversion complete flag 0: AD conversion in progress or before conversion 1: AD conversion completed	AD conversion busy flag 0: AD conversion stopped 1: AD conversion in progress	AD conversion start 0: — 1: start	Analog channel selection 0000: AIN0 0110: AIN6 0001: AIN1 0111: AIN7 0010: AIN2 1000: AIN8 0011: AIN3 1001: AIN9 0100: AIN4 1010 to 1111: Reserved 0101: AIN5			
ADREG	AD Converted Register	00005BH	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
			Read-only							
			Undefined after reset							

(20) SIO

Symbol	Name	Address	7	6	5	4	3	2	1	0
SCBUF	SIO Buffer Register	000066H (Prohibit RMW)	TRB7	TRB6	TRB5	TRB4	TRB3	TRB2	TRB1	TRB0
			R/W							
			Undefined after reset							
SCMOD	SIO Control Register	000067H (Prohibit RMW)	FFSI	SRES	SMD1	SMD0	SIFT	CLKSI	SCKS	SIOE
			R	R/W	R/W		R/W	R/W	R/W	R/W
			1	0	0		0	0	0	0
			Serial transfer monitor flag 0: Under transfer-ring 1: Stop	Serial transfer terminate 0: — 1: Terminate (One-shot)	Serial transfer mode select 00: Transmit mode 01: Receive mode 10: reserved 11: Transmit/receive mode		Serial transfer shift edge select 0: Leading edge 1: Trailing edge	Serial transfer internal clock rate select 0: $2^3/f_{SYS}$ 1: $2^7/f_{SYS}$	Serial transfer clock selection 0: Internal clock 1: External clock	Serial transfer start 0: Stop 1: Start
ISCR	Interrupt Source Control Register	00008FH	SELINT							
			R/W							
			0							
			0: INT2 1: INTSIO							

(21) I²C bus (1)

Symbol	Name	Address	7	6	5	4	3	2	1	0
I2CCR1	I²C bus Control Register1	000081H (Prohibit RMW)	—	—	—	ACK	CHS	SCK2	SCK1	SCK0
			(W)			R/W	R/W	W		
			(0)	(0)	(0)	0	0	0	0	0
			These bits must be cleared to “0”			0: Acknowledge not retured to transmitter 1: Acknowledge retured to transmitter	Channel selection 0: Channel0 (SCL0, SDA0) 1: Channel1 (SCL1, SDA1)	Serial clock selection 000: 250 kHz 100: 15.6 kHz 001: 125 kHz 101: 7.8 kHz 010: 62.5 kHz 110: 3.9 Hz 011: 31.2 kHz 111: (Reserved) at fc = 16 MHz		
I2CDBR	I²C bus Data Buffer Register	000082H (Prohibit RMW)	I2DBR7	I2DBR6	I2DBR5	I2DBR4	I2DBR3	I2DBR2	I2DBR1	I2DBR0
			R/W							
			Undefined after reset							
			Can not be read a written data							
I2CAR	I²C bus Address Register	000083H (Prohibit RMW)	SA6	SA5	SA4	SA3	SA2	SA1	SA0	ALS
			Write-only							W
			0	0	0	0	0	0	0	0
			slave address selection							Address recognition mode specification 0: Slave address recognition 1: Non slave address recognition

(21) I²C bus (2)

Symbol	Name	Address	7	6	5	4	3	2	1	0
I2CCR2	I²C bus Control Register2	000084H (Prohibit RMW)	MST	TRX	BB	PIN	SBIM1	SBIM0	—	—
			Write-only							
			0	0	0	1	0	0	(0)	(0)
			Master/ slave selection 0: Slave 1: Master	Transmitter /receiver selection 0: Receiver 1: Transmit-ter	Start/stop condition generation 0: Stop condition 1: Start condition	Cancel interrupt service request 0: — 1: Cancel interrupt service request	Serial bus interface operation mode selection 00: Port mode 01: (Reserved) 10: I²C bus mode 11: (Reserved)		Fix to 0.	Fix to 0.
I2CSR	I²C bus Status Register	000084H	MST	TRX	BB	PIN	—	AAS	AD0	LRB
			Read-only							
			0	0	0	1	—	0	0	1
			Status monitor 0: Slave 1: Master	Status monitor 0: Receiver 1: Transmit-ter	Status monitor 0: Bus free 1: Bus busy	Interrupt request monitor 0: Request 1: Release		Slave address match detection monitor 0: — 1: Slave address match or GENERAL CALL detected	"GENERAL CALL" detection monitor 0: — 1: GENERAL CALL detected	Last received bit monitor 0: Last received bit 0 1: Last received bit 1

(21) I²C bus (3)

Symbol	Name	Address	7	6	5	4	3	2	1	0
I2CFCR1	I²C bus FIFO Control Register1	000063H (Prohibit RMW)	T/$\overline{R}$	FSCK			CONT	BYTE		
			Write-only							
			0	0			0	0		
			FIFO transfer mode selection 0: Receive mode 1: Transmit mode	Serial transfer clock selection Serial clock selection 000: fc/2^6(250 kHz) 100: fc/2^{10}(15.6 kHz) 001: fc/2^7(125 kHz) 101: fc/2^{11}(7.8 kHz) 010: fc/2^8(62.5 kHz) 110: fc/2^{12}(3.9 Hz) 011: fc/2^9(31.2 kHz) 111: (Reserved) at fc = 16 MHz			Data transfer mode selection 0: Data transfer mode every bit 1: Series data transfer mode	Transfer data byte control 000: 1 byte 100: 5 byte 001: 2 byte 101: 6 byte 010: 3 byte 110: 7 byte 011: 4 byte 111: 8 byte These are enable when <CONT> = 0.		
I2CFCR2	I²C bus FIFO Control Register2	000064H (Prohibit RMW)	$\overline{START}$	$\overline{STOP}$	CHS	$\overline{INT}$	—	—	$\overline{RST}$	—
			W	W	W	W			W	
			1	1	0	1	—	—	1	—
			FIFO buffer transfer start 0: Start/ Restart 1: —	FIFO buffer transfer stop 0: Stop 1: —	I/O channel selection 0: Channel0 (SCL0, SDA0) 1: Channel1 (SCL1, SDA1)	Next transfer start(series data transfer mode) 0: start next transfer 1: —			I2C bus/FIFO control system reset 0: Reset 1: —	
I2CFDBR	I²C bus FIFO Data Buffer Register	000065H (Prohibit RMW)	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
			R/W							
			Undefined after reset							
			Can not be read written data.							

(21) I²C bus (4)

Symbol	Name	Address	7	6	5	4	3	2	1	0
I2CFSR1	I²C bus FIFO Status Register1	000064H	SDA	END	CHS	BUSY	FULL	EMPTY	SCERR	AKERR
			Read-only							
			—	0	0	0	0	0	0	0
			SDA bus monitor 0: Low level 1: High level	FIFO buffer status flag 0: — 1: Finished transfer I2CFCR2 <STOP> = 0 then clear	I/O channel monitor 0: Channel0 1: Channel1	FIFO buffer transfer status monitor 1: Under FIFO buffer data transfer I2CFCR2 <STOP> = 0 then clear	FIFO buffer full/ Receive finishing monitor 0: — 1: FIFO buffer full/ finish receiver	FIFO buffer empty/ transmitter finishing monitor 0: — 1: FIFO buffer empty/ finish transmit-ter	Start con-dition error detector 0: — 1: start condition error genera-tion	Acknow-ledge error detector 0: — 1: Acknow-ledge error genera-tion
I2CFSR2	I²C bus FIFO Status Register2	000069H	NOMAT	LRBM	—	—	—	—	—	—
			R	R						
			0	1	Undefined after reset					
			SCL output/ SCL line matching monitor 0: — 1: SCL line is low by slave device	Last receive monitor (Acknow-ledge monitor) 0: Last receive bit 0 (Acknow-ledge) 1: Last receive bit 1 (Non-Acknow-ledge)						

r

(22) Interrupt priority setting register(1/2)

Symbol	Name	Address	7	6	5	4	3	2	1	0
INT0CP1	INT0/	0070H	INTCAP1				INT0			
	CAP1	(Prohibit	ICAP1C	ICAP1M2	ICAP1M1	ICAP1M0	I0C	I0M2	I0M1	I0M0
	Interrupt	RMW)	R/W	W	W	W	R/W	W	W	W
	Register		0	0	0	0	0	0	0	0
INTCP0TG0	CAP0/	0071H	INTTPG0				INTCAP0			
	TPG0	(Prohibit	ITPG0C	ITPG0M2	ITPG0M1	ITPG0M0	ICAP0C	ICAP0M2	ICAP0M1	ICAP0M0
	Interrupt	RMW)	R/W	W	W	W	R/W	W	W	W
	Register		0	0	0	0	0	0	0	0
INTTP1I2C	TPG1/	0072H	INTI2CB				INTTPG1			
	I^2CBUS	(Prohibit	II2CC	II2CM2	II2CM1	II2CM0	ITPG1C	ITPG1M2	ITPG1M1	ITPG1M0
	Interrupt	RMW)	R/W	W	W	W	R/W	W	W	W
	Register		0	0	0	0	0	0	0	0
INTTBCVA	TBC/	0073H	INTVA				INTTBC			
	VA	(Prohibit	IVAC	IVAM2	IVAM1	IVAM0	ITBCC	ITBCM2	ITBCM1	ITBCM0
	Interrupt	RMW)	R/W	W	W	W	R/W	W	W	W
	Register		0	0	0	0	0	0	0	0
INT12SIO	INT1/	0074H	INT2/SIO				INT1			
	INT2/	(Prohibit	I2C	I2M2	I2M1	I2M0	I1C	I1M2	I1M1	I1M0
	SIO	RMW)	/SIOC	/SIOM2	/SIOM1	/SIOM0				
	Interrupt		R/W	W	W	W	R/W	W	W	W
	Register		0	0	0	0	0	0	0	0
INT43	INT3/	0075H	INT4				INT3			
	INT4	(Prohibit	I4C	I4M2	I4M1	I4M0	I3C	I3M2	I3M1	I3M0
	Interrupt	RMW)	R/W	W	W	W	R/W	W	W	W
	Register		0	0	0	0	0	0	0	0
INTT1T0	Timer0/	0076H	INTT1				INTT0			
	Timer1	(Prohibit	IT1C	IT1M2	I1TM1	IT1M0	IT0C	IT0M2	IT0M1	IT0M0
	Interrupt	RMW)	R/W	W	W	W	R/W	W	W	W
	Register		0	0	0	0	0	0	0	0
INTT3T2	Timer2/	0077H	INTT3				INTT2			
	Timer3	(Prohibit	IT3C	IT3M2	IT3M1	IT3M0	IT2C	IT2M2	IT2M1	IT2M0
	Interrupt	RMW)	R/W	W	W	W	R/W	W	W	W
	Register		0	0	0	0	0	0	0	0
INT5T4	Timer4/	0078H	INTT5				INTT4			
	Timer5	(Prohibit	IT5C	IT5M2	IT5M1	IT5M0	IT4C	IT4M2	IT4M1	IT4M0
	Interrupt	RMW)	R/W	W	W	W	R/W	W	W	W
	Register		0	0	0	0	0	0	0	0

(22) Interrupt priority setting register (2/2)

Symbol	Name	Address	7	6	5	4	3	2	1	0
INTADRTC	AD/	0079H	INTRTC				INTAD			
	RTC	(Prohibit	IRTCC	IRTM2	IRTM1	IRTM0	IADC	IADM2	IADM1	IADM0
	Interrupt	RMW)	R/W	W	W	W	R/W	W	W	W
	Setting		0	0	0	0	0	0	0	0

IxxM2	IxxM1	IxxM0	Function (Write)
0	0	0	Prohibit interrupt request.
0	0	1	Set interrupt request level to 1.
0	1	0	Set interrupt request level to 2.
0	1	1	Set interrupt request level to 3.
1	0	0	Set interrupt request level to 4.
1	0	1	Set interrupt request level to 5.
1	1	0	Set interrupt request level to 6.
1	1	1	Prohibit interrupt request.

IxxC	Function (Read)	Function (Write)
0	Indicates no interrupt request.	Clears interrupt request flag.
1	Indicates interrupt request.	Don't care

Note 1: Read-modify-write is prohibited.

Note 2: Note about clearing interrupt request flag.

The interrupt request flag of INTCAP1, INTCAP0, INTSIO0, INTSIO1, INTRX and INTAD are not cleared by writing 0 to IxxC of they are level interrupts.

They can be cleared only by resetting, reading captured data/ADREG/SC2BUF or reading/writing SC0BUF/SC1BUF.

Note 3: Note about clearing interrupt request flag.

When the INTTPG0 is used for a FIFO empty interrupt (a level signal), the interrupt controller also leaves a request flag (Flip/Flop) after clearing FIFO empty by setting next TPG0 data in an interrupt routin.

Therefore, in this case, the INTTPG0 request flag has to be cleared before executing RETI instruction.

Symbol	Name	Address	7	6	5	4	3	2	1	0
ISCR	Interrupt	00008FH	SELINT	—	—	—	—	—	—	—
	Source		R/W							
	Control		0							
	Register		0: INT2 1: SIO							

(23) Micro DMA Start Vector

Symbol	Name	Address	7	6	5	4	3	2	1	0
DMA0V	micro DMA0 Start Vector	00007CH (Prohibit RMW)			DMA0V5	DMA0V4	DMA0V3	DMA0V2	DMA0V1	DMA0V0
					Write-only					
					0					
					Set micro DMA start vector					
DMA1V	micro DMA1 Start Vector	00007DH (Prohibit RMW)			DMA1V5	DMA1V4	DMA1V3	DMA1V2	DMA1V1	DMA1V0
					Write-only					
					0					
					Set micro DMA start vector					
DMA2V	micro DMA2 Start Vector	00007EH (Prohibit RMW)			DMA2V5	DMA2V4	DMA2V3	DMA2V2	DMA2V1	DMA2V0
					Write-only					
					0					
					Set micro DMA start vector					
DMA3V	micro DMA3 Start Vector	00007FH (Prohibit RMW)			DMA3V5	DMA3V4	DMA3V3	DMA3V2	DMA3V1	DMA3V0
					Write-only					
					0					
					Set micro DMA start vector					

(24) Port0

Symbol	Name	Address	7	6	5	4	3	2	1	0
P0	Port0 data Register	000000H	P07	P06	P05	P04	P03	P02	P01	P00
			R/W							
			0	0	0	0	0	0	0	0
P0CR	Port0 Control Register	000002H (Prohibit RMW)	P07C	P06C	P05C	P04C	P03C	P02C	P01C	P00C
			Write-only							
			0	0	0	0	0	0	0	0
			0: Input mode 1: Output mode							

(25) Port1

Symbol	Name	Address	7	6	5	4	3	2	1	0
P1	Port1 data Register	000001H	P17	P16	P15	P14	P13	P12	P11	P10
			R/W							
			0	0	0	0	0	0	0	0
P1CR	Port1 Control Register	000004H (Prohibit RMW)	P17C	P16C	P15C	P14C	P13C	P12C	P11C	P10C
			Write-only							
			0	0	0	0	0	0	0	0
			0: Input mode 1: Output mode							

(26) Port2

Symbol	Name	Address	7	6	5	4	3	2	1	0
P2	Port2 data Register	000006H	P27	P26	P25	P24	P23	P22	P21	P20
			R/W							
			1	1	1	1	1	1	1	1
P2CR	Port2 Control Register	000008H (Prohibit RMW)	P27C	P26C	P25C	P24C	P23C	P22C	P21C	P20C
			Write-only							
			0	0	0	0	0	0	0	0
			0: Input mode 1: Output mode							

(27) Port 4

Symbol	Name	Address	7	6	5	4	3	2	1	0
P4	Port4 data Register	00000AH	P47	P46	P45	P44	P43	P42	P41	P40
			Read-only							
			Undefined after reset							

(28) Port 5

Symbol	Name	Address	7	6	5	4	3	2	1	0
P5	Port5 data Register	00000BH				P54	P53	P52	P51	P50
						R/W				
						1	1	1	1	1
P5CR	Port5 Control Register	00000CH (Prohibit RMW)	P52F	P51F		P54C	P53C	P52C	P51C	P50C
			W	W		Write-only				
			0	0		0	0	0	0	0
			0: Port52 1: SCK	0: Port51 1: SO		0: Input mode 1: Output mode				
IIMC0	External Interrupt Control Register	00005EH (Prohibit RMW)				I4IE (INT4)	I3IE (INT3)	I2IE (INT2)	I1IE (INT1)	I0IE (INT0)
						W				
						0	0	0	0	0
						External interrupt enable 0: Disable 1: Enable				
IIMC1	External Interrupt Input Mode Control	00005FH (Prohibit RMW)	I4EG	I3EG	I2EG	I1EG	I0EG		INTTPG0E	INTTPG0S
			Write-only						R/W	R/W
			0	0	0	0	0		0	0
			INT4 edge selection 0: Rising edge 1: Falling edge	INT3 edge selection 0: Rising edge 1: Falling edge	INT2 edge selection 0: Rising edge 1: Falling edge	INT1 edge/level selection 0: Rising edge 1: Level	INT0 edge selection 0: Rising edge 1: Falling edge		INTTPG0 (TPG03) edge selection 0: Rising edge 1: Falling edge	INTTPG0 source selection 0: FIFO empty interrupt 1: FIFO empty or TPG03 interrupt

(29) Port 7

Symbol	Name	Address	7	6	5	4	3	2	1	0
P7	Port7 data Register	00000FH		P76	P75	P74	P73			
				R/W						
				1	1	1	1			
P7CR	Port7 Control Register	000011H (Prohibit RMW)		P76C	P75C	P74C	P73C			
				Write-only						
				0	0	0	0			
				0: Input mode 1: Output mode						
P7FC	Port7 Function Register	000013H (Prohibit RMW)		P76F	P75F	P74F	P73F			
				W	W	W	W			
				0	0	0	0			
				0: Port76 1: SCL1	0: Port75 1: SDA1	0: Port74 1: SCL0	0: Port73 1: SDA0			
ODCR1	Open Drain Control Register1	000015H (Prohibit RMW)		POD76	POD75	POD74	POD73			
				Write-only						
				0	0	0	0			
				0: Push-pull 1: Open-drain						
P7ICR	P7 Input Control Register	00000DH (Prohibit RMW)		PR76	PR75	PR74	PR73			
				Write-only						
				0	0	0	0			
				0: Pin 1: Output latch						

(30) Port 8

Symbol	Name	Address	7	6	5	4	3	2	1	0
P8	P8 data Register	000016H	P87	P86	P85	P84	P83	P82	P81	P80
			R/W							
			1	1	1	1	1	1	1	1
P8CR	P8 Control Register	000018H (Prohibit RMW)	P87C	P86C	P85C	P84C	P83C	P82C	P81C	P80C
			Write-only							
			0	0	0	0	0	0	0	0
			0: Input mode 1: Output mode							
P8FC	P8 Function Register	000014H (Prohibit RMW)					P83F			
							W			
							0			
							0: Port83 1: TO1			

(31) Port 9

Symbol	Name	Address	7	6	5	4	3	2	1	0
P9	P9 data Register	000017H	P97	P96	P95	P94	P93	P92	P91	P90
			R/W							
			1	1	1	1	1	1	1	1
P9CR	P9 Control Register	000019H (Prohibit RMW)	P97C	P96C	P95C	P94C	P93C	P92C	P91C	P90C
			Write-only							
			0	0	0	0	0	0	0	0
			0: Input mode 1: Output mode							
P9FC	P9 Function Register	00001AH (Prohibit RMW)	P97F	P96F	P95F	P94F	P93F	P92F	P91F	P90F
			Write-only							
			0	0	0	0	0	0	0	0
			0: Port97 1: TPG11	0: Port96 1: TO1/ TPG10	0: Port95 1: HA	0: Port94 1: CR	0: Port93 1: TPG03	0: Port92 1: TP1	0: Port91 1: TPG01/ VASWP	0: Port90 1: TP0/ TPG00
ODCR2	Open Drain Control Register2	00001BH (Prohibit RMW)	POD97	POD96	POD95	POD94	POD93	POD92	POD91	POD90
			Write-only							
			0	0	0	0	0	0	0	0
			0: Push-pull 1: Open-drain							
HACR	Head Amp Control Register	00008DH	VTPPO1	VTPPO0	TPVASEL	DFFPO1	DFFPO0	COMPS	CRPO	HAPO
			R/W							
			0	0	0	0	0	0	0	0
			0: Rising edge 1: Falling edge	0: Rising edge 1: Falling edge	0: TPG01 1: VASWP	0: Positive 1: Negative	0: Positive 1: Negative	0: Disable 1: Enable	0: Positive 1: Negative	0: Positive 1: Negative
TPCR	Timing Pulse Control Register	000086H	TPGOE1	TPGOE0		TPG1CNT		TP1D		TP0D
			R/W	R/W		R/W		R/W		R/W
			0	0		0		0		0
			TPG10 output control 0: Disable 1: Enable	TPG00 output control 0: Disable 1: Enable		P97 TPG11 output control 0: Disable 1: Enable		TP1 data latch		TP0 data latch

(32) Port A

Symbol	Name	Address	7	6	5	4	3	2	1	0
PA	PortA data Register	00001CH					PA3			PA0
							R/W			R/W
							1			1
PACR	PortA Control Register	00001EH (Prohibit RMW)					PA3C			PA0C
							W			W
							0			0
							0: Input mode 1: Output mode			0: Input mode 1: Output mode
ODCR3	Open-drain Control Register3	000021H (Prohibit RMW)				PWMOD1 (PWM1)	PWMOD0 (PWM0)			PODA3 (PortA3)
						Write-only				W
						0	0			0
						PWM0,1 Open-drain control 0: Push-pull 1: Open-drain				PortA Open-drain control 0: Push-pull 1: Open-drain
PAFC	PortA Function Register	00006BH (Prohibit RMW)					PA3F		PA0F2	PA0F1
							W		W	
							0		0	
							0: Port A3 1: PWM2		00: Port A0 01: PVPH 10: PWM3 11: Reserved	

(33) Port B

Symbol	Name	Address	7	6	5	4	3	2	1	0
PB	PortB data Register	00001DH							PB1	PB0
									R/W	
									1	1
									(SYSCR0<XTEN> = 0)	
PBCR	PortB Control Register	00001FH (Prohibit RMW)							PB1C	PB0C
									Write-only	
									0	0
									0: Input mode 1: Output mode	

(34) Port C, D, E, F

Symbol	Name	Address	7	6	5	4	3	2	1	0
PC	PC data Register	000087H	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
			R/W							
			0	0	0	0	0	0	0	0
PD	PD data Register	000088H							PD1	PD0
									R/W	
									0	0
PE	PE data Register	000089H	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
			R/W							
			0	0	0	0	0	0	0	0
PF	PF data Register	00008AH			PF5	PF4	PF3	PF2	PF1	PF0
					R/W					
					0	0	0	0	0	0
PECR	PE Control Register	00008BH (Prohibit RMW)	PE7C	PE6C	PE5C	PE4C	PE3C	PE2C	PE1C	PE0C
			Write-only							
			0	0	0	0	0	0	0	0
			0: Input mode 1: Output mode							
PFCR	PF Control Register	00008CH (Prohibit RMW)	—	—	PF5C	PF4C	PF3C	PF2C	PF1C	PF0C
					Write-only					
					0	0	0	0	0	0
					0: Input mode 1: Output mode					

(35) CLK output

Symbol	Name	Address	7	6	5	4	3	2	1	0
SYSCR3	System Control Register 3	00006DH (Prohibit RMW)	—	—	—	—	—	—	—	CLKEN
			(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)		R/W
			(1)	(1)	(1)	(1)	(1)	(1)		0
			Fix to 1.	Fix to 1.	Fix to 1.	Fix to 1.	Fix to 1. Note: This bit is read as 1 always.	Fix to 1. Note: This bit is read as 1 always.		0: Disable 1: Enable

6. Port Section Equivalent Circuit Diagram

- Reading the circuit diagram

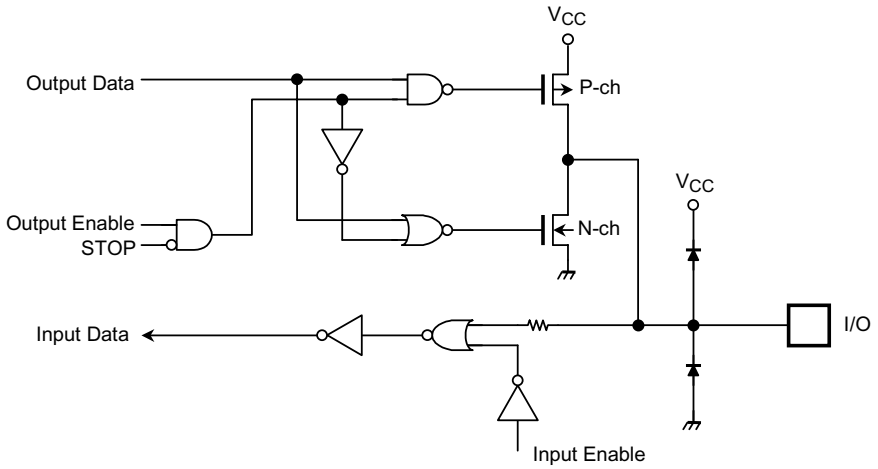
  Basically, the gate symbols are written the same as those used for the standard CMOS logic IC [74HCxx] series.

  The dedicated signal is described below.

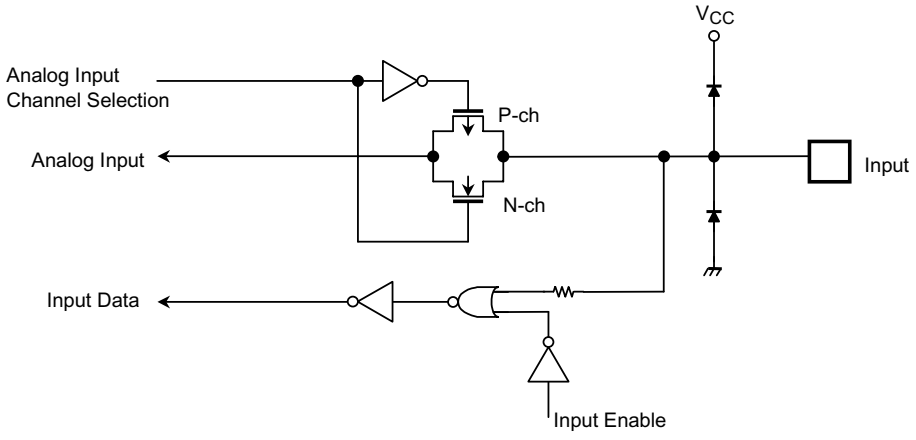
  STOP: This signal becomes active 1 when the halt mode setting register is set to the STOP mode (WDMOD<HALT1,0> = 0, 1) and the CPU executes the HALT instruction. When the drive enable bit WDMOD<DRVE> is set to 1, however, STOP remains at 0.

- The input protection resistans ranges from several tens ohms to several hundreds ohms.

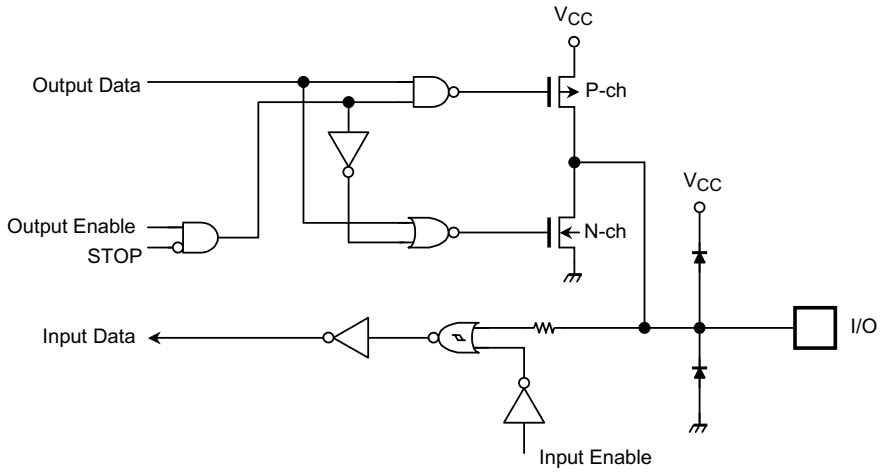
■ P0, P1, P2



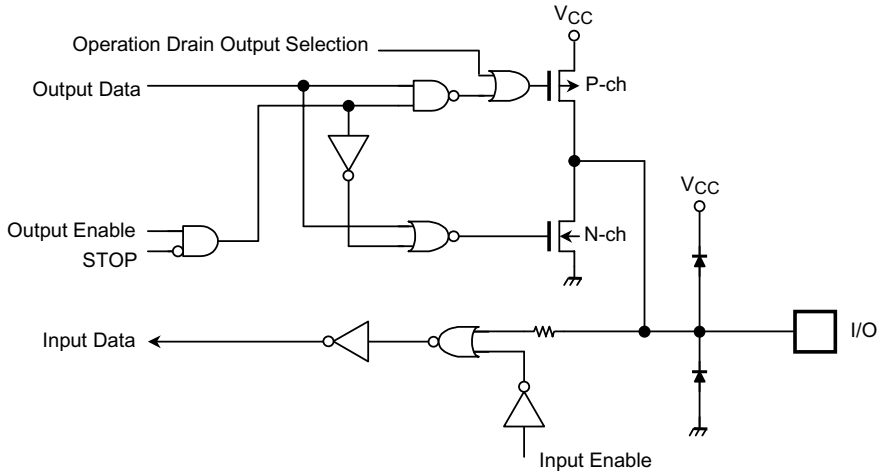
■ P4



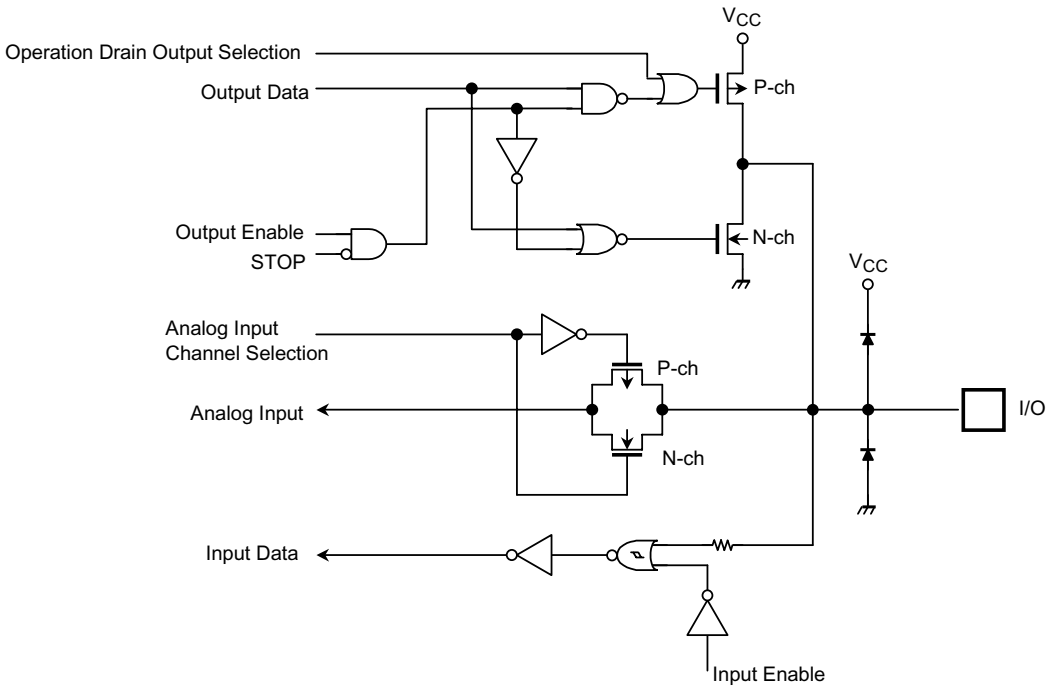
■ P5, P8


VCC
Output Data
P-ch
VCC
Output Enable
STOP
N-ch
Input Data
I/O
Input Enable

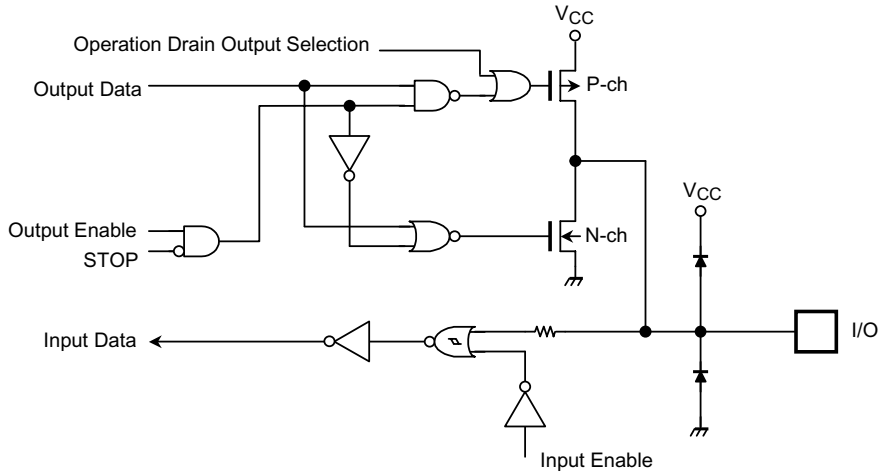
■ P9, PA


VCC
Operation Drain Output Selection
Output Data
P-ch
VCC
Output Enable
STOP
N-ch
Input Data
I/O
Input Enable

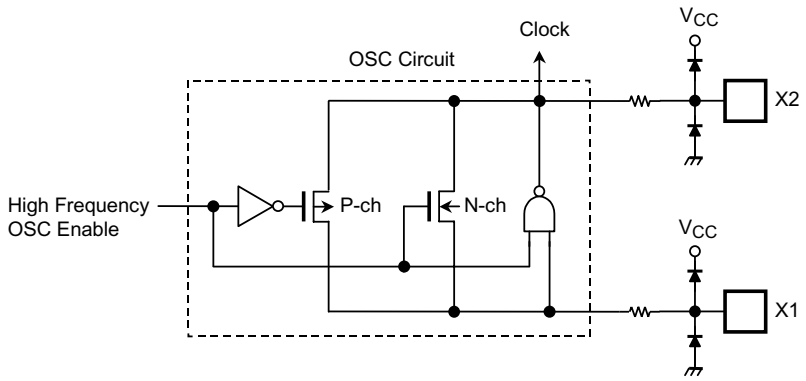
■ P75, P76



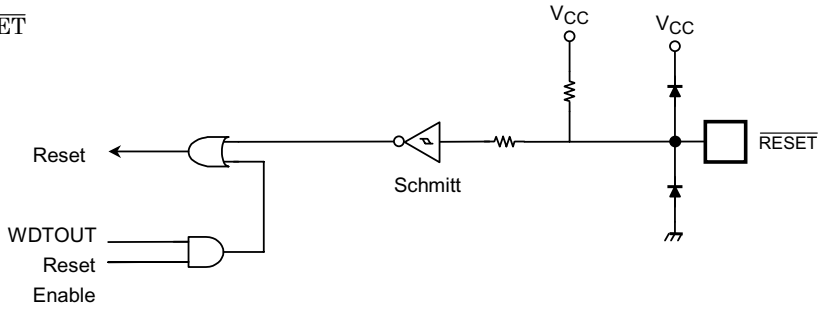
■ P73, P74



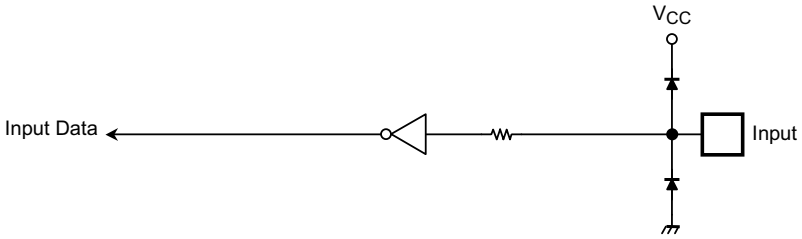
■ X1, X2



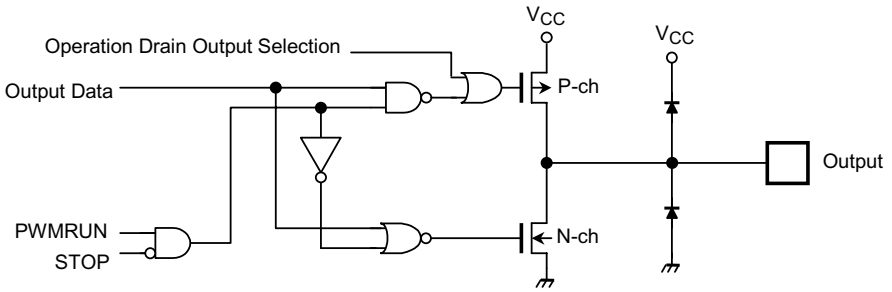
■ $\overline{\text{RESET}}$



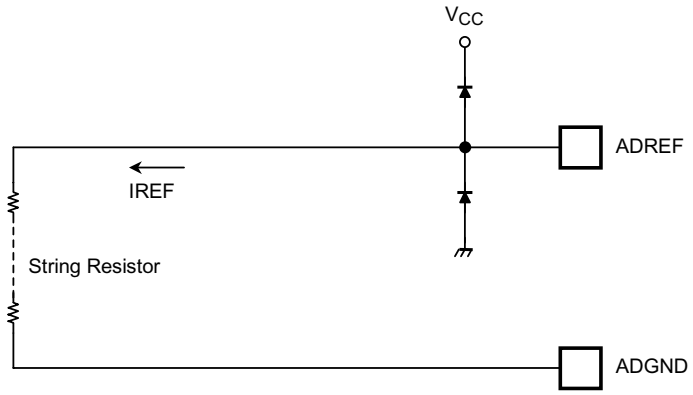
■ $\overline{\text{TEST}}$



■ PWM0, PWM1

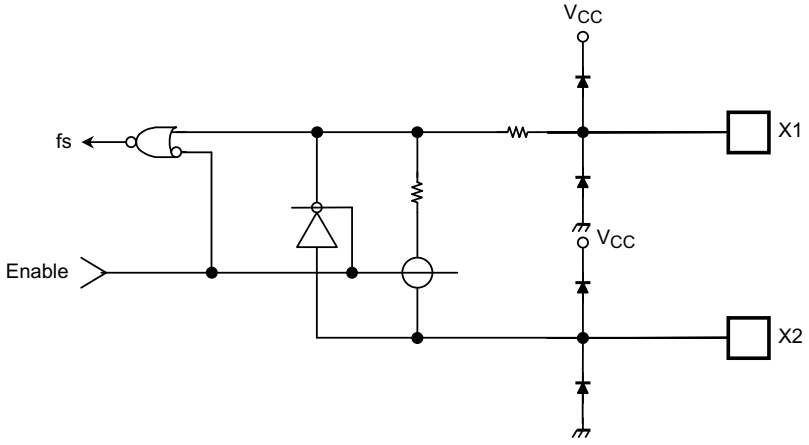


■ ADREF, ADGND



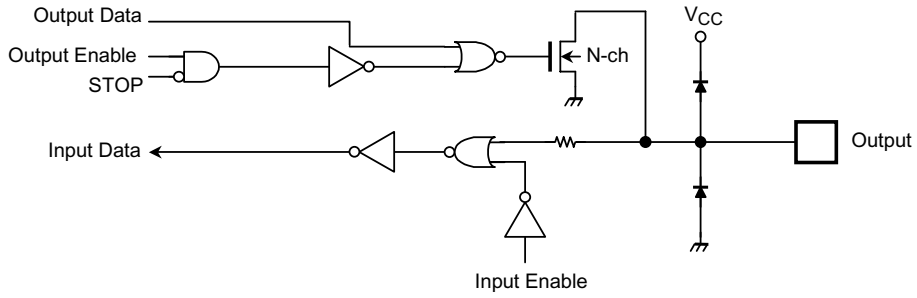
Note: IREF flows continuously at standby.

■ XT1, XT2



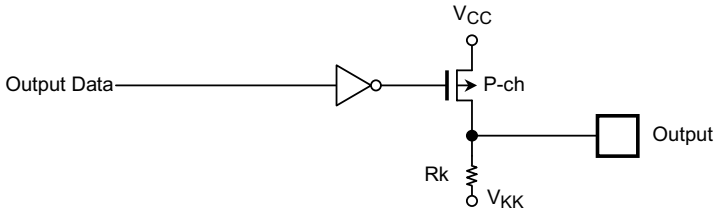
Note: Share PB1 and PB1

■ PB

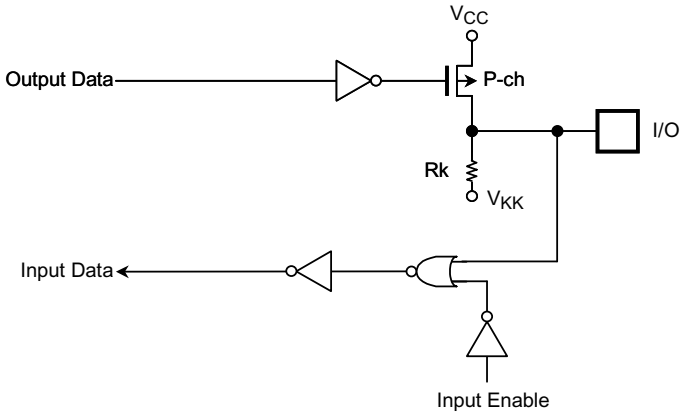


Note: Share XT1 and XT2

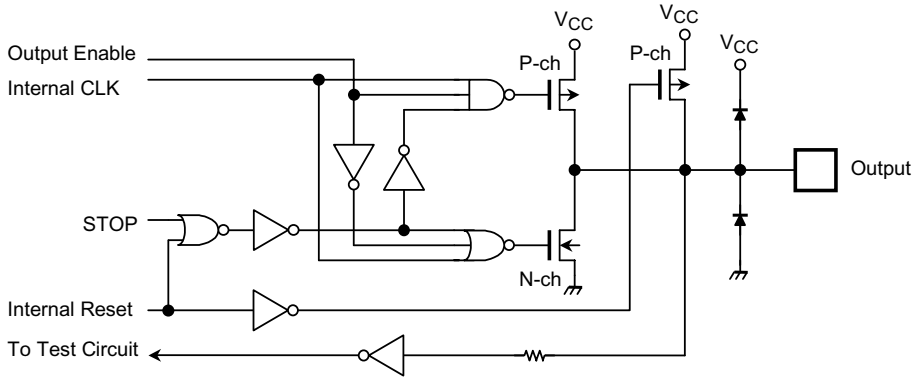
■ PC, PD



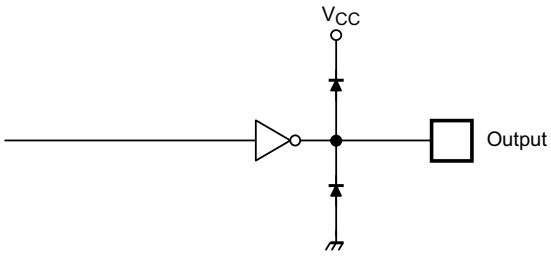
■ PE, PF



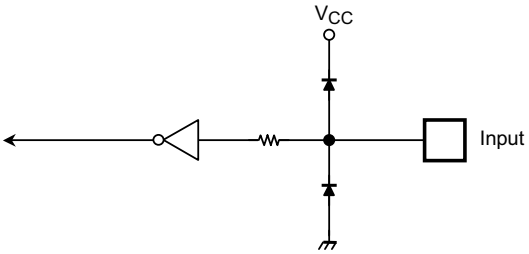
■ CLK



■ TEST1



■ TEST2



■ TEST3

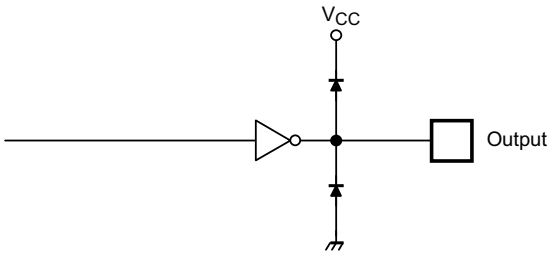


Table 6.1 Port enable

Port	Pin	Input/ Output	Output mode	Shared Function	Condition of input enable	Remark
P0	P00 to P07	I/O	P-P		P0∗OBF	
P1	P10 to P17	I/O	P-P		P1∗OBF	
P2	P20 to P27	I/O	P-P		P2∗OBF	
P4	P40 to P47	I	—	AIN2 to AIN9	P4∗OBF	Analog Input
P5	P50	I/O	P-P	INT4/TI3TI5/SI (Schmitt)	OBF	
	P51	I/O	P-P	INT3/TI2TI4/SO (Schmitt)	OBF	
	P52	I/O	P-P	INT2/TI1/TI0/SCK (Schmitt)	OBF	
	P53	I/O	P-P	INT1 (Schmitt)	OBF	
	P54	I/O	P-P	INT0 (Schmitt)	OBF	
P7	P73	I/O	P-P/O-D	SDA0 (I/O) (Schmitt)	OBF	
	P74	I/O	P-P/O-D	SCL0 (I/O) (Schmitt)	OBF	
	P75	I/O	P-P/O-D	SDA1/AIN0 (I/O) (Schmitt)	OBF	Analog Input
	P76	I/O	P-P/O-D	SCL1/AIN1 (I/O) (Schmitt)	OBF	Analog Input
P8	P80	I/O	P-P	CTLIN (Schmitt)	OBF	
	P81	I/O	P-P	DFGIN (Schmitt)	OBF	
	P82	I/O	P-P	RMTIN (Schmitt)	OBF	
	P83	I/O	P-P	EXT/TO1 (Schmitt)	OBF	
	P84	I/O	P-P	DPGIN (Schmitt)	OBF	
	P85	I/O	P-P	CFGIN (Schmitt)	OBF	
	P86	I/O	P-P	CSYNCIN (Schmitt)	OBF	
	P87	I/O	P-P	COMPIN (Schmitt)	OBF	
P9	P90	I/O	P-P/O-D	TP0/TPG00 (o)	P9∗OBF	
	P91	I/O	P-P/O-D	TPG01/VASWP (3-state)	P9∗OBF	
	P92	I/O	P-P/O-D	TP1 (o)	P9∗OBF	
	P93	I/O	P-P/O-D	TPG03 (o)	P9∗OBF	
	P94	I/O	P-P/O-D	CR (o)	P9∗OBF	
	P95	I/O	P-P/O-D	HA (o)	P9∗OBF	
	P96	I/O	P-P/O-D	TO1/TPG10 (o)	P9∗OBF	
	P97	I/O	P-P/O-D	TPG11 (3-state)	P9∗OBF	
PA	PA0	I/O	P-P	PVPH/PWM3 (3-state)	PA∗OBF	
	PA3	I/O	P-P/O-D	PWM2 (o)	PA∗OBF	
PB	PB0	I/O	O-D	XT1 (Xtal)	OBF	
	PB1	I/O	O-D	XT2 (Xtal)	OBF	
PC	PC0 to PC7	O	H-V	VFT (Grid)	—	High Voltage port
PD	PD0, PD1	O	H-V	VFT (Grid)	—	High Voltage port
PE	PE0 to PE7	I/O	H-V/ O-D	VFT (Segment)	OBF	High Voltage port
PF	PF0 to PF5	I/O	H-V/ O-D	VFT (Segment)	OBF	High Voltage port

P-P: Push-Pull, O-D: Open-drain, (O): Output, (I/O): Input/Output, (Schmitt): Schmitt input, except (Schmitt): CMOS input, OBF: $\overline{\text{STOP}\cdot\overline{\text{WDMOD}<\text{DRVE}>}}$, P0 to PA: Access to Port register

7. Points of Concern and Restriction

(1) Notation

a. Explanation of a built-in I/O register: Register Symbol <Bit Symbol>

e.g.) TRUN<T0RUN> … Bit T0RUN of Register TRUN

b. Read, Modify and Write Instruction

An instruction in which the CPU executes following by one instruction.

i) CPU reads data of the memory.
ii) CPU modifies the data.
iii) CPU writes the data to the same memory.

ex1) SET 3, (TRUN) set bit 3 of TRUN
ex2) INC 1, (100H) increment the data of 100H

- A sample Read, Modify and Write instructions using the TLCS-900

Exchange

EX	(mem), R		

Arithmetic Operation

ADD	(mem), R/#	ADC	(mem), R/#
SUB	(mem), R/#	SBC	(mem), R/#
INC	#3, (mem)	DEC	#3, (mem)

Logical Operation

AND	(mem), R/#	OR	(mem), R/#
XOR	(mem), R/#		

Bit Manipulation

STCF	#3/A, (mem)	SET	#3, (mem)
RES	#3, (mem)	TSET	#3, (mem)
CHG	#3, (mem)		

Rotate and Shift

RLC	(mem)	RRC	(mem)
RL	(mem)	RR	(mem)
SLA	(mem)	SRA	(mem)
SLL	(mem)	SRL	(mem)
RLD	(mem)	RRD	(mem)

c. fc, fs, f_{FPH}, f_{SYS}, 1 state

The clock frequency input from pins X1 and X2 pin is called fc, and the clock frequency input from XT1, XT2 pin is called fs. The clock frequency selected by SYSCR1<SYSCK> is called system clock f_{FPH}, and the clock frequency given by f_{FPH} divided by 2 is called f_{SYS}. One cycle of f_{SYS} is called 1 state.

(2) Care Points

a. Warming-up Counter

The warm-up counter operates when STOP mode is released even if the system is using an external oscillator. As a result, it takes warm-up time from inputting the releasing request to outputting the system clock.

b. WatchDog Timer

The watchdog timer starts operation immediately after the reset is released. When the watchdog timer is not used, disable it.

c. CPU (Micro DMA)

Only the "LDC cr, r", "LDC r, cr" instructions can be used to access the control registers in the CPU (like the transfer source address register (DMASn)).

d. $\overline{TEST}$, TEST1, TEST2, TEST3

Each pins for test is used as follows.

$\overline{TEST}$: V_{CC} level

TEST1, TEST2: Short on the PCB

TEST3: OPEN

e. POP SR instruction

Please execute POP SR instruction during DI condition.

f. Releasing the HALT mode by requesting an interruption

Usually, interrupts can release all halts status. However, the interrupts = (INT0, INT1), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of fc or fs) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.