

Low Voltage/Low Power

## CMOS 16-Bit Microcontroller TMP93CM40F

### 1. Outline and Device Characteristics

The TMP93CM40 is high-speed, advanced 16-bit microcontroller developed for controlling medium to large-scale equipment. They enable low voltage and low-power-consumption operation.

The TMP93CM40 is housed in 100-pin flat packages.

The device characteristics are as follows:

- (1) Original 16-bit CPU (900/L CPU)
  - TLCS-90 instruction mnemonic upward compatible
  - 16-Mbyte linear address space
  - General-purpose registers, register bank system
  - 16-bit multiplication, 16-bit division, bit transfer and bit manipulation instructions
  - Micro DMA: 4 channels (1.6  $\mu$ s per 2 bytes at 20 MHz)
- (2) Minimum instruction execution time: 200 ns at 20 MHz
- (3) Internal RAM: 2 Kbytes  
Internal ROM: 32 Kbytes
- (4) External memory expansion
  - Can be expanded up to 16 Mbytes (for both programs and data).
  - AM8/ $\overline{\text{AM16}}$  pin (select the external data bus width)
  - Can mix 8- and 16-bit external data buses. (Dynamic bus sizing)
- (5) 8-bit timer: 2 channels
- (6) 8-bit PWM timer: 2 channels
- (7) 16-bit timer: 2 channels
- (8) 4-bit pattern generator: 2 channels
- (9) Serial interface: 2 channels
- (10) 10-bit AD converter: 8 channels

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- (11) Watchdog timer
- (12) Chip select and wait controller: 3 blocks
- (13) Interrupt functions: 29
- 9 CPU interrupts (SWI instruction, and illegal instruction)
  - 14 internal interrupts  7-level priority can be set.
  - 6 external interrupts
- (14) I/O ports: 79
- (15) Standby function: 4 HALT modes (RUN, IDLE2, IDLE1, STOP)
- (16) Clock gear function
- Dual clock operation
  - Clock gear: High-frequency clock can be changed from  $f_c$  to  $f_c/16$ .
- (17) Wide range of operating voltage
- $V_{cc} = 2.7$  to  $5.5$  V
- (18) Package

| Type No.   | Package            |
|------------|--------------------|
| TMP93CM40F | P-QFP100-1414-0.50 |

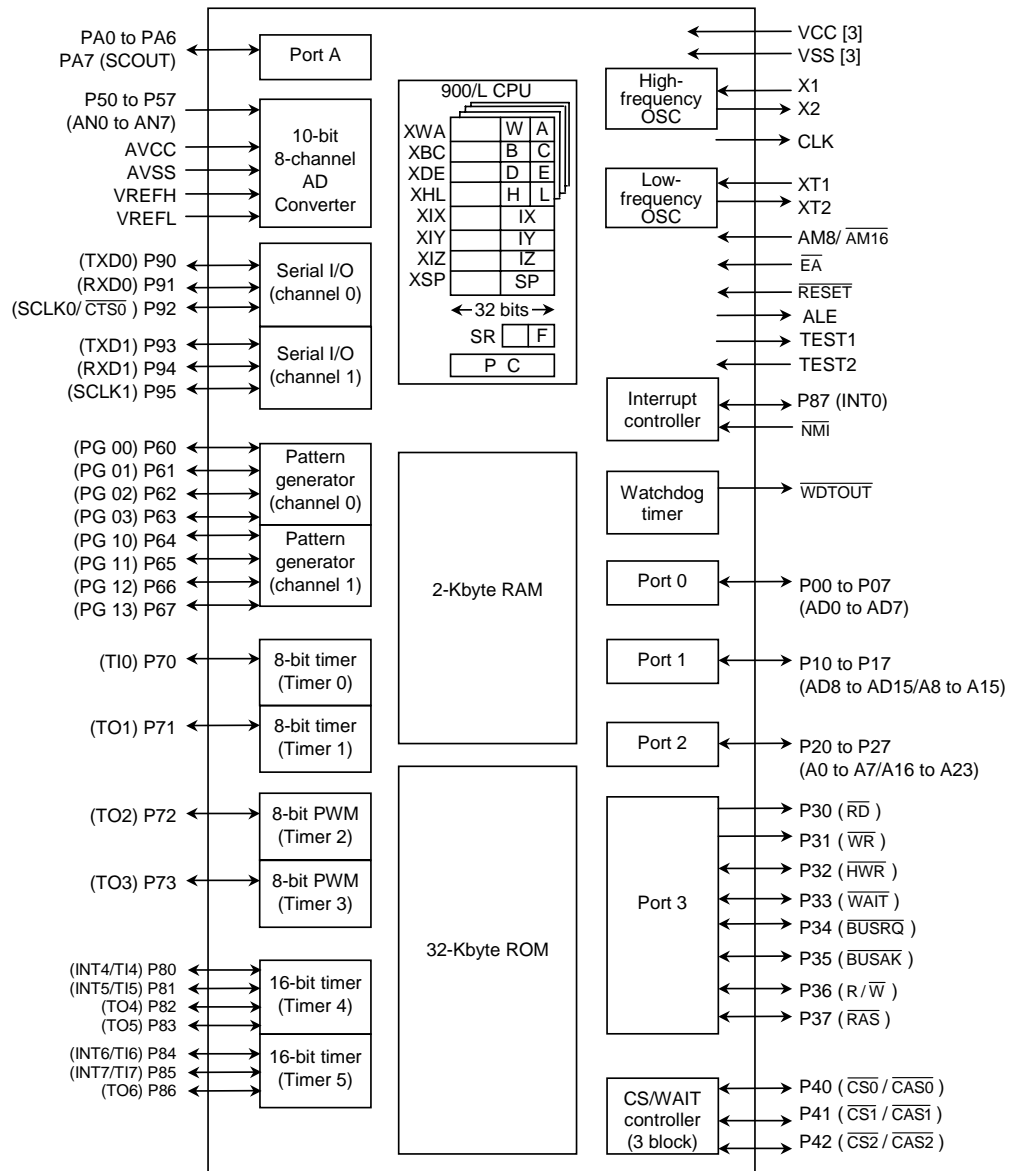


Figure 1.1 TMP93CM40 Block Diagram

## 2. Pin Assignment and Functions

The assignment of input and output pins for the TMP93CM40, their names and functions are described below.

### 2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of the TMP93CM40F.

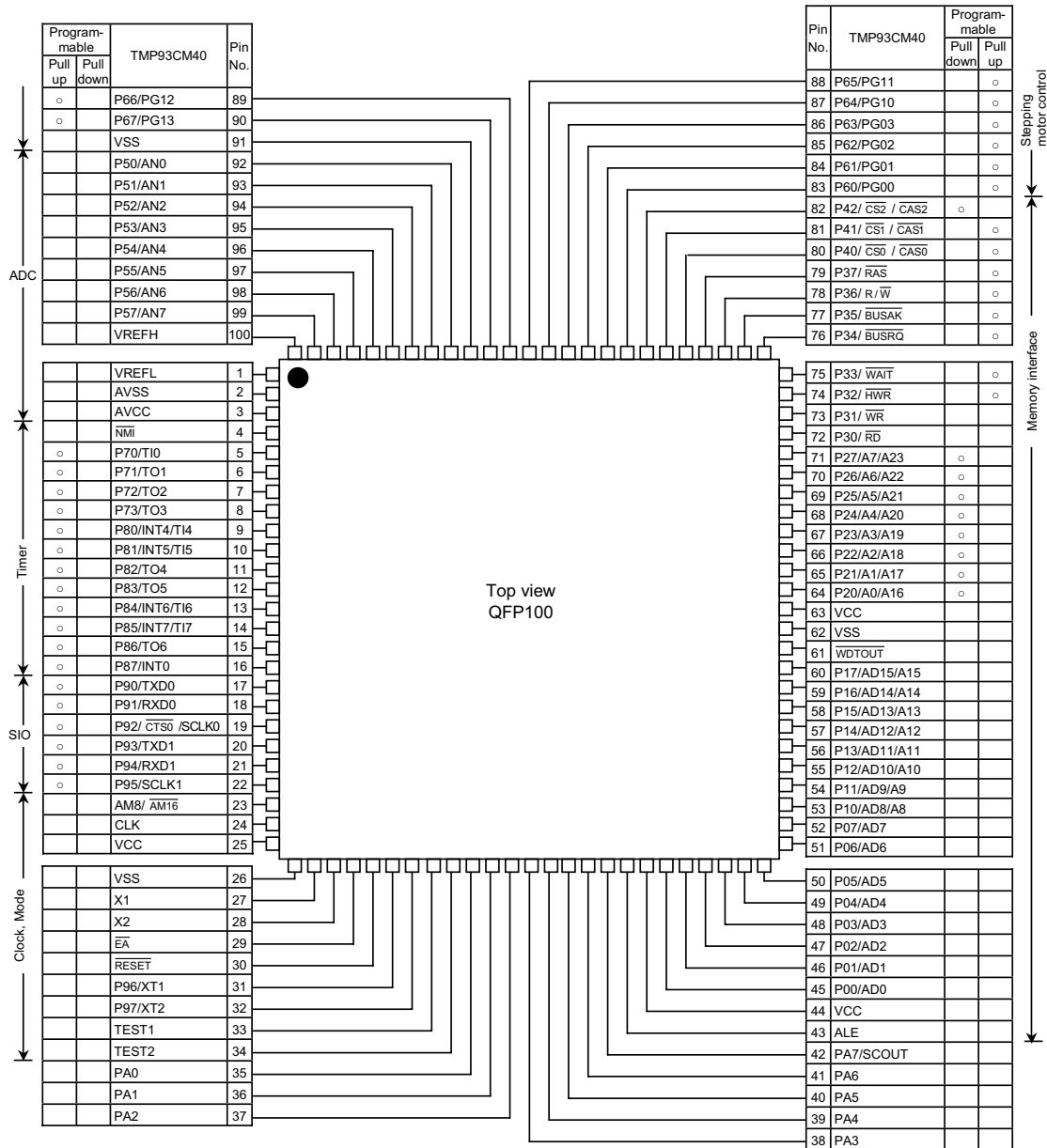


Figure 2.1.1 Pin Assignment (100-pin QFP)

## 2.2 Pin Names and Functions

The names of the input/output pins and their functions are described below.

Table 2.2.1 to Table 2.2.4 show pin names and functions.

Table 2.2.1 Pin Names and Functions (1/4)

| Pin Names  | Number of Pins | I/O                         | Functions   |
|--|----------------|-----------------------------|---|
| P00 to P07<br>AD0 to AD7                         | 8              | I/O<br>3-state              | Port 0: I/O port that allows I/O to be selected at the bit level.<br>Address and data (lower): Bits 0 to 7 for address and data bus.  |
| P10 to P17<br>AD8 to AD15<br>A8 to A15           | 8              | I/O<br>3-state<br>Output    | Port 1: I/O port that allows I/O to be selected at the bit level.<br>Address and data (upper): Bits 8 to 15 for address and data bus.<br>Address: Bits 8 to 15 for address bus.   |
| P20 to P27<br>A0 to A7<br>A16 to A23             | 8              | I/O<br><br>Output<br>Output | Port 2: I/O port that allows to be selected at the bit level (with pull-down resistor).<br>Address: Bits 0 to 7 for address bus.<br>Address: Bits 16 to 23 for address bus.   |
| P30<br>$\overline{RD}$                           | 1              | Output<br>Output            | Port 30: Output port.<br>Read: Strobe signal for reading external memory.   |
| P31<br>$\overline{WR}$                           | 1              | Output<br>Output            | Port 31: Output port.<br>Write: Strobe signal for writing data on pins AD0 to AD7.  |
| P32<br>$\overline{HWR}$                          | 1              | I/O<br>Output               | Port 32: I/O port (with pull-up resistor).<br>High write: Strobe signal for writing data on pins AD8 to AD15.   |
| P33<br>$\overline{WAIT}$                         | 1              | I/O<br>Input                | Port 33: I/O port (with pull-up resistor).<br>Wait: Pin used to request CPU bus wait.   |
| P34<br>$\overline{BUSRQ}$                        | 1              | I/O<br>Input                | Port 34: I/O port (with pull-up resistor).<br>Bus request: Signal used to request bus release.  |
| P35<br>$\overline{BUSAK}$                        | 1              | I/O<br>Output               | Port 35: I/O port (with pull-up resistor).<br>Bus acknowledge: Signal used to acknowledge bus release.  |
| P36<br>R/ $\overline{W}$                         | 1              | I/O<br>Output               | Port 36: I/O port (with pull-up resistor).<br>Read/write: 1 represents read or dummy cycle; 0 represents write cycle.   |
| P37<br>$\overline{RAS}$                          | 1              | I/O<br>Output               | Port 37: I/O port (with pull-up resistor).<br>Row address strobe: Outputs $\overline{RAS}$ strobe for DRAM.   |
| P40<br>$\overline{CS0}$<br><br>$\overline{CAS0}$ | 1              | I/O<br><br>Output<br>Output | Port 40: I/O port (with pull-up resistor).<br>Chip select 0: Outputs 0 when address is within specified address area.<br>Column address strobe 0: Outputs $\overline{CAS}$ strobe for DRAM when address is within specified address area. |

Note: This device's built-in memory or built-in I/O cannot be accessed by an external DMA controller, using the  $\overline{BUSRQ}$  and  $\overline{BUSAK}$  signals.

Table 2.2.2 Pin Names and Functions (2/4)

| Pin Names                                    | Number of Pins | I/O                     | Functions   |
|--|----------------|-------------------------|---|
| P41<br>$\overline{CS1}$<br>$\overline{CAS1}$ | 1              | I/O<br>Output<br>Output | Port 41: I/O port (with pull-up resistor).<br>Chip select 1: Outputs 0 if address is within specified address area.<br>Column address strobe 1: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.   |
| P42<br>$\overline{CS2}$<br>$\overline{CAS2}$ | 1              | I/O<br>Output<br>Output | Port 42: I/O port (with pull-down resistor).<br>Chip select 2: Outputs 0 if address is within specified address area.<br>Column address strobe 2: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area. |
| P50 to P57<br>AN0 to AN7                     | 8              | Input<br>Input          | Port 5: Pin used to input port.<br>Analog input: Pin used to input to AD converter.   |
| VREFH  | 1              | Input                   | Pin for reference voltage input to AD converter. (H)  |
| VREFL  | 1              | Input                   | Pin for reference voltage input to AD converter. (L)  |
| P60 to P63<br>PG00 to PG03                   | 4              | I/O<br>Output           | Port 60 to 63: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor).<br>Pattern generator ports: 00 to 03.  |
| P64 to P67<br>PG10 to PG13                   | 4              | I/O<br>Output           | Port 64 to 67: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor).<br>Pattern generator ports: 10 to 13.  |
| P70<br>TI0                                   | 1              | I/O<br>Input            | Port 70: I/O port (with pull-up resistor).<br>Timer input 0: Timer 0 input.   |
| P71<br>TO1                                   | 1              | I/O<br>Output           | Port 71: I/O port (with pull-up resistor).<br>Timer output 1: Timer 0 or 1 output.  |
| P72<br>TO2                                   | 1              | I/O<br>Output           | Port 72: I/O port (with pull-up resistor).<br>PWM output 2: 8-bit PWM timer 2 output.   |
| P73<br>TO3                                   | 1              | I/O<br>Output           | Port 73: I/O port (with pull-up resistor).<br>PWM output 3: 8-bit PWM timer 3 output.   |
| P80<br>TI4<br>INT4                           | 1              | I/O<br>Input<br>Input   | Port 80: I/O port (with pull-up resistor).<br>Timer input 4: Timer 4 count/capture trigger signal input.<br>Interrupt request pin 4: Interrupt request pin with programmable rising/falling edge.                                       |
| P81<br>TI5<br>INT5                           | 1              | I/O<br>Input<br>Input   | Port 81: I/O port (with pull-up resistor).<br>Timer input 5: Timer 4 count/capture trigger signal input.<br>Interrupt request pin 5: Interrupt request pin with rising edge.  |
| P82<br>TO4                                   | 1              | I/O<br>Output           | Port 82: I/O port (with pull-up resistor).<br>Timer output 4: Timer 4 output pin.   |
| P83<br>TO5                                   | 1              | I/O<br>Output           | Port 83: I/O port (with pull-up resistor).<br>Timer output 5: Timer 4 output pin.   |

Table 2.2.3 Pin Names and Functions (3/4)

| Pin Names                                | Number of Pins | I/O                   | Functions   |
|--|----------------|-----------------------|---|
| P84<br>TI6<br>INT6                       | 1              | I/O<br>Input<br>Input | Port 84: I/O port (with pull-up resistor).<br>Timer input 6: Timer 5 count/capture trigger signal input.<br>Interrupt request pin 6: Interrupt request pin with programmable rising/falling edge. |
| P85<br>TI7<br>INT7                       | 1              | I/O<br>Input<br>Input | Port 85: I/O port (with pull-up resistor).<br>Timer input 7: Timer 5 count/capture trigger signal input.<br>Interrupt request pin 7: Interrupt request pin with rising edge.                      |
| P86<br>TO6                               | 1              | I/O<br>Output         | Port 86: I/O port (with pull-up resistor).<br>Timer output 6: Timer 5 output pin.   |
| P87<br>INT0                              | 1              | I/O<br>Input          | Port 87: I/O port (with pull-up resistor).<br>Interrupt request pin 0: Interrupt request pin with programmable level/rising edge.   |
| P90<br>TXD0                              | 1              | I/O<br>Output         | Port 90: I/O port (with pull-up resistor).<br>Serial send data 0.   |
| P91<br>RXD0                              | 1              | I/O<br>Input          | Port 91: I/O port (with pull-up resistor).<br>Serial receive data 0.  |
| P92<br>$\overline{\text{CTS0}}$<br>SCLK0 | 1              | I/O<br>Input<br>I/O   | Port 92: I/O port (with pull-up resistor).<br>Serial data send enable 0. (Clear to send)<br>Serial Clock I/O 0.   |
| P93<br>TXD1                              | 1              | I/O<br>Output         | Port 93: I/O port (with pull-up resistor).<br>Serial send data 1.   |
| P94<br>RXD1                              | 1              | I/O<br>Input          | Port 94: I/O port (with pull-up resistor).<br>Serial receive data 1.  |
| P95<br>SCLK1                             | 1              | I/O<br>I/O            | Port 95: I/O port (with pull-up resistor).<br>Serial clock I/O 1.   |
| PA0 to PA6                               | 7              | I/O                   | Port A0 to A6: I/O port.  |
| PA7<br>SCOUT                             | 1              | I/O<br>Output         | Port A7: I/O port.<br>System clock output: outputs $f_{\text{PPH}}$ or $f_{\text{SYS}}$ clock.  |
| $\overline{\text{WDTOUT}}$               | 1              | Output                | Watchdog timer output pin.  |
| NMI                                      | 1              | Input                 | Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge or both edges.   |
| CLK                                      | 1              | Output                | Clock output: Outputs $[f_{\text{SYS}} \div 2]$ clock.<br>Pulled-up during reset.<br>Can be disabled for reducing noise.  |
| $\overline{\text{EA}}$                   | 1              | Input                 | External access: The VCC pin should be connected.   |

Table 2.2.4 Pin Names and Functions (4/4)

| Pin Names                     | Number of Pins | I/O              | Functions   |
|-------------------------------|----------------|------------------|---|
| AM8/ $\overline{\text{AM16}}$ | 1              | Input            | Address mode: Selects external data bus width.<br>The VCC pin should be connected. The data bus width for external access is set by the chip select/wait control register, port 1 control register. |
| ALE                           | 1              | Output           | Address latch enable.<br>Can be disabled for reducing noise.  |
| $\overline{\text{RESET}}$     | 1              | Input            | Reset: Initializes TMP93CM40. (with pull-up resistor)   |
| X1/X2                         | 2              | Input/Output     | High frequency oscillator connecting pin.   |
| P96                           | 1              | I/O              | Port 96: I/O port. (Open-drain output)  |
| XT1                           | 1              | Input            | Low frequency oscillator connecting pin.  |
| P97                           | 1              | I/O              | Port 97: I/O port. (Open-drain output)  |
| XT2                           | 1              | Output           | Low-frequency oscillator connecting pin.  |
| TEST1/TEST2                   | 2              | Output<br>/Input | TEST1 should be connected with TEST2 pin.<br>Do not connect to any other pins.  |
| VCC                           | 3              |                  | Power supply pin. (All VCC pins should be connected with the power supply pin.)   |
| VSS                           | 3              |                  | GND pin (0 V). (All VSS pins should be connected with GND (0 V).)   |
| AVCC                          | 1              |                  | Power supply pin for AD converter.  |
| AVSS                          | 1              |                  | GND pin for AD converter (0 V).   |

Note: All pins that have built-in pull-up/pull-down resistors (other than the  $\overline{\text{RESET}}$  pin) can be disconnected from the built-in pull-up/pull-down resistor by software.



### 3. Operation

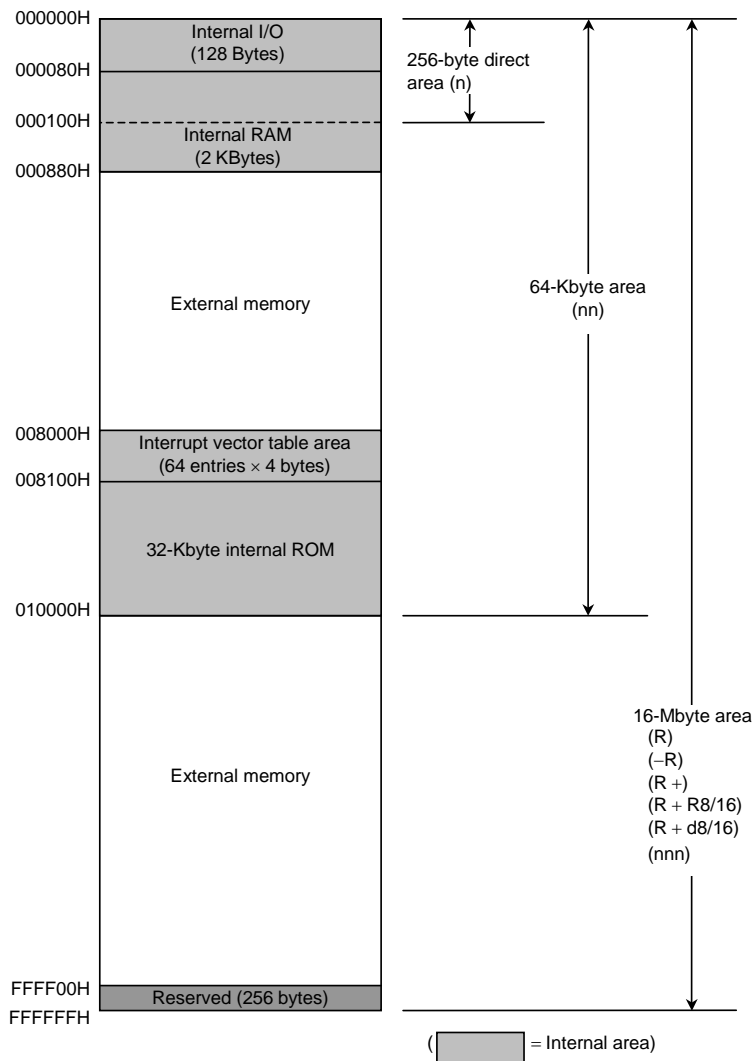
This section describes the functions and basic operation of all blocks of the TMP93CM40 devices.

#### 3.1 CPU

The TMP93CM40 has a built-in high performance 16-bit CPU (900/L CPU). (For a description of this CPU's operation, see the sub section TLCS-900/L CPU in the previous section.

#### 3.2 Memory Map

Figure 3.2.1 is a memory map of the TMP93CM40.



Note: The 256-byte area from FFFF00H to FFFFFFFH cannot be used.

Figure 3.2.1 Memory Map

## 4. Electrical Characteristics

### 4.1 Maximum Ratings (TMP93CM40F)

"X" used in an expression shows a frequency for the clock  $f_{FH}$  selected by  $SYSCR1<SYSCK>$ . The value of "X" changes according to whether a clock gear or a low speed oscillator is selected. An example value is calculated for  $f_c$ , with gear = 1/ $f_c$  ( $SYSCR1<SYSCK, GEAR2:0> = "0000"$ )

| Parameter                                      | Symbol          | Rating                 | Unit             |
|--|-----------------|------------------------|------------------|
| Power supply voltage                           | $V_{CC}$        | -0.5 to 6.5            | V                |
| Input voltage                                  | $V_{IN}$        | -0.5 to $V_{CC} + 0.5$ | V                |
| Output current (total)                         | $\Sigma I_{OL}$ | 120                    | mA               |
| Output current (total)                         | $\Sigma I_{OH}$ | -80                    | mA               |
| Power dissipation ( $T_a = 85^\circ\text{C}$ ) | $P_D$           | 600                    | mW               |
| Soldering temperature (10 s)                   | $T_{SOLDER}$    | 260                    | $^\circ\text{C}$ |
| Storage temperature                            | $T_{STG}$       | -65 to 150             | $^\circ\text{C}$ |
| Operating temperature                          | $T_{OPR}$       | -40 to 85              | $^\circ\text{C}$ |

Note: The maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no maximum rating value will ever be exceeded.

## 4.2 DC Characteristics (1/2)

| Parameter   |                                  | Symbol    | Condition  | Min             | Typ.<br>(Note 1) | Max            | Unit |
|---|----------------------------------|-----------|--|-----------------|------------------|----------------|------|
| Power supply voltage<br>( $V_{CC} = V_{CC}$<br>$V_{SS} = V_{SS} = 0\text{ V}$ ) |                                  | $V_{CC}$  | fc = 4 to 16 MHz<br>fs = 30 to 34 kHz<br>( $T_a = -40$ to $85^\circ\text{C}$ ) | 4.5             |                  | 5.5            | V    |
|   |                                  |           | fc = 4 to 20 MHz<br>fs = 30 to 34 kHz<br>( $T_a = -20$ to $70^\circ\text{C}$ ) |                 |                  |                |      |
|   |                                  |           | fc = 4 to 10 MHz<br>fs = 30 to 34 kHz<br>( $T_a = -40$ to $85^\circ\text{C}$ ) | 2.7<br>(Note 2) |                  |                |      |
| Input low voltage   | AD0 to AD15                      | $V_{IL}$  | $V_{CC} \geq 4.5\text{ V}$<br>$V_{CC} < 4.5\text{ V}$                          | -0.3            |                  | 0.8<br>0.6     | V    |
|   | Port 2 to port A<br>(except P87) | $V_{IL1}$ | $V_{CC} = 2.7$ to $5.5\text{ V}$   |                 |                  | 0.3 $V_{CC}$   |      |
|   | RESET, NMI, INT0                 | $V_{IL2}$ |  |                 |                  | 0.25 $V_{CC}$  |      |
|   | $\overline{EA}$ , AM8/AM16       | $V_{IL3}$ |  |                 |                  | 0.3            |      |
|   | X1, Port 5                       | $V_{IL4}$ |  |                 |                  | 0.2 $V_{CC}$   |      |
| Input high voltage  | AD0 to AD15                      | $V_{IH}$  | $V_{CC} \geq 4.5\text{ V}$<br>$V_{CC} < 4.5\text{ V}$                          | 2.2<br>2.0      |                  | $V_{CC} + 0.3$ | V    |
|   | Port 2 to port A<br>(except P87) | $V_{IH1}$ | $V_{CC} = 2.7$ to $5.5\text{ V}$   | 0.7 $V_{CC}$    |                  |                |      |
|   | RESET, NMI, INT0                 | $V_{IH2}$ |  | 0.75 $V_{CC}$   |                  |                |      |
|   | $\overline{EA}$ , AM8/AM16       | $V_{IH3}$ |  | $V_{CC} - 0.3$  |                  |                |      |
|   | X1                               | $V_{IH4}$ |  | 0.8 $V_{CC}$    |                  |                |      |
| Output low voltage  |                                  | $V_{OL}$  | $I_{OL} = 1.6\text{ mA}$<br>( $V_{CC} = 2.7$ to $5.5\text{ V}$ )               |                 |                  | 0.45           | V    |
| Output high voltage   |                                  | $V_{OH1}$ | $I_{OH} = -400\text{ }\mu\text{A}$<br>( $V_{CC} = 3\text{ V} \pm 10\%$ )       | 2.4             |                  |                |      |
|   |                                  | $V_{OH2}$ | $I_{OH} = -400\text{ }\mu\text{A}$<br>( $V_{CC} = 5\text{ V} \pm 10\%$ )       | 4.2             |                  |                |      |

Note 1: Typical values are for  $T_a = 25^\circ\text{C}$  and  $V_{CC} = 5\text{ V}$  unless otherwise noted.

Note 2: The operation of the AD converter is guaranteed at  $5\text{ V} \pm 10\%$ .

## 4.2 DC Characteristics (2/2)

| Parameter   | Symbol                | Condition   | Min                     | Typ.<br>(Note 1) | Max        | Unit      |
|---|-----------------------|---|-------------------------|------------------|------------|-----------|
| Darlington drive current<br>(8 output pins max)                 | $I_{DAR}$<br>(Note 2) | $V_{EXT} = 1.5 V$<br>$R_{EXT} = 1.1 k\Omega$<br>(only when<br>$V_{CC} = 5 V \pm 10\%$ ) | -1.0                    |                  | -3.5       | mA        |
| Input leakage current   | $I_{LI}$              | $0.0 \leq V_{IN} \leq V_{CC}$   |                         | 0.02             | $\pm 5$    | $\mu A$   |
| Output leakage current  | $I_{LO}$              | $0.2 \leq V_{IN} \leq V_{CC} - 0.2$   |                         | 0.05             | $\pm 10$   |           |
| Power down voltage<br>(at STOP, RAM back-up)                    | $V_{STOP}$            | $V_{IL2} = 0.2 V_{CC}$ ,<br>$V_{IL2} = 0.8 V_{CC}$                                      | 2.0                     |                  | 6.0        | V         |
| $\overline{RESET}$ pull-up resistor                             | $R_{RST}$             | $V_{CC} = 5 V \pm 10\%$<br>$V_{CC} = 3 V \pm 10\%$                                      | 50<br>80                |                  | 150<br>200 | $k\Omega$ |
| Pin capacitance   | $C_{IO}$              | $f_c = 1 MHz$   |                         |                  | 10         |           |
| Schmitt width<br>$\overline{RESET}$ , $\overline{NMI}$ , $INT0$ | $V_{TH}$              |   | 0.4                     | 1.0              |            | V         |
| Programmable<br>pull-down resistor                              | $R_{KL}$              | $V_{CC} = 5 V \pm 10\%$<br>$V_{CC} = 3 V \pm 10\%$                                      | 10<br>30                |                  | 80<br>150  | $k\Omega$ |
| Programmable<br>pull-up resistor                                | $R_{KH}$              | $V_{CC} = 5 V \pm 10\%$<br>$V_{CC} = 3 V \pm 10\%$                                      | 50<br>100               |                  | 150<br>300 |           |
| NORMAL (Note 3)   | $I_{CC}$              | $V_{CC} = 5 V \pm 10\%$<br>$f_c = 20 MHz$   |                         | 19               | 25         | mA        |
| NORMAL2 (Note 4)  |                       |   |                         | 24               | 30         |           |
| RUN   |                       |   |                         | 17               | 25         |           |
| IDLE2   |                       |   |                         | 10               | 15         |           |
| IDLE1   |                       |   |                         | 3.5              | 5          |           |
| NORMAL (Note 3)   |                       | $V_{CC} = 3 V \pm 10\%$<br>$f_c = 10 MHz$<br>(Typ: $V_{CC} = 3.0 V$ )                   |                         | 5.5              | 8          | mA        |
| NORMAL2 (Note 4)  |                       |   |                         | 8.5              | 11         |           |
| RUN   |                       |   |                         | 4.0              | 7          |           |
| IDLE2   |                       |   |                         | 2.5              | 4          |           |
| IDLE1   |                       |   |                         | 0.7              | 1.2        |           |
| SLOW (Note 3)   |                       | $V_{CC} = 3 V \pm 10\%$<br>$f_s = 32.768 kHz$<br>(Typ: $V_{CC} = 3.0 V$ )               |                         | 20               | 35         | $\mu A$   |
| RUN   |                       |   |                         | 16               | 30         |           |
| IDLE2   |                       |   |                         | 10               | 20         |           |
| IDLE1   |                       |   |                         | 5                | 15         |           |
| STOP  |                       |   | $V_{CC} = 2.7 to 5.5 V$ |                  | 0.2        |           |

Note 1: Typical values are for  $T_a = 25^\circ C$  and  $V_{CC} = 5 V$  unless otherwise noted.

Note 2:  $I_{DAR}$  is guaranteed for up to eight ports.

Note 3:  $I_{CC}$  measurement conditions (NORMAL, SLOW): Only CPU is operational; output pins are open and input pins are fixed.

Note 4:  $I_{CC}$  measurement conditions (NORMAL 2): All functions are operational; output pins are open and input pins are fixed.

## 4.3 AC Electrical Characteristics

(1)  $V_{CC} = 5\text{ V} \pm 10\%$ 

| No. | Parameter   | Symbol            | Variable  |            | 16 MHz |     | 20 MHz |     | Unit |
|-----|---|-------------------|-----------|------------|--------|-----|--------|-----|------|
|     |   |                   | Min       | Max        | Min    | Max | Min    | Max |      |
| 1   | Osc. period (=x)  | t <sub>OSC</sub>  | 50        | 31250      | 62.5   |     | 50     |     | ns   |
| 2   | CLK pulse width   | t <sub>CLK</sub>  | 2x – 40   |            | 85     |     | 60     |     | ns   |
| 3   | A0 to A23 fall → CLK hold   | t <sub>AK</sub>   | 0.5x – 20 |            | 11     |     | 5      |     | ns   |
| 4   | CLK valid → A0 to A 23 hold   | t <sub>KA</sub>   | 1.5x – 70 |            | 24     |     | 5      |     | ns   |
| 5   | A0 to A15 valid → ALE fall  | t <sub>AL</sub>   | 0.5x – 15 |            | 16     |     | 10     |     | ns   |
| 6   | ALE fall → A0 to A15 hold   | t <sub>LA</sub>   | 0.5x – 20 |            | 11     |     | 5      |     | ns   |
| 7   | ALE high pulse width  | t <sub>LL</sub>   | x – 40    |            | 23     |     | 10     |     | ns   |
| 8   | ALE fall → $\overline{\text{RD}} / \overline{\text{WR}}$ fall   | t <sub>LC</sub>   | 0.5x – 25 |            | 6      |     | 0      |     | ns   |
| 9   | $\overline{\text{RD}} / \overline{\text{WR}}$ rise → ALE rise   | t <sub>CL</sub>   | 0.5x – 20 |            | 11     |     | 5      |     | ns   |
| 10  | A0 to A15 valid → $\overline{\text{RD}} / \overline{\text{WR}}$ fall  | t <sub>ALC</sub>  | x – 25    |            | 38     |     | 25     |     | ns   |
| 11  | A0 to A23 valid → $\overline{\text{RD}} / \overline{\text{WR}}$ fall  | t <sub>ACH</sub>  | 1.5x – 50 |            | 44     |     | 25     |     | ns   |
| 12  | $\overline{\text{RD}} / \overline{\text{WR}}$ rise → A0 to A23 hold   | t <sub>CA</sub>   | 0.5x – 25 |            | 6      |     | 0      |     | ns   |
| 13  | A0 to A15 valid → D0 to D15 input   | t <sub>ADL</sub>  |           | 3.0x – 55  |        | 133 |        | 95  | ns   |
| 14  | A0 to A23 valid → D0 to D15 input   | t <sub>ADH</sub>  |           | 3.5x – 65  |        | 154 |        | 110 | ns   |
| 15  | $\overline{\text{RD}}$ fall → D0 to D15 input   | t <sub>RD</sub>   |           | 2.0x – 60  |        | 65  |        | 40  | ns   |
| 16  | $\overline{\text{RD}}$ low pulse width  | t <sub>RR</sub>   | 2.0x – 40 |            | 85     |     | 60     |     | ns   |
| 17  | $\overline{\text{RD}}$ rise → D0 to D15 hold  | t <sub>HR</sub>   | 0         |            | 0      |     | 0      |     | ns   |
| 18  | $\overline{\text{RD}}$ rise → A0 to A15 output  | t <sub>RAE</sub>  | x – 15    |            | 48     |     | 35     |     | ns   |
| 19  | $\overline{\text{WR}}$ low pulse width  | t <sub>WW</sub>   | 2.0x – 40 |            | 85     |     | 60     |     | ns   |
| 20  | D0 to D15 valid → $\overline{\text{WR}}$ rise   | t <sub>DW</sub>   | 2.0x – 55 |            | 70     |     | 45     |     | ns   |
| 21  | $\overline{\text{WR}}$ rise → D0 to D15 hold  | t <sub>WD</sub>   | 0.5x – 15 |            | 16     |     | 10     |     | ns   |
| 22  | A0 to A23 valid → $\overline{\text{WAIT}}$ input <small>(1+N) WAIT mode</small>                                   | t <sub>AWH</sub>  |           | 3.5x – 90  |        | 129 |        | 85  | ns   |
| 23  | A0 to A15 valid → $\overline{\text{WAIT}}$ input <small>(1+N) WAIT mode</small>                                   | t <sub>AWL</sub>  |           | 3.0x – 80  |        | 108 |        | 70  | ns   |
| 24  | $\overline{\text{RD}} / \overline{\text{WR}}$ fall → $\overline{\text{WAIT}}$ hold <small>(1+N) WAIT mode</small> | t <sub>CW</sub>   | 2.0x + 0  |            | 125    |     | 100    |     | ns   |
| 25  | A0 to A23 valid → Port input  | t <sub>APH</sub>  |           | 2.5x – 120 |        | 36  |        | 5   | ns   |
| 26  | A0 to A23 valid → Port hold   | t <sub>APH2</sub> | 2.5x + 50 |            | 206    |     | 175    |     | ns   |
| 27  | $\overline{\text{WR}}$ rise → Port valid  | t <sub>CP</sub>   |           | 200        |        | 200 |        | 200 | ns   |
| 28  | A0 to A23 valid → $\overline{\text{RAS}}$ fall  | t <sub>ASRH</sub> | 1.0x – 40 |            | 23     |     | 10     |     | ns   |
| 29  | A0 to A15 valid → $\overline{\text{RAS}}$ fall  | t <sub>ASRL</sub> | 0.5x – 15 |            | 16     |     | 10     |     | ns   |
| 30  | $\overline{\text{RAS}}$ fall → D0 to D15 input  | t <sub>RAC</sub>  |           | 2.5x – 70  |        | 86  |        | 55  | ns   |
| 31  | $\overline{\text{RAS}}$ fall → A0 to A15 hold   | t <sub>RAH</sub>  | 0.5x – 15 |            | 16     |     | 10     |     | ns   |
| 32  | $\overline{\text{RAS}}$ low pulse width   | t <sub>RAS</sub>  | 2.0x – 40 |            | 85     |     | 60     |     | ns   |
| 33  | $\overline{\text{RAS}}$ high pulse width  | t <sub>RP</sub>   | 2.0x – 40 |            | 85     |     | 60     |     | ns   |
| 34  | $\overline{\text{CAS}}$ fall → $\overline{\text{RAS}}$ rise   | t <sub>RSH</sub>  | 1.0x – 40 |            | 23     |     | 10     |     | ns   |
| 35  | $\overline{\text{RAS}}$ rise → $\overline{\text{CAS}}$ rise   | t <sub>RSC</sub>  | 0.5x – 25 |            | 6      |     | 0      |     | ns   |
| 36  | $\overline{\text{RAS}}$ fall → $\overline{\text{CAS}}$ fall   | t <sub>RCD</sub>  | 1.0x – 40 |            | 23     |     | 10     |     | ns   |
| 37  | $\overline{\text{CAS}}$ fall → D0 to D15 input  | t <sub>CAC</sub>  |           | 1.5x – 65  |        | 29  |        | 10  | ns   |
| 38  | $\overline{\text{CAS}}$ low pulse width   | t <sub>CAS</sub>  | 1.5x – 30 |            | 64     |     | 40     |     | ns   |

## AC measuring condition

- Output level: High 2.2 V/Low 0.8 V,  $C_L = 50\text{ pF}$   
(However,  $C_L = 100\text{ pF}$  for AD0 to AD15, A0 to A23, ALE,  $\overline{\text{RD}}$ ,  $\overline{\text{WR}}$ ,  $\overline{\text{HWR}}$ ,  $\overline{\text{R/W}}$ , CLK,  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS0}}$  to  $\overline{\text{CAS2}}$ )
- Input level: High 2.4 V/Low 0.45 V (AD0 to AD15)  
High  $0.8 \times V_{CC}$ /Low  $0.2 \times V_{CC}$  (except AD0 to AD15)

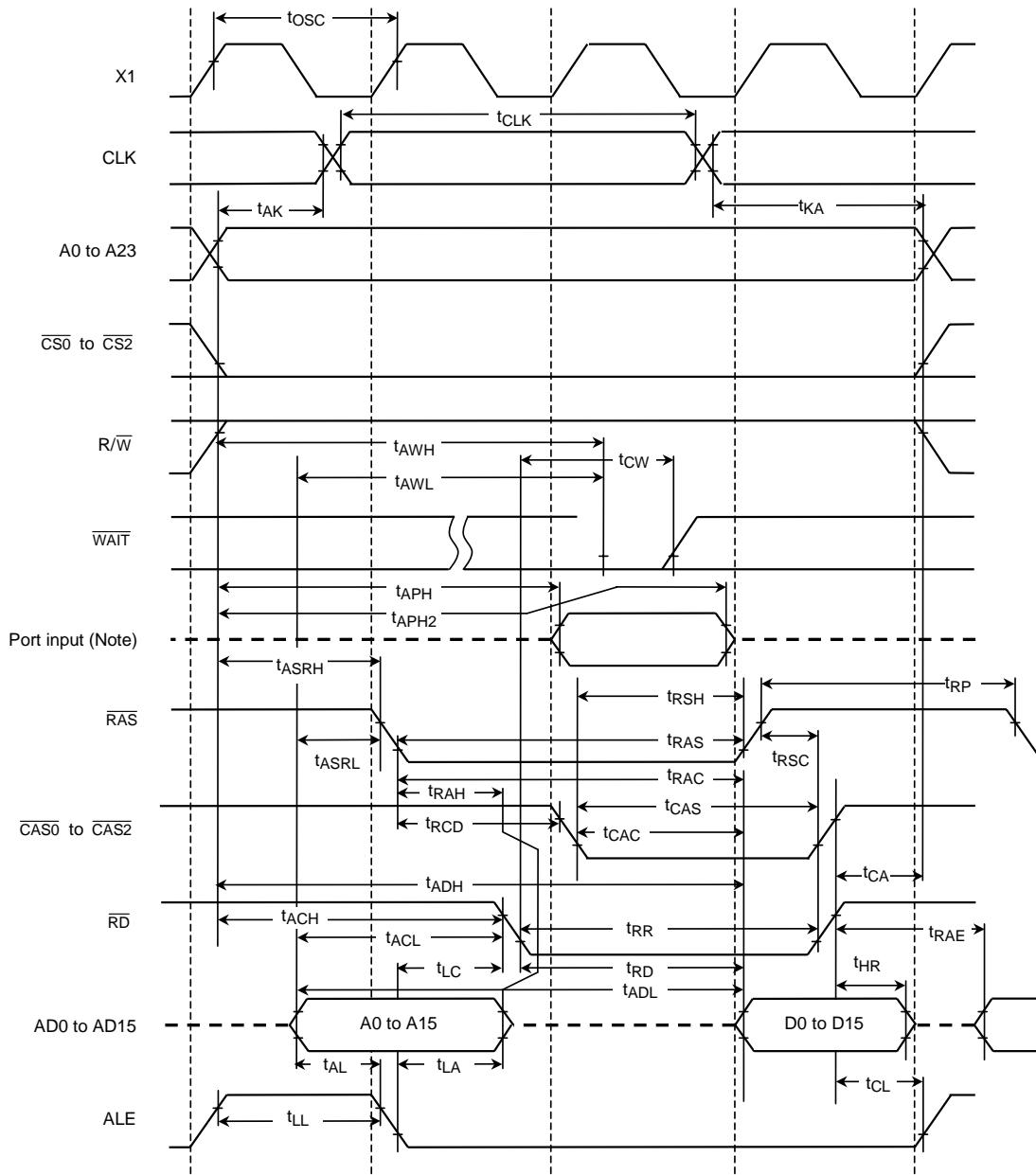
(2)  $V_{CC} = 3V \pm 10\%$  (TMP93CM40F is guaranteed up to 10 MHz operation.)

| No. | Parameter  | Symbol             | Variable   |            | 10 MHz |     | Unit |
|-----|--|--------------------|------------|------------|--------|-----|------|
|     |  |                    | Min        | Max        | Min    | Max |      |
| 1   | Osc. period (= x)  | t <sub>OSC</sub>   | 100        | 31250      | 100    |     | ns   |
| 2   | CLK pulse width  | t <sub>CLK</sub>   | 2x - 40    |            | 160    |     | ns   |
| 3   | A0 to A23 fall → CLK hold  | t <sub>AK</sub>    | 0.5x - 30  |            | 20     |     | ns   |
| 4   | CLK valid → A0 to A 23 hold  | t <sub>KA</sub>    | 1.5x - 80  |            | 70     |     | ns   |
| 5   | A0 to A15 valid → ALE fall   | t <sub>AL</sub>    | 0.5x - 35  |            | 15     |     | ns   |
| 6   | ALE fall → A0 to A15 hold  | t <sub>LA</sub>    | 0.5x - 35  |            | 15     |     | ns   |
| 7   | ALE high pulse width   | t <sub>LL</sub>    | x - 60     |            | 40     |     | ns   |
| 8   | ALE fall → $\overline{RD}$ / $\overline{WR}$ fall  | t <sub>LC</sub>    | 0.5x - 35  |            | 15     |     | ns   |
| 9   | $\overline{RD}$ / $\overline{WR}$ rise → ALE rise  | t <sub>CL</sub>    | 0.5x - 40  |            | 10     |     | ns   |
| 10  | A0 to A15 valid → $\overline{RD}$ / $\overline{WR}$ fall                                       | t <sub>ALC</sub>   | x - 50     |            | 50     |     | ns   |
| 11  | A0 to A23 valid → $\overline{RD}$ / $\overline{WR}$ fall                                       | t <sub>ACH</sub>   | 1.5x - 50  |            | 100    |     | ns   |
| 12  | $\overline{RD}$ / $\overline{WR}$ rise → A0 to A23 hold  | t <sub>CA</sub>    | 0.5x - 40  |            | 10     |     | ns   |
| 13  | A0 to A15 valid → D0 to D15 input  | t <sub>ADL</sub>   |            | 3.0x - 110 |        | 190 | ns   |
| 14  | A0 to A23 valid → D0 to D15 input  | t <sub>ADH</sub>   |            | 3.5x - 125 |        | 225 | ns   |
| 15  | $\overline{RD}$ fall → D0 to D15 input   | t <sub>RD</sub>    |            | 2.0x - 115 |        | 85  | ns   |
| 16  | $\overline{RD}$ low pulse width  | t <sub>RR</sub>    | 2.0x - 40  |            | 160    |     | ns   |
| 17  | $\overline{RD}$ rise → D0 to D15 hold  | t <sub>HR</sub>    | 0          |            | 0      |     | ns   |
| 18  | $\overline{RD}$ rise → A0 to A15 output  | t <sub>RAE</sub>   | x - 25     |            | 75     |     | ns   |
| 19  | $\overline{WR}$ low pulse width  | t <sub>WW</sub>    | 2.0x - 40  |            | 160    |     | ns   |
| 20  | D0 to D15 valid → $\overline{WR}$ rise   | t <sub>DW</sub>    | 2.0x - 120 |            | 80     |     | ns   |
| 21  | $\overline{WR}$ rise → D0 to D15 hold  | t <sub>WD</sub>    | 0.5x - 40  |            | 10     |     | ns   |
| 22  | A0 to A23 valid → $\overline{WAIT}$ input <small>(1+N) WAIT mode</small>                       | t <sub>AWH</sub>   |            | 3.5x - 130 |        | 220 | ns   |
| 23  | A0 to A15 valid → $\overline{WAIT}$ input <small>(1+N) WAIT mode</small>                       | t <sub>AWL</sub>   |            | 3.0x - 100 |        | 200 | ns   |
| 24  | $\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ hold <small>(1+N) WAIT mode</small> | t <sub>CW</sub>    | 2.0x + 0   |            | 200    |     | ns   |
| 25  | A0 to A23 valid → Port input   | t <sub>APH</sub>   |            | 2.5x - 245 |        | 5   | ns   |
| 26  | A0 to A23 valid → Port hold  | t <sub>APH2</sub>  | 2.5x + 50  |            | 300    |     | ns   |
| 27  | $\overline{WR}$ rise → Port valid  | t <sub>CP</sub>    |            | 200        |        | 200 | ns   |
| 28  | A0 to A23 valid → $\overline{RAS}$ fall  | t <sub>ASRH</sub>  | 1.0x - 60  |            | 40     |     | ns   |
| 29  | A0 to A15 valid → $\overline{RAS}$ fall  | t <sub>ASRL</sub>  | 0.5x - 40  |            | 10     |     | ns   |
| 30  | $\overline{RAS}$ fall → D0 to D15 input  | t <sub>RAC</sub>   |            | 2.5x - 90  |        | 160 | ns   |
| 31  | $\overline{RAS}$ fall → A0 to A15 hold   | t <sub>RAH</sub>   | 0.5x - 25  |            | 25     |     | ns   |
| 32  | $\overline{RAS}$ low pulse width   | t <sub>RAS</sub>   | 2.0x - 40  |            | 160    |     | ns   |
| 33  | $\overline{RAS}$ high pulse width  | t <sub>RP</sub>    | 2.0x - 40  |            | 160    |     | ns   |
| 34  | $\overline{CAS}$ fall → $\overline{RAS}$ rise  | t <sub>RSRSH</sub> | 1.0x - 55  |            | 45     |     | ns   |
| 35  | $\overline{RAS}$ rise → $\overline{CAS}$ rise  | t <sub>RSC</sub>   | 0.5x - 25  |            | 25     |     | ns   |
| 36  | $\overline{RAS}$ fall → $\overline{CAS}$ fall  | t <sub>RCD</sub>   | 1.0x - 40  |            | 60     |     | ns   |
| 37  | $\overline{CAS}$ fall → D0 to D15 input  | t <sub>CAC</sub>   |            | 1.5x - 120 |        | 30  | ns   |
| 38  | $\overline{CAS}$ low pulse width   | t <sub>CAS</sub>   | 1.5x - 40  |            | 110    |     | ns   |

## AC measuring condition

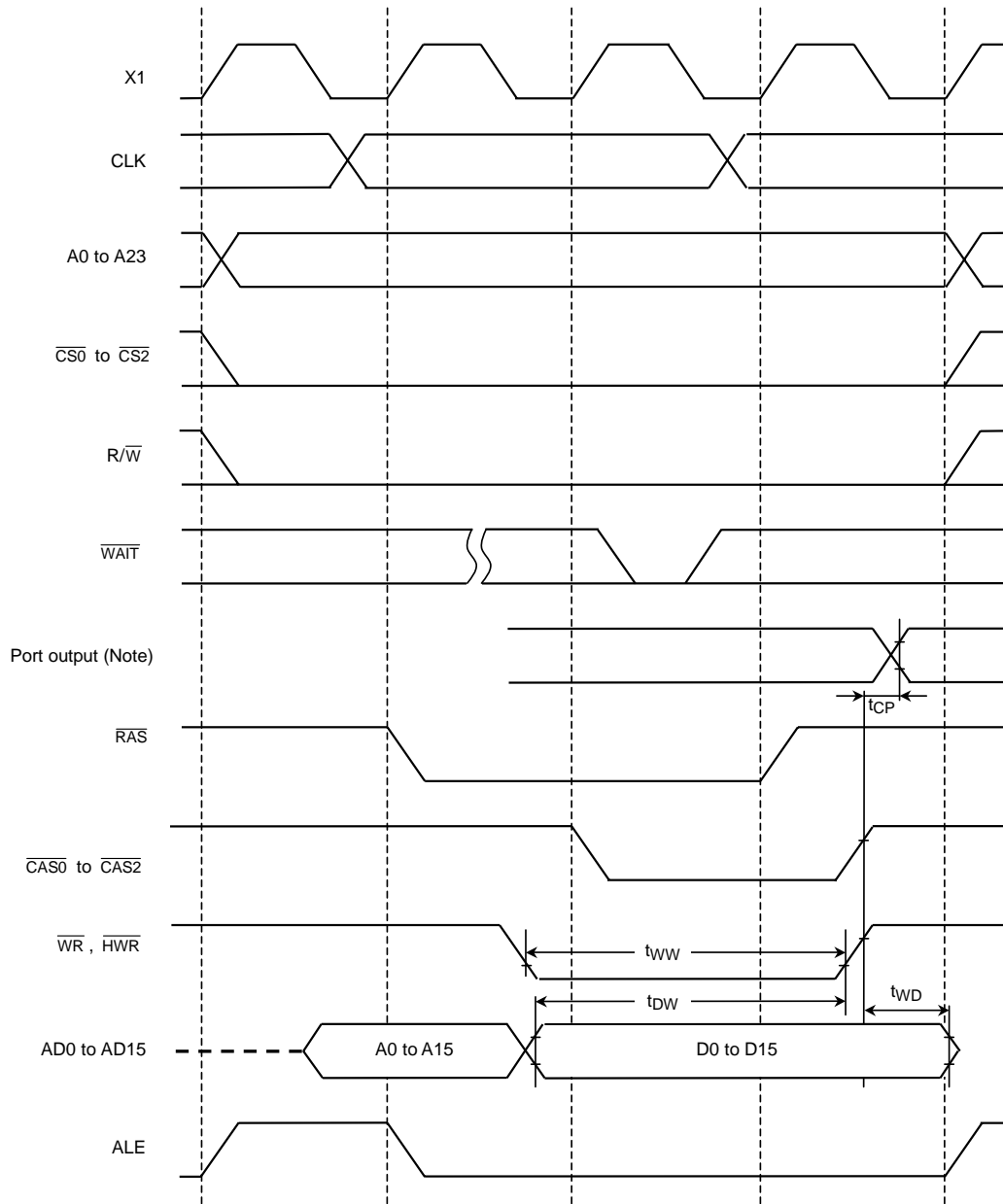
- Output level: High  $0.7 \times V_{CC}$ /Low  $0.3 \times V_{CC}$ ,  $C_L = 50$  pF
- Input level: High  $0.9 \times V_{CC}$ /Low  $0.1 \times V_{CC}$

(1) Read cycle



Note: Since the CPU accesses the internal area to read data from a port, the control signals of external pins such as  $\overline{RD}$  and  $\overline{CS}$  are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

(2) Write cycle



Note: Since the CPU accesses the internal area to write data to a port, the control signals of external pins such as  $\overline{WR}$  and  $\overline{CS}$  are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.



## 4.4 AD Conversion Characteristics

AVCC = VCC, AVSS = VSS

| Parameter   | Symbol                | Min         | Typ. | Max         | Unit |
|---|-----------------------|-------------|------|-------------|------|
| Analog reference voltage (+)  | VREFH                 | VCC - 0.2 V | VCC  | VCC         | V    |
| Analog reference voltage (-)  | VREFL                 | VSS         | VSS  | VSS + 0.2 V |      |
| Analog input voltage range  | VAIN                  | VREFL       |      | VREFH       |      |
| Analog current for analog reference voltage<br>VCC = 5 V ± 10% <VREFON> = 1 | IREF<br>(VREFL = 0 V) |             | 0.5  | 1.5         | mA   |
| VCC = 5 V ± 10% <VREFON> = 0  |                       |             | 0.02 | 5.0         | μA   |
| Error (not including quantizing errors)                                     | -                     |             | ±3.0 | ±6          | LSB  |

Note 1:  $1\text{LSB} = (V_{\text{REFH}} - V_{\text{REFL}}) / 2^{10}$  [V]

Note 2: The operation above is guaranteed for  $f_{\text{FPH}} \geq 4$  MHz.

Note 3: The value I<sub>CC</sub> includes the current which flows through the AVCC pin.

Note 4: The operation of this AD converter is guaranteed at 5 V ± 10%.

### 4.5 Serial Channel Timing

(1) I/O interface mode

a. SCLK input mode

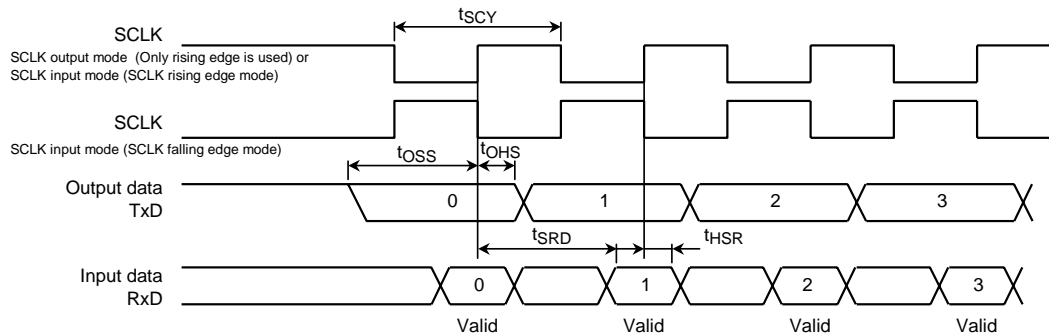
| Parameter  | Symbol    | Variable              |     | 32.768 kHz<br>(Note 1) |     | 10 MHz      |     | 20 MHz |     | Unit   |
|--|-----------|-----------------------|-----|------------------------|-----|-------------|-----|--------|-----|--------|
|  |           | Min                   | Max | Min                    | Max | Min         | Max | Min    | Max |        |
| SCLK cycle   | $t_{SCY}$ | 16x                   |     | 488 $\mu$ s            |     | 1600        |     | 800    |     | ns     |
| Output data $\rightarrow$ Rising edge or falling edge (Note 2) of SCLK       | $t_{OSS}$ | $t_{SCY}/2 - 5x - 50$ |     | 91.5 $\mu$ s           |     | 250         |     | 100    |     | ns     |
| SCLK rising edge or falling edge (Note 2) $\rightarrow$ Output data hold     | $t_{OHS}$ | $5x - 100$            |     | 152 $\mu$ s            |     | 400         |     | 150    |     | ns     |
| SCLK rising edge or falling edge (Note 2) $\rightarrow$ Input data hold      | $t_{HSR}$ | 0                     |     | 0                      |     | 0           |     | 0      |     | ns     |
| SCLK rising edge or falling edge (Note 2) $\rightarrow$ Effective data input | $t_{SRD}$ |                       |     | $t_{SCY} - 5x - 100$   |     | 336 $\mu$ s |     | 1000   |     | 450 ns |

Note 1: System clock is fs, or input clock to prescaler is divisor clock of fs.

Note 2: The rising edge is used in SCLK rising mode.  
The falling edge is used SCLK falling mode.

b. SCLK output mode

| Parameter   | Symbol    | Variable             |       | 32.768 kHz<br>(Note) |        | 10 MHz      |       | 20 MHz |       | Unit    |
|---|-----------|----------------------|-------|----------------------|--------|-------------|-------|--------|-------|---------|
|   |           | Min                  | Max   | Min                  | Max    | Min         | Max   | Min    | Max   |         |
| SCLK cycle (Programmable)                           | $t_{SCY}$ | 16X                  | 8192X | 488                  | 250 ms | 1.6         | 819.2 | 0.8    | 409.6 | $\mu$ s |
| Output data $\rightarrow$ SCLK rising edge          | $t_{OSS}$ | $t_{SCY} - 5X - 150$ |       | 427 $\mu$ s          |        | 1250        |       | 550    |       | ns      |
| SCLK rising edge $\rightarrow$ Output data hold     | $t_{OHS}$ | $2x - 80$            |       | 60 $\mu$ s           |        | 120         |       | 20     |       | ns      |
| SCLK rising edge $\rightarrow$ Input data hold      | $t_{HSR}$ | 0                    |       | 0                    |        | 0           |       | 0      |       | ns      |
| SCLK rising edge $\rightarrow$ Effective data input | $t_{SRD}$ |                      |       | $t_{SCY} - 2x - 150$ |        | 428 $\mu$ s |       | 1250   |       | 550 ns  |



Note: System clock is fs, or input clock to prescaler is divisor clock of fs.

## 4.6 Timer/Counter Input Clock (TI0, TI4, TI5, TI6 and TI7)

| Parameter                    | Symbol     | Variable   |     | 10 MHz |     | 20 MHz |     | Unit |
|------------------------------|------------|------------|-----|--------|-----|--------|-----|------|
|                              |            | Min        | Max | Min    | Max | Min    | Max |      |
| Clock cycle                  | $t_{VCK}$  | $8X + 100$ |     | 900    |     | 500    |     | ns   |
| Low level clock pulse width  | $t_{VCKL}$ | $4X + 40$  |     | 440    |     | 240    |     | ns   |
| High level clock pulse width | $t_{VCKH}$ | $4X + 40$  |     | 440    |     | 240    |     | ns   |

## 4.7 Interrupt and Capture

(1)  $\overline{NMI}$ , INT0 interrupts

| Parameter                                      | Symbol      | Variable |     | 10 MHz |     | 20 MHz |     | Unit |
|--|-------------|----------|-----|--------|-----|--------|-----|------|
|  |             | Min      | Max | Min    | Max | Min    | Max |      |
| $\overline{NMI}$ , INT0 low level pulse width  | $t_{INTAL}$ | 4X       |     | 400    |     | 200    |     | ns   |
| $\overline{NMI}$ , INT0 high level pulse width | $t_{INTAH}$ | 4X       |     | 400    |     | 200    |     | ns   |

(2) INT4 to 7 interrupt, capture

The INT4 to 7 input pulse width depends on the CPU operation clock and timer (9-bit prescaler). The following shows the pulse width for each clock.

| System Clock Selected<br><SYSCK> | Prescaler Clock Selected<br><PRCK1:0> | $t_{INTBL}$ (INT4 to 7 low-level pulse width) |        | $t_{INTBH}$ (INT4 to 7 high-level pulse width) |        | Unit    |
|----------------------------------|---------------------------------------|---|--------|--|--------|---------|
|                                  |                                       | Variable                                      | 20 MHz | Variable                                       | 20 MHz |         |
|                                  |                                       | Min   | Min    | Min  | Min    |         |
| 0 (fc)                           | 00 ( $f_{IFPH}$ )                     | $8X + 100$                                    | 500    | $8X + 100$                                     | 500    | ns      |
|                                  | 01 (fs)                               | $8XT + 0.1$                                   | 244.3  | $8XT + 0.1$                                    | 244.3  |         |
|                                  | 10 (fc/16)                            | $128X + 0.1$                                  | 6.5    | $128X + 0.1$                                   | 6.5    |         |
| 1 (fs)<br>(Note 2)               | 00 ( $f_{IFPH}$ )                     | $8XT + 0.1$                                   | 244.3  | $8XT + 0.1$                                    | 244.3  | $\mu s$ |
|                                  | 01 (fs)                               |   |        |  |        |         |

Note 1: XT represents the frequency of the low-frequency clock fs. It is calculated at fs = 32.768 kHz.

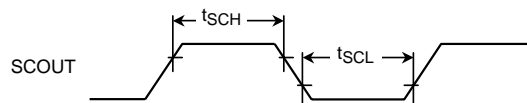
Note 2: When using fs as the system clock, fc/16 cannot be selected as the prescaler clock.

## 4.8 SCOUT Pin AC Characteristics

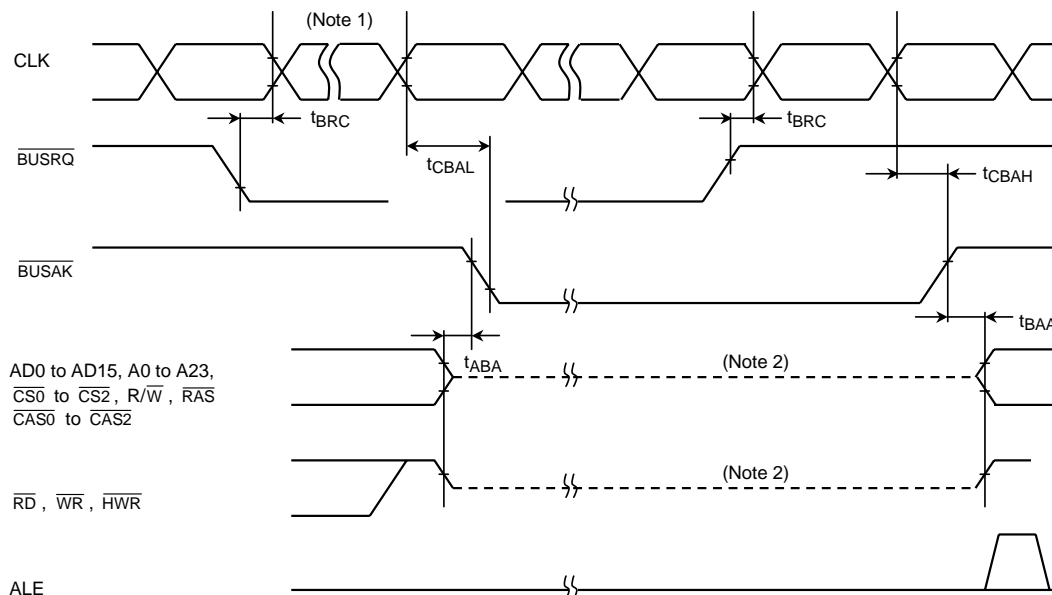
| Parameter   | Symbol    | Variable    |     | 10 MHz |     | 20 MHz |     | Unit |
|---|-----------|-------------|-----|--------|-----|--------|-----|------|
|   |           | Min         | Max | Min    | Max | Min    | Max |      |
| High-level pulse width<br>$V_{CC} = 5 V \pm 10\%$ | $t_{SCH}$ | $0.5X - 10$ |     | 40     |     | 15     |     | ns   |
| High-level pulse width<br>$V_{CC} = 3 V \pm 10\%$ |           |             |     | 30     |     | -      | -   |      |
| Low-level pulse width<br>$V_{CC} = 5 V \pm 10\%$  | $t_{SCL}$ | $0.5X - 10$ |     | 40     |     | 15     |     | ns   |
| Low-level pulse width<br>$V_{CC} = 3 V \pm 10\%$  |           |             |     | 30     |     | -      | -   |      |

Measurement condition

- Output level: High 2.2 V/Low 0.8 V,  $C_L = 10pF$



4.9 Timing Chart for Bus Request ( $\overline{\text{BUSRQ}}$ )/Bus Acknowledge ( $\overline{\text{BUSAK}}$ )



| Parameter                                      | Symbol | Variable |              | 10 MHz |     | 20 MHz |     | Unit |
|--|--------|----------|--------------|--------|-----|--------|-----|------|
|  |        | Min      | Max          | Min    | Max | Min    | Max |      |
| $\overline{\text{BUSRQ}}$ set-up time to CLK   | tBRC   | 120      |              | 120    |     | 120    |     | ns   |
| CLK → $\overline{\text{BUSAK}}$ falling edge   | tCBAL  |          | $0.5x + 120$ |        | 270 |        | 195 | ns   |
| CLK → $\overline{\text{BUSAK}}$ rising edge    | tCBAH  |          | $0.5x + 40$  |        | 90  |        | 65  | ns   |
| Output buffer off to $\overline{\text{BUSAK}}$ | tABA   | 0        | 80           | 0      | 80  | 0      | 80  | ns   |
| $\overline{\text{BUSAK}}$ to output buffer on  | tBAA   | 0        | 80           | 0      | 80  | 0      | 80  | ns   |

Note 1: Even if the  $\overline{\text{BUSRQ}}$  signal goes low, the bus will not be released while the  $\overline{\text{WAIT}}$  signal is low. The bus will only be released when  $\overline{\text{BUSRQ}}$  goes low while  $\overline{\text{WAIT}}$  is high.

Note 2: This line shows only that the output buffer is in the off state.

It does not indicate that the signal level is fixed.

Just after the bus is released, the signal level set before the bus was released is maintained dynamically by the external capacitance. Therefore, to fix the signal level using an external resistor during bus release, careful design is necessary, as fixing of the level is delayed.

The internal programmable pull-up/pull-down resistor is switched between the active and non-active states by the internal signal.

#### 4.10 Recommended Oscillator

The TMP93CM40 is evaluated with various resonators. The evaluation results are displayed below to enable appropriate selection for any given application.

Note: The load capacitance of the resonator consists of the load capacitors C1 and C2 which are to be connected, and the floating capacitance of the target board.

Even if the specified values of C1 and C2 are used, there is a possibility that the oscillator will malfunction due to varying load capacitance on the target boards. Hence the oscillator's wiring patterns on the board should be designed to be as short as possible.

It is recommended that evaluation of the resonators be conducted on the target board.

##### (1) Examples of resonator connection

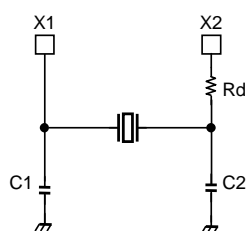


Figure 1: Example of High-frequency Resonator Connection

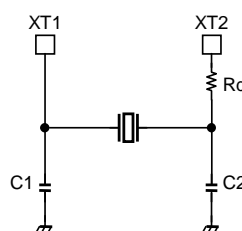


Figure 2: Example of Low-frequency Resonator Connection

##### (2) Ceramic resonator: Murata Manufacturing Co., Ltd. (Note 1)

Ta = -20 to 80°C

| Parameter                  | Frequency (MHz) | Recommended Resonator | Recommended Value   |                     |                     | V <sub>CC</sub> [V] |
|----------------------------|-----------------|-----------------------|---------------------|---------------------|---------------------|---------------------|
|                            |                 |                       | C <sub>1</sub> [pF] | C <sub>2</sub> [pF] | R <sub>d</sub> [kΩ] |                     |
| High-frequency oscillation | 4.00            | CSA4.00MGU            | 30                  | 30                  | 0                   | 2.7 to 5.5          |
|                            |                 | CST4.00MGWU           | (30)<br>(Note 2)    | (30)<br>(Note 2)    |                     |                     |
|                            | 10.00           | CSA10.00MTZ093        | 30                  | 30                  |                     |                     |
|                            |                 | CST10.00MTW093        | (30)<br>(Note 2)    | (30)<br>(Note 2)    |                     |                     |
|                            | 16.00           | CSA16.00MXZ040        | 5                   | 5                   |                     | 4.5 to 5.5          |
| 20.00                      | CSA20.00MXZ040  | 5                     | 5                   |                     |                     |                     |

Note 1: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change.

For up-to-date information, please refer to the following URL:  
<http://www.murata.com/>

Note 2: For built-in condenser type

5. Package Dimensions

P-QFP100-1414-0.50

Unit: mm

