Low Voltage/Low Power CMOS 16-Bit Microcontrollers

TMP93CS40F/TMP93CS41F
TMP93CS40DF/TMP93CS41DF

1. Outline and Device Characteristics

The TMP93CS40/S41 are high-speed advanced 16-bit microcontrollers developed for controlling medium to large-scale equipment. The TMP93CS41 does not have a ROM; the TMP93CS40 has a built-in ROM. Otherwise, the devices function in the same way.

The TMP93CS40/S41F are housed in a 100-pin flat package.

The device characteristics are as follows:

(1) Original 16-bit CPU (900/L CPU)
- TLCS-90 instruction mnemonic upward compatible
- 16-Mbyte linear address space
- General-purpose registers, register bank system
- 16-bit multiplication/division and bit transfer/arithmetic instructions
- Micro DMA: 4 channels (1.6 μs/2 bytes at 20 MHz)

(2) Minimum instruction execution time: 200 ns at 20 MHz

(3) Internal RAM: 2 Kbytes
Internal ROM:

TMP93CS40	64-Kbyte ROM
TMP93CS41	None

(4) External memory expansion
- Can be expanded up to 16 Mbytes (for both programs and data).
- AM8/$\overline{\text{AM16}}$ pin (selects the external data bus width)
- Can mix 8-/16-bit external data buses.
..... Dynamic bus sizing

(5) 8-bit timer: 2 channels

(6) 8-bit PWM timer: 2 channels

(7) 16-bit timer: 2 channels

(8) 4-bit pattern generator: 2 channels

(9) Serial interface: 2 channels

(10) 10-bit AD converter: 8 channels

(11) Watchdog timer

(12) Chip select/wait controller: 3 blocks

(13) Interrupt functions: 29

- 9 CPU interrupts .... SWI instruction, and illegal instruction
- 14 internal interrupts ⎤ 7-level priority can be set.
- 6 external interrupts ⎦

(14) I/O ports
79 pins for TMP93CS40 and 61 pins for TMP93CS41

(15) Standby function: 4 HALT modes (RUN, IDLE2, IDLE1, STOP)

(16) Clock gear function

- Dual clock operation
- Clock gear: High-frequency clock can be varied from fc to fc/16.

(17) Wide operating voltage

- Vcc = 2.7 to 5.5 V

(18) Package

Type No.	Package
TMP93CS40F TMP93CS41F	P-QFP100-1414-0.50
TMP93CS40DF TMP93CS41DF	P-LQFP100-1414-0.50F

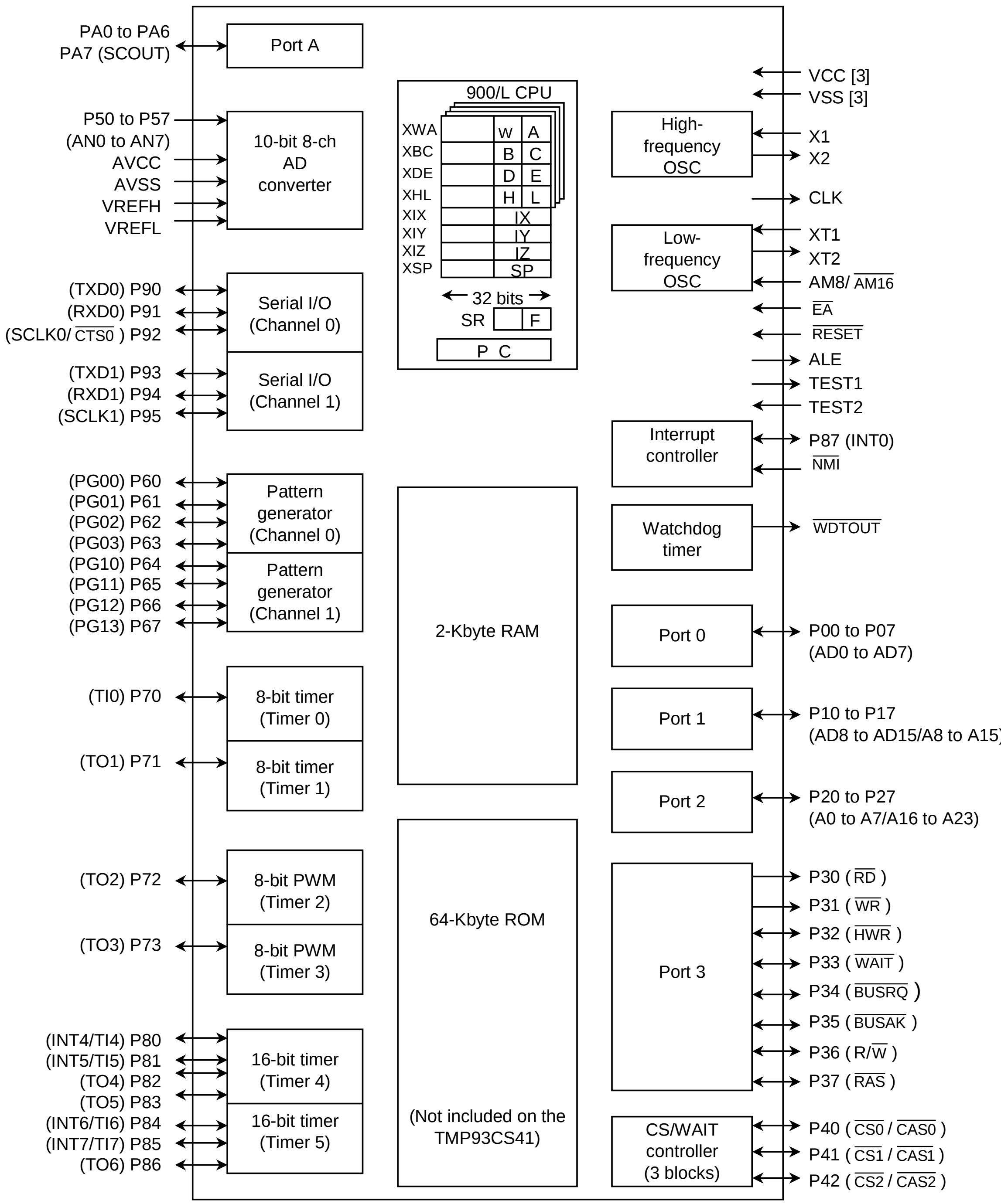


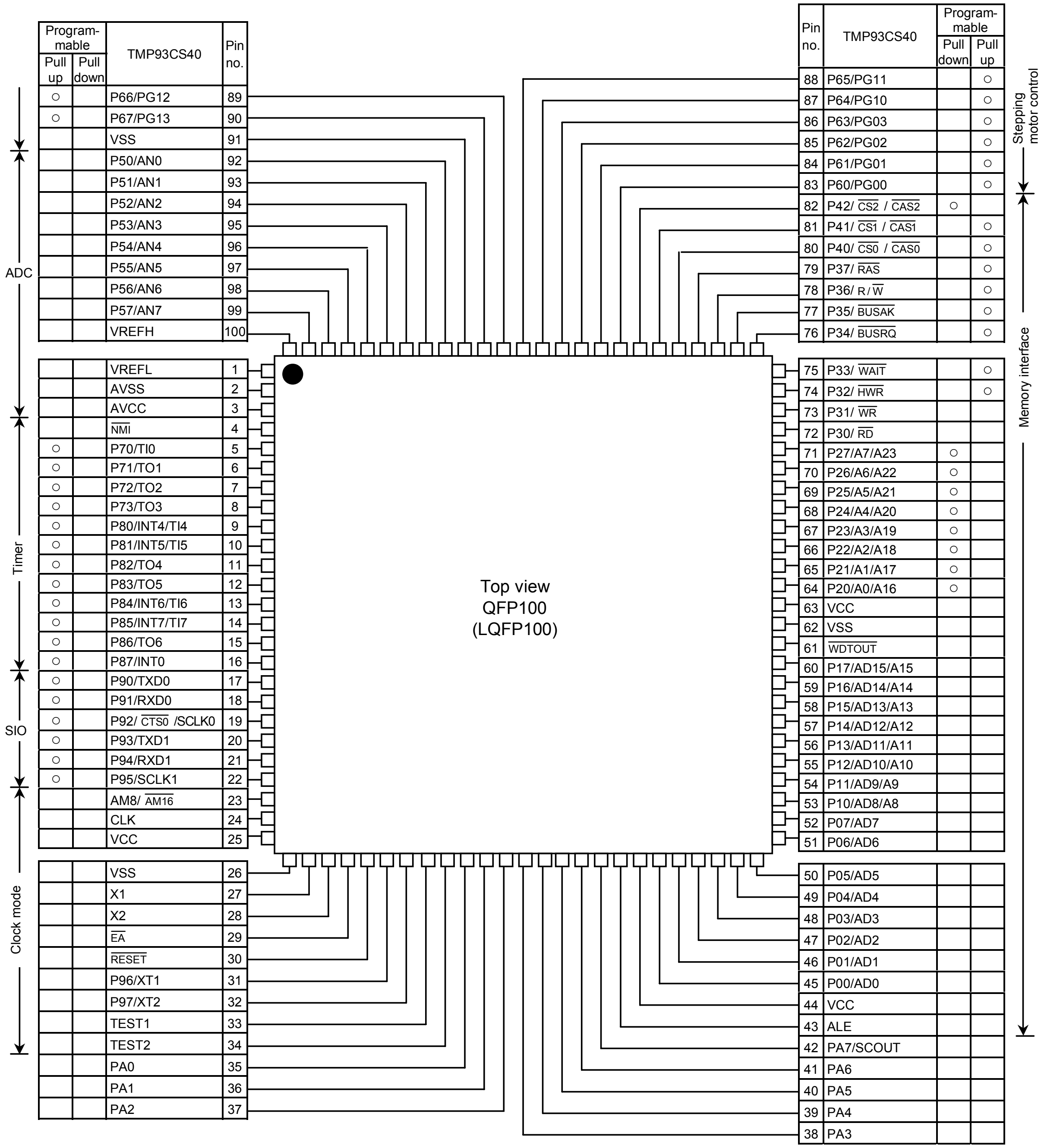
Figure 1.1 TMP93CS40/TMP93CS41 Block Diagram

2. Pin Assignment and Functions

The assignment of input/output pins on the TMP93CS40/TMP93CS41, their names and outline functions are described below.

2.1 Pin Assignment

Figure 2.1.1 shows the pin assignment for the TMP93CS40F/S41F and TMP93CS40DF/S41DF.



Note: Because the TMP93CS41 does not have an internal ROM, pins P00 to P17 are tied to AD0 to AD15 (when AM8/$\overline{\text{AM16}}$ = 0), or to AD0 to AD7 and A8 to A15 (when AM8/$\overline{\text{AM16}}$ = 1). P30 is tied to $\overline{\text{RD}}$, P31 to $\overline{\text{WR}}$.

Figure 2.1.1 Pin Assignment (100-Pin QFP and 100-Pin LQFP)

2.2 Pin Names and Functions

The names of the input/output pins and their functions are described below.

Table 2.2.1 to Table 2.2.4 show pin names and functions.

Table 2.2.1 Pin Names and Functions (1/4)

Pin Names	Number of Pins	I/O	Functions
P00 to P07 AD0 to AD7	8	I/O Tri-state	Port 0: I/O port that allows at the bit level Address/data (lower): Bits 0 to 7 of address/data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O Tri-state Output	Port 1: I/O port that allows at the bit level Address data (upper): Bits 8 to 15 of address/data bus Address: Bits 8 to 15 of address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows selection of I/O at the bit level (with pull-down resistor) Address: bits 0 to 7 of address bus Address: bits 16 to 23 of address bus
P30 $\overline{\text{RD}}$	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory
P31 $\overline{\text{WR}}$	1	Output Output	Port 31: Output port Write: Strobe signal for writing data on pins AD0 to AD7
P32 $\overline{\text{HWR}}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data on pins AD8 to AD15
P33 $\overline{\text{WAIT}}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: in used to request CPU bus wait
P34 $\overline{\text{BUSRQ}}$	1	I/O Input	Port 34: I/O port (with pull-up resistor) Bus request: Signal used to request bus release
P35 $\overline{\text{BUSAK}}$	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus acknowledge: Signal used to acknowledge bus release
P36 R/$\overline{\text{W}}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/write: 1 represents read or dummy cycle; 0 represents write cycle.
P37 $\overline{\text{RAS}}$	1	I/O Output	Port 37: I/O port (with pull-up resistor) Row address strobe: Outputs $\overline{\text{RAS}}$ strobe for DRAM.
P40 $\overline{\text{CS0}}$ $\overline{\text{CAS0}}$	1	I/O Output Output	Port 40: I/O port (with pull-up resistor) Chip select 0: Outputs 0 when address is within specified address area. Column address strobe 0: Outputs $\overline{\text{CAS}}$ strobe for DRAM when address is within specified address area.

Note: This device's built-in memory or built-in I/O cannot be accessed by an external DMA controller using the BUSRQ and BUSAK signals.

Table 2.2.2 Pin Names and Functions (2/4)

Pin Names	Number of Pins	I/O	Functions
P41 $\overline{CS1}$ $\overline{CAS1}$	1	I/O Output Output	Port 41: I/O port (with pull-up resistor) Chip select 1: Outputs 0 if address is within specified address area. Column address strobe 1: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P42 $\overline{CS2}$ $\overline{CAS2}$	1	I/O Output Output	Port 42: I/O port (with pull-down resistor) Chip select 2: Outputs 0 if address is within specified address area. Column address strobe 2: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P50 to P57 AN0 to AN7	8	Input Input	Port 5: Input port Analog input: Analog signal input for AD converter
VREFH	1	Input	Pin for high level reference voltage input to AD converter
VREFL	1	Input	Pin for low level reference voltage input to AD converter
P60 to P63 PG00 to PG03	4	I/O Output	Ports 60 to 63: I/O ports that allow selection of I/O at the bit level (with pull-up resistor) Pattern generator ports: 00 to 03
P64 to P67 PG10 to PG13	4	I/O Output	Ports 64 to 67: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor) Pattern generator ports: 10 to 13
P70 TI0	1	I/O Input	Port 70: I/O port (with pull-up resistor) Timer input 0: Timer 0 input
P71 TO1	1	I/O Output	Port 71: I/O port (with pull-up resistor) Timer output 1: Timer 0 or timer 1 output
P72 TO2	1	I/O Output	Port 72: I/O port (with pull-up resistor) PWM output 2: 8-bit PWM timer 2 output
P73 TO3	1	I/O Output	Port 73: I/O port (with pull-up resistor) PWM output 3: 8-bit PWM timer 3 output
P80 TI4 INT4	1	I/O Input Input	Port 80: I/O port (with pull-up resistor) Timer input 4: Timer 4 count/capture trigger signal input Interrupt request pin 4: Interrupt request pin with programmable rising/falling edge
P81 TI5 INT5	1	I/O Input Input	Port 81: I/O port (with pull-up resistor) Timer input 5: Timer 5 count/capture trigger signal input Interrupt request pin 5: Interrupt request pin with rising edge
P82 TO4	1	I/O Output	Port 82: I/O port (with pull-up resistor) Timer output 4: Timer 4 output pin
P83 TO5	1	I/O Output	Port 83: I/O port (with pull-up resistor) Timer output 5: Timer 4 output pin

Table 2.2.3 Pin Names and Functions (3/4)

Pin Names	Number of Pins	I/O	Functions
P84 TI6 INT6	1	I/O Input Input	Port 84: I/O port (with pull-up resistor) Timer input 6: Timer 5 count/capture trigger signal input Interrupt request pin 6: Interrupt request pin with programmable rising/falling edge
P85 TI7 INT7	1	I/O Input Input	Port 85: I/O port (with pull-up resistor) Timer input 7: Timer 5 count/capture trigger signal input Interrupt request pin 7: Interrupt request pin with rising edge
P86 TO6	1	I/O Output	Port 86: I/O port (with pull-up resistor) Timer output 6: Timer 5 output pin
P87 INT0	1	I/O Input	Port 87: I/O port (with pull-up resistor) Interrupt request pin 0: Interrupt request pin with programmable level/rising edge
P90 TXD0	1	I/O Output	Port 90: I/O port (with pull-up resistor) Serial data send 0
P91 RXD0	1	I/O Input	Port 91: I/O port (with pull-up resistor) Serial data receive 0
P92 $\overline{CTS0}$ SCLK0	1	I/O Input I/O	Port 92: I/O port (with pull-up resistor) Serial data send enable 0 (Clear to send) Serial Clock I/O 0
P93 TXD1	1	I/O Output	Port 93: I/O port (with pull-up resistor) Serial data send 1
P94 RXD1	1	I/O Input	Port 94: I/O port (with pull-up resistor) Serial data receive 1
P95 SCLK1	1	I/O I/O	Port 95: I/O port (with pull-up resistor) Serial clock I/O 1
PA0 to PA6	7	I/O	Ports A0 to A6: I/O ports
PA7 SCOUT	1	I/O Output	Port A7: I/O port System clock output: Outputs f_{FPH} or f_{SYS} clock.
$\overline{WDTOUT}$	1	Output	Watchdog timer output pin
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge or with both edges programmable.
CLK	1	Output	Clock output: Outputs [f_{SYS} ÷ 2] clock. Pulled-up during reset. Can be disabled to reduce noise.
$\overline{EA}$	1	Input	External access: On the TMP93CS41, the Vss pin should be connected. On the TMP93CS40, the Vcc pin should be connected.

Table 2.2.4 Pin Names and Functions (4/4)

Pin Names	Number of Pins	I/O	Functions
AM8/ $\overline{\text{AM16}}$	1	Input	Address mode: Selects external data bus width. (On the TMP93CS40) The Vcc pin should be connected. The data bus width for external access is set by the chip select/WAIT control register, port 1 control register. (On the TMP93CS41) The Vss pin should be connected to access either fixed 16-bit bus width, or 16-bit bus interchangeable with 8-bit bus. The Vcc pin should be connected to access a fixed 8-bit bus width.
ALE	1	Output	Address latch enable (Can be disabled to reduce noise.)
$\overline{\text{RESET}}$	1	Input	Reset: Initializes TMP93CS40/TMP93CS41. (with pull-up resistor)
X1/X2	2	I/O	High-frequency oscillator connecting pin
P96 XT1	1	I/O Input	Port 96: I/O port (open-drain output) Low-frequency oscillator connecting pin
P97 XT2	1	I/O Output	Port 97: I/O port (open drain output) Low-frequency oscillator connecting pin
TEST1/TEST2	2	Output/Input	TEST1 pin should be connected to TEST2 pin. Don't connect to any other pins.
VCC	3		Power supply pin (All VCC pins should be connected to the power supply pin.)
VSS	3		GND pin (0 V) (All VSS pins should be connected to GND (0 V).)
AVCC	1		Power supply pin for AD converter
AVSS	1		GND pin for AD converter (0 V)

Note: All pins that have built-in pull-up/pull-down resistors (other than the $\overline{\text{RESET}}$ pin) can be disconnected from the built-in pull-up/pull-down resistor by software.

3. Operation

This section describes in blocks the functions and basic operations of TMP93CS40 and TMP93CS41 devices. Please also refer to section 7. Precautions in use, which describes some points requiring careful attention.

3.1 CPU

TMP93CS40 and TMP93CS41 devices have a built-in high-performance 16-bit CPU (900/L CPU). (For basics of the CPU operation, see the information on the TLCS-900/L CPU in the previous chapter.)

This section describes some CPU functions unique to the TMP93CS40 and TMP93CS41, that are not described in the previous chapter, entitled TLCS-900/L CPU.

3.1.1 Reset

When resetting the TMP93CS40 and TMP93CS41 microcontroller, ensure that the power supply voltage is within the operating voltage range, and that the internal high-frequency oscillator has stabilized. Then set the $\overline{\text{RESET}}$ input to low level at least for 10 system clocks (16 μs at 20 MHz). Thus, when turn on the switch, be set to the power supply voltage is within the operating voltage range, and that the internal high-frequency oscillator has stabilized. Then hold the $\overline{\text{RESET}}$ input to low level at least for 10 system clocks.

Clock gear is initialized 1/16 mode by reset operation. It means that the system clock mode f_{SYS} is set to fc/32 (= fc/16 × 1/2).

When a reset signal is accepted, the CPU sets itself as follows:

- The program counter (PC) is set according to the reset vector that is stored from 8000H to 8002H.

  PC<7:0> ← Data in location 8000H

  PC<15:8> ← Data in location 8001H

  PC<23:16> ← Data in location 8002H
- The stack pointer (XSP) for system mode is set to 100H.
- The <IFF2:0> bits of the status register SR are set to 111. (Sets mask register to interrupt level 7.)
- The <MAX> bit of SR is set to 1. (Sets to maximum mode. See previous chapter.)
- The <RFP2:0> bits of SR are set to 000. (Clears register banks to 0.)

When the reset is released, instruction execution starts from PC (The reset vector). The reset makes no changes in any CPU internal registers other than those specifically mentioned above.

When a reset is received, signal and data processing for built-in I/Os, ports, and other pins is affected as follows:

- Initializes built-in I/O registers as per specifications.
- Sets port pins (including pins also used as built-in I/Os) to general-purpose input/output port mode.
- Sets the $\overline{\text{WDTOUT}}$ pin to 0. (The watchdog timer is set to enable after reset.)
- Pulls up the CLK pin to 1.
- Sets the ALE pin to 0 in the case of the TMP93CS41, and to high impedance (High-Z) in the case of TMP93CS40.

Note 1: Resetting makes no change in any register in the CPU except the program counter (PC), status register (SR) and stack pointer (XSP), nor in the data in the internal RAM.

Note 2: The CLK pin is pulled up during reset. When the voltage is externally reduced, there is a possibility of causing malfunctions.

Figure 3.1.1 and Figure 3.1.2 show the reset timing chart of the TMP93CS41 and TMP93CS40.

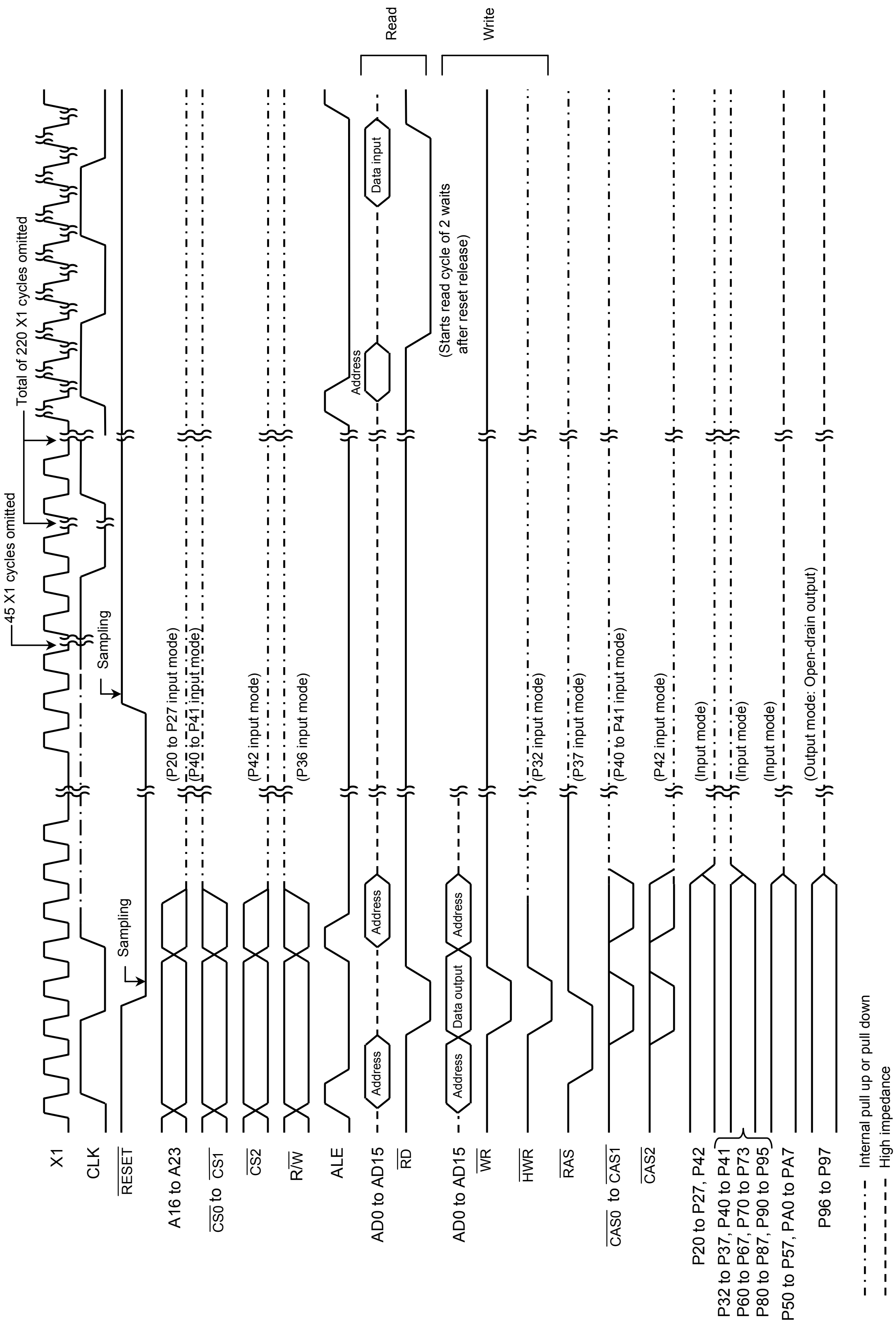


Figure 3.1.1 TMP93CS41 Reset Timing Chart

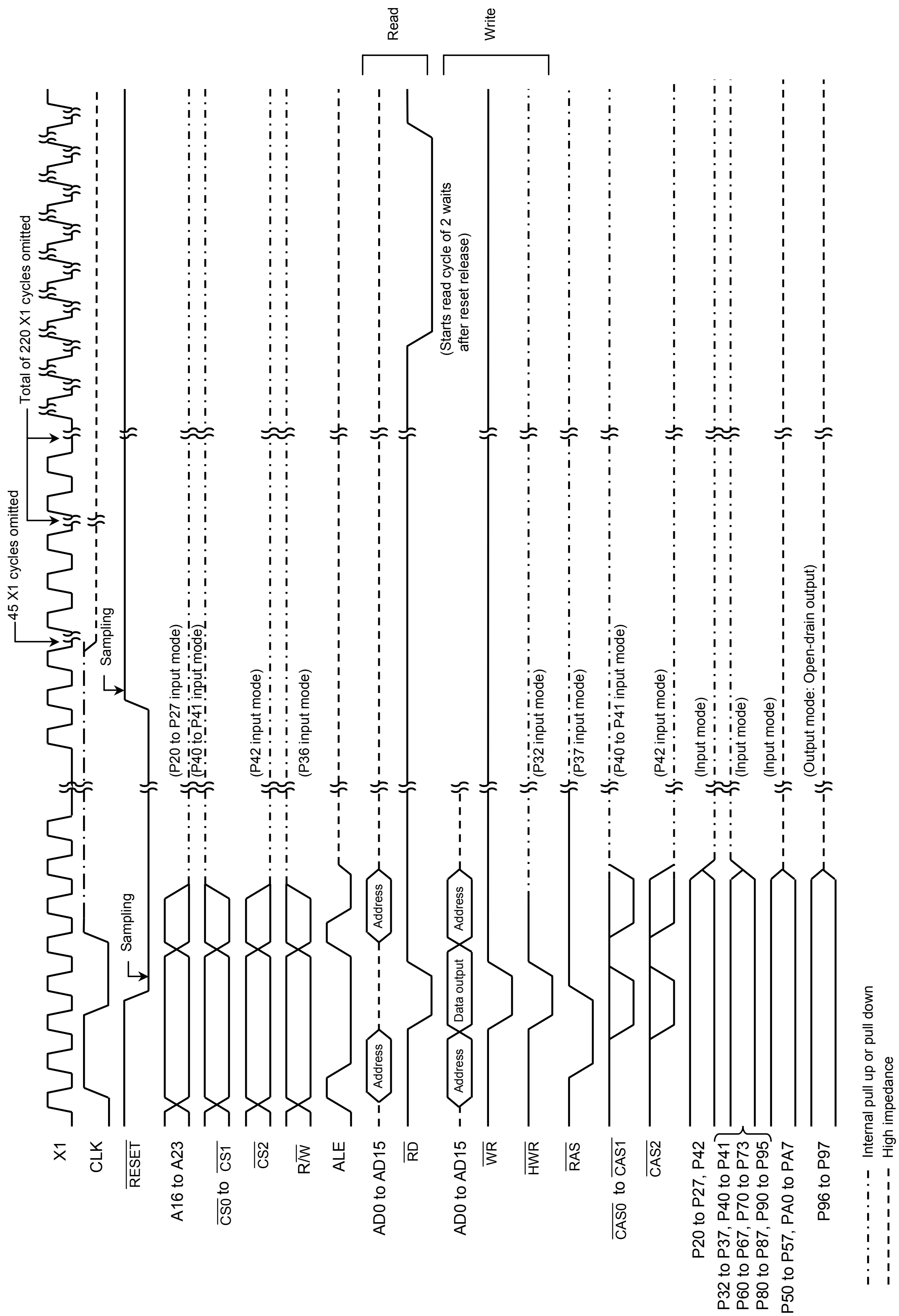


Figure 3.1.2 TMP93CS40 Reset Timing Chart

3.1.2 AM8/$\overline{\text{AM16}}$ Pin

(1) TMP93CS40

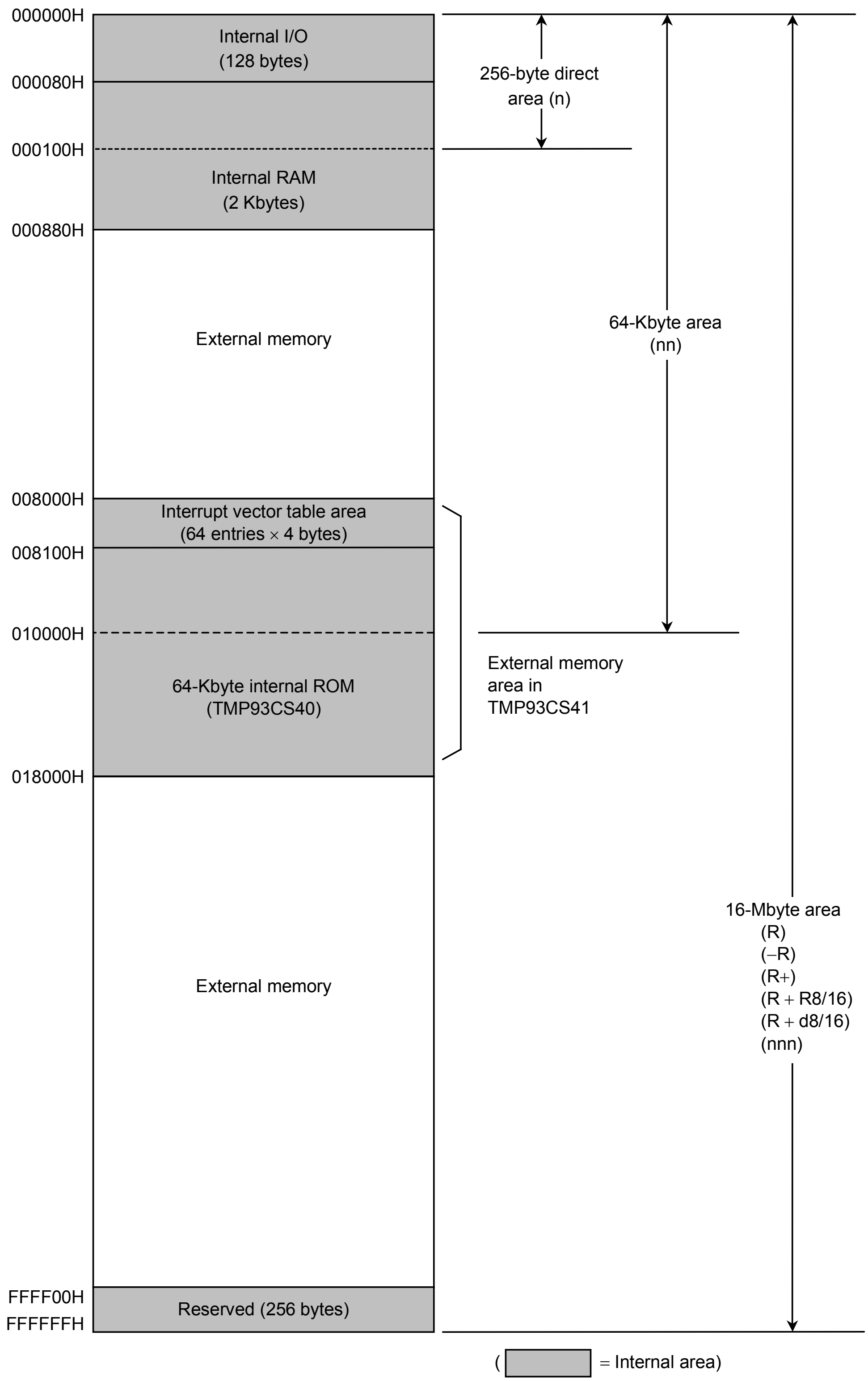
Set this pin to 1. Resetting accesses a built-in ROM via the internal 16-bit bus. When accessing externally, the bus width is set by the chip select/wait control register described in 3.6.3, and the registers of port 1.

(2) TMP93CS41

1. With fixed 16-bit data bus or with 16-bit data bus interchangeable with 8-bit data bus.
   Set this pin to 0. Port 1, AD8 to AD15 or A8 to A15 pins are fixed to AD8 to AD15 functions. Any values set in the port 1 control register or the port 1 function register are invalid.
   The external data bus width is set by the chip select/wait control register.
   After reset, it is necessary to set the program memory to be accessed, to 16-bit data bus.
2. With fixed external 8-bit data bus
   Set this pin to 1. Port 1, AD8 to AD15 or A8 to A15 pins are fixed to A8 to A15 functions. Any values set in the port 1 control register or the port 1 function register are invalid.
   The values of Bit4 <B0BUS>, <B1BUS> and <B2BUS> in the chip select/wait control register, which are described in 3.6.2, are invalid. The external 8-bit data bus is fixed.

3.2 Memory Map

Figure 3.2.1 is a memory map of the TMP93CS40 and TMP93CS41.



Note: The 256-byte area from FFFF00H to FFFFFFH can not be used.

Figure 3.2.1 Memory Map

4. Electrical Characteristics

"X" used in an expression shows a frequency for the clock f_{FPH} selected by SYSCR1<SYSCK>. The value of X changes according to whether a clock gear or a low speed oscillator is selected. An example value is calculated for fc, with gear = 1/fc (SYSCR1<SYSCK, GEAR2:0> = 0000).

4.1 Maximum Ratings

(TMP93CS40F, TMP93CS41F
TMP93CS40DF, TMP93CS41DF)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.5 to 6.5	V
Input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
Output current (Total)	ΣI_{OL}	120	mA
Output current (Total)	ΣI_{OH}	−80	mA
Power dissipation (Ta = 85°C)	P_D	600	mW
Soldering temperature (10 s)	T_{SOLDER}	260	°C
Storage temperature	T_{STG}	−65 to 150	°C
Operating temperature	T_{OPR}	−40 to 85	°C

Note: The maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2)

Ta = −40 to 85°C

<table>
<tr><th colspan="2">Parameter</th><th>Symbol</th><th colspan="2">Condition</th><th>Min</th><th>Typ. (Note)</th><th>Max</th><th>Unit</th></tr>
<tr><td colspan="2" rowspan="2">Power supply voltage
(AV_{CC} = V_{CC}
AV_{CC} = V_{SS} = 0 V)</td><td rowspan="2">V_{CC}</td><td>fc = 4 to 20 MHz</td><td rowspan="2">fs = 30 to 34 kHz</td><td>4.5</td><td rowspan="2"></td><td rowspan="2">5.5</td><td rowspan="2">V</td></tr>
<tr><td>fc = 4 to 12.5 MHz</td><td>2.7</td></tr>
<tr><td rowspan="7">Input low voltage</td><td rowspan="2">AD0 to AD15</td><td rowspan="2">V_{IL}</td><td colspan="2">V_{CC} ≥ 4.5 V</td><td rowspan="7">−0.3</td><td></td><td>0.8</td><td rowspan="13">V</td></tr>
<tr><td colspan="2">V_{CC} < 4.5 V</td><td></td><td>0.6</td></tr>
<tr><td>Port 2 to port A (except P87)</td><td>V_{IL1}</td><td colspan="2" rowspan="4">V_{CC} = 2.7 to 5.5 V</td><td></td><td>0.3 V_{CC}</td></tr>
<tr><td>$\overline{RESET}$, $\overline{NMI}$, INT0</td><td>V_{IL2}</td><td></td><td>0.25 V_{CC}</td></tr>
<tr><td>$\overline{EA}$, AM8/ $\overline{AM16}$</td><td>V_{IL3}</td><td></td><td>0.3</td></tr>
<tr><td>X1</td><td>V_{IL4}</td><td></td><td>0.2 V_{CC}</td></tr>
<tr><td rowspan="6">Input high voltage</td><td rowspan="2">AD0 to AD15</td><td rowspan="2">V_{IH}</td><td colspan="2">V_{CC} ≥ 4.5 V</td><td>2.2</td><td></td><td rowspan="6">V_{CC} + 0.3</td></tr>
<tr><td colspan="2">V_{CC} < 4.5 V</td><td>2.0</td><td></td></tr>
<tr><td>Port 2 to port A (except P87)</td><td>V_{IH1}</td><td colspan="2" rowspan="4">V_{CC} = 2.7 to 5.5 V</td><td>0.7 V_{CC}</td><td></td></tr>
<tr><td>$\overline{RESET}$, $\overline{NMI}$, INT0</td><td>V_{IH2}</td><td>0.75 V_{CC}</td><td></td></tr>
<tr><td>$\overline{EA}$, AM8/ $\overline{AM16}$</td><td>V_{IH3}</td><td>V_{CC} − 0.3</td><td></td></tr>
<tr><td>X1</td><td>V_{IH4}</td><td>0.8 V_{CC}</td><td></td></tr>
<tr><td colspan="2">Output low voltage</td><td>V_{OL}</td><td colspan="2">I_{OL} = 1.6 mA (V_{CC} = 2.7 to 5.5 V)</td><td></td><td></td><td>0.45</td><td rowspan="3">V</td></tr>
<tr><td colspan="2" rowspan="2">Output high voltage</td><td>V_{OH1}</td><td colspan="2">I_{OH} = −400 μA (V_{CC} = 3 V ± 10%)</td><td>2.4</td><td></td><td></td></tr>
<tr><td>V_{OH2}</td><td colspan="2">I_{OH} = −400 μA (V_{CC} = 5 V ± 10%)</td><td>4.2</td><td></td><td></td></tr>
</table>

Note: Typical values are for Ta = 25°C and V_{CC} = 5 V unless otherwise noted.

4.2 DC Characteristics (2/2)

Parameter	Symbol	Condition	Min	Typ. (Note 1)	Max	Unit
Darlington drive current (8 output pins max)	I_{DAR} (Note 2)	$V_{EXT} = 1.5$ V $R_{EXT} = 1.1$ kΩ (when $V_{CC} = 5$ V ± 10%)	−1.0		−3.5	mA
Input leakage current	I_{LI}	$0.0 \le V_{IN} \le V_{CC}$		0.02	±5	μA
Output leakage current	I_{LO}	$0.2 \le V_{IN} \le V_{CC} - 0.2$		0.05	±10	μA
Powerdown voltage (at stop, RAM backup)	V_{STOP}	$V_{IL2} = 0.2\ V_{CC}$, $V_{IH2} = 0.8\ V_{CC}$	2.0		6.0	V
$\overline{RESET}$ pull-up resistor	R_{RST}	$V_{CC} = 5$ V ± 10%	50		150	kΩ
		$V_{CC} = 3$ V ± 10%	80		200	
Pin capacitance	C_{IO}	fc = 1 MHz			10	pF
Schmitt width $\overline{RESET}$, $\overline{NMI}$, INT0	V_{TH}		0.4	1.0		V
Programmable pull-down resistor	R_{KL}	$V_{CC} = 5$ V ± 10%	10		80	kΩ
		$V_{CC} = 3$ V ± 10%	30		150	
Programmable pull-up resistor	R_{KH}	$V_{CC} = 5$ V ± 10%	50		150	
		$V_{CC} = 3$ V ± 10%	100		300	
NORMAL (Note 3)	I_{CC}	$V_{CC} = 5$ V ± 10% fc = 20 MHz		19	25	mA
NORMAL2 (Note 4)				24	30	
RUN				17	25	
IDLE2				10	15	
IDLE1				3.5	5	
NORMAL (Note 3)		$V_{CC} = 3$ V ± 10% fc = 12.5 MHz (Typ: $V_{CC} = 3.0$ V)		6.5	10	mA
NORMAL2 (Note 4)				9.5	13	
RUN				5.0	9	
IDLE2				3.0	5	
IDLE1				0.8	1.5	
SLOW (Note 3)		$V_{CC} = 3$ V ± 10% fs = 32.768 kHz (Typ: Vcc = 3.0 V)		20	35	μA
RUN				16	30	
IDLE2				10	20	
IDLE1				5	15	
STOP		$V_{CC} = 2.7$ to 5.5 V		0.2	10	μA

Note 1: Typical values are for Ta = 25°C and $V_{CC} = 5$ V unless otherwise noted.

Note 2: I_{DAR} is guaranteed for up to eight ports.

Note 3: I_{CC} measurement conditions (NORMAL, SLOW):
Only CPU is operational; output pins are open and input pins are fixed.

Note 4: I_{CC} measurement conditions (NORMAL2):
All functions are operational; output pins are open and input pins are fixed.

4.3 AC Characteristics

(1) V_{CC} = 5 V ± 10%

No.	Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Osc. period (= X)	t_{OSC}	50	31250	62.5		50		ns
2	CLK pulse width	t_{CLK}	2x – 40		85		60		ns
3	A0 to A23 valid → CLK hold	t_{AK}	0.5x – 20		11		5		ns
4	CLK valid → A0 to A23 hold	t_{KA}	1.5x – 70		24		5		ns
5	A0 to A15 valid → ALE fall	t_{AL}	0.5x – 15		16		10		ns
6	ALE fall → A0 to A15 hold	t_{LA}	0.5x – 20		11		5		ns
7	ALE high pulse width	t_{LL}	x – 40		23		10		ns
8	ALE fall → $\overline{RD}$ / $\overline{WR}$ fall	t_{LC}	0.5x – 25		6		0		ns
9	$\overline{RD}$ / $\overline{WR}$ rise → ALE rise	t_{CL}	0.5x – 20		11		5		ns
10	A0 to A15 valid → $\overline{RD}$ / $\overline{WR}$ fall	t_{ACL}	x – 25		38		25		ns
11	A0 to A23 valid → $\overline{RD}$ / $\overline{WR}$ fall	t_{ACH}	1.5x – 50		44		25		ns
12	$\overline{RD}$ / $\overline{WR}$ rise → A0 to A23 hold	t_{CA}	0.5x – 25		6		0		ns
13	A0 to A15 valid → D0 to D15 input	t_{ADL}		3.0x – 55		133		95	ns
14	A0 to A23 valid → D0 to D15 input	t_{ADH}		3.5x – 65		154		110	ns
15	$\overline{RD}$ fall → D0 to D15 input	t_{RD}		2.0x – 60		65		40	ns
16	$\overline{RD}$ low pulse width	t_{RR}	2.0x – 40		85		60		ns
17	$\overline{RD}$ rise → D0 to D15 hold	t_{HR}	0		0		0		ns
18	$\overline{RD}$ rise → A0 to A15 output	t_{RAE}	x – 15		48		35		ns
19	$\overline{WR}$ low pulse width	t_{WW}	2.0x – 40		85		60		ns
20	D0 to D15 valid → $\overline{WR}$ rise	t_{DW}	2.0x – 55		70		45		ns
21	$\overline{WR}$ rise → D0 to D15 hold	t_{WD}	0.5x – 15		16		10		ns
22	A0 to A23 valid → $\overline{WAIT}$ input (1 + N) WAIT mode	t_{AWH}		3.5x – 90		129		85	ns
23	A0 to A15 valid → $\overline{WAIT}$ input (1 + N) WAIT mode	t_{AWL}		3.0x – 80		108		70	ns
24	$\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ hold (1 + N) WAIT mode	t_{CW}	2.0x + 0		125		100		ns
25	A0 to A23 valid → Port input	t_{APH}		2.5x – 120		36		5	ns
26	A0 to A23 valid → Port hold	t_{APH2}	2.5x + 50		206		175		ns
27	$\overline{WR}$ rise → Port valid	t_{CP}		200		200		200	ns
28	A0 to A23 valid → $\overline{RAS}$ fall	t_{ASRH}	1.0x – 40		23		10		ns
29	A0 to A15 valid → $\overline{RAS}$ fall	t_{ASRL}	0.5x – 15		16		10		ns
30	$\overline{RAS}$ fall → D0 to D15 input	t_{RAC}		2.5x – 70		86		55	ns
31	$\overline{RAS}$ fall → A0 to A15 hold	t_{RAH}	0.5x – 15		16		10		ns
32	$\overline{RAS}$ low pulse width	t_{RAS}	2.0x – 40		85		60		ns
33	$\overline{RAS}$ high pulse width	t_{RP}	2.0x – 40		85		60		ns
34	$\overline{CAS}$ fall → $\overline{RAS}$ rise	t_{RSH}	1.0x – 40		23		10		ns
35	$\overline{RAS}$ rise → $\overline{CAS}$ rise	t_{RSC}	0.5x – 25		6		0		ns
36	$\overline{RAS}$ fall → $\overline{CAS}$ fall	t_{RCD}	1.0x – 40		23		10		ns
37	$\overline{CAS}$ fall → D0 to D15 input	t_{CAC}		1.5x – 65		29		10	ns
38	$\overline{CAS}$ low pulse width	t_{CAS}	1.5x – 30		64		40		ns

AC measuring conditions

- Output level: High 2.2 V/Low 0.8 V, C_L = 50 pF
  (However, C_L = 100 pF for AD0 to AD15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, CLK, $\overline{RAS}$, $\overline{CAS0}$ to $\overline{CAS2}$)
- Input level: High 2.4 V/Low 0.45 V (AD0 to AD15)
  High 0.8 × V_{CC}/Low 0.2 × V_{CC} (except for AD0 to AD15)

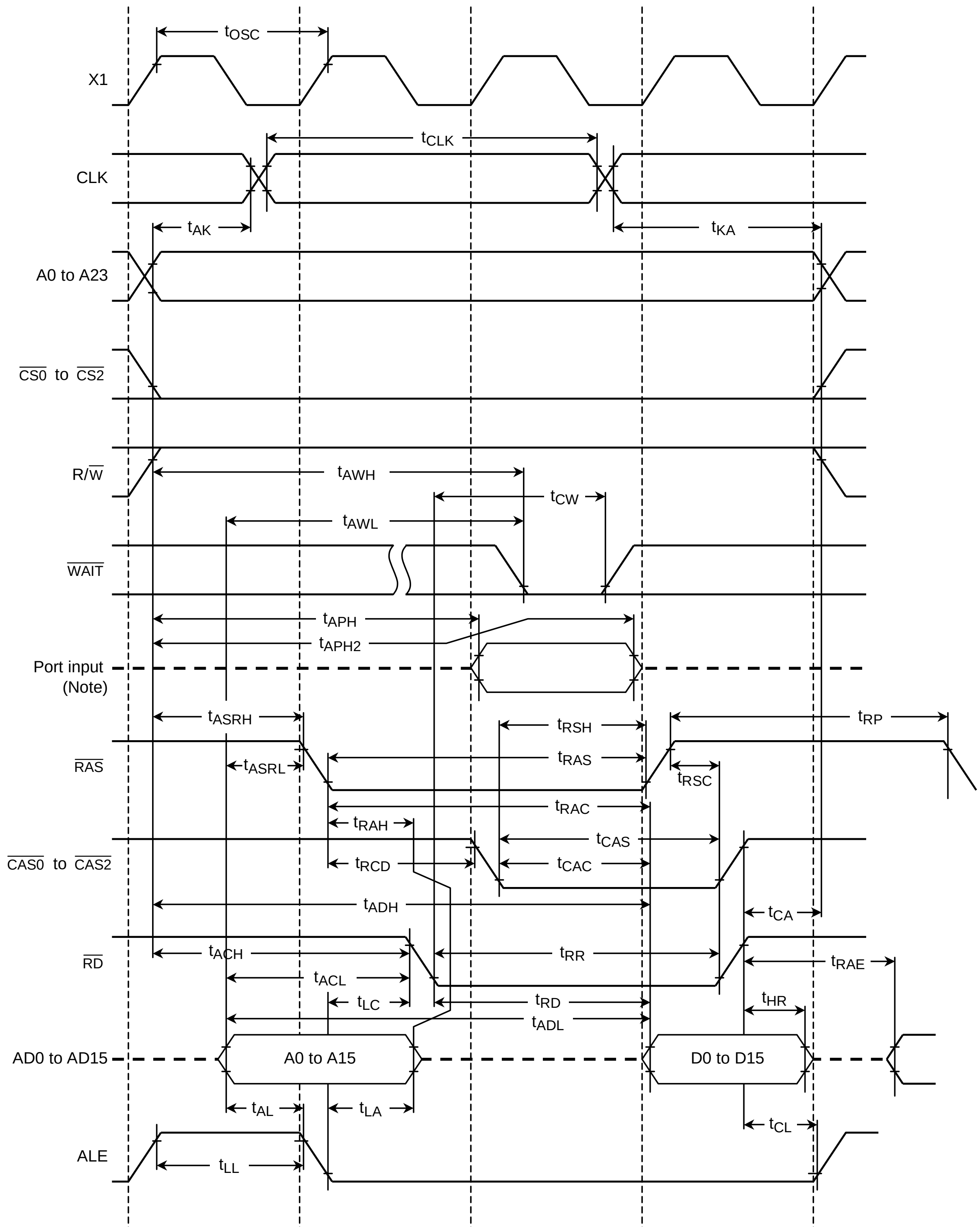
(2) V_{CC} = 3 V ± 10%

No.	Parameter		Symbol	Variable		12.5 MHz		Unit
				Min	Max	Min	Max	
1	Osc. period (= X)		t_{OSC}	80	31250	80		ns
2	CLK pulse width		t_{CLK}	2x – 40		120		ns
3	A0 to A23 valid → CLK hold		t_{AK}	0.5x – 30		10		ns
4	CLK valid → A0 to A23 hold		t_{KA}	1.5x – 80		40		ns
5	A0 to A15 valid → ALE fall		t_{AL}	0.5x – 35		5		ns
6	ALE fall → A0 to A15 hold		t_{LA}	0.5x – 35		5		ns
7	ALE high pulse width		t_{LL}	x – 60		20		ns
8	ALE fall → $\overline{RD}$ / $\overline{WR}$ fall		t_{LC}	0.5x – 35		5		ns
9	$\overline{RD}$ / $\overline{WR}$ rise → ALE rise		t_{CL}	0.5x – 40		0		ns
10	A0 to A15 valid → $\overline{RD}$ / $\overline{WR}$ fall		t_{ACL}	x – 50		30		ns
11	A0 to A23 valid → $\overline{RD}$ / $\overline{WR}$ fall		t_{ACH}	1.5x – 50		70		ns
12	$\overline{RD}$ / $\overline{WR}$ rise → A0 to A23 hold		t_{CA}	0.5x – 40		0		ns
13	A0 to A15 valid → D0 to D15 input		t_{ADL}		3.0x – 110		130	ns
14	A0 to A23 valid → D0 to D15 input		t_{ADH}		3.5x – 125		155	ns
15	$\overline{RD}$ fall → D0 to D15 input		t_{RD}		2.0x – 115		45	ns
16	$\overline{RD}$ low pulse width		t_{RR}	2.0x – 40		120		ns
17	$\overline{RD}$ rise → D0 to D15 hold		t_{HR}	0		0		ns
18	$\overline{RD}$ rise → A0 to A15 output		t_{RAE}	x – 25		55		ns
19	$\overline{WR}$ low pulse width		t_{WW}	2.0x – 40		120		ns
20	D0 to D15 valid → $\overline{WR}$ rise		t_{DW}	2.0x – 120		40		ns
21	$\overline{WR}$ rise → D0 to D15 hold		t_{WD}	0.5x – 40		0		ns
22	A0 to A23 valid → $\overline{WAIT}$ input	(1 + N) WAIT mode	t_{AWH}		3.5x – 130		150	ns
23	A0 to A15 valid → $\overline{WAIT}$ input	(1 + N) WAIT mode	t_{AWL}		3.0x – 100		140	ns
24	$\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ hold	(1 + N) WAIT mode	t_{CW}	2.0x + 0		160		ns
25	A0 to A23 valid → Port input		t_{APH}		2.5x – 195		5	ns
26	A0 to A23 valid → Port hold		t_{APH2}	2.5x + 50		250		ns
27	$\overline{WR}$ rise → Port valid		t_{CP}		200		200	ns
28	A0 to A23 valid → $\overline{RAS}$ fall		t_{ASRH}	1.0x – 60		20		ns
29	A0 to A15 valid → $\overline{RAS}$ fall		t_{ASRL}	0.5x – 40		0		ns
30	$\overline{RAS}$ fall → D0 to D15 input		t_{RAC}		2.5x – 90		110	ns
31	$\overline{RAS}$ fall → A0 to A15 hold		t_{RAH}	0.5x – 25		15		ns
32	$\overline{RAS}$ low pulse width		t_{RAS}	2.0x – 40		120		ns
33	$\overline{RAS}$ high pulse width		t_{RP}	2.0x – 40		120		ns
34	$\overline{CAS}$ fall → $\overline{RAS}$ rise		t_{RSH}	1.0x – 55		25		ns
35	$\overline{RAS}$ rise → $\overline{CAS}$ rise		t_{RSC}	0.5x – 25		15		ns
36	$\overline{RAS}$ fall → $\overline{CAS}$ fall		t_{RCD}	1.0x – 40		40		ns
37	$\overline{CAS}$ fall → D0 to D15 input		t_{CAC}		1.5x – 120		0	ns
38	$\overline{CAS}$ low pulse width		t_{CAS}	1.5x – 40		80		ns

AC measuring conditions

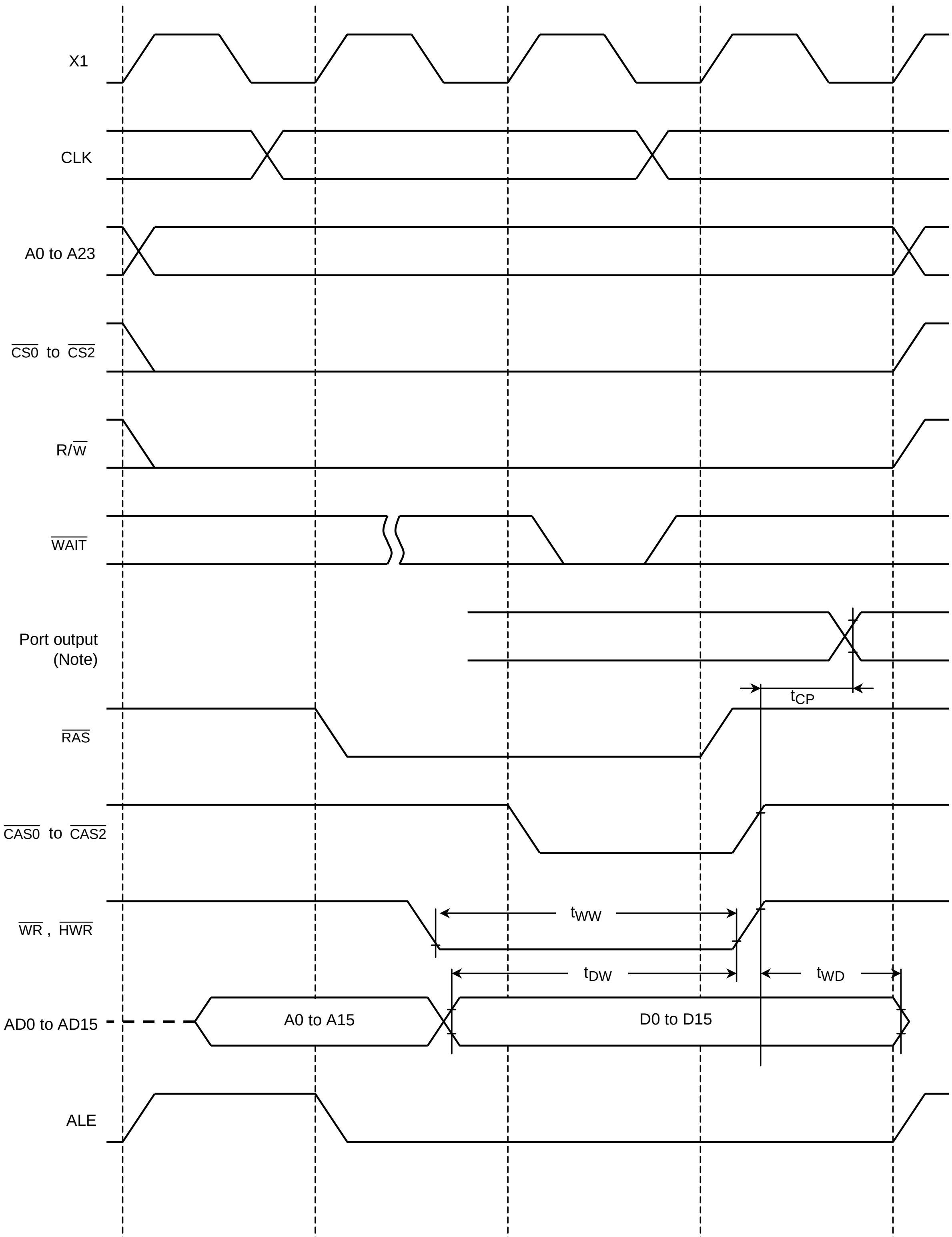
- Output level: High 0.7 × V_{CC}/Low 0.3 × V_{CC}, C_L = 50 pF
- Input level: High 0.9 × V_{CC}/Low 0.1 × V_{CC}

(1) Read cycle



Note: Since the CPU accesses the internal area to read data from a port, the control signals of external pins such as RD and CS are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

(2) Write cycle



Note: Since the CPU accesses the internal area to write data to a port, the control signals of external pins such as $\overline{WR}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

4.4 AD Conversion Characteristics

$AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$

Parameter	Symbol	Power Supply	Min	Typ	Max	Unit
Analog reference voltage (+)	V_{REFH}	$V_{CC} = 5\ V \pm 10\%$	$V_{CC} - 1.5\ V$	V_{CC}	V_{CC}	V
		$V_{CC} = 3\ V \pm 10\%$	$V_{CC} - 0.2\ V$	V_{CC}	V_{CC}	
Analog reference voltage (−)	V_{REFL}	$V_{CC} = 5\ V \pm 10\%$	V_{SS}	V_{SS}	$V_{SS} + 0.2\ V$	
		$V_{CC} = 3\ V \pm 10\%$	V_{SS}	V_{SS}	$V_{SS} + 0.2\ V$	
Analog input voltage range	V_{AIN}		V_{REFL}		V_{REFH}	
Analog current for analog reference voltage <VREFON> = 1	I_{REF} ($V_{REFL} = 0\ V$)	$V_{CC} = 5\ V \pm 10\%$		0.5	1.5	mA
		$V_{CC} = 3\ V \pm 10\%$		0.3	0.9	
<VREFON> = 0		$V_{CC} = 2.7$ to $5.5\ V$		0.02	5.0	μA
Error (not including quantizing errors)	−	$V_{CC} = 5\ V \pm 10\%$		±1.0	±3.0	LSB
		$V_{CC} = 3\ V \pm 10\%$		±1.0	±3.0	

Note 1: $1LSB = (V_{REFH} - V_{REFL})/2^{10}$ [V]

Note 2: The operation of this AD converter is guaranteed only using fc (The high-frequency oscillator). It is not guaranteed for fs.
The operation above is guaranteed for $f_{FPH} \geq 4$ MHz.

Note 3: The value I_{CC} includes the current which flows through the AVCC pin.

4.5 Serial Channel Timing

(1) I/O interface mode

1. SCLK input mode

Parameter	Symbol	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
SCLK cycle	t_{SCY}	16X		488		1.28		0.8		μs
Output data → Rising edge or falling edge* of SCLK	t_{OSS}	$t_{SCY}/2 - 5X - 50$		91.5 μs		190		100		ns
SCLK rising edge or falling edge* → Output data hold	t_{OHS}	$5X - 100$		152 μs		300		150		ns
SCLK rising edge or falling edge* → Input data hold	t_{HSR}	0		0		0		0		ns
SCLK rising edge or falling edge* → Effective data input	t_{SRD}		$t_{SCY} - 5X - 100$		336 μs		780		450	ns

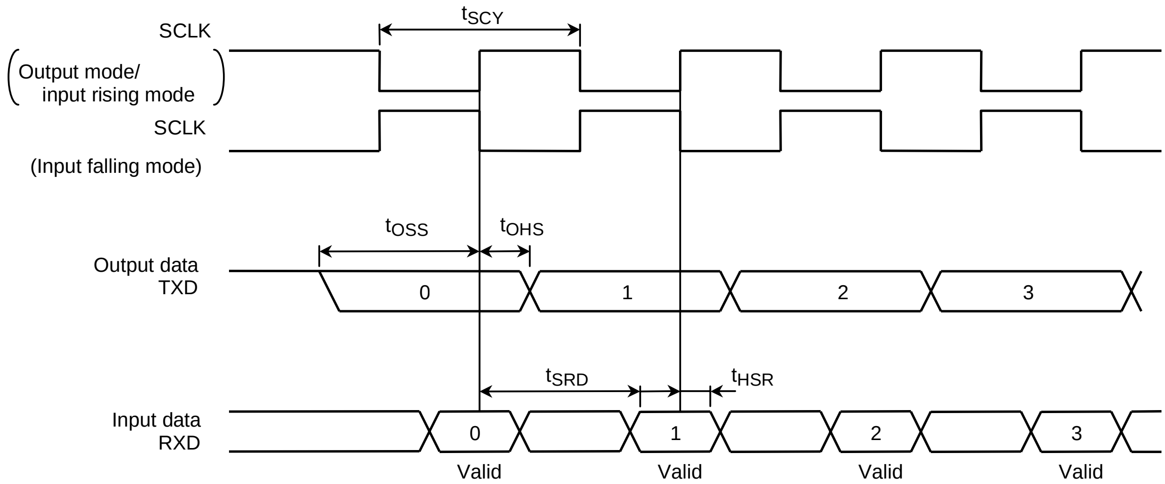
Note: System clock is fs, or input clock to prescaler is divisor clock of fs.

* The rising edge is used in SCLK rising mode.
The falling edge is used SCLK falling mode.

2. SCLK output mode

Parameter	Symbol	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
SCLK cycle (Programmable)	t_{SCY}	16X	8192X	488	250 ms	1.28	655.36	0.8	409.6	μs
Output data → SCLK rising edge	t_{OSS}	$t_{SCY} - 2X - 150$		427 μs		970		550		ns
SCLK rising edge → Output data hold	t_{OHS}	$2X - 80$		60 μs		80		20		ns
SCLK rising edge → Input data hold	t_{HSR}	0		0		0		0		ns
SCLK rising edge → Effective data input	t_{SRD}		$t_{SCY} - 2X - 150$		428 μs		970		550	ns

Note: System clock is fs, or input clock to prescaler is divisor clock of fs.



4.6 Timer/Counter Input Clock (TI0, TI4, TI5, TI6 and TI7)

Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock cycle	t_{VCK}	8X + 100		740		500		ns
Low level clock pulse width	t_{VCKL}	4X + 40		360		240		ns
High level clock pulse width	t_{VCKH}	4X + 40		360		240		ns

4.7 Interrupt and Capture

(1) $\overline{\text{NMI}}$ and INT0 interrupts

Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{\text{NMI}}$, INT0 low level pulse width	t_{INTAL}	4X		320		200		ns
$\overline{\text{NMI}}$, INT0 high level pulse width	t_{INTAH}	4X		320		200		ns

(2) INT4 to INT7 interrupts, capture

The INT4 to INT7 input pulse width depends on the CPU operation clock and timer (9-bit prescaler). The following shows the pulse width for each clock.

System Clock Selected <SYSCK>	Prescaler Clock Selected <PRCK1:0>	t_{INTBL} (INT4 to INT7 low level pulse width)		t_{INTBH} (INT4 to INT7 high level pulse width)		Unit
		Variable	20 MHz	Variable	20 MHz	
		Min	Min	Min	Min	
0 (fc)	00 (f_{FPH})	8X + 100	500	8X + 100	500	ns
	01 (fs)	8XT + 0.1	244.3	8XT + 0.1	244.3	μs
	10 (fc/16)	128x + 0.1	6.5	128X + 0.1	6.5	
1 (fs) (Note 2)	00 (f_{FPH})	8XT + 0.1	244.3	8XT + 0.1	244.3	
	01 (fs)					

Note 1: XT represents the frequency of the low-frequency clock fs. Calculated at fs = 32.768 kHz.

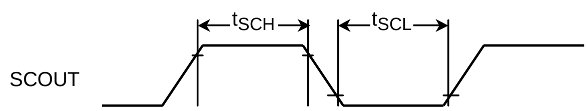
Note 2: When using fs as the system clock, fc/16 cannot be selected as the prescaler clock.

4.8 SCOUT Pin AC Characteristics

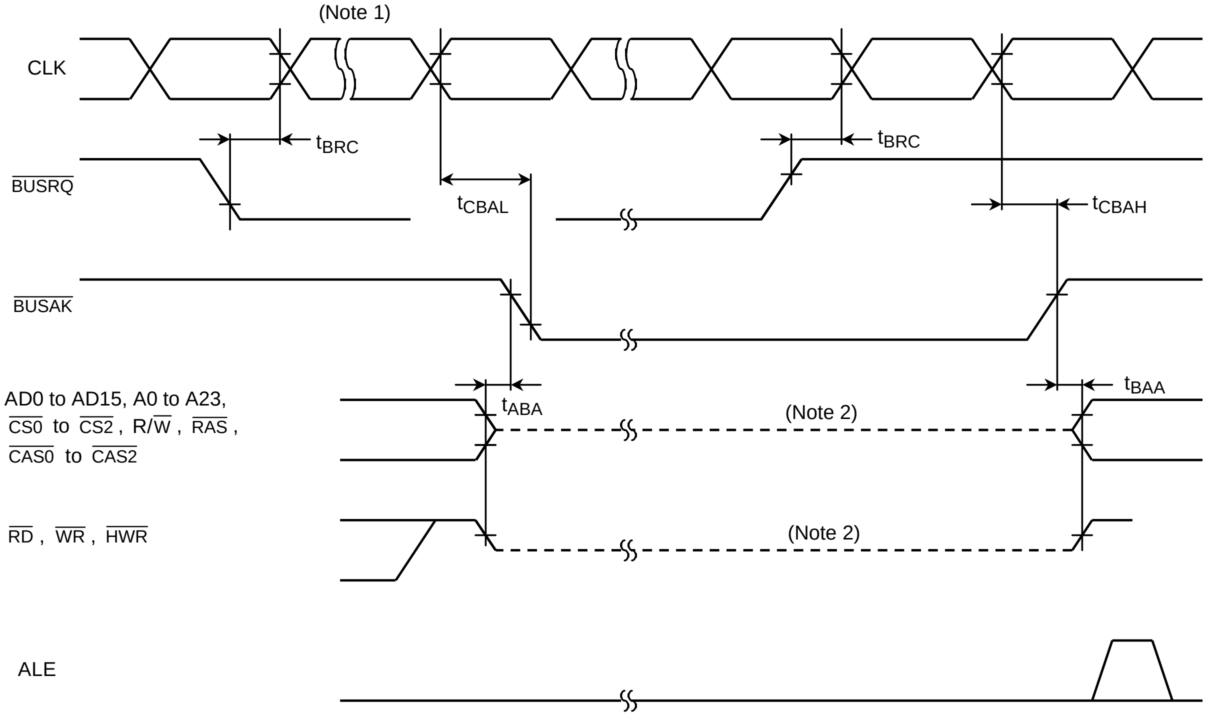
Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
High-level pulse width V_{CC} = 5 V ± 10%	t_{SCH}	0.5X − 10		40		15		ns
High-level pulse width V_{CC} = 3 V ± 10%		0.5X − 20		30		–	–	
Low-level pulse width V_{CC} = 5 V ± 10%	t_{SCL}	0.5X − 10		40		15		ns
Low-level pulse width V_{CC} = 3 V ± 10%		0.5X − 20		30		–	–	

Measurement condition

- Output level: High 2.2 V/Low 0.8 V, C_L = 10 pF



4.9 Timing Chart for Bus Request ($\overline{\text{BUSRQ}}$)/Bus Acknowledge ($\overline{\text{BUSAK}}$)



Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{\text{BUSRQ}}$ setup time to CLK	t_{BRC}	120		120		120		ns
CLK→$\overline{\text{BUSAK}}$ falling edge	t_{CBAL}		1.5X + 120		240		195	ns
CLK→$\overline{\text{BUSAK}}$ rising edge	t_{CBAH}		0.5x + 40		80		65	ns
Output buffer off to $\overline{\text{BUSAK}}$ ↘	t_{ABA}	0	80	0	80	0	80	ns
$\overline{\text{BUSAK}}$ ↗ to output buffer on	t_{BAA}	0	80	0	80	0	80	ns

Note 1: Even if the $\overline{\text{BUSRQ}}$ signal goes low, the bus will not be released while the $\overline{\text{WAIT}}$ signal is low. The bus will only be released when $\overline{\text{BUSRQ}}$ goes low while $\overline{\text{WAIT}}$ is high.

Note 2: This line shows only that the output buffer is in the off state.
It does not indicate that the signal level is fixed.
Just after the bus is released, the signal level set before the bus was released is maintained dynamically by the external capacitance. Therefore, to fix the signal level using an external resistor during bus release, careful design is necessary, as fixing of the level is delayed.
The internal programmable pull-up/pull-down resistor is switched between the active and non-active states by the internal signal.

4.10 Recommended Oscillator

The TMP93CS40/S41 are evaluated with various resonators. The evaluation results are displayed below to enable appropriate selection for any given application.

Note: The load capacitance of the resonator consists of the load capacitors C1 and C2 which are to be connected and the floating capacitance of the target board.
Even if the specified values of C1 and C2 are used, there is a possibility that the oscillator will malfunction due to varying load capacitance on the target boards. Hence the oscillator's wiring patterns on the board should be designed to be as short as possible.
It is recommended that evaluation of the resonators be conducted on the target board.

(1) Examples of resonator connection

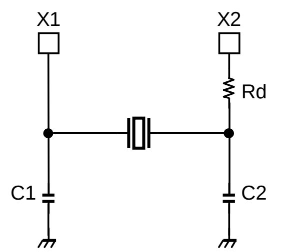


Figure1: Example of High-frequency Resonator Connection

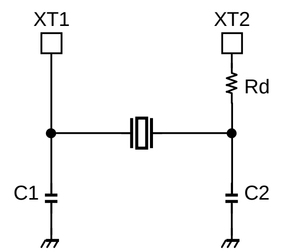


Figure2: Example of Low-frequency Resonator Connection

(2) Ceramic resonator: Murata Manufacturing. Co., Ltd (Note 1)

Ta = −20 to 80°C

Parameter	Frequency (MHz)	Recommended Resonator	Recommended Value			V_{CC} [V]
			C1 [pF]	C2 [pF]	Rd [kΩ]	
High-frequency oscillation	4.00	CSA4.00MG	30	30	0	2.7 to 5.5
		CST4.00MGW	(30) (Note 2)	(30) (Note 2)		
	10.00	CSA10.0MTZ093	30	30		
		CST10.0MTW093	(30) (Note 2)	(30) (Note 2)		
	12.50	CSA12.5MTZ093	30	30		
		CST12.5MTW093	(30) (Note 2)	(30) (Note 2)		
	16.00	CSA16.00MXZ040	5	5		4.5 to 5.5
		CST16.00MXW0C1	(5) (Note 2)	(5) (Note 2)		
	20.00	CSA20.00MXZ040	3	3		

Note 1: Murata Manufacturing. Co., Ltd. (Japan)
The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change.
For up-to-date information, please refer to the following URL:
http://www.murata.com/

Note 2: For built-in condenser type

(3) Crystal resonator: Nihon Denpa Kogyo (Note 1)

Ta = −10 to 60°C

Parameter	Frequency (MHz)	Recommended Resonator	Recommended Value			Vcc [V]
			C1 [pF]	C2 [pF]	Rd [kΩ]	
High-frequency oscillation	4.00	NT040016A	12	12	0	2.7 to 5.5
	10.00	NT100016A	10	10		
	12.50	NT125016A	10	10		
	16.00	NT160016A	10	10		4.5 to 5.5
	20.00	NT200016A	7	7		

Note 1:

NDK AMERICA, INC.: U.S.A	Phone: +1-510-623-6512,	Fax: +1-510-623-6590
NDK ELECTRONICS SINGAPORE PTE, LTD.	Phone: +65-6298-9878,	Fax: +65-6293-1150
NDK ELECTRONICS (HK) LIMITED: HONG KONG	Phone: +852-2956-3181,	Fax: +852-2956-1567
NDK EUROPE LIMITED: ENGLAND	Phone: +44-20-8390-8344,	Fax: +44-20-8390-6926
NDK FRANCE SARL: FRANCE	Phone: +33-1-60-95-0000,	Fax: +33-1-60-95-8200
NDK ITALY SRL: ITALY	Phone: +39-02-96702920,	Fax: +39-02-96703284

Note 2: High-frequency resonator

NR-18:	Lead mount type
AT-51:	Lead mount type
CP12A:	Surface mount type