Low Voltage / Low Power CMOS 16-bit MICROCONTROLLERS

# TMP93CU44DF

## 1. OUTLINE AND DEVICE CHARACTERISTICS

The TMP93CU44 are high-speed, advanced 16-bit microcontrollers developed for controlling medium to large-scale equipment.
The TMP93CU44DF are housed in 80-pin flat package (QFP80-P-1420-0.80B).
The device characteristics are as follows:

(1) Original 16-bit CPU (900 / L CPU)

- TLCS-90 instruction mnemonic upward compatible
- 16M-byte linear address space
- General-purpose registers and register bank system
- 16-bit multiplication / division and bit transfer / arithmetic instructions
- Micro DMA : 4 channels (1.6 $\mu$s per 2 bytes at 20 MHz)

(2) Minimum instruction execution time : 200 ns at 20 MHz

(3) Internal RAM : 3K bytes

Internal ROM : 96K bytes

(4) External memory expansion

- Can be expanded up to16M-bytes (for both programs and data).
- AM8 / $\overline{16}$ pin (select the external data bus width)
- Can mix 8- and 16-bit external data buses. (Dynamic bus sizing)

(5) 8-bit timer : 4 channels

(6) 16-bit timer : 2 channel

(7) Serial interface : 2 channels

(8) I2C bus channel : 1 channel

(9) 10-bit A/D converter : 8 channels

(10) High current output : 8 ports

(11) Watchdog timer

(12) Bus width / wait controller : 3 blocks

(13) Interrupt functions : 33

- 9 CPU interrupts
- 17 internal interrupts
- 7 external interrupts

] 7-level priority can be set.

(14) I/O ports : 62 pins

(15) Standby function : 4 halt modes (RUN, IDLE2, IDLE1, STOP)

(16) Clock gear function

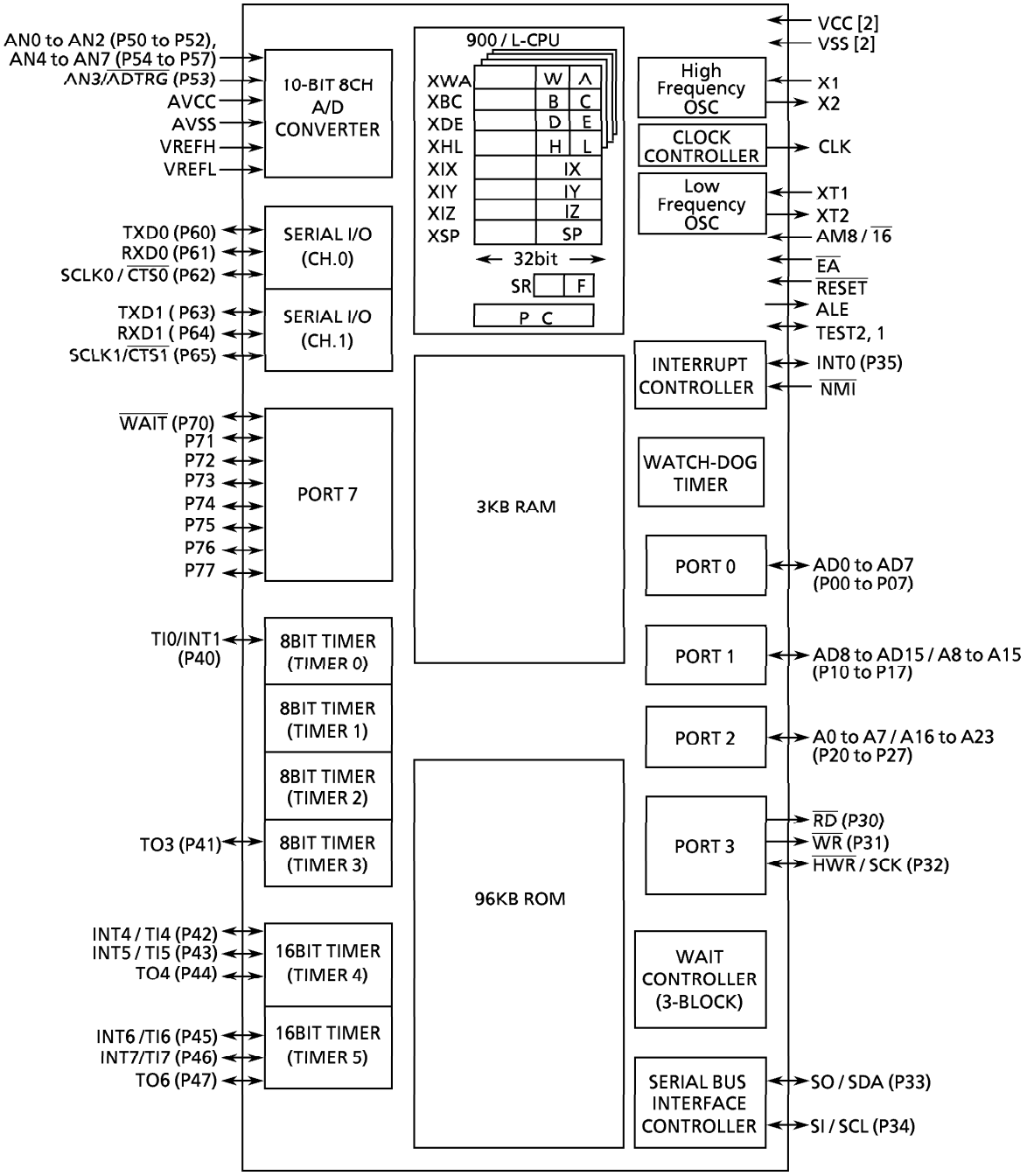
- High-frequency clock can be changed from fc to fc / 16.
- Dual clock Operation

(17) Wide Range of Operating Voltage

- Vcc = 2.7 to 5.5 V

(18) Package

- QFP80-P-1420-0.80B




Note) The items in parentheses ( ) are the initial setting after reset.

Figure 1 TMP93CU44 Block Diagram

## 2. PIN ASSIGNMENT AND FUNCTIONS

The assignment of input and output pins for the TMP93CU44, their names and functions are described below.

### 2.1 Pin Assignment

Figure 2.1 shows pin assignment of the TMP93CU44DF.

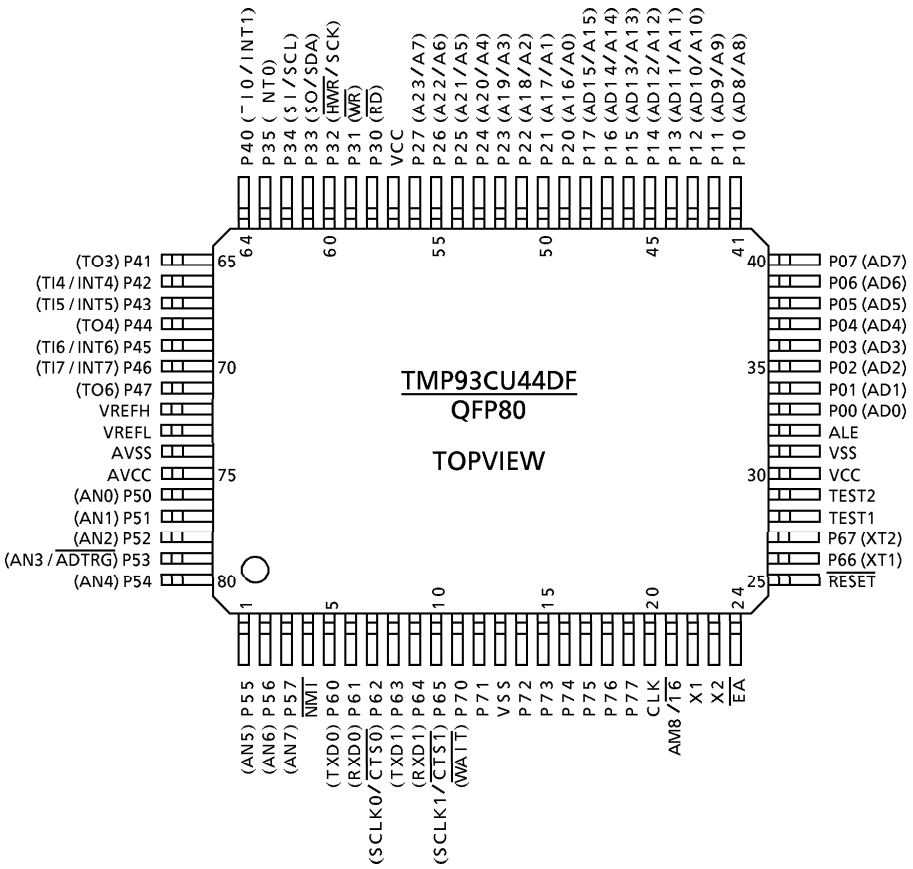



Figure 2.1 Pin Assignment (QFP80-P-1420-0.80B)

## 2.2 Pin Names and Functions

The names of input / output pins and their functions are described below.
Table 2.2 Pin Names and Functions.

Table 2.2 Pin Names and Function (1/3)

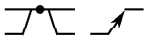
| Pin name | Number of pins | I/O | Functions |
|---|---|---|---|
| P00 to P07 / AD0 to AD7 | 8 | I/O | Port 0: I/O port that allows selection of I/O on a bit basis |
| | | 3-state | Address/data (lower): Bits 0 to 7 for address/data bus |
| P10 to P17 / AD8 to AD15 / A8 to A15 | 8 | I/O | Port 1: I/O port that allows selection of I/O on a bit basis |
| | | 3-state | Address data (upper): Bits 8 to 15 for address/data bus |
| | | Output | Address: Bits 8 to 15 for address bus |
| P20 to P27 / A0 to A7 / A16 to A23 | 8 | I/O | Port 2: I/O port that allows selection of I/O on a bit basis (with pull-up resistor) |
| | | Output | Address: Bits 0 to 7 for address bus |
| | | Output | Address: Bits 16 to 23 for address bus |
| P30 / $\overline{RD}$ | 1 | Output | Port 30: Output port |
| | | Output | Read: Strobe signal for reading external memory |
| P31 / $\overline{WR}$ | 1 | Output | Port 31: Output port |
| | | Output | Write: Strobe signal for writing data on pins AD0 to 7 |
| P32 / $\overline{HWR}$ / SCK | 1 | I/O | Port 32: I/O port (with pull-up resistor) |
| | | Output | High write: Strobe signal for writing data on pins AD8 to 15 |
| | | I/O | Mode clock SBI SIO mode clock |
| P33 / SO / SDA | 1 | I/O | Port 33: I/O port |
| | | Output | Serial Send Data |
| | | I/O | SBI $I^2C$ bus mode channel data |
| P34 / SI / SCL | 1 | I/O | Port 34: I/O port |
| | | Input | Serial Receive Data |
| | | I/O | SBI $I^2C$ bus mode clock |
| P35 / INT0 | 1 | I/O | Port 35: I/O port |
| | | Input | Interrupt request pin 0: Interrupt request pin with programmable level/rising edge  |
| P40 / TI0 / INT1 | 1 | I/O | Port 40: I/O port |
| | | Input | Timer input 0: Timer 0 input |
| | | Input | Interrupt request pin 1: Interrupt request pin with rising edge  |
| P41 / TO3 | 1 | I/O | Port 41: I/O port |
| | | Output | Timer output 3: 8-bit Timer 3 output |
| P42 / TI4 / INT4 | 1 | I/O | Port 42: I/O port |
| | | Input | Timer input 4: Timer 4 input |
| | | Input | Interrupt request pin 4: Interrupt request pin with programmable rising / falling edge  |
| P43 / TI5 / INT5 | 1 | I/O | Port 43: I/O port |
| | | Input | Timer input 5: Timer 4 input |
| | | Input | Interrupt request pin 5: Interrupt request pin with rising edge  |
| P44 / TO4 | 1 | I/O | Port 44 : I/O port |
| | | Output | Timer output 4: Timer 4 output pin |

Table 2.2 Pin Names and Function (2/3)

| Pin name | Number of pins | I/O | Functions |
|---|---|---|---|
| P45 / TI6 / INT6 | 1 | I/O | Port 45: I/O port |
| | | Input | Timer input 6: Timer 5 input |
| | | Input | Interrupt request pin 6: Interrupt request pin with programmable rising / falling edge |
| P46 / TI7 / INT7 | 1 | I/O | Port 46: I/O port |
| | | Input | Timer input 7: Timer 5 input |
| | | Input | Interrupt request pin 7: Interrupt request pin with rising edge |
| P47 / TO6 | 1 | I/O | Port 47: I/O port |
| | | Output | Timer output 6: Timer 5 output pin |
| P50 to P52, P54 to P57 / AN0 to AN2, AN4 to AN7 | 7 | Input | Port 50 to Port 52, Port 54 to Port 57: Input port |
| | | Input | Analog input: Analog signal input for A/D converter |
| P53 / AN3 / $\overline{\text{ADTRG}}$ | 1 | Input | Port53: Input Port |
| | | Input | Analog input: Analog signal input for A/D converter |
| | | Input | A/D converter external start trigger input |
| P60 / TXD0 | 1 | I/O | Port 60: I/O port (with pull-up resistor) |
| | | Output | Serial send data 0 |
| P61 / RXD0 | 1 | I/O | Port 61: I/O port (with pull-up resistor) |
| | | Input | Serial receive data 0 |
| P62 / $\overline{\text{CTS0}}$ / SCLK0 | 1 | I/O | Port 62: I/O port (with pull-up resistor) |
| | | Input | Serial data send enable 0 (Clear to Send) |
| | | I/O | Serial Clock I/O 0 |
| P63 / TXD1 | 1 | I/O | Port 63: I/O port (with pull-up resistor) |
| | | Output | Serial send data 1 |
| P64 / RXD1 | 1 | I/O | Port 64: I/O port (with pull-up resistor) |
| | | Input | Serial receive data 1 |
| P65 / $\overline{\text{CTS1}}$ / SCLK1 | 1 | I/O | Port 65: I/O port (with pull-up resistor) |
| | | Input | Serial data send enable 1 (Clear to Send) |
| | | I/O | Serial clock I/O 1 |
| P70 / $\overline{\text{WAIT}}$ | 1 | I/O | Port 70: I/O port (High current output available) |
| | | Input | WAIT: Pin used to request CPU bus wait (It is active in 1 WAIT + N mode. Set by the Bus-width/wait control register.) |
| P71 to P77 | 7 | I/O | Port 7: I/O port (High current output available) |
| $\overline{\text{NMI}}$ | 1 | Input | Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at falling and rising edges by program. |
| CLK | 1 | Output | Clock output: Outputs "$f_{SYS} \div 2$" Clock. Pulled-up during reset. Can be disabled for reducing noise. |
| $\overline{\text{EA}}$ | 1 | Input | External access: "1" should be inputted with TMP93CU44. |

Table 2.2 Pin Names and Function (3/3)

| Pin name | Number of pins | I/O | Functions |
|---|---|---|---|
| AM8 / $\overline{16}$ | 1 | Input | Address Mode: Selects external Data Bus width.<br>(the case of TMP93CU44)<br>"1" should be inputted. The Data Bus Width for external access is set by Chip Select / WAIT Control register, Port 1 Control register. |
| ALE | 1 | Output | Address Latch Enable<br>Can be disabled for reducing noise. |
| $\overline{\text{RESET}}$ | 1 | Input | Reset: Initializes TMP93CU44. (With pull-up resistor) |
| VREFH | 1 | Input | Pin for high level reference voltage input to A/D converter |
| VREFL | 1 | Input | Pin for low level reference voltage input to A/D converter |
| AVCC | 1 | | Power supply pin for A/D converter |
| AVSS | 1 | | GND pin for A/D converter (0 V) |
| X1 | 1 | Input | High Frequency Oscillator connecting pin |
| X2 | 1 | Output | High Frequency Oscillator connecting pin |
| P66 | 1 | I/O | Port 66: I/O port (Open Drain Output) |
| / XT1 | | Input | Low Frequency Oscillator connecting pin |
| P67 | 1 | I/O | Port 67: I/O port (Open Drain Output) |
| / XT2 | | Output | Low Frequency Oscillator connecting pin |
| TEST1 / TEST2 | 2 | Output / Input | TEST1 Should be connected with TEST2 pin. |
| VCC | 2 | | Power supply pin (All $V_{CC}$ pins should be connected with GND (0V).) |
| VSS | 2 | | GND pin (0 V) (All $V_{SS}$ pins should be connected with GND (0V).) |

Note : Built-in Pull-up resistors can be released from the pins other than the $\overline{\text{RESET}}$ pin by software.

## 3. OPERATION

This section describes the functions and basic operational blocks of TMP93CU44 devices.

### 3.1 CPU

TMP93CU44 devices have a built-in high-performance 16-bit CPU (900 / L CPU). (For CPU operation, see TLCS-900 / L CPU in the previous section)

### 3.2 Memory Map

Figure 3.2 is a memory map of the TMP93CU44.

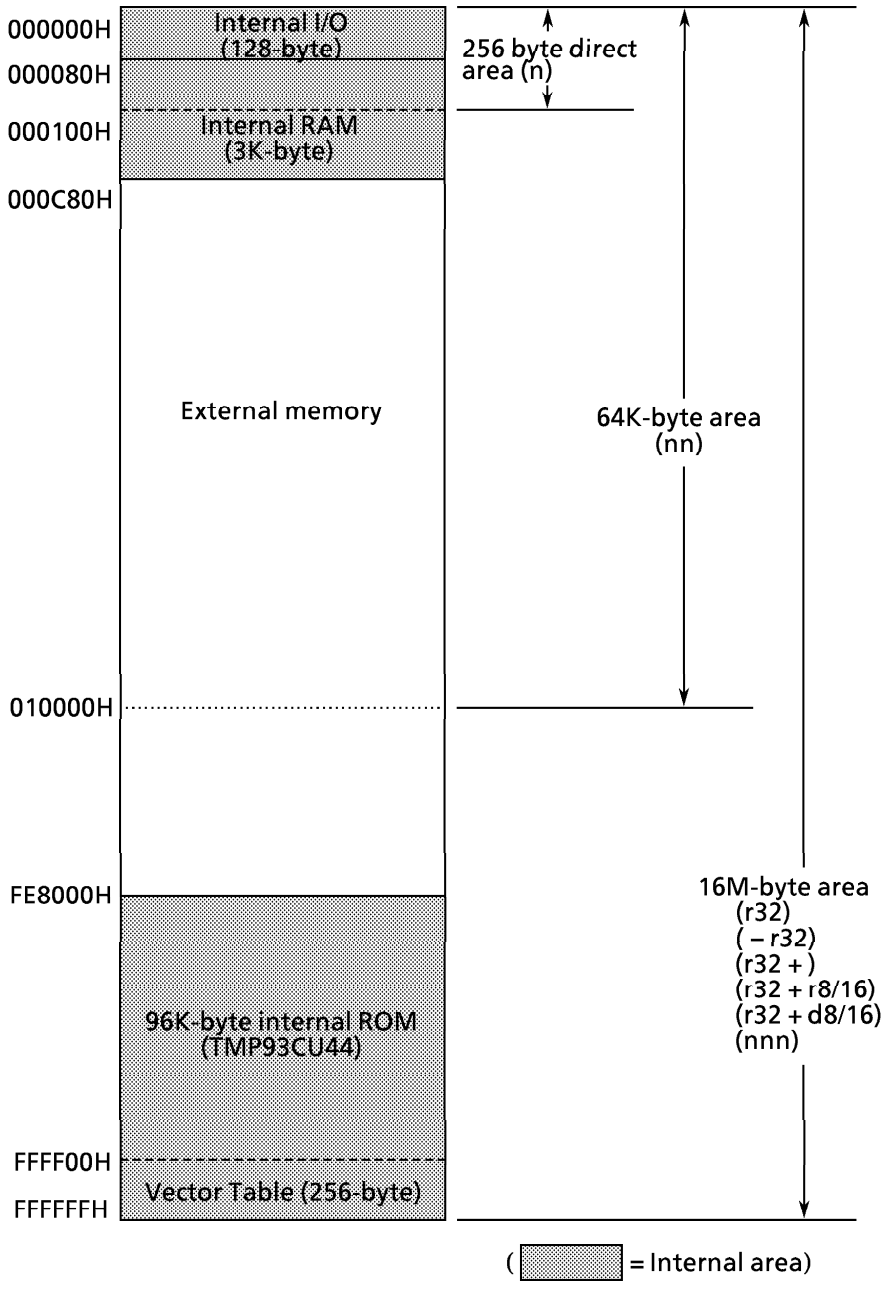



Figure 3.2 Memory map

## 4. ELECTRICAL CHARACTERISTICS (PRELIMINARY)

"X" used in an expression shows a cycle of clock $f_{FPH}$ selected by SYSCR1<SYSCK>. If a clock gear or a low speed oscillator is selected, a value of "X" is different. The value as an example is calculated at fc, gear = 1/fc (SYSCR1<SYSCK, GEAR 2 to 0> = "0000").

### 4.1 Absolute Maximum Ratings (TMP93CU44DF)

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| Vcc | Power Supply Voltage | – 0.5 to 6.5 | V |
| $V_{IN}$ | Input Voltage | – 0.5 to Vcc + 0.5 | V |
| $I_{OL1}$ | Output current (Per 1 pin) P7 | 20 | mA |
| $I_{OL2}$ | Output current (Per 1 pin) except P7 | 2 | mA |
| $\Sigma I_{OL1}$ | Output Current (P7 total) | 80 | mA |
| $\Sigma I_{OL}$ | Output Current (total) | 120 | mA |
| $\Sigma I_{OH}$ | Output Current (total) | – 80 | mA |
| $P_D$ | Power Dissipation (Ta = 85 ℃) | 350 | mW |
| $T_{SOLDER}$ | Soldering Temperature (10 s) | 260 | ℃ |
| $T_{STG}$ | Storage Temperature | – 65 to 150 | ℃ |
| $T_{OPR}$ | Operating Temperature | – 40 to 85 | ℃ |

### 4.2 DC Characteristics (1/2)

Ta = – 40 to 85°C

| Symbol | Parameter | | Min. | Typ. (Note1) | Max. | Unit | Condition |
|---|---|---|---|---|---|---|---|
| Vcc | Power Supply Voltage | | 4.5<br>2.7 | | 5.5 | V | fc = 4 to 20 MHz<br>fc = 4 to 12.5 MHz<br>fs = 30 to 34 kHz |
| $V_{IL}$ | Input Low Voltage | AD0 to 15 | – 0.3 | | 0.8<br>0.6 | | Vcc ≧ 4.5V<br>Vcc < 4.5V |
| $V_{IL1}$ | | Port2 to 7 (except P35) | | | 0.3Vcc | V | Vcc = 2.7 to 5.5V |
| $V_{IL2}$ | | RESET, NMI, INT0 | | | 0.25Vcc | | |
| $V_{IL3}$ | | EA, AM8/16 | | | 0.3 | | |
| $V_{IL4}$ | | X1 | | | 0.2Vcc | | |
| $V_{IH}$ | Input High Voltage | AD0 to 15 | 2.2<br>2.0 | | Vcc + 0.3 | | Vcc≧4.5V<br>Vcc<4.5V |
| $V_{IH1}$ | | Port2 to 7 (except P35) | 0.7Vcc | | | | Vcc = 2.7 to 5.5V |
| $V_{IH2}$ | | RESET, NMI, INT0 | 0.75Vcc | | | | |
| $V_{IH3}$ | | EA, AM8/16 | Vcc – 0.3 | | | | |
| $V_{IH4}$ | | X1 | 0.8Vcc | | | | |
| $V_{OL}$ | Output Low Voltage | | | | 0.45 | | $I_{OL}$ = 1.6 mA (Vcc = 2.7 to 5.5V) |
| $I_{OL7}$ | Output Low current (P7) | | 16<br>7 | | | mA | $V_{OL}$ = 1.0V (Vcc = 5V ± 10 %)<br>(Vcc = 3V ± 10 %) |
| $V_{OH1}$ | Output High Voltage | | 2.4 | | | V | $I_{OH}$ = – 400 μA (Vcc = 3V ± 10%) |
| $V_{OH2}$ | | | 4.2 | | | V | $I_{OH}$ = – 400 μA (Vcc = 5V ± 10%) |

Note 1: Typical values are for Ta = 25 °C and $V_{CC}$ = 5 V unless otherwise noted.

### 4.2 DC Characteristics (2/2)

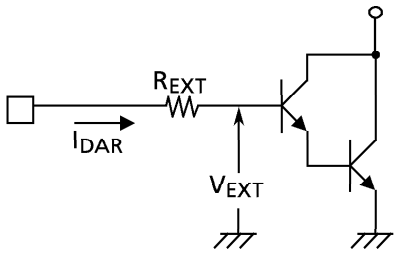
| Symbol | Parameter | Min | Typ.(Note1) | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $I_{DAR}$ (Note2) | Darlington Drive Current (8 Output Pins max.) | −1.0 | | −3.5 | mA | $V_{EXT}$ = 1.5 V, $R_{EXT}$ = 1.1 kΩ (Vcc = 5 V ± 10 % only) |
| $I_{LI}$ | Input Leakage Current | | 0.02 | ±5 | μA | 0.0 ≦ $V_{IN}$ ≦ $V_{CC}$ |
| $I_{LO}$ | Output Leakage Current | | 0.05 | ±10 | μA | 0.2 ≦ $V_{IN}$ ≦ $V_{CC}$ − 0.2 |
| $V_{STOP}$ | Power Down Voltage (at STOP, RAM Back up) | 2.0 | | 6.0 | V | $V_{IL2}$ = 0.2 Vcc, $V_{IH2}$ = 0.8 Vcc |
| $R_{PU}$ | Pull Up Resistance | 45 | | 130 | kΩ | Vcc = 5.5 V |
| | | 50 | | 160 | | Vcc = 4.5 V |
| | | 70 | | 280 | | Vcc = 3.3 V |
| | | 90 | | 400 | | Vcc = 2.7 V |
| $C_{IO}$ | Pin Capacitance | | | 10 | pF | fc = 1 MHz |
| $V_{TH}$ | Schmitt Width RESET, NMI, INT0 | 0.4 | 1.0 | | V | |
| Icc | NORMAL (Note3) | | 21 | 28 | mA | Vcc = 5 V ± 10 %, fc = 20 MHz |
| | RUN | | 17 | 25 | | |
| | IDLE2 | | 12.5 | 17 | | |
| | IDLE1 | | 2.5 | 4 | | |
| | NORMAL (Note3) | | 7 | 10 | | Vcc = 3 V ± 10 %, fc = 12.5 MHz (Typ. : Vcc = 3.0 V) |
| | RUN | | 5.5 | 9 | | |
| | IDLE2 | | 4.5 | 6 | | |
| | IDLE1 | | 0.7 | 1 | | |
| | SLOW (Note3) | | 20 | 35 | μA | Vcc = 3 V ± 10 %, fs = 32.768 kHz (Typ. : Vcc = 3.0 V) |
| | RUN | | 16 | 30 | | |
| | IDLE2 | | 11 | 25 | | |
| | IDLE1 | | 4 | 15 | | |
| | STOP | | 0.2 | 10 | μA | Ta ≦ 50 °C, Vcc = 2.7 V to 5.5 V |
| | | | | 20 | | Ta ≦ 70 °C |
| | | | | 50 | | Ta ≦ 85 °C |

Note 1: Typical values are for Ta = 25 °C and $V_{CC}$ = 5 V unless otherwise noted.

Note 2: $I_{DAR}$ is guranteed for total of up to 8 ports.

Note 3: $I_{CC}$ measurement conditions (NORMAL, SLOW).
Only CPU is operational; output pins are open and input pins are fixed.

(Reference) Definition of $I_{DAR}$



### 4.3 AC Characteristics

(1) Vcc = 5 V ± 10 %

| No. | Symbol | Parameter | Variable | | 16 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| 1 | $t_{OSC}$ | Osc. Period ( = x) | 50 | 31250 | 62.5 | | 50 | | ns |
| 2 | $t_{CLK}$ | CLK width | 2x – 40 | | 85 | | 60 | | ns |
| 3 | $t_{AK}$ | A0 to 23 Valid→ CLK Hold | 0.5x – 20 | | 11 | | 5 | | ns |
| 4 | $t_{KA}$ | CLK Valid→ A0 to 23 Hold | 1.5x – 70 | | 24 | | 5 | | ns |
| 5 | $t_{AL}$ | A0 to 15 Valid→ ALE fall | 0.5x – 15 | | 16 | | 10 | | ns |
| 6 | $t_{LA}$ | ALE fall→ A0 to 15 Hold | 0.5x – 20 | | 11 | | 5 | | ns |
| 7 | $t_{LL}$ | ALE High width | x – 40 | | 23 | | 10 | | ns |
| 8 | $t_{LC}$ | ALE fall→ $\overline{RD}/\overline{WR}$ fall | 0.5x – 25 | | 6 | | 0 | | ns |
| 9 | $t_{CL}$ | $\overline{RD}/\overline{WR}$ rise→ ALE rise | 0.5x – 20 | | 11 | | 5 | | ns |
| 10 | $t_{ACL}$ | A0 to 15 Valid→ $\overline{RD}/\overline{WR}$ fall | x – 25 | | 38 | | 25 | | ns |
| 11 | $t_{ACH}$ | A0 to 23 Valid→ $\overline{RD}/\overline{WR}$ fall | 1.5x – 50 | | 44 | | 25 | | ns |
| 12 | $t_{CA}$ | $\overline{RD}/\overline{WR}$ rise→ A0 to 23 Hold | 0.5x – 25 | | 6 | | 0 | | ns |
| 13 | $t_{ADL}$ | A0 to 15 Valid→ D0 to 15 input | | 3.0x – 55 | | 133 | | 95 | ns |
| 14 | $t_{ADH}$ | A0 to 23 Valid→ D0 to 15 input | | 3.5x – 65 | | 154 | | 110 | ns |
| 15 | $t_{RD}$ | $\overline{RD}$ fall → D0 to 15 input | | 2.0x – 60 | | 65 | | 40 | ns |
| 16 | $t_{RR}$ | $\overline{RD}$ Low pulse width | 2.0x – 40 | | 85 | | 60 | | ns |
| 17 | $t_{HR}$ | $\overline{RD}$ rise→ D0 to 15 Hold | 0 | | 0 | | 0 | | ns |
| 18 | $t_{RAE}$ | $\overline{RD}$ rise→ A0 to 15output | x – 15 | | 48 | | 35 | | ns |
| 19 | $t_{WW}$ | $\overline{WR}$ Low pulse width | 2.0x – 40 | | 85 | | 60 | | ns |
| 20 | $t_{DW}$ | D0 to 15 Valid→ $\overline{WR}$ rise | 2.0x – 55 | | 70 | | 45 | | ns |
| 21 | $t_{WD}$ | $\overline{WR}$ rise →D0 to 15 Hold | 0.5x – 15 | | 16 | | 10 | | ns |
| 22 | $t_{AWH}$ | A0 to 23 Valid→ $\overline{WAIT}$ input $(^{1\ WAIT}_{+n\ mode})$ | | 3.5x – 90 | | 129 | | 85 | ns |
| 23 | $t_{AWL}$ | A0 to 15 Valid→ $\overline{WAIT}$ input $(^{1\ WAIT}_{+n\ mode})$ | | 3.0x – 80 | | 108 | | 70 | ns |
| 24 | $t_{CW}$ | $\overline{RD}/\overline{WR}$ fall→$\overline{WAIT}$ Hold $(^{1\ WAIT}_{+n\ mode})$ | 2.0x + 0 | | 125 | | 100 | | ns |
| 25 | $t_{APH}$ | A0 to 23 Valid→ PORT input | | 2.5x – 120 | | 36 | | 5 | ns |
| 26 | $t_{APH2}$ | A0 to 23 Valid→ PORT Hold | 2.5x + 50 | | 206 | | 175 | | ns |
| 27 | $t_{CP}$ | $\overline{WR}$ rise→ PORT Valid | | 200 | | 200 | | 200 | ns |

AC Measuring Conditions

- Output Level : High 2.2 V / Low 0.8 V , CL = 50 pF
  (However CL = 100 pF for AD0 to AD15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, CLK)
- Input Level : High 2.4 V / Low 0.45 V (AD0 to AD15)
  High 0.8 Vcc / Low 0.2 Vcc (Except for AD0 to AD15)

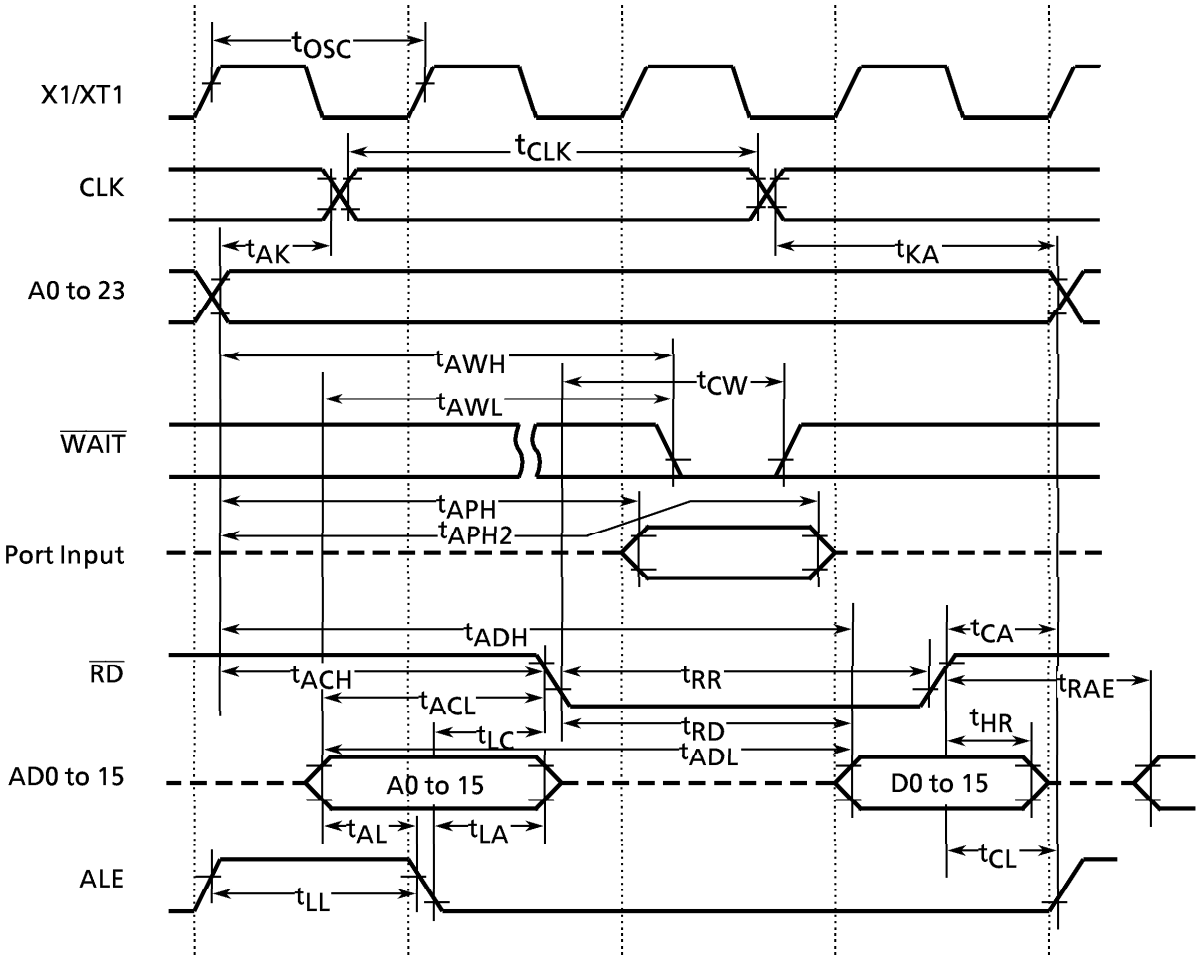
(2) Vcc = 3 V ± 10 %

| No. | Symbol | Parameter | Variable | | 12.5 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| 1 | $t_{OSC}$ | Osc. Period ( = x) | 80 | 31250 | 80 | | ns |
| 2 | $t_{CLK}$ | CLK width | 2x – 40 | | 120 | | ns |
| 3 | $t_{AK}$ | A0 to 23 Valid→ CLK Hold | 0.5x – 30 | | 10 | | ns |
| 4 | $t_{KA}$ | CLK Valid→ A0 to 23 Hold | 1.5x – 80 | | 40 | | ns |
| 5 | $t_{AL}$ | A0 to 15 Valid→ ALE fall | 0.5x – 35 | | 5 | | ns |
| 6 | $t_{LA}$ | ALE fall→ A0 to 15 Hold | 0.5x – 35 | | 5 | | ns |
| 7 | $t_{LL}$ | ALE High width | x – 60 | | 20 | | ns |
| 8 | $t_{LC}$ | ALE fall→ $\overline{RD}/\overline{WR}$ fall | 0.5x – 35 | | 5 | | ns |
| 9 | $t_{CL}$ | $\overline{RD}/\overline{WR}$ rise→ ALE rise | 0.5x – 40 | | 0 | | ns |
| 10 | $t_{ACL}$ | A0 to 15 Valid→ $\overline{RD}/\overline{WR}$ fall | x – 50 | | 30 | | ns |
| 11 | $t_{ACH}$ | A0 to 23 Valid→ $\overline{RD}/\overline{WR}$ fall | 1.5x – 50 | | 70 | | ns |
| 12 | $t_{CA}$ | $\overline{RD}/\overline{WR}$ rise→ A0 to 23 Hold | 0.5x – 40 | | 0 | | ns |
| 13 | $t_{ADL}$ | A0 to 15 Valid→ D0 to 15 input | | 3.0x – 110 | | 130 | ns |
| 14 | $t_{ADH}$ | A0 to 23 Valid→ D0 to 15 input | | 3.5x – 125 | | 155 | ns |
| 15 | $t_{RD}$ | $\overline{RD}$fall →D0 to 15 input | | 2.0x – 115 | | 45 | ns |
| 16 | $t_{RR}$ | $\overline{RD}$ Low pulse width | 2.0x – 40 | | 120 | | ns |
| 17 | $t_{HR}$ | $\overline{RD}$rise→ D0 to 15 Hold | 0 | | 0 | | ns |
| 18 | $t_{RAE}$ | $\overline{RD}$rise→ A0 to 15output | x – 25 | | 55 | | ns |
| 19 | $t_{WW}$ | $\overline{WR}$ Low pulse width | 2.0x – 40 | | 120 | | ns |
| 20 | $t_{DW}$ | D0 to 15 Valid→ $\overline{WR}$rise | 2.0x – 120 | | 40 | | ns |
| 21 | $t_{WD}$ | $\overline{WR}$ rise →D0 to 15 Hold | 0.5x – 40 | | 0 | | ns |
| 22 | $t_{AWH}$ | A0 to 23 Valid→ $\overline{WAIT}$ input $(^{1\ WAIT}_{+n\ mode})$ | | 3.5x – 130 | | 150 | ns |
| 23 | $t_{AWL}$ | A0 to 15 Valid→ $\overline{WAIT}$ input $(^{1\ WAIT}_{+n\ mode})$ | | 3.0x – 100 | | 140 | ns |
| 24 | $t_{CW}$ | $\overline{RD}/\overline{WR}$ fall→$\overline{WAIT}$ Hold $(^{1\ WAIT}_{+n\ mode})$ | 2.0x + 0 | | 160 | | ns |
| 25 | $t_{APH}$ | A0 to 23 Valid→ PORT input | | 2.5x – 120 | | 80 | ns |
| 26 | $t_{APH2}$ | A0 to 23 Valid→ PORT Hold | 2.5x + 50 | | 250 | | ns |
| 27 | $t_{CP}$ | $\overline{WR}$ rise→ PORT Valid | | 200 | | 200 | ns |

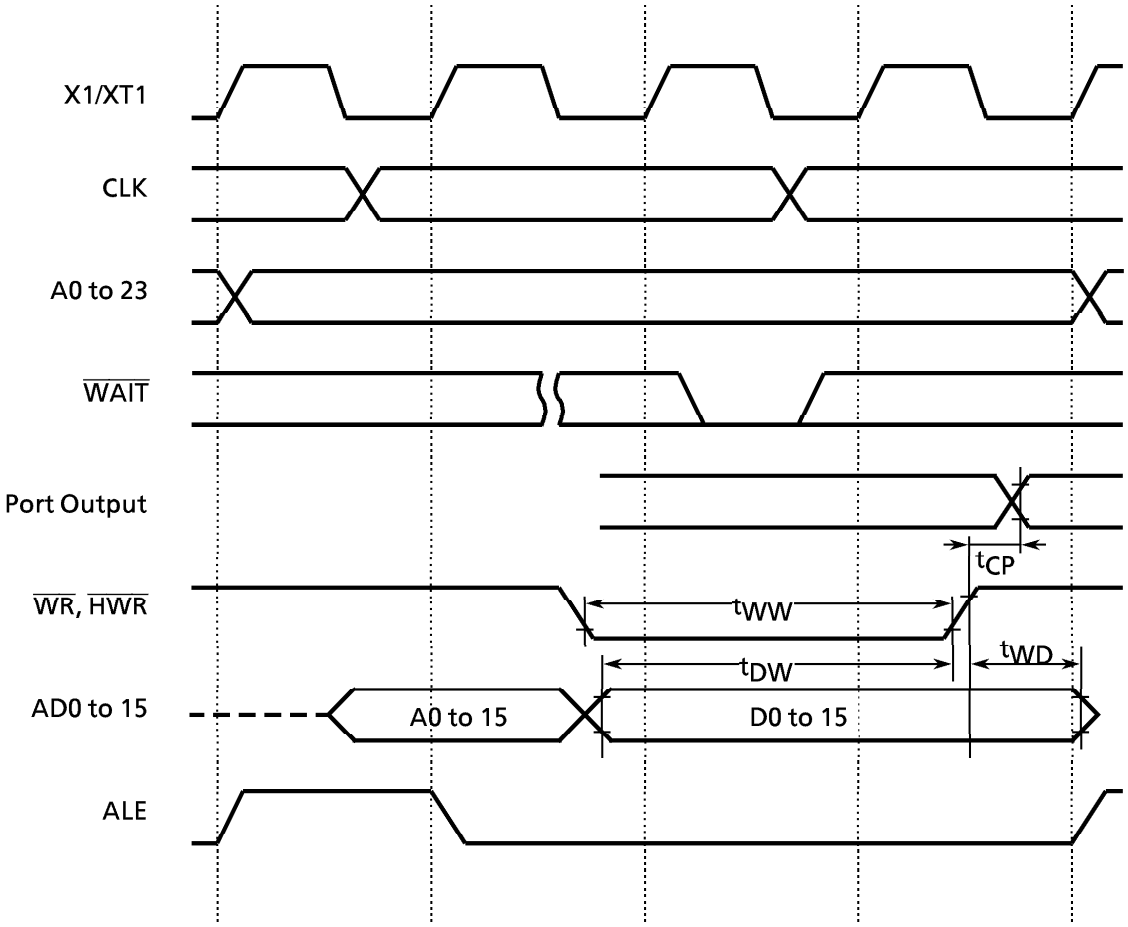
AC Measuring Conditions

- Output Level : High 0.7 × $V_{CC}$ / Low 0.3 × $V_{CC}$ , CL = 50 pF
- Input Level : High 0.9 × $V_{CC}$ / Low 0.1 × $V_{CC}$

(1) Read Cycle


X1/XT1
CLK
A0 to 23
WAIT
Port Input
RD
AD0 to 15
ALE
tOSC
tCLK
tAK
tKA
tAWH
tAWL
tCW
tAPH
tAPH2
tADH
tCA
tACH
tRR
tRAE
tACL
tLC
tRD
tHR
tADL
A0 to 15
D0 to 15
tAL
tLA
tCL
tLL

(2) Write Cycle



## 4.4 Serial Channel Timing

### (1) I/O Interface Mode

#### ① SCLK Input Mode

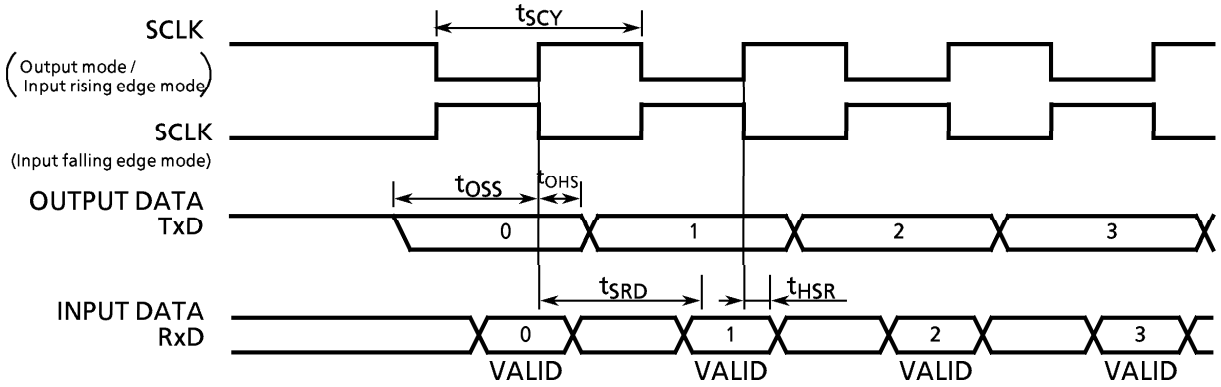
| Symbol | Parameter | Variable | | 32.768 MHz (Note) | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{SCY}$ | SCLK cycle | 16X | | 488 μs | | 1.28 | | 0.8 | | μs |
| $t_{OSS}$ | Output Data → falling edge of SCLK | $t_{SCY}/2 - 5X - 50$ | | 91.5 μs | | 190 | | 100 | | ns |
| $t_{OHS}$ | SCLK rising / falling edge → Output Data hold | 5X – 100 | | 152 μs | | 300 | | 150 | | ns |
| $t_{HSR}$ | SCLK rising / falling edge → Input Data hold | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{SRD}$ | SCLK rising / falling edge → effective data input | | $t_{SCY} - 5X - 100$ | | 336 μs | | 780 | | 450 | ns |

Note 1: When fs is used as system clock or fs divided by 4 is used as input clock to prescaler.
Note 2: SCLK rising/falling timing; SCLK rising in the rising mode of SCLK, SCLK falling in the falling mode of SCLK.

#### ② SCLK Output Mode

| Symbol | Parameter | Variable | | 32.768 MHz (Note) | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{SCY}$ | SCLK cycle (Programmable) | 16X | 8192X | 488 μs | 250 ms | 1.28 | 865.36 | 0.8 | 409.6 | μs |
| $t_{OSS}$ | Output Data → SCLK rising edge | $t_{SCY} - 2X - 150$ | | 427 μs | | 970 | | 550 | | ns |
| $t_{OHS}$ | SCLK rising edge → Output Data hold | 2X – 80 | | 60 μs | | 80 | | 20 | | ns |
| $t_{HSR}$ | SCLK rising edge → Input Data hold | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{SRD}$ | SCLK rising edge → effective Data input | | $t_{SCY} - 2X - 150$ | | 428 μs | | 970 | | 550 | ns |

Note: When fs is used as system clock or fs divided by 4 is used as input clock to prescaler.



(2) UART Mode ( SCLK0, 1 are external input)

| Symbol | Parameter | Variable | | 32.768 kHz (Note) | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{SCY}$ | SCLK cycle | 4x + 20 | | 122 μs | | 340 | | 220 | | ns |
| $t_{SCYL}$ | SCLK Low level pulse width | 2x + 5 | | 6 μs | | 165 | | 105 | | ns |
| $t_{SCYH}$ | SCLK High level pulse width | 2x + 5 | | 6 μs | | 165 | | 105 | | ns |

Note: When fs is used as system clock or fs divided by 4 is used as input clock to prescaler.

## 4.5 A/D Conversion Characteristics

$AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$

| Symbol | Parameter | Power Supply | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VREFH | Analog reference voltage ( + ) | $V_{CC}$ = 5V ± 10 % | $V_{CC}$ – 0.2 V | $V_{CC}$ | $V_{CC}$ | V |
| | | $V_{CC}$ = 3V ± 10 % | $V_{CC}$ – 0.2 V | $V_{CC}$ | $V_{CC}$ | |
| VREFL | Analog reference voltage ( – ) | $V_{CC}$ = 5V ± 10 % | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.2 V | |
| | | $V_{CC}$ = 3V ± 10 % | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.2 V | |
| $V_{AIN}$ | Analog input voltage range | | VREFL | | VREFH | |
| $I_{REF}$ ($V_{REFL}$ = 0 V) | Analog current for analog reference voltage <VREFON> = 1 | $V_{CC}$ = 5V ± 10 % | | 0.5 | 1.5 | mA |
| | | $V_{CC}$ = 3V ± 10 % | | 0.3 | 0.9 | |
| | <VREFON> = 0 | $V_{CC}$ = 2.7 to 5.5V | | 0.02 | 5.0 | μA |
| – | Error (except quantization errors) | $V_{CC}$ = 5V ± 10 % | | ± 1.0 | ± 3.0 | LSB |
| | | $V_{CC}$ = 3V ± 10 % | | ± 1.0 | ± 5.0 | |

Note 1: 1LSB = (VREFH – VREFL) / $2^{10}$ [V]
Note 2: The operation above is guaranteed for $f_{FPH} \geqq 4$ MHz.
Note 3: The value $I_{CC}$ includes the current which flows through the AVCC pin.

## 4.6 Event Counter Input Clock (external input clock : TI0, TI4, TI5, TI6, TI7)

| Symbol | Parameter | Variable | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{VCK}$ | Clock Cycle | 8X + 100 | | 740 | | 500 | | ns |
| $t_{VCKL}$ | Low level clock Pulse width | 4X + 40 | | 360 | | 240 | | ns |
| $t_{VCKH}$ | High level clock Pulse width | 4X + 40 | | 360 | | 240 | | ns |

## 4.7 Interrupt and Capture Operation

(1) $\overline{NMI}$, INT0 Interrupts

| Symbol | Parameter | Variable | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{INTAL}$ | $\overline{NMI}$, INT0 Low level Pulse width | 4X | | 320 | | 200 | | ns |
| $t_{INTAH}$ | $\overline{NMI}$, INT0 High level Pulse width | 4X | | 320 | | 200 | | ns |

(2) INT1, 4 to 7 Interrupts and Capture

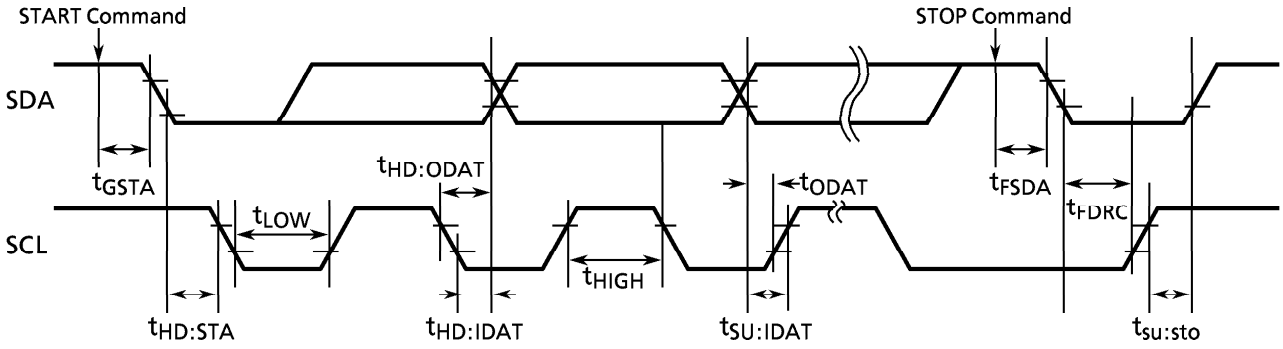
| Symbol | Parameter | Variable | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{INTBL}$ | INT1, INT4 to INT7 Low level Pulse width | 4X + 100 | | 420 | | 300 | | ns |
| $t_{INTBH}$ | INT1, INT4 to INT7 High level Pulse width | 4X + 100 | | 420 | | 300 | | ns |

## 4.8 Serial Bus Interface Timing

(1) $I^2C$ Bus Mode

| Symbol | Parameter | Variable | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $t_{GSTA}$ | START command → SDA fall | 3X | | | s |
| $t_{HD:STA}$ | Hold time START condition | $2^n$X | | | s |
| $t_{LOW}$ | SCL Low level pulse width | $2^n$X | | | s |
| $t_{HIGH}$ | SCL High level pulse width | $2^n$X + 12X | | | s |
| $t_{HD:IDAT}$ | Data hold time (input) | 0 | | | ns |
| $t_{SU:IDAT}$ | Data set-up time (input) | 250 | | | ns |
| $t_{HD:ODAT}$ | Data hold time (output) | 7X | | 11X | s |
| $t_{ODAT}$ | Data output → SCL Rising edge | | $2^n$X – $t_{HD:ODAT}$ | | s |
| $t_{FSDA}$ | STOP command → SDA fall | 3X | | | s |
| $t_{FDRC}$ | SDA Falling edge → SCL Rising edge | $2^n$X | | | s |
| $t_{SU:STO}$ | Set-up time STOP condition | $2^n$X + 16X | | | s |

Note : "n" value is set by SBICR1 <SCK2 to 0>



(2) Clocked-synchronous 8-bit SIO Mode

① SCK Input Mode

| Symbol | Parameter | Variable | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{SCY2}$ | SCK cycle | $2^5X$ | | s |
| $t_{OHS2}$ | SCK falling edge→ Output data hold | 6X | | s |
| $t_{OSS2}$ | Output data → SCK rising edge | $t_{SCY2}$ – 6X | | s |
| $t_{HSR2}$ | SCK rising edge→ Input data hold | 6X | | ns |
| $t_{ISS2}$ | Input data→ SCK rising edge | 0 | | ns |

② SCK Output Mode

| Symbol | Parameter | Variable | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{SCY2}$ | SCK cycle | $2^5X$ | $2^{11}X$ | s |
| $t_{OHS2}$ | SCK falling edge → Output data hold | 2X | | s |
| $t_{OSS2}$ | Output data→ SCK rising edge | $t_{SCY2}$ – 2X | | s |
| $t_{HSR2}$ | SCK rising edge→ Input data hold | 2X | | s |
| $t_{ISS2}$ | Input data→ SCK rising edge | 0 | | ns |