CMOS 16-Bit Microcontroller

TMP93PF76F

1. Outline and Feature

The TMP93PF76F is a system evaluation LSI having a built in One-Time PROM (192 Kbytes) for TMP93CF76/77F.

A programming and verification for the internal PROM is achieved by using a general EPROM programmer with an adapter socket.

The function of this device is exactly same as the TMP93CF76/77F by programming to the internal PROM and the TMP93PF76F is used as the evaluation chip of TMP93CF76/77F.

Product no.	ROM	RAM	Package	Adapter Socket no.
TMP93PF76F	OTP 192 Kbytes	4.0 Kbytes	P-QFP100-1420-0.65A	BM11146A

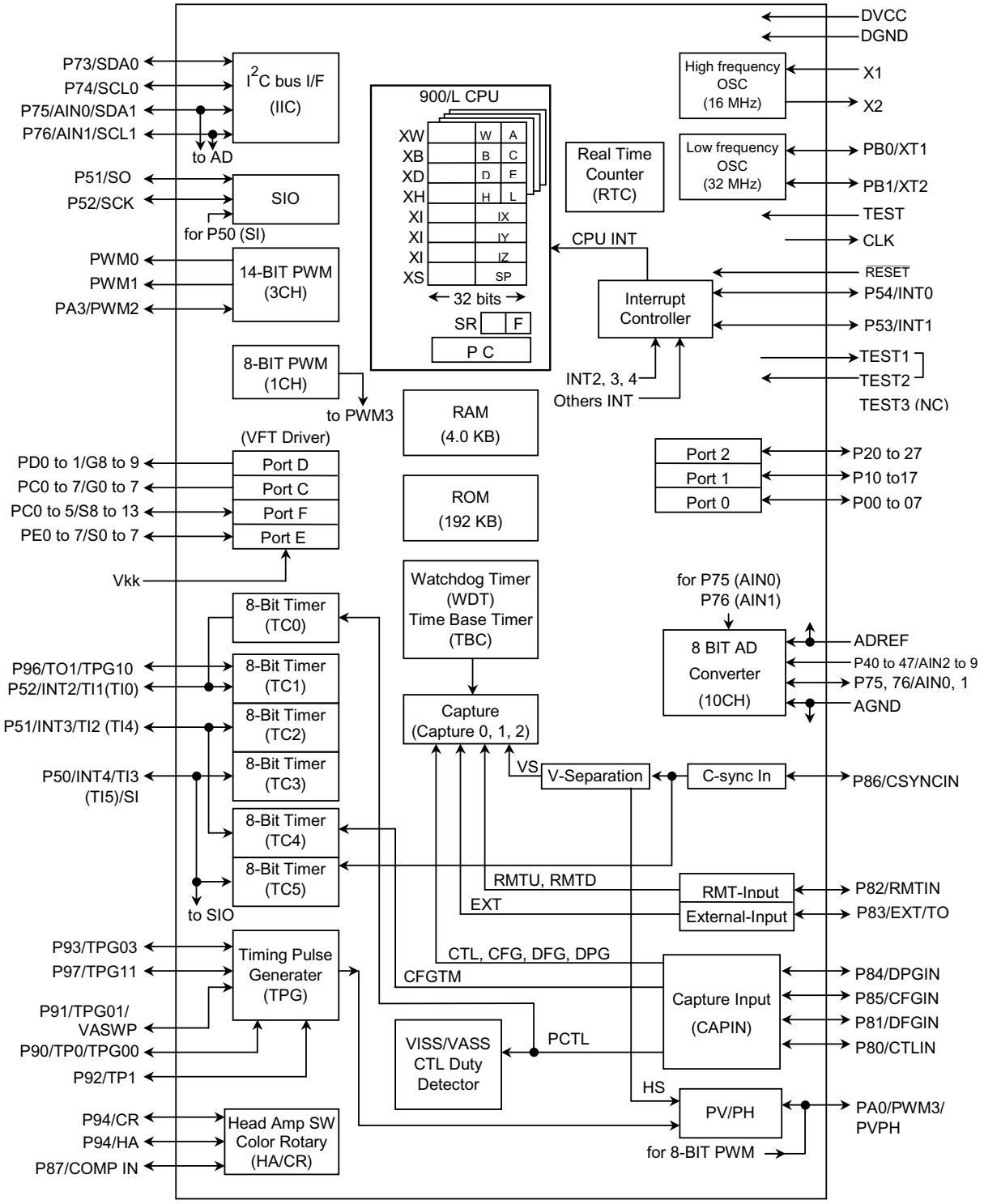


Figure 1.1 TMP93PF76F block diagram

2. Pin Assignment and Functions

The assignment of input and output pins for the TMP93PF76F, their names and functions are described below.

2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of the TMP93PF76F.

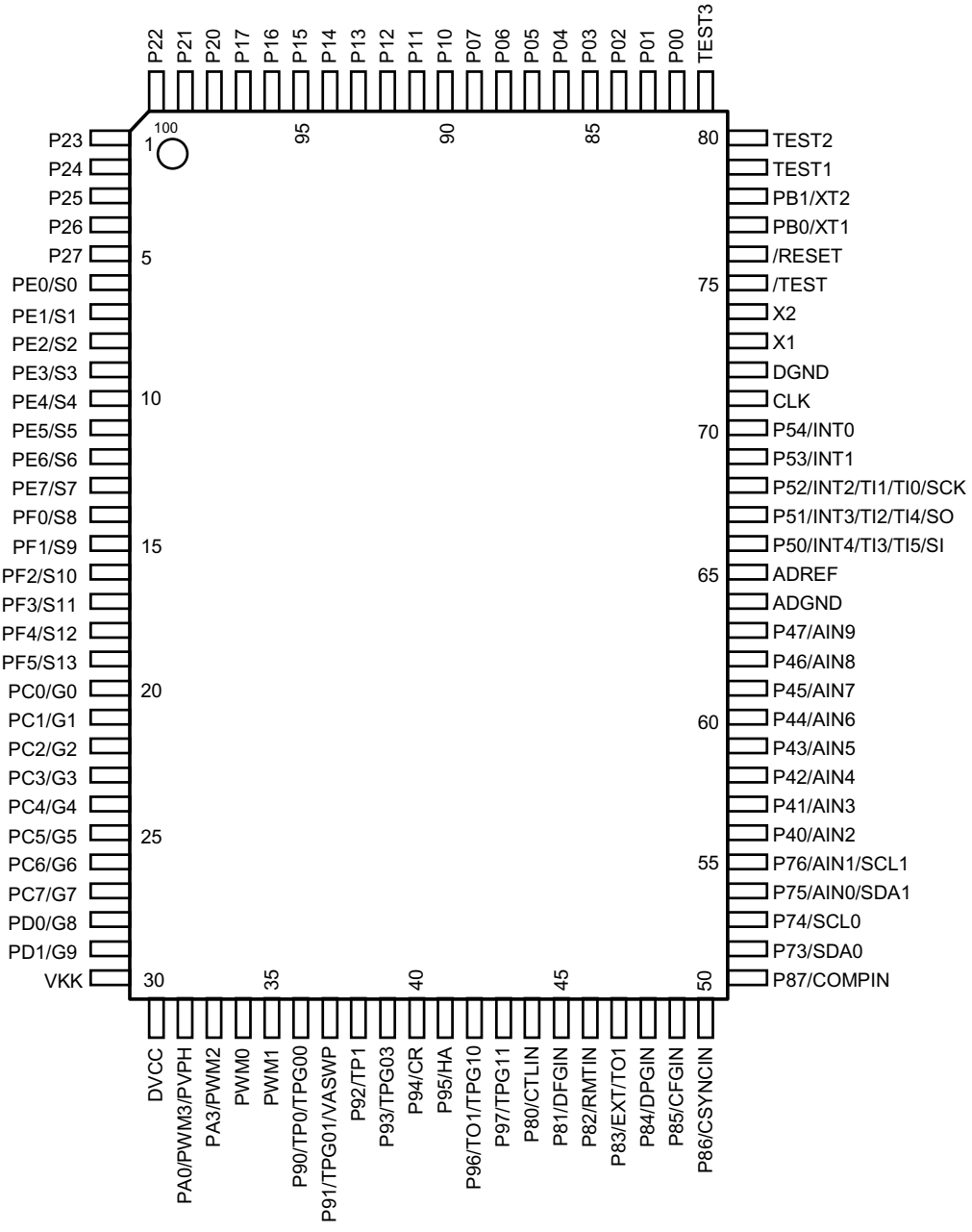


Figure 2.1.1 Pin assignment (100-pin QFP)

2.2 Pin Names and Functions

The names of input/output pins and their functions are described below.

(1) MCU mode

Table 2.2.1 Pin names and function (1/3)

Pin name	Number of pins	I/O	Functions
P00 to P07	8	I/O	port0: I/O ports
P10 to P17	8	I/O	port1: I/O ports
P20 to P27	8	I/O	port2: I/O ports
P40 to P47	8	Input	port4: Input ports
AIN2 to AIN9		Input	Analog input: Input to AD converter
P50	1	I/O	Port50: I/O port (schmitt input)
INT4		Input	External Interrupt request input 4: Rising edge/Falling edge programable
TI3		Input	16-bit timer3 (TC3) Input 3
TI5		Input	16-bit timer5 (TC5) input 5
SI		Input	SIO received data
P51	1	I/O	Port51: I/O port (schmitt input)
INT3		Input	External Interrupt request input 3: Rising edge/Falling edge programable
TI2		Input	16-bit timer2 (TC2): Input 2
TI4		Input	16-bit timer4(TC4): input 4
SO		Output	SIO sending data
P52	1	I/O	Port52: I/O port (schmitt input)
INT2		Input	External Interrupt request input 2: Rising edge/Falling edge programable
TI1		Input	16-bit timer1 (TC1) Input 1
TI0		Input	8-bit Timer0 (TC0) Input 0
SCK		I/O	SIO clock line
P53	1	I/O	Port53: I/O port (schmitt input)
INT1		Input	External Interrupt request pin1: Rising edge/Level programable
P54	1	I/O	Port54: I/O port (schmitt input)
INT0		Input	External Interrupt request pin0: Rising edge/Falling edge programable
P73	1	I/O	Port73: I/O port (schmitt input, Push-pull or open-drain output selectables)
SDA0		I/O	I^2C bus SDA0 line
P74	1	I/O	Port74: I/O port (schmitt input, Push-pull or open-drain output selectable)
SCL0		I/O	I^2C bus SCL0 line
P75	1	I/O	Port75: I/O port (schmitt input, Push-pull or open-drain output selectable)
SDA1		I/O	I^2C bus SDA1 line
AIN0		Input	Analog input 0: Analog input signal for AD converter
P76	1	I/O	Port76: Input port (schmitt input, Push-pull or open-drain output selectable)
SCL1		I/O	I^2C bus SCL1 line
AIN1		Input	Analog input 1: Analog input signal for AD converter
P80	1	I/O	Port80: I/O port (schmitt input)
CTLIN		Input	CTL Capture input (Capture 0)
P81	1	I/O	Port81: I/O port (schmitt input)
DFGIN		Input	DFG Capture input (Capture 1)

Table 2.2.1 Pin names and function (2/3)

Pin name	Number of pins	I/O	Functions
P82	1	I/O	Port82: I/O port (schmitt input)
RMTIN		Input	Remote Control Signal Capture input
P83	1	I/O	Port83: I/O port (schmitt input)
EXT		Input	External Capture input (Capture 0)
TO1		Output	Timer Out 1
P84	1	I/O	Port84: I/O port (schmitt input)
DPGIN		Input	DPG Capture input (Capture 0)
P85	1	I/O	Port85: I/O port (schmitt input)
CFGIN		Input	CFG Capture input (Capture 2)
P86	1	I/O	Port86: I/O port (schmitt input)
CSYNCIN		Input	C.sync Capture input
P87	1	I/O	Port87: I/O port (schmitt input)
COMPIN		Input	Envelope Comparate Input (to HA/CR)
P90	1	I/O	Port90: I/O port (Push-pull or open-drain output selectable)
TP0		Output	Timing Pulse output 0
TPG00		Output	TPG00: TPG0 output
P91	1	I/O	Port91: I/O port (Push-pull or open-drain output selectable)
VASWP		Output	Video/Audio head switching control signal output
TPG01		Output	TPG01: TPG0 output
P92	1	I/O	Port92: I/O port (Push-pull or open-drain output selectable)
TP1		Output	Timing Pulse output 1
P93	1	I/O	Port93: I/O port (Push-pull or open-drain output selectable)
TPG03		Output	TPG03: TPG0 output
P94	1	I/O	Port94: I/O port (Push-pull or open-drain output selectable)
CR		Output	Color Rotary Output
P95	1	I/O	Port95: I/O port (Push-pull or open-drain output selectable)
HA		Output	Head Amp Switching Control Output
P96	1	I/O	Port96: I/O port (Push-pull or open-drain output selectable)
TO1		Output	Timer Out 1
TPG10		Output	TPG10: TPG1 output
P97	1	I/O	Port97: I/O port (Push-pull or open-drain output selectable)
TPG11		Output	TPG11: TPG1 output
PA0	1	I/O	PortA0: I/O port
PVPH		Output	PVPH 3-state Output
PWM3		Output	PWM(8 bits) output 3
PA3	1	I/O	PortA3: I/O port (Push-pull or open-drain output selectable)
PWM2		Output	PWM(14 bits) output 2

Table 2.2.1 Pin names and function (3/3)

Pin name	Number of pins	I/O	Functions
PWM0	1	Output	PWM(14 bits) output 0 (Push-pull or open-drain output selectable)
PWM1	1	Output	PWM(14 bits) output 1 (Push-pull or open-drain output selectable)
PB0 XT1	1	I/O Input	PortB0: I/O port (Open-drain Output) Low Frequency Oscillator connecting pin
PB1 XT2	1	I/O Output	PortB1: I/O port (Open-drain Output) Low Frequency Oscillator connecting pin
PC0 to PC7 G0 to G7	8	Output Output	PortC: Output (High break down voltage outputs with pull-down resistor) Grid Drivers
PD0,1 G8, 9	2	Output Output	PortD: Output (High break down voltage outputs with pull-down resistor) Grid Driver
PE0 to PE7 S0 to S7	8	I/O Output	PortE: I/O ports (High break down voltage outputs with pull-down resistor) Segment Driver
PF0 to PF5 S8 to S13	6	I/O Output	PortF: I/O ports (High break down voltage outputs with pull-down resistor) Segment Driver
TEST1	1	Output	TEST1 should be connected with TEST2 pin.
TEST2	1	Input	
TEST3	1	Output	TEST3 (NC) should be open connection.
CLK	1	Output	Clock output: Output (System Clock ÷ 2) clock. Pulled-up during reset. Can be set to output disable for reducing noise.(Initial Disable)
$\overline{\text{TEST}}$	1	Input	Test pin: Always set to “Vcc” level
$\overline{\text{RESET}}$	1	Input	Reset: Initializes LSI. (with pull-up resistor)
X1	1	Input	High Frequency Oscillator connecting pins (16 MHz)
X2	1	Output	High Frequency Oscillator connecting pins (16 MHz)
VKK	1		VFT Driver power supply pin
DVCC	1		Power supply pin
DGND	1		GND pin (0 V)
ADREF	1		Reference Voltage input for AD converter
ADGND	1		GND pin for AD converter

(2) PROM mode

Table 2.2.2 shows pin function of the TMP93PF76F in PROM mode.

Table 2.2.2 Pin name and function of PROM mode

Pin Function	Number of Pins	I/O	Function	Pin Name (MCU mode)
A7 to A0	8	Input	PROM address input	P27 to P20
A15 to A8	8	Input		P17 to P10
A16	1	Input		PA0
A17	1	Input		P92
A18	1	Input		PA3
D7 to D0	8	I/O	PROM data input/output	P07 to P00
$\overline{CE}$	1	Input	Chip enable	P93
$\overline{OE}$	1	Input	Output control	P91
VPP	1	Power supply	12.5 V/5 V (Program power supply voltage)	$\overline{TEST}$
VCC	1	Power supply	6.25 V/5 V	VCC
VSS	2	Power supply	0 V	DGNG, ADGND

Pin Function	Number of Pins	I/O	Treatment of Pin
P90	1	Input	Fix to low level (security pin)
$\overline{RESET}$	1	Input	Fix to low level (PROM mode)
CLK	1	Input	
TEST3	1	Output	Open
X1	1	Input	Self oscillation with resonator
X2	1	Output	
P76, P75, P97 to P94	6	I/O	Fix to high level
TEST1 / TEST2	2	Output / Input	Short
P47 to P40 P54 to P50 P74, P73 P87 to P80 PB1, PB0 PC7 to PC0 PD1, PD0 PE7 to PE0 PF5 to PF0 PWM0 PWM1 ADREF VKK	53	I/O	Open

3. Operation

This section describes the functions and basic operational blocks of the TMP93PF76F.

The TMP93PF76F has PROM in place of the mask ROM which is included in the TMP93CW76. The other configuration and functions are the same as the TMP93CF76/77F. Regarding the function of the TMP93PF76F (not described), see the part of TMP93CF76/77F.

The TMP93PF76F has two operational modes : MCU mode and PROM mode.

3.1 MCU Mode

(1) Mode-setting and function

The MCU mode is set by opening the CLK pin (pin open). In the MCU mode, the operation is same as TMP93CF76/77F.

(2) Memory-map

The memory map of TMP93PF76F is same as that of TMP93CF76F. Figure 3.1.1 shows the memory map in MCU mode. Figure 3.1.2 show that in PROM mode.

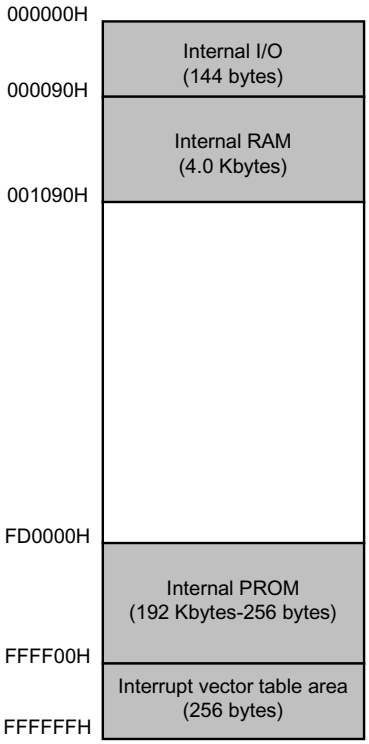


Figure 3.1.1 Memory map in MCU mode

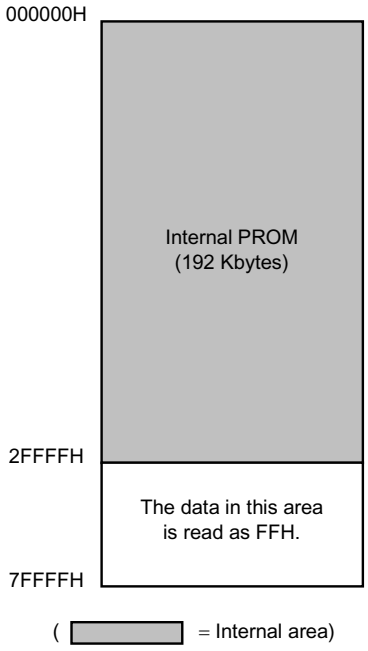


Figure 3.1.2 Memory map in PROM mode

ROM areas of TMP93CF76/77F are shown in Table 3.1.1. When TMP93PF76F is used as the evaluation-chip for TMP93CF77, the programmable area located address 00000H to 07FFFH should be full of data FFH.

Table 3.1.1 Memory of TMP93CF76/77

Product No.	ROM Area	
	MCU Mode	PROM Mode
TMP93CF76	FD0000H to FFFFFFH	00000H to 2FFFFH
TMP93CF77	FD8000H to FFFFFFH	08000H to 2FFFFH

4. Electrical Characteristics

4.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Power Supply Voltage	Vcc	−0.5 to 6.5	V
Input Voltage	V_{IN}	−0.5 to Vcc + 0.5	
Output Voltage (except PC, PD, PE, PF)	V_{OUT1}	−0.5 to Vcc + 0.5	
Output Voltage (PC, PD, PE, PF)	V_{OUT2}	Vcc−40	
Output Current (except PC, PD, PE, PF) (per 1 pin)	I_{OH1}	−3.2	mA
Output Current (PC, PD) (per 1 pin)	I_{OH2}	−25	
Output Current (PE, PF) (per 1 pin)	I_{OH3}	−15	
Output Current (per 1 pin)	I_{OL}	3.2	
Output Current (total except PC, PD, PE, PF)	ΣI_{OH1}	−40	
Output Current (total of PC, PD, PE, PF)	ΣI_{OH2}	−120	
Output Current (total)	ΣI_{OL}	120	
Power Dissipation (Ta = 70°C)	PD	600	mW
Soldering Temperature	Tsolder	260	°C
Storage Temperature	Tstg	−65 to 150	
Operating Temperrature	Topr	−20 to 70	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics

Ta = −20 to 70°C

Parameter		Symbol	Condition	Min	Typ.	Max	Unit
Power Supply Voltage		Vcc	fc = 4 to 16 MHz	4.5		5.5	V
			fs = 30 to 34 kHz	2.7			
Input Low Voltage	P0, P1, P2, P4, P9, PA, PB, PE, PF	V_{IL1} (CMOS)	Vcc = 2.7 to 5.5 V	−0.3		0.3 Vcc	
	$\overline{RESET}$, P5, P7, P8	V_{IL2} (Schmitt)				0.25 Vcc	
	$\overline{TEST}$	V_{IL3} (Fixed)				0.3	
	X1	V_{IL4} (Xtal)				0.2 Vcc	
Input High Voltage	P0, P1, P2, P4, P9, PA, PB, PE, PF	V_{IL1} (CMOS)		0.7 Vcc		Vcc + 0.3	
	$\overline{RESET}$, P5, P7, P8	V_{IH2} (Schmitt)		0.75 Vcc			
	$\overline{TEST}$	V_{IH3} (Fixed)		Vcc − 0.3			
	X1	V_{IH4} (Xtal)		0.8 Vcc			
Output Low Voltage		V_{OL}	IOL = 1.6 mA (Vcc = 2.7 to 5.5 V)			0.45	V
Output High Voltage		V_{OH}	IOH = −400 μA (Vcc = 2.7 to 5.5 V)	2.4			V
		V_{OH1}	IOH = −700 μA (Vcc = 4.5 to 5.5 V)	4.1			
PE, PF		I_{OH}	Vcc = 4.5 V VOH = 2.4 V	−5			mA
PC, PD				−15			
Input Leakage Current		I_{LI}	0.0 ≦ Vin ≦ Vcc		0.02	±5	μA
Output Leakage Current		I_{LO}	0.2 ≦ Vin ≦ Vcc-0.2		0.05	±10	
Power Down Voltage		V_{STOP}	VIL2 = 0.2 Vcc, VIH2 = 0.8 Vcc	2.0		6.0	V
$\overline{RESET}$ Pull Up Resistor		R_{RST}	Vcc = 5 V ± 10%	50		150	kΩ
			Vcc = 3 V ± 10%	80		200	
Pin Capacitance		C_{IO}	osc = 1 MHz/100 mVp-p			10	pF
Schmitt Width $\overline{RESET}$, P5, P7, P8		V_{TH}			1.0		V
NORMAL		Icc	Vcc = 5 V ± 10% fc = 16 MHz		30	50	mA
RUN					18	28	
IDLE2					15	25	
IDLE1					5	8	
SLOW			Vcc = 3 V ± 10% fs = 32.768 kHz (typ: V_{CC} = 3.0 V)		50	80	μA
RUN					30	45	
IDLE2					25	40	
IDLE1					6	15	
STOP			Vcc = 2.7 to 5.5 V		0.2	10	

Note 1: Typical value are for Ta = 25°C and Vcc = 5 V unless otherwise noted.

Note 2: Icc measurement conditions (NORMAL, SLOW).
Only CPU is operational;output pins are open and input pins are fixed.

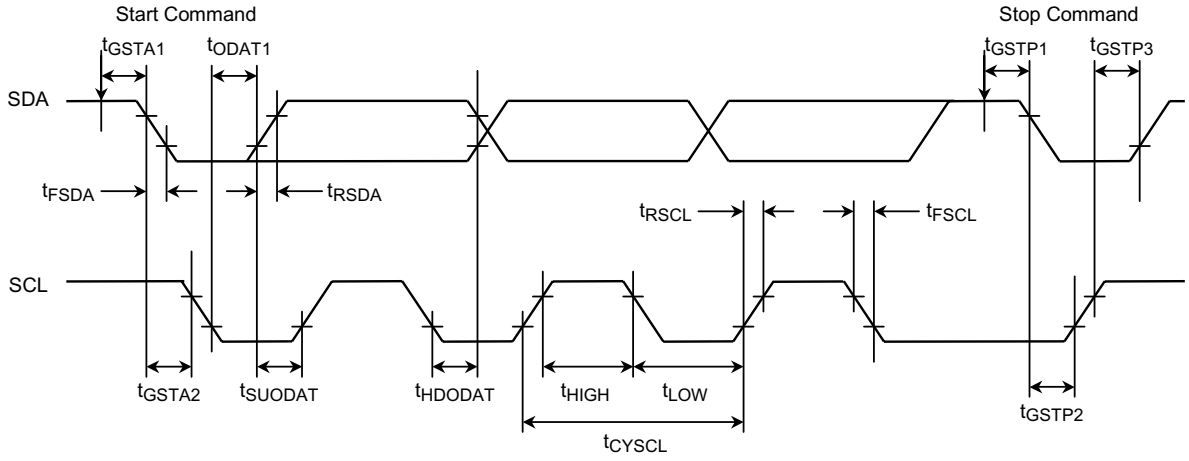
4.3 AD Conversion Characteristics

Ta = −20 to 70°C, Vcc = 4.5 to 5.5 V

Parameter	Symbol	Min	Typ.	Max	Unit
Analog Reference Voltage Supply	ADREF	Vcc-1.5	Vcc	Vcc	V
	ADGND	Vss	Vss	Vss	V
Analog Input Voltage Range	VAIN	ADGND	—	ADREF	V
Analog Current for ADREF	IREF	—	1.0	1.5	mA
Total tolerance (excludes quantization error) (Ta = 25°C, Vcc = ADREF = 5 V)	E_T	—	—	±3	LSB

4.4 Serial BUS Interface Timing

(1) I^2C bus Logic Timing



Parameter		Symbol	Min	Typ.	Max	Unit
SCL cycle		t_{CYCSCL}	2^N/fc	—	—	s
SCL low pulse width		t_{LOW}	—	2^{N-1}/fc	—	s
SCL High pulse width		t_{HIGH}	2^{N-1}/fc	—	—	s
SDA Rising Time	(Note 1)	t_{RSDA}	—	—	—	s
SDA Falling Time	(Note 1)	t_{FSDA}	—	—	—	s
SCL Rising Time	(Note 1)	t_{RSCL}	—	—		s
SCL Falling Time	(Note 1)	t_{FSCL}	—	—		s
The time from start command write to start sheecense		t_{GSTA1}	—	—	2^N/fc	s
Start condition hold time, start generation of the first clock after this		t_{GSTA2}	—	2^{N-1}/fc		s
Delay time from SCL falling to data output	(Note 2)	t_{ODAT1}	—	—	5/fc	s
Set up time of data output for SCL rising	(Note 2)	t_{SUODAT}	0	—	—	s
The time of holding data for SCL rising	(Note 3)	t_{HODAT}	4/fc	—	—	s
The time from stop command write to starting stop sheecense		t_{GSTP1}	—	—	2^{N-1}/fc	s
The time from SDA falling to SCL rising (during stop sheecense)		t_{GSTP2}	2^{N-2}/fc	—	—	s
Stop condition set up time		t_{GSTP3}	2^{N-1}/fc	—	—	s

Note 1: The time of rising/falling depend on the feature of bus interface.

Note 2: The worst case is at the first bit of slave address.

Note 3: The worst case is at the acknowledge bit.

Note 4: N: Diving value set by I2CCR1 <SCK 2:0>

SCK	N
000	6
001	7
010	8
011	9
100	10
101	11
110	12
111	reserved

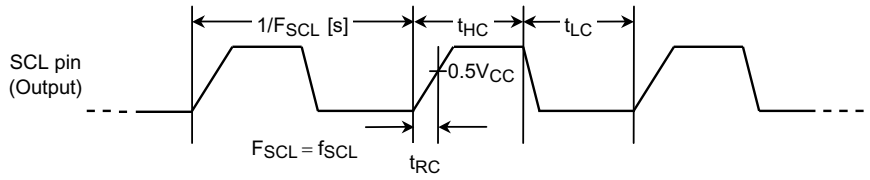
(2) Master SCL output timing

The I2CCR1 <SCK 2:0> are used to select a maximum transfer frequency directed from the SCL pin in the master mode. When rising time of the output clock (t_{RC}) is at least 8/fc [s], a high-level time of the output clock (t_{HC}) is t_{SCL}.

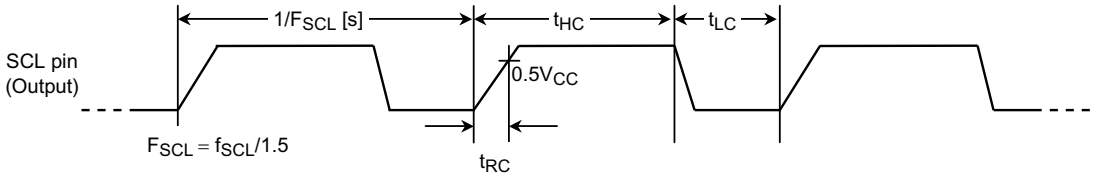
While the SCL line is fixed to low-level by a slave device, the output clock stops.

The first clock (t_{HC} [s]) after restart is ($t_{SCL}/2$) ≤ t_{HC} ≤ t_{SCL}.

(a) In case of t_{RC}< (8/fc) [s] $t_{HC} = t_{LC} = t_{SCL}/2$ [s] ($t_{SCL} = 1/f_{SCL}$ [s])



(b) In case of $t_{RC} \geq$ (8/fc) [s] $t_{HC} = t_{SCL}$ [s], $t_{LC} = t_{SCL}/2$ [s]



(3) Clock Syncro 8 bit SIO mode

a. SCK Input mode

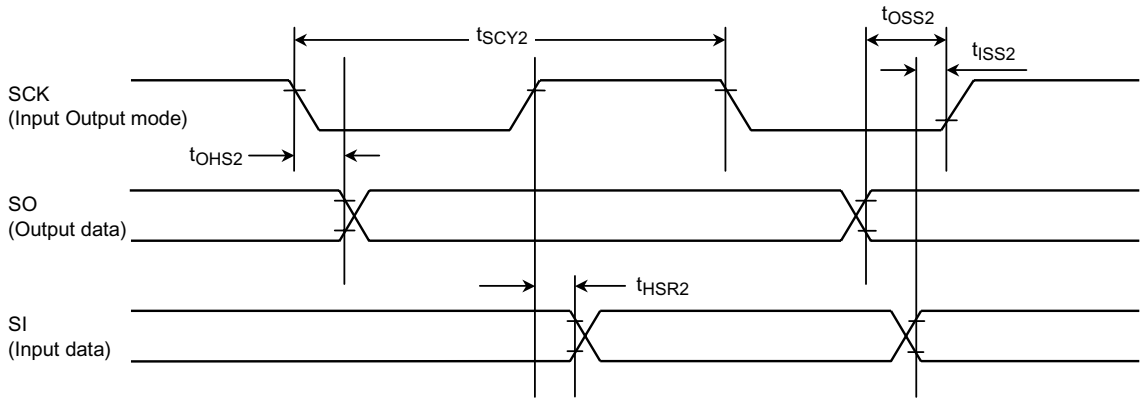
Parameter	Symbol	Expression		Unit
		Min	Max	
SCK cycle	t_{SCY2}	2^5X		s
SCK falling → Latch output data	t_{OHS2}	6X		s
Enable output data → SCK raising	t_{OSS2}		$t_{SCY2} - 16X$	s
SCK raising → Latch input data	t_{HSR2}	6X		ns
Enable input data → SCK raising	t_{ISS2}	0		ns

Note: X = 1/fc

b. SCK Output mode

Parameter	Symbol	Expression		Unit
		Min	Max	
SCK cycle	t_{SCY2}	2^5X	$2^{11}X$	s
SCK falling → Latch output data	t_{OHS2}	2X		s
Enable output data → SCK raising	t_{OSS2}		$t_{SCY2} - 2X$	s
SCK raising → Latch input data	t_{HSR2}	2X		s
Enable input data → SCK raising	t_{ISS2}	0		ns

Note: X = 1/fc



4.5 Read operation in PROM mode

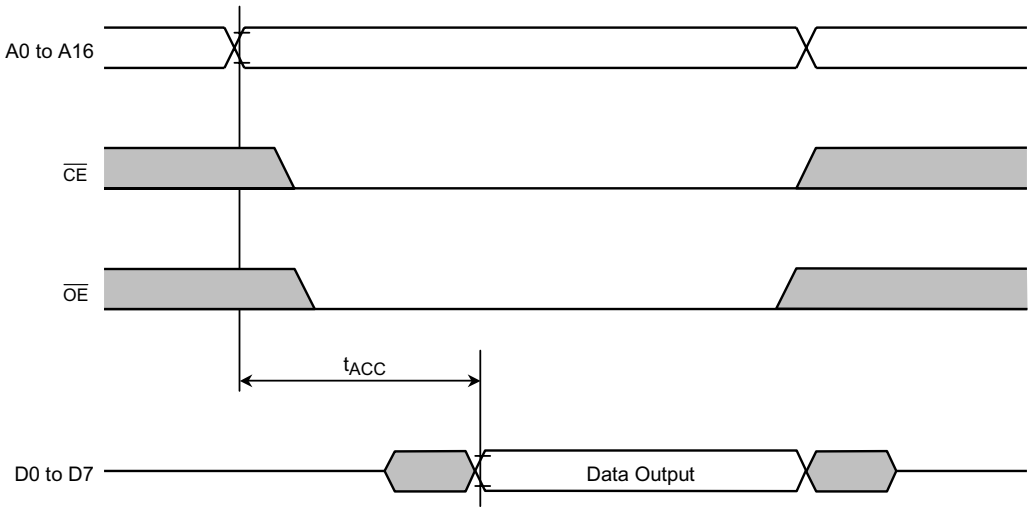
DC/AC characteristics

Ta = 25 + 5°C Vcc = 5 V ± 10 %

Parameter	Symbol	Condition	Min	Max	Unit
V_{PP} Read Voltage	V_{PP}	–	4.5	5.5	V
Input High Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IH1}	–	2.2	VCC + 0.3	V
Input low Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IL1}	–	–0.3	0.8	V
Address to Output Delay	t_{ACC}	CL = 50 pF	–	$2.25T_{CYC} + \alpha$	ns

T_{CYC} = 400 ns (10 MHz Clock)

α = 200 ns

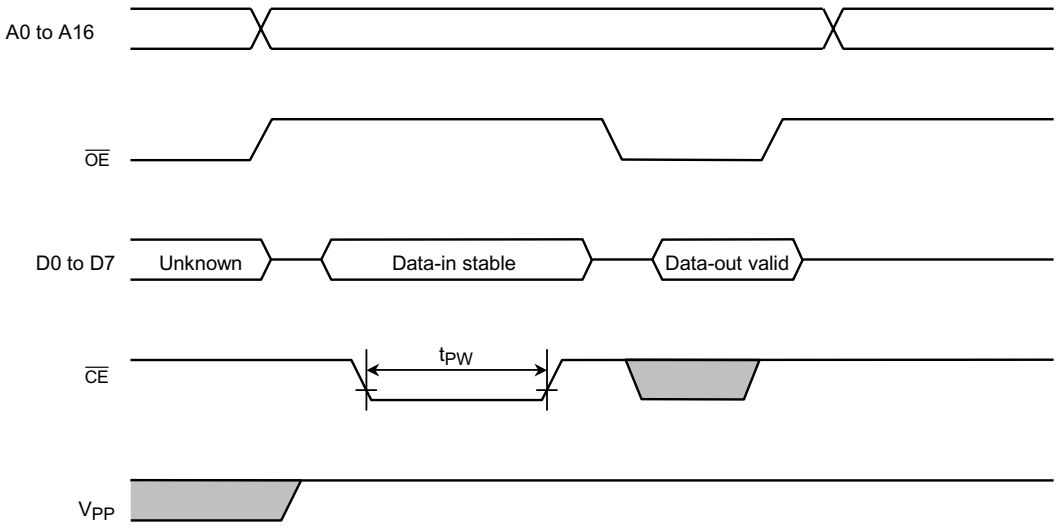


4.6 Program Operation in PROM Mode

DC/AC characteristics

Ta = 25 + 5°C Vcc = 6.25 V ± 0.25 %

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Programming Supply Voltage	V_{PP}	–	12.2	12.5	12.8	V
Input High Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IH1}	–	2.2		V_{PP} + 1.0	V
Input low Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IL1}	–	−0.3		0.8	V
V_{CC} Supply Current	I_{CC}	fc = 10 MHz	–		50	mA
V_{PP} Supply Current	I_{PP}	V_{PP} = 13.00 V	–		50	mA
$\overline{PGM}$ Program Pulse Width	PW	C_L = 50 pF	45	50	55	μs



Note 1: The power supply of Vpp (12.5 V) must be set power-on at the same time or the later time for a power supply of Vcc and must be clear power-on at the same time or early time for a power supply of Vcc.

Note 2: The pulling up/down device on condition of Vpp = 12.5 suffers a damage for the device.

Note 3: The maximum spec of Vpp pin is 14.0 V. Be carefull of a overshoot at the programming.