Low-power CMOS

16-Bit Microcontroller

TMP93PW44ADF

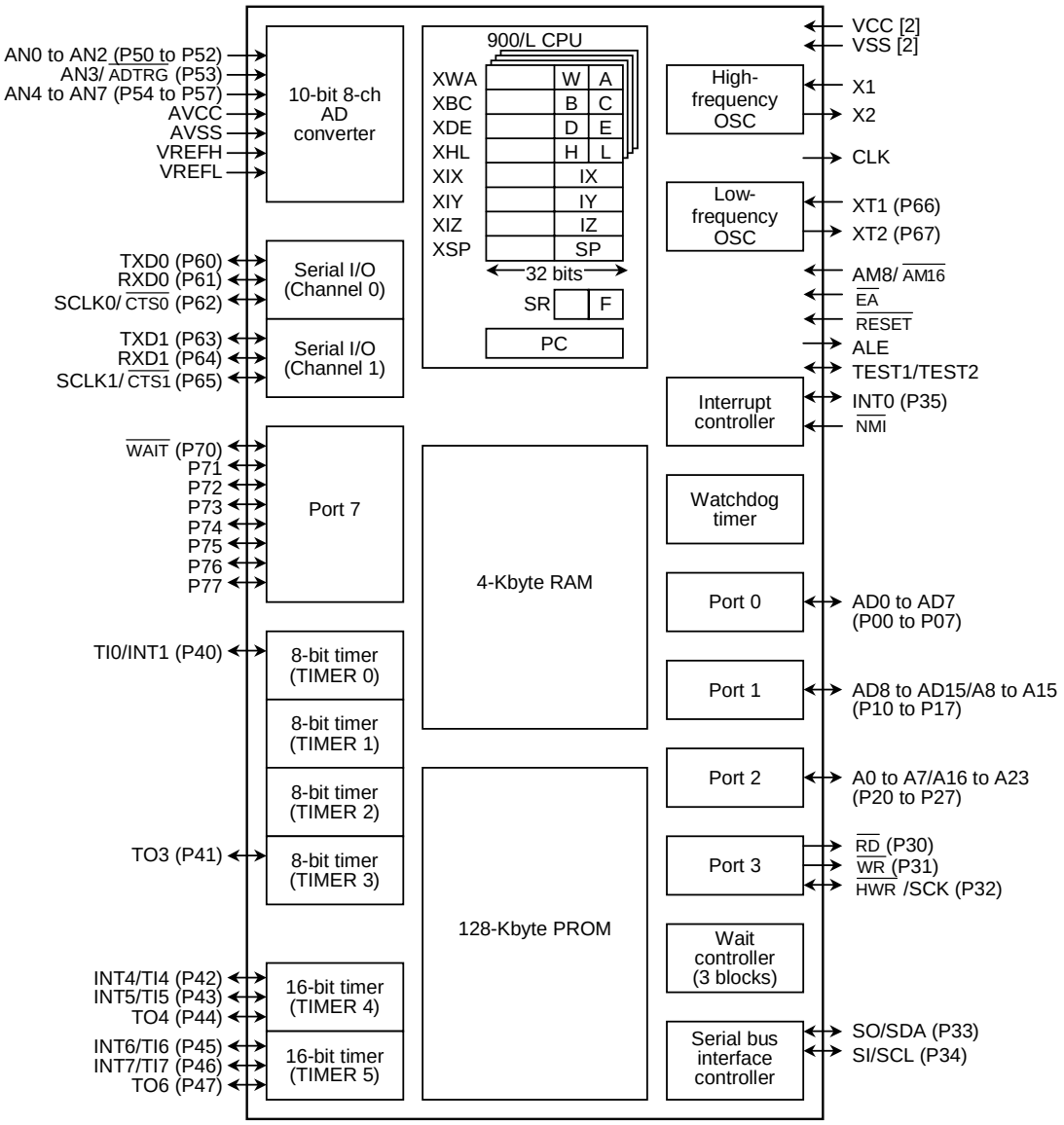
1. Outline and Device Characteristics

The TMP93PW44A is OTP type MCU which includes 128-Kbyte one-time PROM. Using the adapter socket, you can write and verify the data for the TMP93PW44A. The TMP93PW44ADF has the same pin assignment as TMP93CW44 (Mask ROM type).

Writing the program to built-in PROM, the TMP93PW44A operates as the same way as the TMP93CW44.

Note: The operation voltage of TMP93PW44A is V_{CC} = 4.5 to 5.5 V though the operation voltage of TMP93CS44/45, TMP93PS44, TMP93CU44 and TMP93CW44 is V_{CC} = 2.7 to 5.5 V. Especially, be careful when TMP93CU44, TMP93CW44 and TMP93PW44A are used. Please refer to the fourth chapter electric characteristic of each product for details.

MCU	ROM	RAM	Package	Adapter Socket
TMP93PW44ADF	OTP 128 Kbytes	4 Kbytes	P-QFP80-1420-0.80B	BM11152



Note: The items in parentheses ( ) are the initial setting after reset.

Figure 1.1 TMP93PW44A Block Diagram

2. Pin Assignment and Functions

The assignment of input/output pins for the TMP93PW44A, their names and outline functions are described below.

2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of the TMP93PW44ADF.

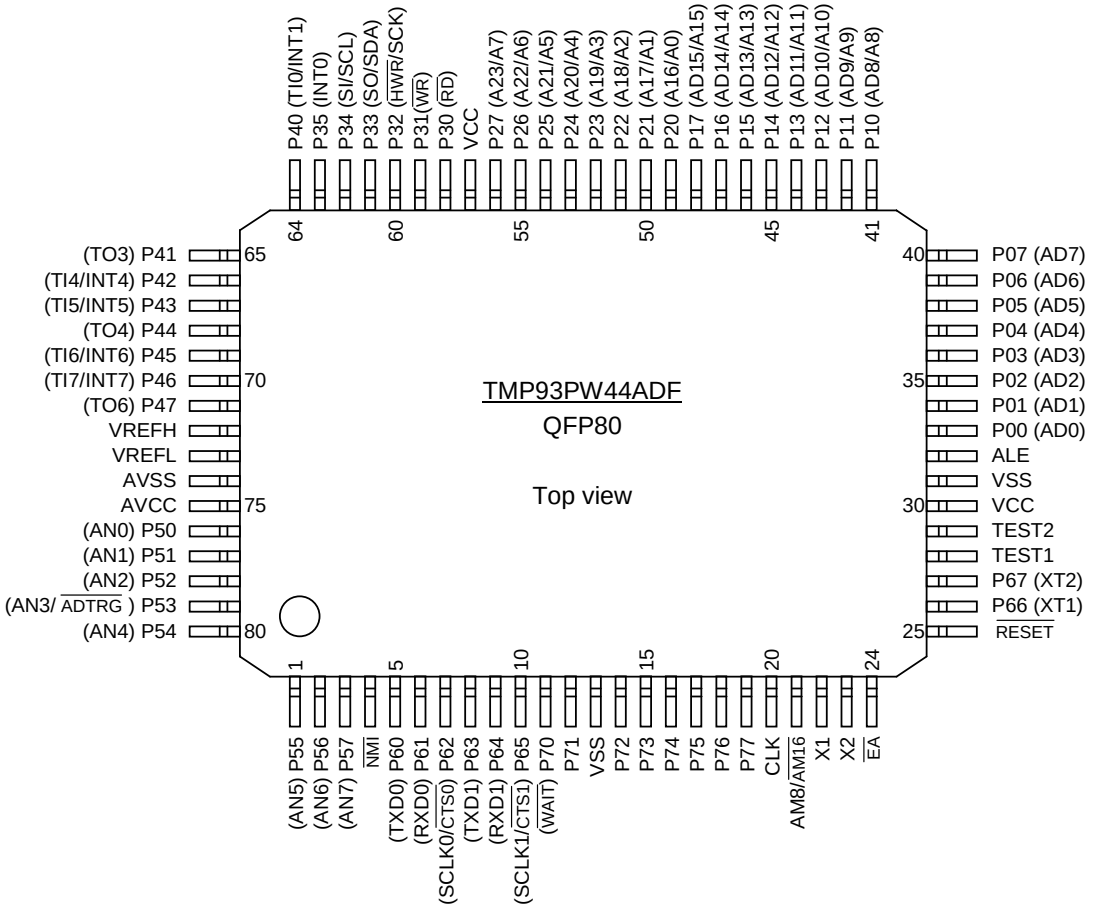


Figure 2.1.1 Pin Assignment (P-QFP80-1420-0.80B)

2.2 Pin Names and Functions

The TMP93PW44A has MCU mode and PROM mode.

(1) Table 2.2.1 shows pin function of TMP93PW44A in MCU mode.

Table 2.2.1 Pin Names and Functions (1/3)

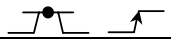
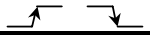
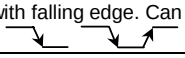
Pin Name	Number of Pins	I/O	Functions
P00 to P07	8	I/O	Port 0: I/O port that allows selection of I/O on a bit basis
AD0 to AD7		3-state	Address/data (Lower): Bits 0 to 7 for address/data bus
P10 to P17	8	I/O	Port 1: I/O port that allows selection of I/O on a bit basis
AD8 to AD15		3-state	Address/data (Upper): Bits 8 to 15 for address/data bus
A8 to A15		Output	Address: Bits 8 to 15 for address bus
P20 to P27	8	I/O	Port 2: I/O port that allows selection of I/O on a bit basis (with pull-up resistor)
A0 to A7		Output	Address: Bits 0 to 7 for address bus
A16 to A23		Output	Address: Bits 16 to 23 for address bus
P30	1	Output	Port 30: Output port
$\overline{RD}$		Output	Read: Strobe signal for reading external memory
P31	1	Output	Port 31: Output port
$\overline{WR}$		Output	Write: Strobe signal for writing data on pins AD0 to AD7
P32	1	I/O	Port 32: I/O port (with pull-up resistor)
$\overline{HWR}$		Output	High write: Strobe signal for writing data on pins AD8 to AD15
SCK		I/O	Mode clock SBI SIO mode clock
P33	1	I/O	Port 33: I/O port
SO		Output	Serial send data
SDA		I/O	SBI I^2C bus mode channel data
P34	1	I/O	Port 34: I/O port
SI		Input	Serial receive data
SCL		I/O	SBI I^2C bus mode clock
P35	1	I/O	Port 35: I/O port
INT0		Input	Interrupt request pin 0: Interrupt request pin with programmable level/rising edge 
P40	1	I/O	Port 40: I/O port
TI0		Input	Timer input 0: Timer 0 input
INT1		Input	Interrupt request pin 1: Interrupt request pin with rising edge 
P41	1	I/O	Port 41: I/O port
TO3		Output	PWM output 3: 8-bit PWM timer 3 output
P42	1	I/O	Port 42: I/O port
TI4		Input	Timer input 4: Timer 4 count/capture trigger signal input
INT4		Input	Interrupt request pin 4: Interrupt request pin with programmable rising/falling edge 

Table 2.2.2 Pin Names and Functions (2/3)

Pin Name	Number of Pins	I/O	Functions
P43	1	I/O	Port 43: I/O port
TI5		Input	Timer input 5: Timer 4 count/capture trigger signal input
INT5		Input	Interrupt request pin 5: Interrupt request pin with rising edge
P44	1	I/O	Port 44: I/O port
TO4		Output	Timer output 4: Timer 4 output pin
P45	1	I/O	Port 45: I/O port
TI6		Input	Timer input 6: Timer 5 count/capture trigger signal input
INT6		Input	Interrupt request pin 6: Interrupt request pin with programmable rising/falling edge
P46	1	I/O	Port 46: I/O port
TI7		Input	Timer input 7: Timer 5 count/capture trigger signal input
INT7		Input	Interrupt request pin 7: Interrupt request pin with rising edge
P47	1	I/O	Port 47: I/O port
TO6		Output	Timer output 6: Timer 5 output pin
P50 to P52, P54 to P57	7	Input	Port 50 to 52, port 54 to 57: Input port
AN0 to AN2, AN4 to AN7		Input	Analog input: Analog signal input for AD converter
P53	1	Input	Port 53: Input port
AN3		Input	Analog input: Analog signal input for AD converter
$\overline{\text{ADTRG}}$		Input	AD converter external start trigger input
P60	1	I/O	Port 60: I/O port (with pull-up resistor)
TXD0		Output	Serial send data 0
P61	1	I/O	Port 61: I/O port (with pull-up resistor)
RXD0		Input	Serial receive data 0
P62	1	I/O	Port 62: I/O port (with pull-up resistor)
$\overline{\text{CTS0}}$		Input	Serial data send enable 0 (Clear to send)
SCLK0		I/O	Serial clock I/O 0
P63	1	I/O	Port 63: I/O port (with pull-up resistor)
TXD1		Output	Serial send data 1
P64	1	I/O	Port 64: I/O port (with pull-up resistor)
RXD1		Input	Serial receive data 1
P65	1	I/O	Port 65: I/O port (with pull-up resistor)
SCLK1		I/O	Serial clock I/O 1
$\overline{\text{CTS1}}$		Input	Serial data send enable 1 (Clear to send)
P66	1	I/O	Port 66: I/O port (Open-drain output)
XT1		Input	Low-frequency oscillator connecting pin
P67	1	I/O	Port 67: I/O port (Open-drain output)
XT2		Output	Low-frequency oscillator connecting pin

Table 2.2.3 Pin Names and Functions (3/3)

Pin Name	Number of Pins	I/O	Functions
P70	1	I/O	Port 70: I/O port (High current output available)
$\overline{WAIT}$		Input	WAIT: Pin used to request CPU bus wait. (It is active in (1 + N) WAIT mode. Set by the bus-width/wait control register.)
P71 to P77	7	I/O	Port 71 to 77: I/O port (High current output available)
AVCC	1	Input	Power supply pin for AD converter
AVSS	1	Input	GND pin for AD converter (0 V)
VREFH	1	Input	Pin for high level reference voltage input to AD converter
VREFL	1	Input	Pin for low level reference voltage input to AD converter
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at falling and rising edges by program. 
X1	1	Input	High-frequency oscillator connecting pin
X2	1	Output	High-frequency oscillator connecting pin
$\overline{RESET}$	1	Input	Reset: Initializes TMP93PW44A (with pull-up resistor).
ALE	1	Output	Address latch enable Can be disabled for reducing noise.
CLK	1	Output	Clock output: Outputs "$f_{SYS} \div 2$" clock. Pulled-up during reset. Can be disabled for reducing noise.
$\overline{EA}$	1	Input	External access: "1" should be inputted
AM8/ $\overline{AM16}$	1	Input	Address mode: Selects external data bus width. "1" should be inputted. The data bus width for external access is set by chip select/WAIT control register, port 1 control register.
VCC	2	Input	Power supply pin
VSS	2	Input	GND pin (All VSS pins are connected to the GND (0 V)).
TEST1/TEST2	2	Output/Input	TEST1 should be connected with TEST2 pin. Do not connect to any other pins.

Note: Built-in pull-up resistors can be released from the pins other than the $\overline{RESET}$ pin by software.

(2) PROM mode

Table 2.2.4 shows pin functions of the TMP93PW44A in PROM mode.

Table 2.2.4 Pin Names and Functions of PROM Mode

Pin Function	Number of Pins	Input/Output	Function	Pin Name (MCU Mode)
A7 to A0	8	Input	Memory address of program	P27 to P20
A15 to A8	8	Input		P17 to P10
A16	1	Input		P33
D7 to D0	8	I/O	Memory data of pfogram	P07 to P00
$\overline{CE}$	1	Input	Chip enable	P32
$\overline{OE}$	1	Input	Output control	P30
$\overline{PGM}$	1	Input	Program control	P31
VPP	1	Power supply	12.75 V/5 V (Power supply of program)	$\overline{EA}$
VCC	3	Power supply	6.25 V/5 V	VCC, AVCC
VSS	3	Power supply	0 V	VSS, AVSS

Pin Function	Number of Pins	Input/Output	Disposal of Pin
P60	1	Input	Fix to low level (Security pin)
$\overline{RESET}$	1	Input	Fix to low level (PROM mode)
CLK	1	Input	
ALE	1	Output	Open
X1	1	Input	Self oscillation with resonator
X2	1	Output	
P66 to P61 AM8/ $\overline{AM16}$	7	Input	Fix to high level
TEST1/TEST2	2	Input/Output	TEST1 should be connected with TEST2 pin. Do not connect to any other pins.
P35, P34 P47 to P40 P57 to P50 P67 P77 to P70 VREFH VREFL $\overline{NMI}$	30	I/O	Open

3. Operation

This section describes the functions and basic operational blocks of the TMP93PW44A.

The TMP93PW44A has PROM in place of the mask ROM which is included in the TMP93CW44. The other configuration and functions are the same as the TMP93CW44. Regarding the function of the TMP93PW44A (Not described), see the part of TMP93CW44.

The TMP93PW44A has two operational modes: MCU mode and PROM mode.

3.1 MCU mode

(1) Mode setting and function

The MCU mode is set by opening the CLK pin (Pin open). In the MCU mode, the operation is same as TMP93CW44.

(2) Memory map

The memory map of TMP93PW44A is same as that of TMP93CW44. Figure 3.1.1 shows the memory map in MCU mode. Figure 3.1.2 show that in PROM mode.

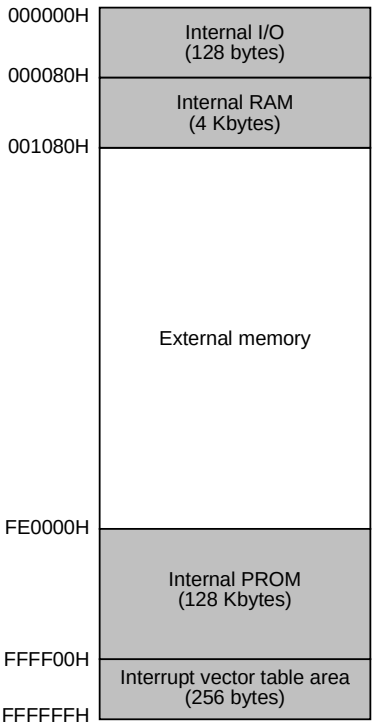


Figure 3.1.1 Memory Map in MCU Mode

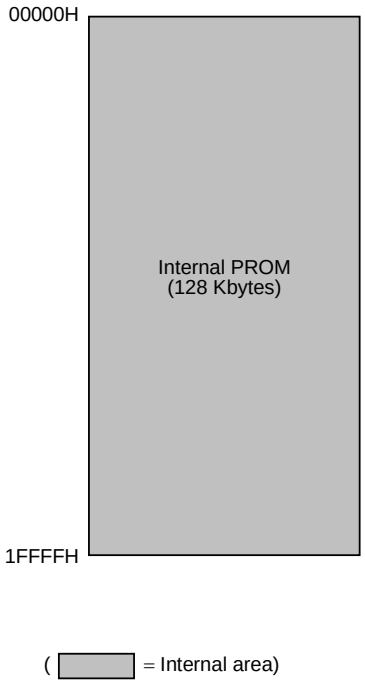


Figure 3.1.2 Memory Map in PROM Mode

3.2 PROM Mode

(1) Mode setting and function

PROM mode is set by setting the $\overline{\text{RESET}}$ and CLK pins to the "L" level. The programming and verification for the internal PROM is achieved by using a general EPROM programmer with the adaptor socket.

1. Preparation of OTP adaptor

   BM11152: for TMP93PW44ADF

2. Setting of OTP adaptor

   The switch (SW1) is set to N side.

3. Setting of PROM writer

   i) Set PROM type to TC 571000D.

      Size: 1 Mbits (128 K × 8 bits)

      VPP: 12.75 V

      t_{PW}: 100 μs

      Electric signature mode: None

   ii) Data transmittion

      In TMP93PW44A, PROM is placed on addresses 00000H to 1FFFFH in PROM mode, and addresses FE0000H to FFFFFFH in MCU mode. Therefore data should be transferred to addresses 00000H to 1FFFFH in PROM mode using the object converter (tuconv) or the block transfer mode (See instruction manual of PROM programmer.)

   iii) Setting of the program address

      Start address: 00000H

      End address: 1FFFFH

4. Programming

   Program and verify according to operating process of PROM programmer.

Figure 3.2.1 shows the setting of the pins in PROM mode.

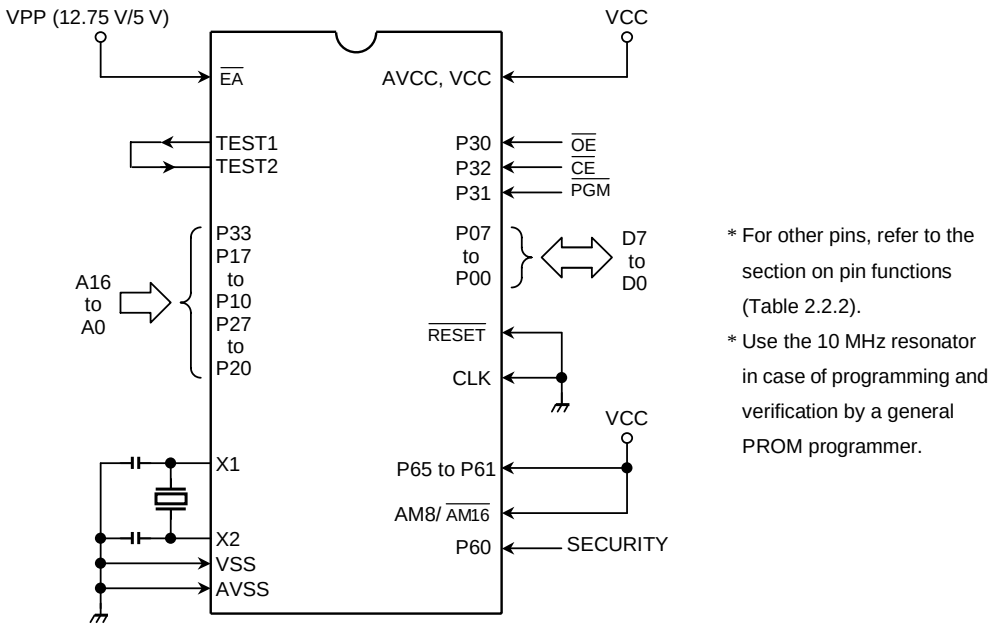


Figure 3.2.1 PROM Mode Pin Setting

(2) Caution for electric signature

The TMP93PW44A dose not support the electric signature mode (Hereinafter referred to as "signature"). If PROM programmer used the signature, the device would be damaged because of applying voltage of 12 ± 0.5 V to pin 9 (A9) of the address.

Please use without setting the signature.

(3) Program mode

All bits of the TMP93PW44A are "1" when delivered (The erase state). Data "0" is written in the necessary bit location during program operating.

Writing function can be operated at V_{PP} = 12.5 V, $\overline{OE}$ = V_{IH}, $\overline{CE}$ = V_{IL}. Built-in one time PROM can be written in any sequence. It is possible to write only special address.

(4) Adopter socket (BM11152: for TMP93PW44ADF)

BM11152 is the adapter sockets to write data into the TMP93PW44A. The TMP93PW44A has built-in one time PROM using a general EPROM programmer.

(5) Program storing area of PROM mode

The TMP93PW44A has the program space (FE0000H to FFFFFFH) of 128 Kbytes. The address 0000H to 1FFFFH of PROM mode equals to the address FE0000H to FFFFFFH of MCU mode.

(6) Program write setting method using a general PROM programmer

PROM to be prepared should equal to TC571000D functions.

1. Set the switch (SW1) of BM11152 (Hereinafter referred to as "adapter") to the program side (NOR) (Note 1).
2. Connect MCU to the adapter (Note 2).
3. Connect the adapter to PROM programmer (Note 2).
4. Set the PROM type of PROM programmer to TC571000D.
5. Set the start address for writing PROM to 0000H, and the end address to 1FFFFH (Note 3).
6. Writing to built-in one time PROM and verifying should be operated according to the operation procedures of PROM programmer.

Note 1: If data is written to built-in one time PROM without setting the switch (SW1) to the program side, the device would be damaged.

Note 2: Please set with the first pin of the adapter and that of PROM programmer socket matched. If the first pin is conversely set, MCU or programmer would be damaged.

Note 3: If data "0" is written to the address which is over 1FFFFH, the contents of the original program would be damaged because of writing "0" to the addresses 0000H to 1FFFFH.

(7) Programming flow chart

The programming mode is set by applying 12.75 V (Programming voltage) to the VPP pin when the following pins are set as follows,

(VCC: 6.25 V, $\overline{\text{RESET}}$: "L" level, CLK: "L" level).

While address and data are fixed and $\overline{\text{CE}}$ pin is set to "L" level, 0.1 ms of "L" level pulse is applied to $\overline{\text{PGM}}$ pin to program the data.

Then the data in the address is verified.

If the programmed data is incorrect, another 0.1 ms pulse is applied to $\overline{\text{PGM}}$ pin.

This programming procedure is repeated until correct data is read from the address (25 times maximum).

Subsequently, all data are programmed in all addresses.

The verification for all data is done under the condition of $V_{PP} = V_{CC} = 5$ V after all data were written.

Figure 3.2.2 shows the programming flowchart.

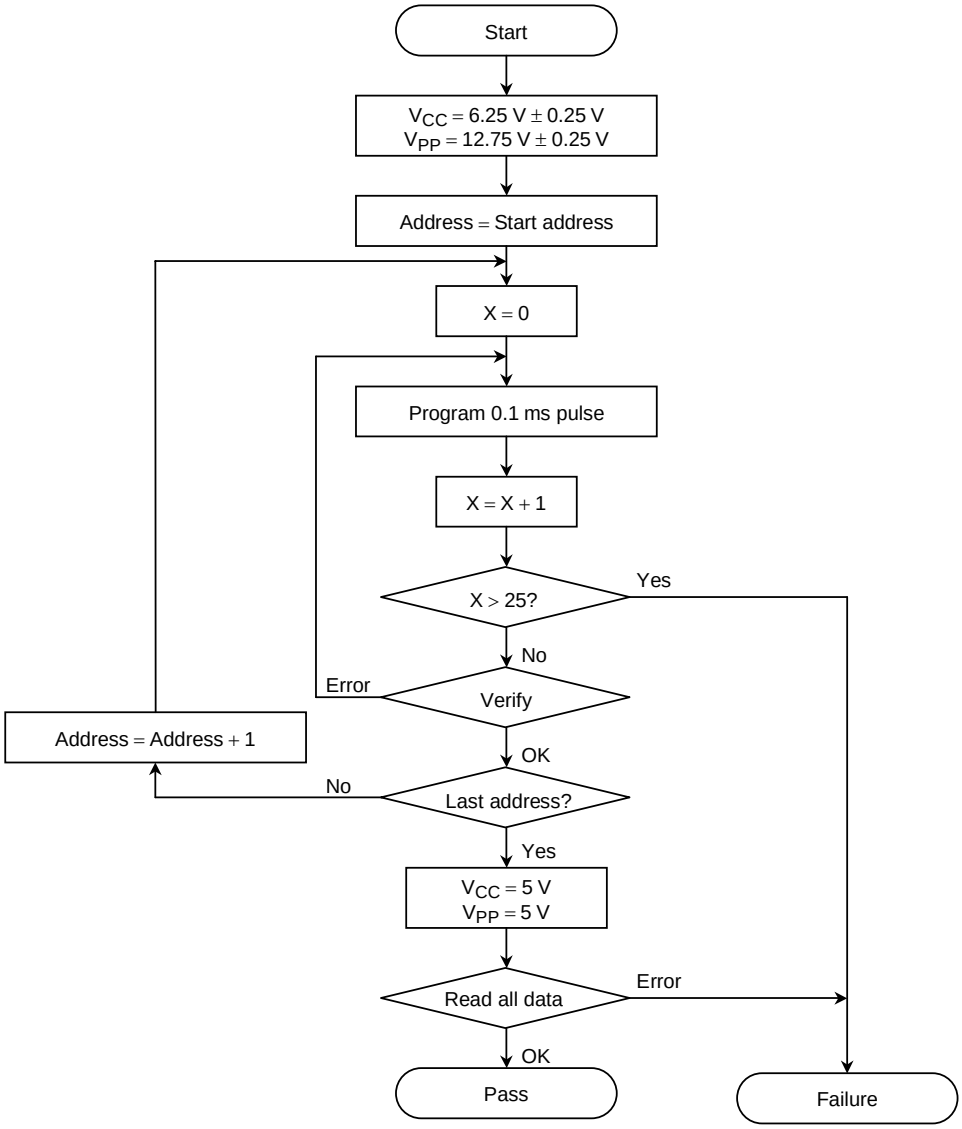


Figure 3.2.2 Flowchart (High-speed program writing)

(8) Security bit

The TMP93PW44A has a security bit in PROM cell.

If the security bit is programmed to "0", the content of the PROM is disable to be read (FFH data) in PROM mode.

(How to program the security bit)

The difference from the programming procedures described in section 3.2 (1) are as follows.

1. Setting OTP adaptor

   Set the switch (SW1) to S side.

2. Setting PROM programmer

   i) Transferring the data

   ii) Setting of programming address

   The security bit is in bit0 of address 00000H.

   Set the start address 00000H and the end address 00000H.

   Set the data FEH at the address 00000H.

4. Electrical Characteristics

"X" used in an expression shows a cycle of clock f_{FPH} selected by SYSCR1<SYSCK>. If a clock gear or a low speed oscillator is selected, a value of "X" is different. The value as an example is calculated at fc, gear=1/fc (SYSCR1<SYSCK, GEAR2:0> = "0000").

4.1 Maximum Ratings (TMP93PW44AD)

Parameter	Symbol	Rating		Unit
Power supply voltage	V_{CC}	−0.5 to 6.5		V
Input voltage	V_{IN}	except $\overline{EA}$ pin	−0.5 to V_{CC} + 0.5	
		$\overline{EA}$ pin	−0.5 to 14.0	
Output current (Per 1 pin) P7	I_{OL1}	20		mA
Output current (Per 1 pin) except P7	I_{OL2}	2		
Output current (P7 total)	ΣI_{OL1}	80		
Output current (Total)	ΣI_{OL}	120		
Output current (Total)	ΣI_{OH}	−80		
Power dissipation (Ta = 85°C)	P_D	350		mW
Soldering temperature (10 s)	T_{SOLDER}	260		°C
Storage temperature	T_{STG}	−65 to 150		
Operating temperature	T_{OPR}	−40 to 85		

Note: The maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2)

V_{CC} = 5 V ± 10%, Ta = −40 to 85°C

Parameter		Symbol	Condition	Min	Typ. (Note 1)	Max	Unit
Power supply voltage ($AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS} = 0$ V)		V_{CC}	fc = 4 to 20 MHz fs = 30 to 34 kHz	4.5 (Note 2)		5.5	V
Input low voltage	AD0 to AD15	V_{IL}	V_{CC} = 5 V ± 10%	−0.3		0.8	V
	Port 2 to 7 (except P35)	V_{IL1}				0.3 V_{CC}	
	$\overline{RESET}$, $\overline{NMI}$, INT0	V_{IL2}				0.25 V_{CC}	
	$\overline{EA}$, AM8/$\overline{AM16}$	V_{IL3}				0.3	
	X1	V_{IL4}				0.2 V_{CC}	
Input high voltage	AD0 to AD15	V_{IH}	V_{CC} = 5 V ± 10%	2.2		V_{CC} + 0.3	
	Port 2 to 7 (except P35)	V_{IH1}		0.7V_{CC}			
	$\overline{RESET}$, $\overline{NMI}$, INT0	V_{IH2}		0.75V_{CC}			
	$\overline{EA}$, AM8/$\overline{AM16}$	V_{IH3}		V_{CC} − 0.3			
	X1	V_{IH4}		0.8 V_{CC}			
Output low voltage		V_{OL}	I_{OL} = 1.6 mA			0.45	V
Output low current (P7)		I_{OL7}	V_{OL} = 1.0 V	16			mA
Output high voltage		V_{OH}	I_{OH} = −400 μA	4.2			V

Note 1: Typical values are for Ta = 25°C and V_{CC} = 5 V unless otherwise noted.

Note 2: The minimum operation voltage of TMP93CU44/TMP93CW44 is V_{CC} = 2.7 V (at fc = 4 to 12.5 MHz, fs = 30 to 34 kHz).

DC Characteristics (2/2)

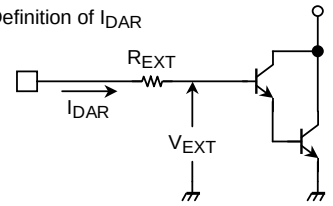
Parameter	Symbol	Condition	Min	Typ. (Note 1)	Max	Unit
Darlington drive current (8 output pins max)	I_{DAR} (Note 2)	V_{EXT} = 1.5 V, R_{EXT} = 1.1 kΩ	−1.0		−3.5	mA
Input leakage current	I_{LI}	0.0 ≤ V_{IN} ≤ V_{CC}		0.02	±5	μA
Output leakage current	I_{LO}	0.2 ≤ V_{IN} ≤ V_{CC} − 0.2		0.05	±10	
Power down voltage (at STOP, RAM backup)	V_{STOP}	V_{IL2} = 0.2V_{CC}, V_{IH2} = 0.8V_{CC}	2.0		6.0	V
$\overline{RESET}$ pull-up resistance	R_{RST}	V_{CC} = 5.5 V	45		130	kΩ
		V_{CC} = 4.5 V	50		160	
Pin capacitance	C_{IO}	fc = 1 MHz			10	pF
Schmitt width $\overline{RESET}$, $\overline{NMI}$, INT0	V_{TH}		0.4	1.0		V
Programmable pull-up resistance	R_{KH}	V_{CC} = 5.5 V	45		130	kΩ
		V_{CC} = 4.5 V	50		160	
NORMAL (Note 3)	I_{CC}	fc = 20 MHz		27	33	mA
RUN				22	27	
IDLE2				16	19	
IDLE1				4.2	7	
SLOW (Note 3)		fs = 32.768 kHz		85	140	μA
RUN				50	100	
IDLE2				35	75	
IDLE1				20	65	
STOP		Ta ≤ 50°C		0.2	10	μA
		Ta ≤ 70°C			20	
		Ta ≤ 85°C			50	

Note 1: Typical values are for Ta = 25°C and V_{CC} = 5 V unless otherwise noted.

Note 2: I_{DAR} is guranteed for total of up to 8 ports.

Note 3: I_{CC} measurement conditions (NORMAL, SLOW):
Only CPU is operational; output pins are open and input pins are fixed.

(Reference) Definition of I_{DAR}



4.3 AC Electrical Characteristics

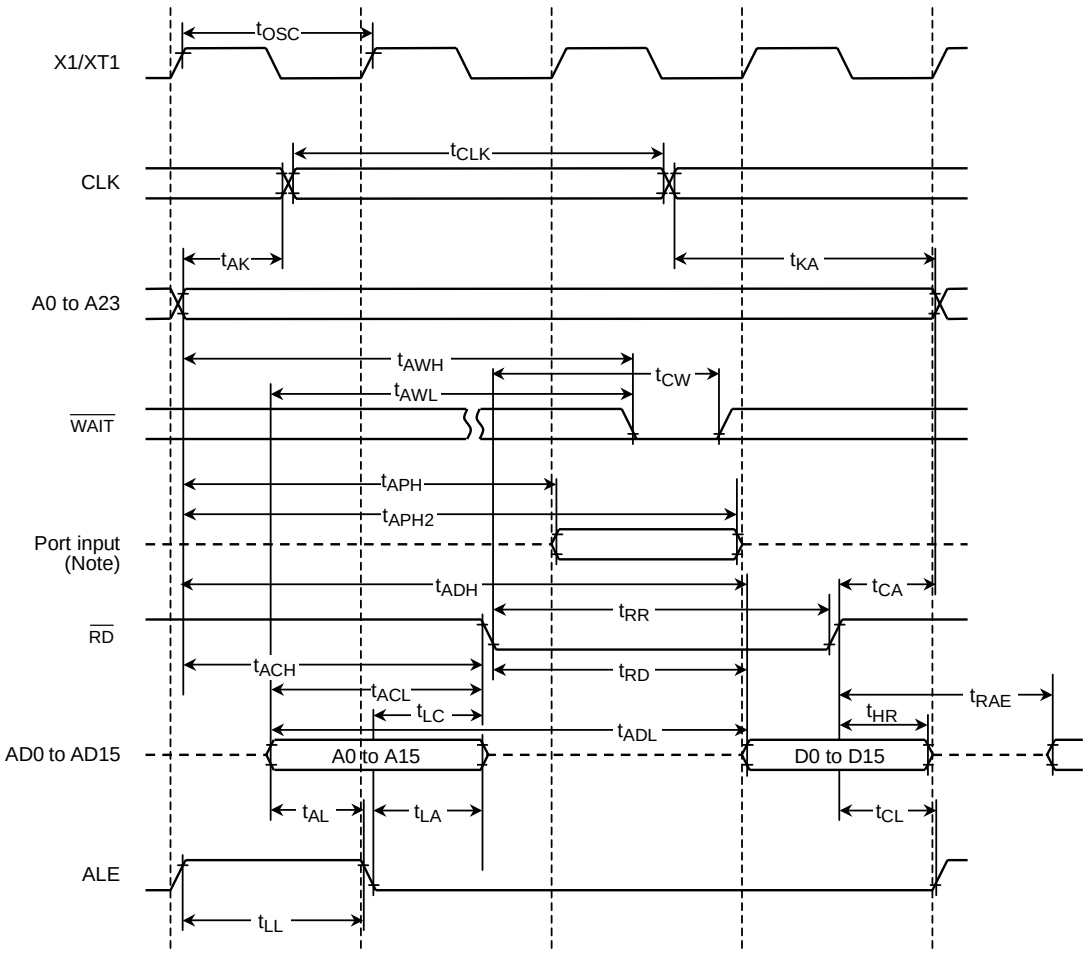
(1) $V_{CC} = 5\ V \pm 10\%$

No.	Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Osc. period (= X)	t_{OSC}	50	31250	62.5		50		ns
2	CLK pulse width	t_{CLK}	2X – 40		85		60		ns
3	A0 to A23 valid → CLK hold	t_{AK}	0.5X – 20		11		5		ns
4	CLK valid → A0 to A23 hold	t_{KA}	1.5X – 70		24		5		ns
5	A0 to A15 valid → ALE fall	t_{AL}	0.5X – 15		16		10		ns
6	ALE fall → A0 to A15 hold	t_{LA}	0.5X – 20		11		5		ns
7	ALE high pulse width	t_{LL}	X – 40		23		10		ns
8	ALE fall → $\overline{RD}$ / $\overline{WR}$ fall	t_{LC}	0.5X – 25		6		0		ns
9	$\overline{RD}$ / $\overline{WR}$ rise → ALE rise	t_{CL}	0.5X – 20		11		5		ns
10	A0 to A15 valid → $\overline{RD}$ / $\overline{WR}$ fall	t_{ACL}	X – 25		38		25		ns
11	A0 to A23 valid → $\overline{RD}$ / $\overline{WR}$ fall	t_{ACH}	1.5X – 50		44		25		ns
12	$\overline{RD}$ / $\overline{WR}$ rise → A0 to A23 hold	t_{CA}	0.5X – 25		6		0		ns
13	A0 to A15 valid → D0 to D15 input	t_{ADL}		3.0X – 55		133		95	ns
14	A0 to A23 valid → D0 to D15 input	t_{ADH}		3.5X – 65		154		110	ns
15	$\overline{RD}$ fall → D0 to D15 input	t_{RD}		2.0X – 60		65		40	ns
16	$\overline{RD}$ low pulse width	t_{RR}	2.0X – 40		85		60		ns
17	$\overline{RD}$ rise → D0 to D15 hold	t_{HR}	0		0		0		ns
18	$\overline{RD}$ rise → A0 to A15 output	t_{RAE}	X – 15		48		35		ns
19	$\overline{WR}$ low pulse width	t_{WW}	2.0X – 40		85		60		ns
20	D0 to D15 valid → $\overline{WR}$ rise	t_{DW}	2.0X – 55		70		45		ns
21	$\overline{WR}$ rise → D0 to D15 hold	t_{WD}	0.5X – 15		16		10		ns
22	A0 to A23 valid → $\overline{WAIT}$ input ((1 + N) WAIT mode)	t_{AWH}		3.5X – 90		129		85	ns
23	A0 to A15 valid → $\overline{WAIT}$ input ((1 + N) WAIT mode)	t_{AWL}		3.0X – 80		108		70	ns
24	$\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ hold ((1 + N) WAIT mode)	t_{CW}	2.0X + 0		125		100		ns
25	A0 to A23 valid → PORT input	t_{APH}		2.5X – 120		36		5	ns
26	A0 to A23 valid → PORT hold	t_{APH2}	2.5X + 50		206		175		ns
27	$\overline{WR}$ rise → PORT valid	t_{CP}		200		200		200	ns

AC Measuring Conditions

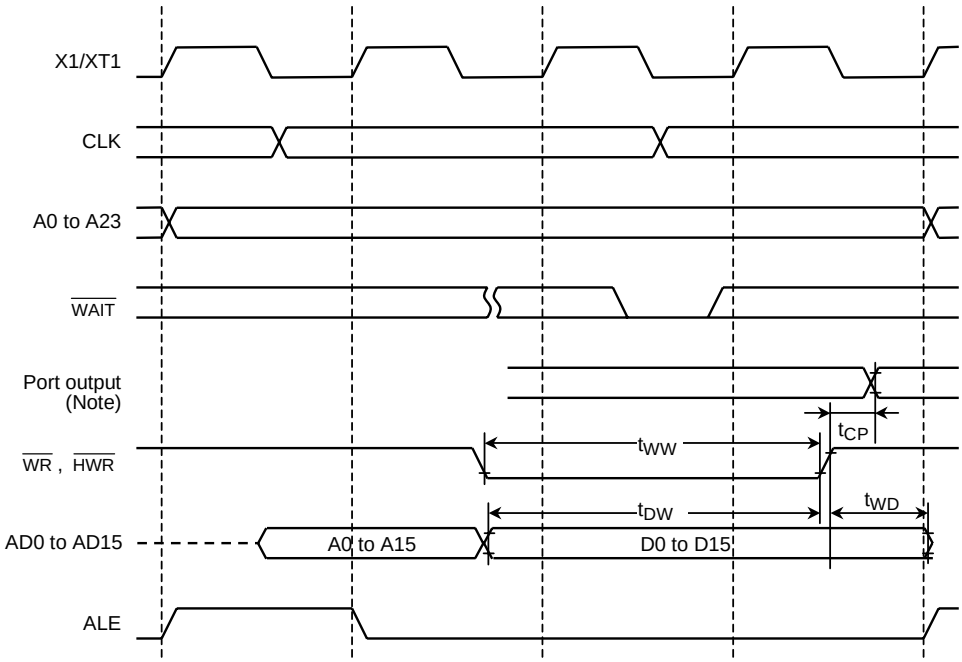
- Output level: High 2.2 V/Low 0.8 V, CL = 50 pF
  (However CL = 100 pF for AD0 to AD15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, CLK)
- Input level: High 2.4 V/Low 0.45 V (AD0 to AD15)
  High 0.8 × V_{CC}/Low 0.2 × V_{CC} (except for AD0 to AD15)

(2) Read cycle



Note: Since the CPU accesses the internal area to read data from a port, the control signals of external pins such as $\overline{RD}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

(3) Write cycle



Note: Since the CPU accesses the internal area to write data to a port, the control signals of external pins such as $\overline{WR}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

4.4 Serial Channel Timing

(1) I/O interface mode

1. SCLK input mode

Parameter	Symbol	Variable		32.768 MHz (Note)		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle	t_{SCY}	16X		488 μs		0.8 μs		ns
Output data → Falling edge of SCLK	t_{OSS}	$t_{SCY}/2 - 5X - 50$		91.5 μs		100		ns
SCLK rising/falling edge → Output data hold	t_{OHS}	5X – 100		152 μs		150		ns
SCLK rising/falling edge → Input data hold	t_{HSR}	0		0		0		ns
SCLK rising/falling edge → Effective data input	t_{SRD}		$t_{SCY} - 5X - 100$		336 μs		450	ns

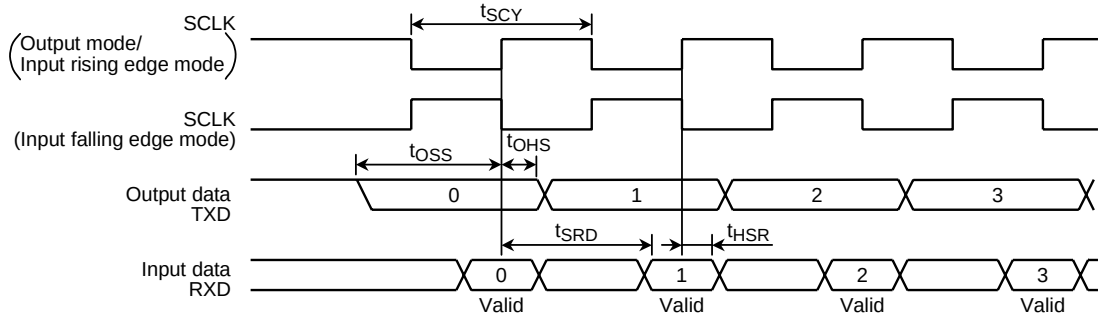
Note 1: When fs is used as system clock or fs divided by 4 is used as input clock to prescaler.

Note 2: SCLK rising/falling timing; SCLK rising in the rising mode of SCLK, SCLK falling in the falling mode of SCLK.

2. SCLK output mode

Parameter	Symbol	Variable		32.768 MHz (Note)		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle (Programmable)	t_{SCY}	16X	8192X	488 μs	250 ms	0.8 μs	409.6 μs	ns
Output data → SCLK rising edge	t_{OSS}	$t_{SCY} - 2X - 150$		427 μs		550		ns
SCLK rising edge → Output data hold	t_{OHS}	2X – 80		60 μs		20		ns
SCLK rising edge → Input data hold	t_{HSR}	0		0		0		ns
SCLK rising edge → Effective data input	t_{SRD}		$t_{SCY} - 2X - 150$		428 μs		550	ns

Note: When fs is used as system clock or fs divided by 4 is used as input clock to prescaler.



(2) UART mode (SCLK0 and SCLK 1 are external input)

Parameter	Symbol	Variable		32.768 MHz (Note)		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle	t_{SCY}	4X + 20		122 μs		220		ns
SCLK low level pulse width	t_{SCYL}	2X + 5		6 μs		105		ns
SCLK high level pulse width	t_{SCYH}	2X + 5		6 μs		105		ns

Note: When fs is used as system clock or fs divided by 4 is used as input clock to prescaler.

4.5 AD Conversion Characteristics

$AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$

Parameter	Symbol	Power Supply	Min	Typ.	Max	Unit
Analog reference voltage (+)	V_{REFH}	V_{CC} = 5 V ± 10%	V_{CC} − 0.2 V	V_{CC}	V_{CC}	V
Analog reference voltage (−)	V_{REFL}		V_{SS}	V_{SS}	V_{SS} + 0.2 V	
Analog input voltage range	V_{AIN}		V_{REFL}		V_{REFH}	
Analog current for analog reference voltage <VREFON> = 1	I_{REF} (V_{REFL} = 0 V)			0.5	1.5	mA
<VREFON> = 0				0.02	5.0	μA
Error (except quantization errors)	−			±1.0	±3.0	LSB

Note 1: 1LSB = $(V_{REFH} - V_{REFL})/2^{10}$ [V]

Note 2: The operation above is guaranteed for $f_{FPH} \geq 4$ MHz.

Note 3: The value I_{CC} includes the current which flows through the AVCC pin.

4.6 Event Counter Input Clock (External Input Clock: TI0, TI4, TI5, TI6, TI7)

Parameter	Symbol	Variable		20 MHz		Unit
		Min	Max	Min	Max	
Clock cycle	t_{VCK}	8X + 100		500		ns
Low level clock pulse width	t_{VCKL}	4X + 40		240		ns
High level clock pulse width	t_{VCKH}	4X + 40		240		ns

4.7 Interrupt and Capture Operation

(1) $\overline{NMI}$, INT0 interrupts

Parameter	Symbol	Variable		20 MHz		Unit
		Min	Max	Min	Max	
$\overline{NMI}$, INT0 low level pulse width	t_{INTAL}	4X		200		ns
$\overline{NMI}$, INT0 high level pulse width	t_{INTAH}	4X		200		ns

(2) INT1, INT4 to INT7 interrupts and capture

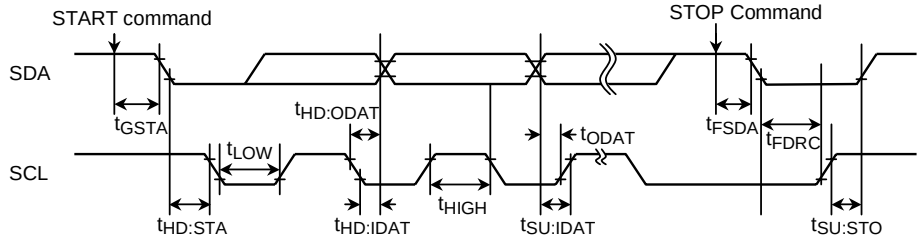
Parameter	Symbol	Variable		20 MHz		Unit
		Min	Max	Min	Max	
INT1, INT4 to INT7 low level pulse width	t_{INTBL}	4X + 100		300		ns
INT1, INT4 to INT7 high level pulse width	t_{INTBH}	4X + 100		300		ns

4.8 Serial Bus Interface Timing

(1) I²C bus mode

Parameter	Symbol	Variable			Unit
		Min	Typ.	Max	
START command → SDA fall	t_{GSTA}	3X			ns
Hold time START condition	$t_{HD:STA}$	2^nX			ns
SCL low level pulse width	t_{LOW}	2^nX			ns
SCL high level pulse width	t_{HIGH}	$2^nX + 12X$			ns
Data hold time (input)	$t_{HD:IDAT}$	0			ns
Data setup time (input)	$t_{SU:IDAT}$	250			ns
Data hold time (output)	$t_{HD:ODAT}$	7X		11X	ns
Data output → SCL rising edge	t_{ODAT}		$2^nX - t_{HD:ODAT}$		ns
STOP command → SDA fall	t_{FSDA}	3X			ns
SDA falling edge → SCL rising edge	t_{FDRC}	2^nX			ns
Setup time STOP condition	$t_{SU:STO}$	$2^nX + 16X$			ns

Note: “n” value is set by SBICR1<SCK2:0>



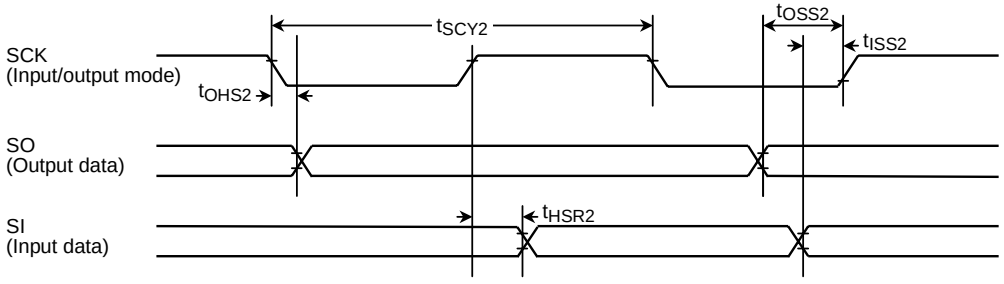
(2) Clocked-synchronous 8-bit SIO mode

1. SCK input mode

Parameter	Symbol	Variable		Unit
		Min	Max	
SCK cycle	t_{SCY2}	2^5X		ns
SCK falling edge → Output data hold	t_{OHS2}	6X		ns
Output data → SCK rising edge	t_{OSS2}	$t_{SCY2} - 6X$		ns
SCK rising edge → Input data hold	t_{HSR2}	6X		ns
Input data → SCK rising edge	t_{ISS2}	0		ns

2. SCK output mode

Parameter	Symbol	Variable		Unit
		Min	Max	
SCK cycle	t_{SCY2}	2^5X	$2^{11}X$	ns
SCK falling edge → Output data hold	t_{OHS2}	2X		ns
Output data → SCK rising edge	t_{OSS2}	$t_{SCY2} - 2X$		ns
SCK rising edge → Input data hold	t_{HSR2}	2X		ns
Input data → SCK rising edge	t_{ISS2}	0		ns



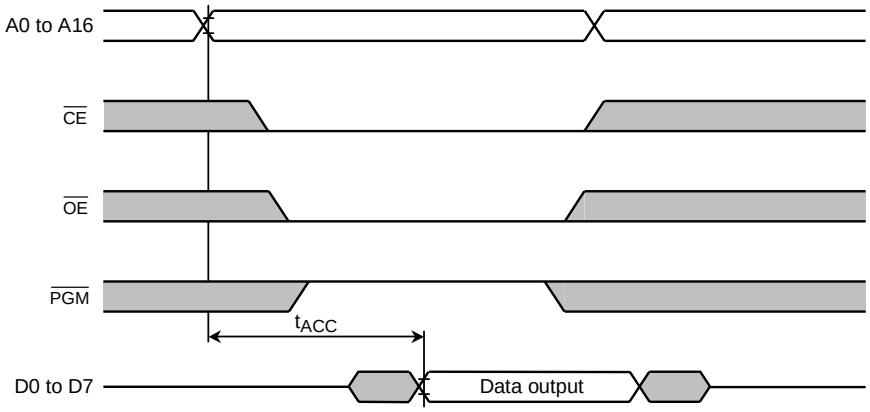
4.9 Read Operation in PROM Mode

DC/AC characteristics

Ta = 25 ± 5°C Vcc = 5 V ± 10%

Parameter	Symbol	Condition	Min	Max	Unit
V_{PP} read voltage	V_{PP}	–	4.5	5.5	V
Input high voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IH1}	–	2.2	V_{CC} + 0.3	
Input low voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IL1}	–	–0.3	0.8	
Address to output delay	t_{ACC}	C_L = 50 pF	–	$2.25T_{CYC} + \alpha$	ns

T_{CYC} = 400 ns (10 MHz clock)
α = 200 ns

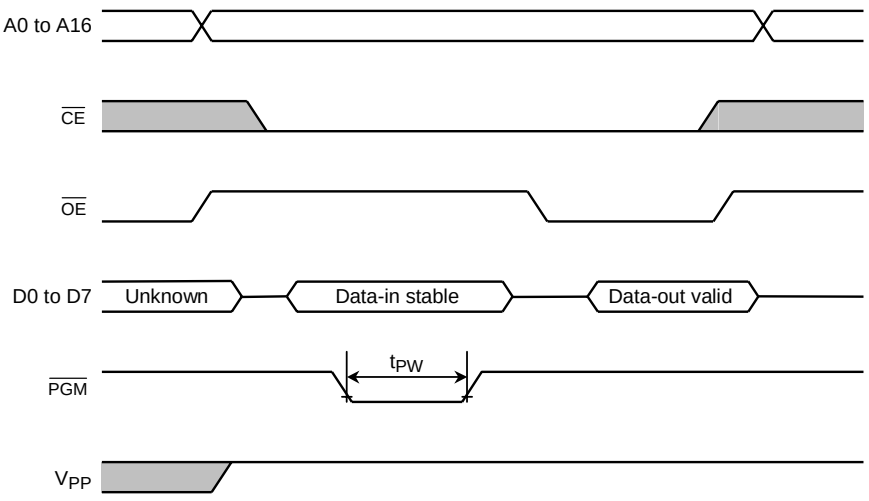


4.10 Program Operation in PROM Mode

DC/AC characteristics

Ta = 25 ± 5°C V_{CC} = 6.25 V ± 0.25 V

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Programming supply voltage	V_{PP}	–	12.50	12.75	13.00	V
Input high voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IH}	–	2.6		V_{CC} + 0.3	
Input low voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IL}	–	−0.3		0.8	
V_{CC} supply current	I_{CC}	fc = 10 MHz	–		50	mA
V_{PP} supply current	I_{PP}	V_{PP} = 13.00 V	–		50	
$\overline{PGM}$ program pulse width	t_{PW}	C_L = 50 pF	0.095	0.1	0.105	ms



Note 1: The power supply of V_{PP} (12.75 V) must be set power-on at the same time or the later time for a power supply of V_{CC} and must be clear power-on at the same time or early time for a power supply of V_{CC}.

Note 2: The pulling up/down device on condition of V_{PP} = 12.75 V suffers a damage for the device.

Note 3: The maximum spec of V_{PP} pin is 14.0 V. Be carefull a overshoot at the programming.

5. Package Dimensions

P-QFP80-1420-0.80B

Unit: mm