CMOS 16-Bit Microcontrollers

TMP95CW54AF

1. Outline and Features

TMP95CW54A is a high-speed 16-bit microcontroller designed for the control of various mid- to large-scale equipment.

TMP95CW54A comes in a 100-pin flat package.

Listed below are the features.

(1) High-speed 16-bit CPU (900/H CPU)
- Instruction mnemonics are upward-compatible with TLCS-90/900
- 16M bytes of linear address space
- General-purpose registers and register banks
- 16-bit multiplication and division instructions; bit transfer and arithmetic instructions
- Micro DMA : Four-channels (667 ns / 2 bytes at 24 MHz)

(2) Minimum instruction execution time : 167 ns (at 24 MHz)

(3) Built-in RAM : 4 Kbytes
Built-in ROM : 128 Kbyte

(4) External memory expansion
- Expandable up to 16 Mbytes (shared program/data area)
- External data bus width select pin (AM8/$\overline{16}$)
- Can simultaneously support 8/16-bit width external data bus
  … Dynamic data bus sizing

(5) 8-bit timers : 8 channels
- With event counter function : 2 channels

(6) 16-bit timer/event counter : 2 channels

(7) General-purpose serial interface : 2 channels

(8) Serial Expansion Interface : 1 channel

(9) CAN Controller : 1 channel

(10) 10-bit AD converter : 8 channels

(11) Watchdog timer

(12) Bus width/wait controller : 4 blocks

(13) Interrupts : 49 interrupts

- 9 CPU interrupts : Software interrupt instruction and illegal instruction
- 30 internal interrupts : Seven selectable priority levels
- 10 external interrupts : Seven selectable priority levels

(14) Input/output ports : 81 pins

(15) Standby mode

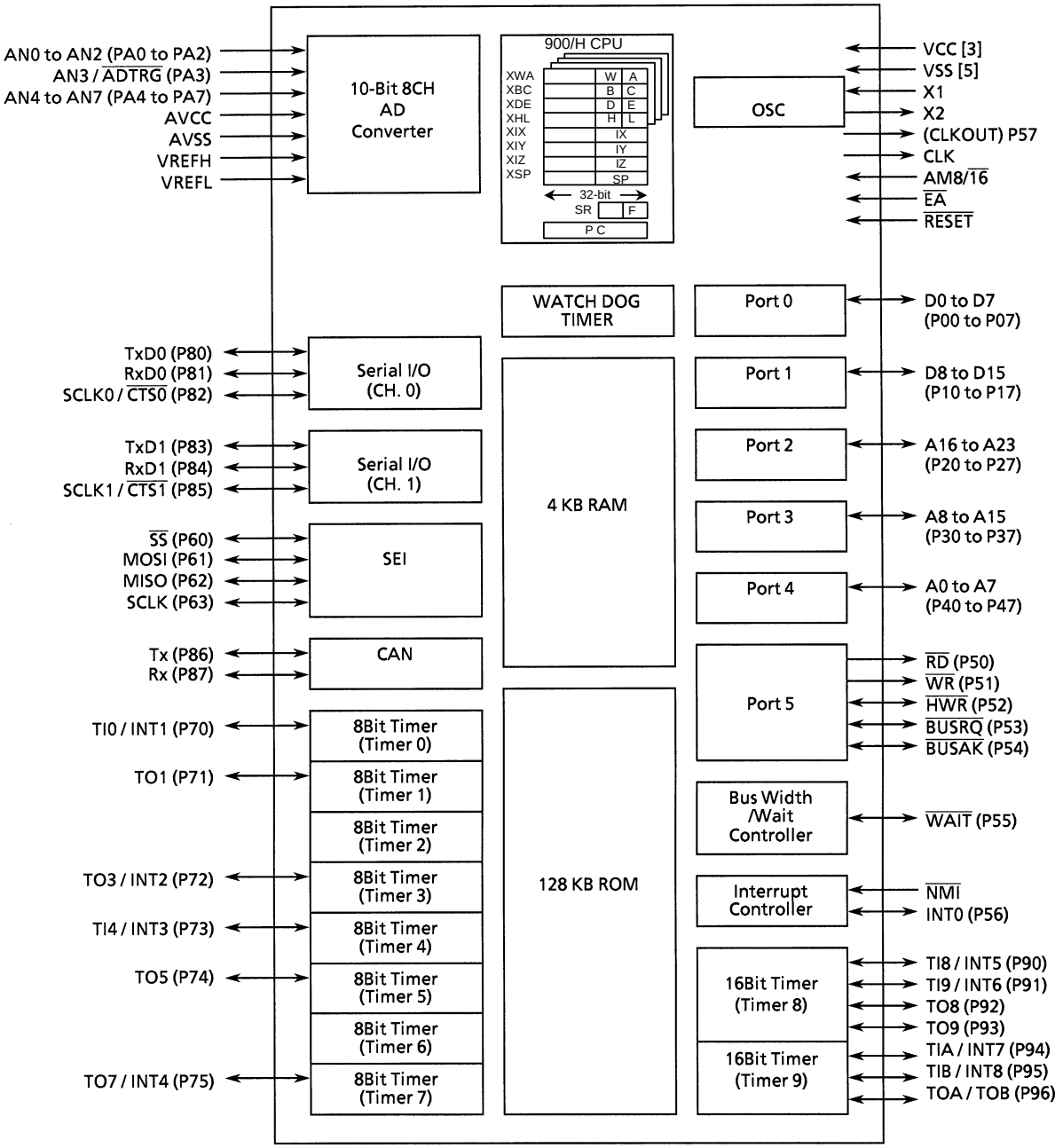
- Four HALT modes : RUN, IDLE2, IDLE1, STOP

(16) Operating voltage

- V_{CC} = 4.5 to 5.5 V

(17) Package

- P-LQFP100-1414-0.50D



Note: After a reset, functions in parentheses ( ) are selected for the shared pins.

Figure 1.1 TMP95CW54A Block Diagram

2. Pin Assignment and Pin Functions

This section shows the TMP95CW54A pin assignment, and the names and an outline of the functions of the input/output pins.

2.1 Pin Assignment Diagram

Figure 2.1.1 is a pin assignment diagram for TMP95CW54A.

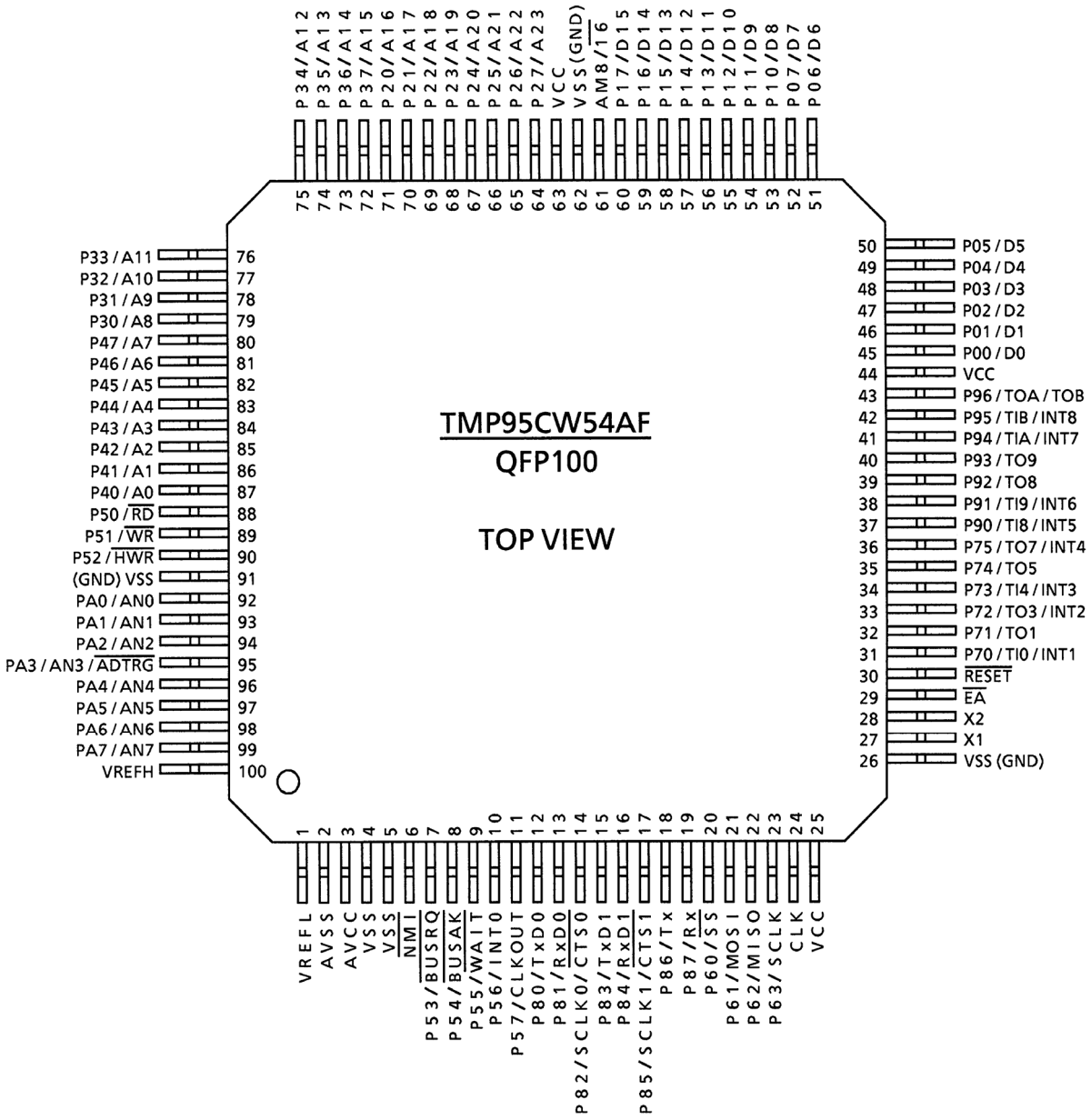


Figure 2.1.1 Pin assignment diagram (100-Pin LQFP)

2.2 Pin Names and Functions

Table 2.2.1 shows the names and functions of the input/output pins.

Table 2.2.1 Pin names and functions (1/4)

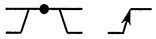
Pin Name	Number of Pins	Input/Output	Function
P00 to P07	8	Input/output	Port 0: I/O port. Input or output specifiable in units of bits
/ D0 to D7		Input/output	Data: Data bus 0 to 7
P10 to P17	8	Input/output	Port 1: I/O port. Input or output specifiable in units of bits
/ D8 to D15		Input/output	Data: Data bus 8 to 15
P20 to P27	8	Input/output	Port 2: I/O port. Input or output specifiable in units of bits
/ A16 to A23		Output	Address: Address bus 16 to 23
P30	1	Input/output	Port 30: I/O port (with built-in pull-up resistor during input mode.)
/ A8		Output	Address: Address bus 8
P31 to P37	7	Input/output	Port 31 to 37: I/O port. Input or output specifiable in units of bits
/ A9 to A15		Output	Address: Address bus 9 to 15
P40 to P47	8	Input/output	Port 4: I/O port. Input or output specifiable in units of bits
/ A0 to A7		Output	Address: Address bus 0 to 7
P50	1	Output	Port 50: Output-only port
/ $\overline{RD}$		Output	Read: Outputs strobe signal to read external memory (setting P5 <P50> = 0 and P5FC <P50F> = 1 outputs strobe signal at all read timings)
P51	1	Output	Port 51: Output-only port.
/ $\overline{WR}$		Output	Write: Outputs strobe signal to write data on pins D0 to D7
P52	1	Input/output	Port 52: I/O port (with built-in pull-up resistor)
/ $\overline{HWR}$		Output	Upper write: Outputs strobe signal to write data on pins D8 to D15
P53	1	Input/output	Port 53: I/O port (with built-in pull-up resistor)
/ $\overline{BUSRQ}$		Input	Bus request: Input pin to request external bus release
P54	1	Input/output	Port 54: I/O port (with built-in pull-up resistor)
/ $\overline{BUSAK}$		Output	Bus acknowledge: Output pin to acknowledge that CPU received $\overline{BUSRQ}$ and released external bus.
P55	1	Input/output	Port 55: I/O port (with built-in pull up resistor)
/ $\overline{WAIT}$		Input	Wait: Bus wait request pin for CPU (Effective when 1 WAIT + N mode, or 0 + N WAIT mode. Set using bus width/wait control register.)
P56	1	Input/output	Port 56: I/O port (with built-in pull-up resistor)
/ INT0		Input	Interrupt request pin 0: Interrupt request pin with programmable level/rising edge. 

Table 2.2.1 Pin names and functions (2/4)

Pin Name	Number of Pins	Input/Output	Function
P57	1	Output	Port 57: Output-only port (with built-in pull-up resistor)
/ CLKOUT		Output	CLKOUT output: Outputs external clock divided by 6. Pulled up during reset.
P60	1	Input/output	Port 60: I/O port
/ $\overline{SS}$		Input	SEI slave select input
P61	1	Input/output	Port 61: I/O port
/ MOSI		Input/output	SEI master output, slave input
P62	1	Input/output	Port 62: I/O port
/ MISO		Input/output	SEI master input, slave output
P63	1	Input/output	Port 63: I/O port
/ SCLK		Input/output	SEI clock input/output
P70	1	Input/output	Port 70: I/O port
/ TI0		Input	Timer input 0: Input pin for timer 0
/ INT1		Input	Interrupt request pin 1: Rising-edge interrupt request pin
P71	1	Input/output	Port 71: I/O port.
/ TO1		Output	Timer output 1: Output pin for timer 0 or 1
P72	1	Input/output	Port 72: I/O port
/ TO3		Output	Timer output 3: Output pin for timer 2 or 3
/ INT2		Input	Interrupt request pin 2: Rising-edge interrupt request pin
P73	1	Input/output	Port 73: I/O port
/ TI4		Input	Timer input 4: Input pin for timer 4
/ INT3		Input	Interrupt request pin 3: Rising-edge interrupt request pin
P74	1	Input/output	Port 74: I/O port
/ TO5		Output	Timer output 5: Output pin for timer 4 or 5
P75	1	Input/output	Port 75: I/O port
/ TO7		Output	Timer output 7: Output pin for timer 6 or 7
/ INT4		Input	Interrupt request pin 4: Rising-edge interrupt request pin
P80	1	Input/output	Port 80: I/O port (with built-in pull-up resistor)
/ TxD0		Output	Serial transmission data 0
P81	1	Input/output	Port 81: I/O port (with built-in pull-up resistor)
/ RxD0		Input	Serial receive data 0
P82	1	Input/output	Port 82: I/O port (with built-in pull-up resistor)
/ SCLK0		Input/output	Serial clock input/output 0
/ $\overline{CTS0}$		Input	Serial data ready to send 0 (Clear-to-send)

Table 2.2.1 Pin names and functions (3/4)

Pin Name	Number of Pins	Input/Output	Function
P83	1	Input/output	Port 83: I/O port (with built-in pull-up resistor)
/ TxD1		Output	Serial transmission data 1
P84	1	Input/output	Port 84: I/O port (with built-in pull-up resistor)
/ RxD1		Input	Serial receive data 1
P85	1	Input/output	Port 85: I/O port (with built-in pull-up resistor)
/ SCLK1		Input/output	Serial clock input/output 1
/ $\overline{\text{CTS1}}$		Input	Serial data ready to send 1 (Clear-to-send)
P86	1	Input/output	Port 86: I/O port (with built-in pull-up resistor)
/ Tx		Output	CAN transmission data
P87	1	Input/output	Port 87: I/O port (with built-in pull-up resistor)
/ Rx		Input	CAN receive data
P90	1	Input/output	Port 90: I/O port
/ TI8		Input	Timer input 8: Input pin for timer 8
/ INT5		Input	Interrupt request pin 5: Interrupt request pin with programmable rising/falling edge
P91	1	Input/output	Port 91: I/O port
/ TI9		Input	Timer input 9: Input pin for timer 8
/ INT6		Input	Interrupt request pin 6: Rising edge interrupt request pin
P92	1	Input/output	Port 92: I/O port
/ TO8		Output	Timer output 8: Output pin for timer 8
P93	1	Input/output	Port 93: I/O port
/ TO9		Output	Timer output 9: Output pin for timer 8
P94	1	Input/output	Port 94: I/O port
/ TIA		Input	Timer input A: Input pin for timer 9
/ INT7		Input	Interrupt request pin 7: Interrupt request pin with programmable rising/falling edge
P95	1	Input/output	Port 95: I/O port
/ TIB		Input	Timer input B: Input pin for timer 9
/ INT8		Input	Interrupt request pin 8: Rising edge interrupt request pin
P96	1	Input/output	Port 96: I/O port
/ TOA		Output	Timer output A: Output pin for timer 9
/ TOB		Output	Timer output B: Output pin for timer 9
PA0 to PA2	3	Input	Port A0 to A2: Input-only port
/ AN0 to AN2		Input	Analog input 0 to 2: AD converter input pins
PA3	1	Input	Port A3: Input-only port
/ AN3		Input	Analog input 3: AD converter input pin
/ $\overline{\text{ADTRG}}$		Input	External start trigger

Table 2.2.1 Pin names and functions (4/4)

Pin Name	Number of Pins	Input/Output	Function
PA4 to PA7	4	Input	Port A4 to A7: Input-only port
/ AN4 to AN7		Input	Analog input 4 to 7: AD converter input pins
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge or both falling and rising edge
CLK	1	Output	Clock output: Outputs external clock divided by 4. Pulled up during reset.
$\overline{EA}$	1	Input	External access: Connect to VCC.
AM8 / $\overline{16}$	1	Input	Address mode: External data bus width select pin Connect this pin to VCC. Data bus width at external access can be set by bus width/wait control register.
$\overline{RESET}$	1	Input	Reset: Initializes TMP95CW54A (with built-in pull-up resistor)
VREFH	1	Input	Reference voltage input pin for AD converter (high)
VREFL	1	Input	Reference voltage input pin for AD converter (low)
AVCC	1		Power supply pin for AD converter: Connect to power supply
AVSS	1		GND pin for AD converter: Connect to GND
X1 / X2	2	Input/output	Oscillator connecting pin
VCC	3		Power supply pin: Connect all VCC pins to power supply
VSS	5		GND pin: Connect all VSS pins to GND (0 V)

Note: Disconnect the pull-up resistors from pins other than $\overline{RESET}$ pin by software.
P30 is pulled-up during reset and input mode.
P57 and CLK pin are pulled-up only during reset.

3. Operation

The following describes the structure and operation of the TMP95CW54A hardware.

This device is created from the TMP95CU54A by expanding its internal ROM size to 128 Kbytes and its internal RAM size to 4 Kbytes. Otherwise, TMP95CW54A is structurally and operationally identical to TMP95CU54A. Accordingly, for functions not described here, see the TMP95CU54A section of the manual.

3.1 MCU Mode

Opening the CLK pin (setting to output) sets MCU mode.
In MCU mode, TMP95CW54A operates the same as TMP95CU54A.

3.2 Memory Map

Figure 3.2.1 shows the memory map in MCU mode and the CPU access area in each addressing mode.

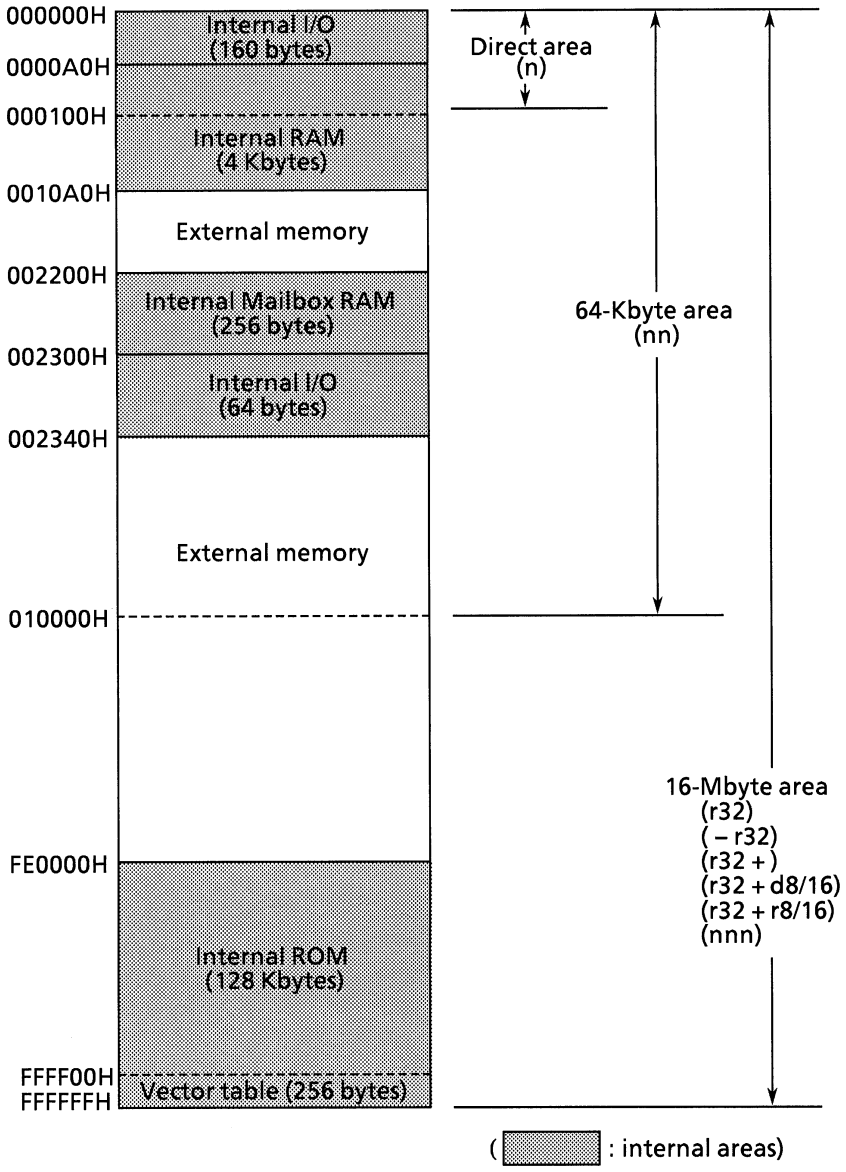


Figure 3.2.1 TMP95CW54A Memory Map

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	− 0.5 to + 6.5	V
Input Voltage	V_{IN}	− 0.5 to Vcc + 0.5	V
Output current (total)	ΣI_{OL}	+ 120	mA
Output current (total)	ΣI_{OH}	− 120	mA
Power Dissipation (Ta = + 85°C)	P_D	600	mW
Soldering Temperature (10 s)	T_{SOLDER}	+ 260	°C
Storage Temperature	T_{STG}	− 65 to + 150	°C
Operating Temperature	T_{OPR}	− 40 to + 85	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Electrical Characteristics

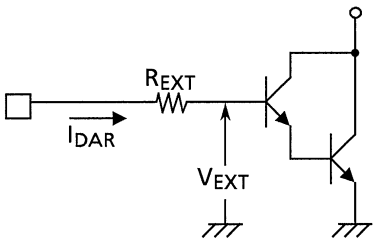
Vcc = +5 V ±10%, Ta = −40 to + 85°C (fc = 8 to 24 MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Low Voltage (D0 to 15) Port 2 to A (except P56, P70, P72, P73, P75) RESET, NMI, INT0 to 4 EA, AM8/16 X1	V_{IL} V_{IL1} V_{IL2} V_{IL3} V_{IL4}		−0.3 −0.3 −0.3 −0.3 −0.3	0.8 0.3 Vcc 0.25 Vcc 0.3 0.2 Vcc	V V V V V
Input High Voltage (D0 to 15) Port 2 to A (except P56, P70, P72, P73, P75) RESET, NMI, INT0 to 4 EA, AM8/16 X1	V_{IH} V_{IH1} V_{IH2} V_{IH3} V_{IH4}		2.2 0.7 Vcc 0.75 Vcc Vcc − 0.3 0.8 Vcc	Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3	V V V V V
Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA		0.45	V
Output High Voltage	V_{OH} V_{OH1} V_{OH2}	I_{OH} = −400 μA I_{OH} = −100 μA I_{OH} = −20 μA	2.4 0.75 Vcc 0.9 Vcc		V V V
Darlington Drive Current (8 Output Pins max.)	I_{DAR}	V_{EXT} = 1.5 V R_{EXT} = 1.1 kΩ	−1.0	−3.5	mA
Input Leakage Current Output Leakage Current	I_{LI} I_{LO}	0.0 ≦ Vin ≦ Vcc 0.2 ≦ Vin ≦ Vcc − 0.2	0.02 (Typ) 0.05 (Typ)	±5 ±10	μA μA
Operating Current (NORMAL) RUN IDLE2 IDLE1	I cc	fc = 24 MHz	70 (Typ) 35 (Typ) 30 (Typ) 5 (Typ)	85 50 40 10	mA mA mA mA
STOP (Ta = −40 to + 85°C) (Ta = −20 to + 70°C)		0.2 ≦ Vin ≦ Vcc − 0.2	0.5 (Typ)	100 50	μA μA
Power Down Voltage (@STOP, RAM Back up)	V_{STOP}	V_{IL2} = 0.2 Vcc, V_{IH2} = 0.8 Vcc	2.0	6.0	V
Pull Up Registance	R_{RP}		45	160	kΩ
Pin Capacitance	C_{IO}	fc = 1 MHz		10	pF
Schmitt Width RESET, NMI, INT0 to 4	V_{TH}		0.4	1.0 (Typ)	V

Note 1 : Typical values are for Ta = +25°C, V_{CC} = +5 V

Note 2 : I_{DAR} guarantees up to eight pins from any output port.

Refer: I_{DAR} definition diagram.



4.3 AC Electrical Characteristics

Vcc = +5 V ±10%, Ta = −40 to +85°C

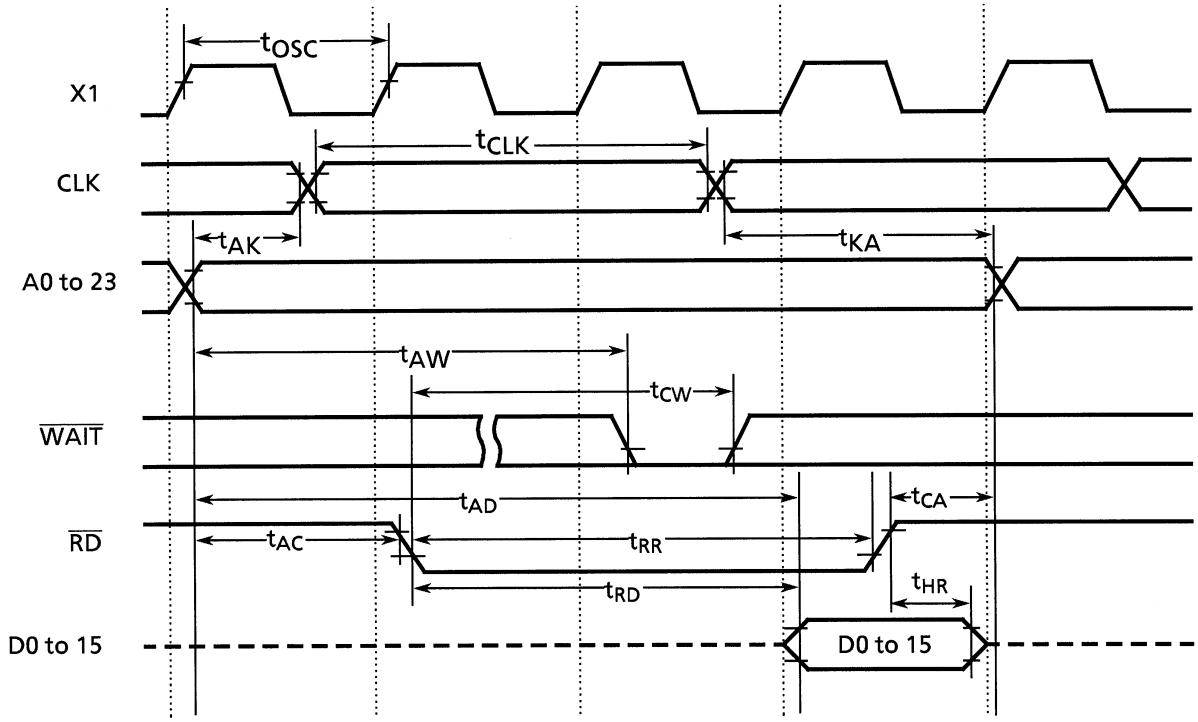
(fc = 8 MHz to 24 MHz)

No.	Parameter	Symbol	Variable		24 MHz		Unit
			Min	Max	Min	Max	
1	Oscillation cycle (= x)	t_{OSC}	42	125	42		ns
2	Clock pulse width	t_{CLK}	2.0x – 40		44		ns
3	A0 to 23 valid → Clock hold	t_{AK}	0.5x – 20		1		ns
4	Clock valid → A0 to 23 hold	t_{KA}	1.5x – 60		3		ns
5	A0 to 23 valid → $\overline{RD}/\overline{WR}$ fall	t_{AC}	1.0x – 20		22		ns
6	$\overline{RD}/\overline{WR}$ rise → A0 to 23 hold	t_{CA}	0.5x – 20		1		ns
7	A0 to 23 valid → D0 to 15 input	t_{AD}		3.5x – 40		107	ns
8	$\overline{RD}$ fall → D0 to 15 input	t_{RD}		2.5x – 45		60	ns
9	$\overline{RD}$ low pulse width	t_{RR}	2.5x – 40		65		ns
10	$\overline{RD}$ rise → D0 to 15 hold	t_{HR}	0		0		ns
11	$\overline{WR}$ low pulse width	t_{WW}	2.5x – 40		65		ns
12	D0 to 15 valid → $\overline{WR}$ rise	t_{DW}	2.0x – 40		44		ns
13	$\overline{WR}$ rise →D0 to 15 hold	t_{WD}	0.5x – 10		11		ns
14	A0 to 23 valid → $\overline{WAIT}$ input ($^{1\ WAIT}_{+\ n\ mode}$)	t_{AW}		3.5x – 90		57	ns
	A0 to 23 valid → $\overline{WAIT}$ input ($^{0+n\ WAIT}_{mode}$)	t_{AW}		1.5x – 40		23	ns
15	$\overline{RD}/\overline{WR}$ fall → $\overline{WAIT}$ hold ($^{1\ WAIT}_{+\ n\ mode}$)	t_{CW}	2.5x + 0		105		ns
	$\overline{RD}/\overline{WR}$ fall → $\overline{WAIT}$ hold ($^{0+n\ WAIT}_{mode}$)	t_{CW}	0.5x + 0		21		ns
16	$\overline{WR}$ rise→ PORT valid	t_{CP}		200		200	ns

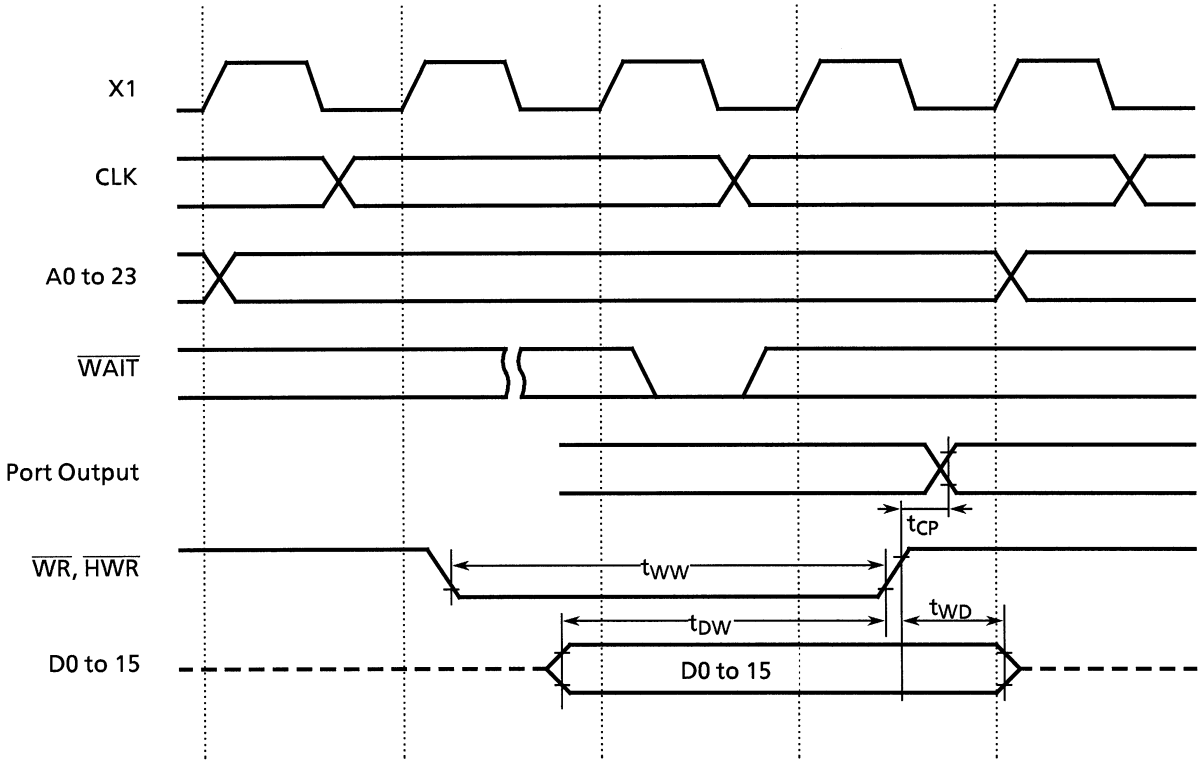
AC measuring conditions

- Output level: High 2.2V / Low 0.8V, CL = 50 pF
- Input level: High 2.4V / Low 0.45V (D0 to D15)
  High 0.8 × Vcc / Low 0.2 × Vcc (except for D0 to D15)

(1) Read cycle



(2) Write cycle



4.4 Serial Channel Timing

(1) I/O interface mode

[1] SCLK input mode

Vcc = +5 V ± 10%, Ta = −40 to +85°C (fc = 8 to 24 MHz)

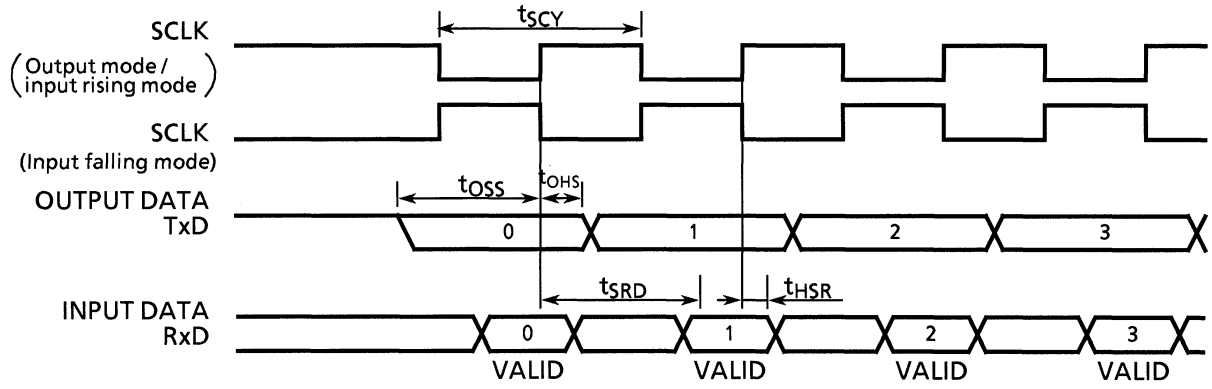
Parameter	Symbol	Variable		24 MHz		Unit
		Min	Max	Min	Max	
SCLK cycle	t_{SCY}	16x		0.667		μs
Output Data →SCLK rise/fall*	t_{OSS}	t_{SCY}/2 − 5x − 50		75		ns
SCLK rise/fall* →Output Data hold	t_{OHS}	5x − 100		108		ns
SCLK rise/fall* →input data hold	t_{HSR}	0		0		ns
SCLK rise/fall* →valid data input	t_{SRD}		t_{SCY} − 5x − 100		358	ns

*) SCLK rise/fall: In SCLK rising edge mode, SCLK rising edge timing; in SCLK falling edge mode, SCLK falling edge timing

[2] SCLK output mode

Vcc = +5 V ± 10%, Ta = −40 to +85°C (fc = 8 to 24 MHz)

Parameter	Symbol	Variable		24 MHz		Unit
		Min	Max	Min	Max	
SCLK cycle (programmable)	t_{SCY}	16x	8192x	0.667	341.3	μs
Output Data →SCLK rising edge	t_{OSS}	t_{SCY} − 2x − 150		433		ns
SCLK rising edge →Output Data hold	t_{OHS}	2x − 80		3		ns
SCLK rising edge →Input Data hold	t_{HSR}	0		0		ns
SCLK rising edge →valid data input	t_{SRD}		t_{SCY} − 2x − 150		433	ns



(2) UART mode (SCLK0 to 1 external input)

Vcc = +5 V ± 10%, Ta = −40 to +85°C (fc = 8 to 24 MHz)

Parameter	Symbol	Variable		24 MHz		Unit
		Min	Max	Min	Max	
SCLK cycle	t_{SCY}	4x + 20		187		ns
Low-level SCLK pulse width	t_{SCYL}	2x + 5		88		ns
High-level SCLK pulse width	t_{SCYH}	2x + 5		88		ns

4.5 AD Conversion Characteristics

Vcc = +5 V ± 10%, Ta = −40 to +85°C (fc = 8 to 24 MHz)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
AD analog reference supply voltage (+)		V_{REFH}		Vcc − 0.2		Vcc	V
AD analog reference supply voltage (−)		V_{REFL}		Vss		Vss + 0.2	
Analog reference voltage		AV_{CC}		Vcc − 0.2		Vcc	
Analog reference voltage		AV_{SS}		Vss		Vss + 0.2	
Analog input voltage		V_{AIN}		V_{REFL}		V_{REFH}	
Analog reference voltage supply current	<VREFON> = 1	I_{REF}	Vcc = +5 V ± 10%			3.7	mA
	<VREFON> = 0		Vcc = +5 V ± 10%		0.02	5.0	μA
Total tolerance (excludes quantization error)		E_T	Vcc = +5 V ± 10%		±1	±3	LSB

Note 1: 1LSB = (VREFH − VREFL) / 2^{10} [V]

Note 2: Power supply current ICC from the VCC pin includes the power supply current from the AVCC pin.

4.6 Event Counter (External Input Clocks: TI0, TI4, TI8, TI9, TIA, TIB)

Vcc = +5 V ± 10%, Ta = −40 to +85°C (fc = 8 to 24 MHz)

Parameter	Symbol	Variable		24 MHz		Unit
		Min	Max	Min	Max	
External input clock cycle	t_{VCK}	8x + 100		433		ns
External low-level input clock pulse width	t_{VCKL}	4x + 40		207		ns
External high-level input clock pulse width	t_{VCKH}	4x + 40		207		ns

4.7 Interrupt Operation

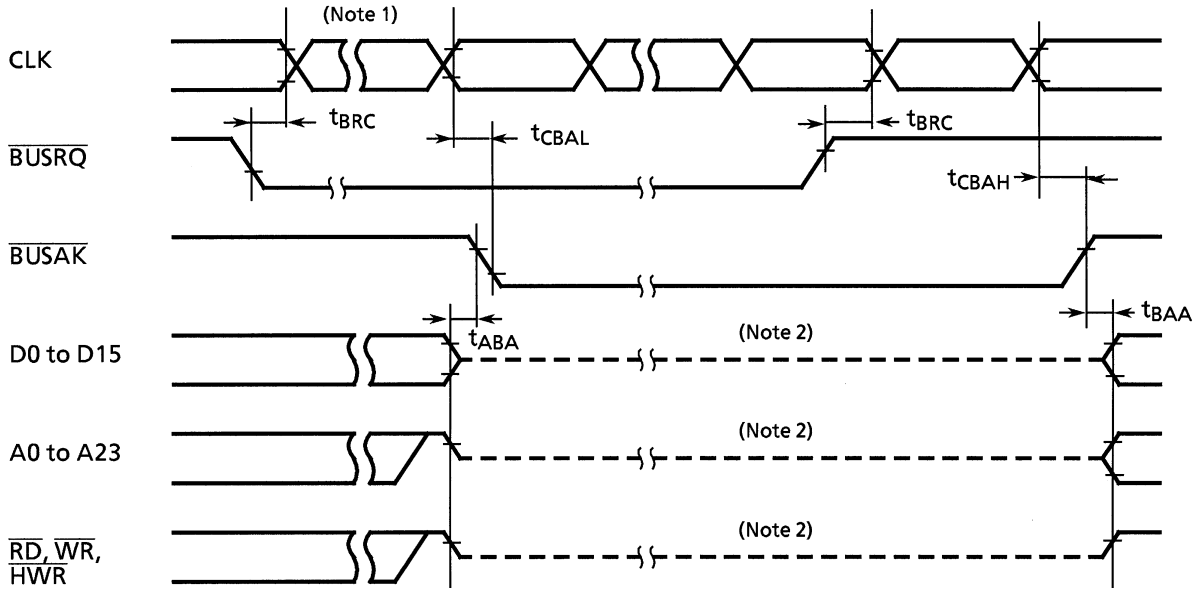
Vcc = +5 V ± 10%, Ta = −40 to +85°C (fc = 8 to 24 MHz)

Parameter	Symbol	Variable		24 MHz		Unit
		Min	Max	Min	Max	
$\overline{NMI}$, INT0 to 4 low-level pulse width	t_{INTAL}	4x		167		ns
$\overline{NMI}$, INT0 to 4 high-level pulse width	t_{INTAH}	4x		167		ns
INT5 to INT8 low-level pulse width	t_{INTBL}	8x + 100		433		ns
INT5 to INT8 high-level pulse width	t_{INTBH}	8x + 100		433		ns

4.8 Bus Request/Bus Acknowledge Timing

Vcc = +5 V ± 10%, Ta = −40 to +85°C (fc = 8 to 24 MHz)

Parameter	Symbol	Variable		24 MHz		Unit
		Min	Max	Min	Max	
$\overline{BUSRQ}$ setup time for CLK	t_{BRC}	120		120		ns
CLK→$\overline{BUSAK}$ fall	t_{CBAL}		2.0x + 120		203	ns
CLK→$\overline{BUSAK}$ rise	t_{CBAH}		0.5x + 40		61	ns
Time from output buffer off until $\overline{BUSAK}$ falling edge	t_{ABA}	0	80	0	80	ns
Time from $\overline{BUSAK}$ rising edge until output buffer on	t_{BAA}	0	80	0	80	ns



Note 1: When $\overline{BUSRQ}$ goes to low level to request bus release, if the current bus cycle is yet complete due to a wait, the bus is not released until the wait completes.

Note 2: The dotted line indicates only that the output buffer is off, not that the signal is at middle level. Immediately after bus release, the signal level prior to the bus release is held dynamically by the external load capacitance. Therefore, designs should allow for the fact that when using an external resistor or similar to fix the signal level while the bus is released, after bus release a delay occurs before the signal goes to its fixed level (due to the CR time constant). The internal programmable pull-up resistor continues to function in accordance with the internal signal level.