TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900 Series

TMP96CM40

TOSHIBA CORPORATION

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, "Points of Note and Restrictions".
Especially, take care below cautions.

CAUTION

How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, INT0), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of X1) with IDLE or STOP mode. (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

CMOS 16-bit Microcontrollers

TMP96CM40F

1. Outline and Device Characteristics

TMP96CM40F is high-speed advanced 16-bit microcontrollers developed for controlling medium to large-scale equipment. The TMP96C141BF does not have a ROM, the TMP96CM40F has a built-in ROM of 32K-byte, and the TMP96PM40 has a built-in OTP of 32K-byte.

TMP96CM40F is housed in an 80-pin flat package.

Device characteristics are as follows:

(1) Original 16-bit CPU
- TLCS-90 instruction mnemonic upward compatible.
- 16M-byte linear address space
- General-purpose registers and register bank system
- 16-bit multiplication / division and bit transfer/arithmetic instructions
- High-speed micro DMA : 4 channels (1.6 μs/2 bytes @ 20 MHz)

(2) Minimum instruction execution time : 200 ns @ 20 MHz

(3) Internal RAM : 1 Kbyte
Internal ROM : 32 Kbyte

(4) External memory expansion
- Can be expanded up to16 Mbytes (for both programs and data).
- Can mix 8- and 16-bit external data buses.

(5) 8-bit timers : 2 channels

(6) 8-bit PWM timers : 2 channels

(7) 16-bit timers : 2 channels

(8) Pattern generators : 4 bits, 2 channels

(9) Serial interface : 2 channels

(10) 10-bit A/D converter : 4 channels

(11) Watchdog timer

(12) Chip select/wait controller : 3 blocks

(13) Interrupt functions
- 3 CPU interrupts··· SWI instruction, priviledged violation, and Illegal instruction
- 14 internal interrupts
- 6 external interrupts

] 7-level priority can be set.

(14) I/O ports : 65 pins

(15) Standby function : 3 halt modes (RUN, IDLE, STOP)

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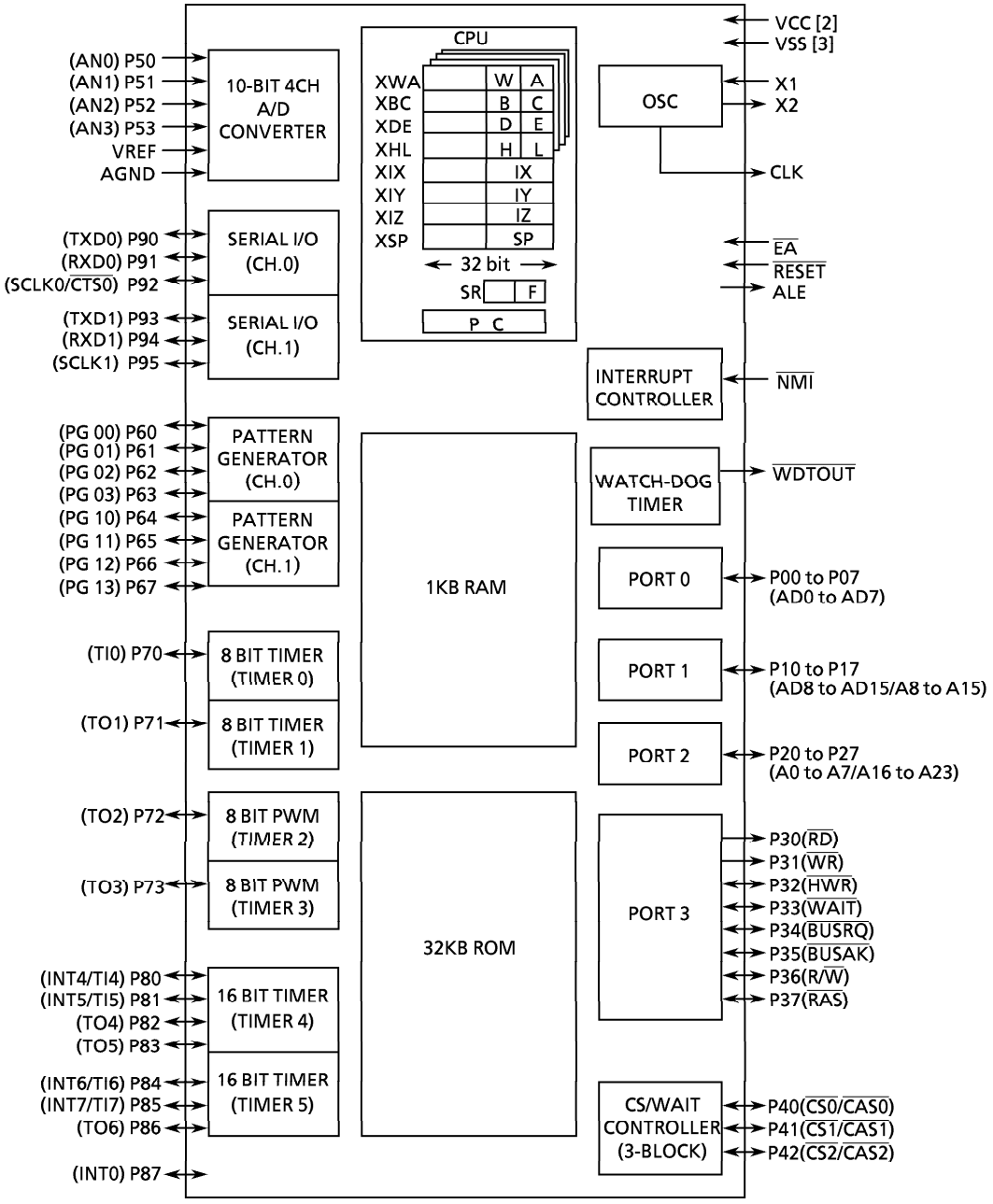


Figure1 TMP96CM40 Block Diagram

2. Pin Assignment and Functions

The assignment of input / output pins for TMP96CM40, their name and outline functions are described below.

2.1 Pin Assignment

Figure 2.1 shows pin assignment of TMP96CM40F.

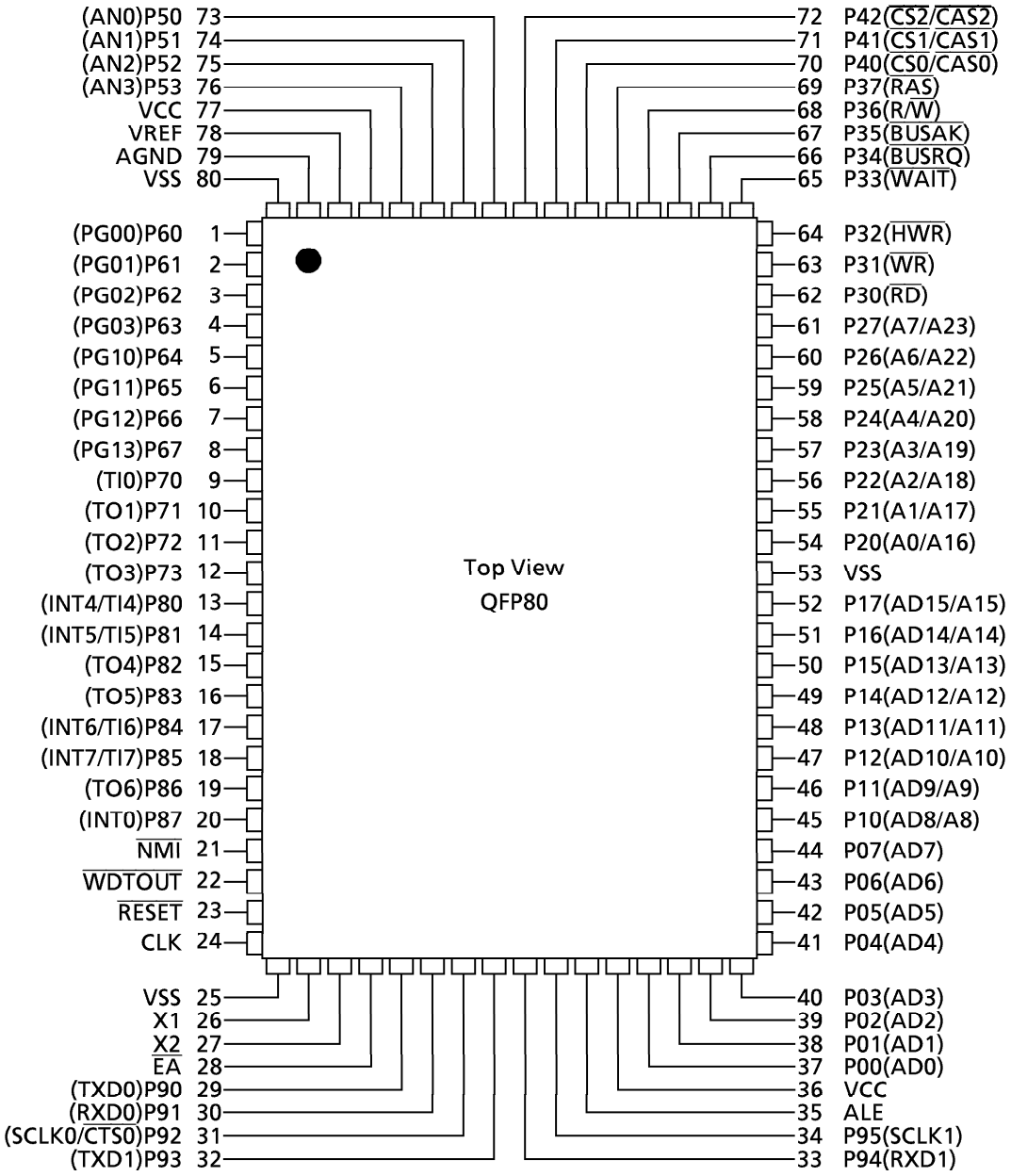


Figure 2.1 Pin Assignment (80-pin QFP)

2.2 Pin Names and Functions

The names of input/output pins and their functions are described below.

Table 2.2 Pin Names and Functions.

Pin name	Number of pins	I/O	Functions
P00 to P07 AD0 to AD7	8	I/O Tri-state	Port 0: I/O port that allows I/O to be selected on a bit basis Address/data (lower): 0 to 7 for address/data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O Tri-state Output	Port 1: I/O port that allows I/O to be selected on a bit basis Address data (upper): 8 to 15 for address/data bus Address: 8 to 15 for address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows selection of I/O on a bit basis (with pull-down resistor) Address: 0 to 7 for address bus Address: 16 to 23 for address bus
P30 $\overline{RD}$	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory
P31 $\overline{WR}$	1	Output Output	Port 31: Output port Write: Strobe signal for writing data on pins AD0 to 7
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data on pins AD8 to 15
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait
P34 $\overline{BUSRQ}$	1	I/O Input	Port34: I/O port (with pull-up resistor) Bus request: Signal used to request high impedance for AD0 to 15, A0 to 23, $\overline{RD}$, $\overline{WR}$,$\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$, $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins. (For external DMAC)
P35 $\overline{BUSAK}$	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus acknowledge: Signal indicating that AD0 to 15, A0 to 23, $\overline{RD}$, $\overline{WR}$,$\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$, $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins are at high impedance after receiving BUSRQ. (For external DMAC)
P36 R/$\overline{W}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/write: 1 represents read or dummy cycle; 0, write cycle.
P37 $\overline{RAS}$	1	I/O Output	Port 37: I/O port (with pull-up resistor) Row address strobe: Outputs RAS strobe for DRAM.
P40 $\overline{CS0}$ $\overline{CAS0}$	1	I/O Output Output	Port 40: I/O port (with pull-up resistor) Chip select 0: Outputs 0 when address is within specified address area. Column address strobe 0: Outputs CAS strobe for DRAM when address is within specified address area.

Note : With the external DMA controller, this device's built-in memory or built-in I/O cannot be accessed using the $\overline{BUSRQ}$ and $\overline{BUSAK}$ pins.

Pin name	Number of pins	I/O	Functions
P41 $\overline{CS1}$ $\overline{CAS1}$	1	I/O Output Output	Port 41: I/O port (with pull-up resistor) Chip select 1: Outputs 0 if address is within specified address area. Column address strobe 1: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P42 $\overline{CS2}$ $\overline{CAS2}$	1	I/O Output Output	Port 42: I/O port (with pull-down resistor) (Note) Chip select 2: Outputs 0 if address is within specified address area. Column address strobe 2: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P50 to P53 AN0 to AN3	4	Input Input	Port 5: Input port Analog input: Input to A/D converter
VREF	1	Input	Pin for reference voltage input to A/D converter
AGND	1	Input	Ground pin for A/D converter
P60 to P63 PG00 to PG03	4	I/O Output	Ports 60 to 63: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor) Pattern generator ports: 00 to 03
P64 to P67 PG10 to PG13	4	I/O Output	Ports 64 to 67: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor) Pattern generator ports: 10 to 13
P70 TI0	1	I/O Input	Port 70: I/O port (with pull-up resistor) Timer input 0: Timer 0 input
P71 TO1	1	I/O Output	Port 71: I/O port (with pull-up resistor) Timer output 1: Timer 0 or 1 output
P72 TO2	1	I/O Output	Port 72: I/O port (with pull-up resistor) PWM output 2: 8-bit PWM timer 2 output
P73 TO3	1	I/O Output	Port 73: I/O port (with pull-up resistor) PWM output 3: 8-bit PWM timer 3 output
P80 TI4 INT4	1	I/O Input Input	Port 80: I/O port (with pull-up resistor) Timer input 4: Timer 4 count/capture trigger signal input Interrupt request pin 4: Interrupt request pin with programmable rising/falling edge
P81 TI5 INT5	1	I/O Input Input	Port 81: I/O port (with pull-up resistor) Timer input 5: Timer 4 count/capture trigger signal input Interrupt request pin 5: Interrupt request pin with rising edge
P82 TO4	1	I/O Output	Port 82: I/O port (with pull-up resistor) Timer output 4: Timer 4 output pin
P83 TO5	1	I/O Output	Port 83: I/O port (with pull-up resistor) Timer output 5: Timer 4 output pin

Note : Case of the settable $\overline{CS2}$ or $\overline{CAS2}$; when TMP96CM40F is bus release, this pin is not added the internal pull-down resistor but is added the internal pull-up resistor.

Pin name	Number of pins	I/O	Functions
P84 TI6 INT6	1	I/O Input Input	Port 84: I/O port (with pull-up resistor) Timer input 6: Timer 5 count/capture trigger signal input Interrupt request pin 6: Interrupt request pin with programmable rising/falling edge
P85 TI7 INT7	1	I/O Input Input	Port 85: I/O port (with pull-up resistor) Timer input 7: Timer 5 count/capture trigger signal input Interrupt request pin 7: Interrupt request pin with rising edge
P86 TO6	1	I/O Output	Port 86: I/O port (with pull-up resistor) Timer output 6: Timer 5 output pin
P87 INT0	1	I/O Input	Port 87: I/O port (with pull-up resistor) Interrupt request pin 0: Interrupt request pin with programmable level/rising edge
P90 TXD0	1	I/O Output	Port 90: I/O port (with pull-up resistor) Serial send data 0
P91 RXD0	1	I/O Input	Port 91: I/O port (with pull-up resistor) Serial receive data 0
P92 $\overline{CTS0}$ SCLK0	1	I/O Input I/O	Port 92: I/O port (with pull-up resistor) Serial data send enable 0 (Clear to Send) Serial clock I/O 0
P93 TXD1	1	I/O Output	Port 93: I/O port (with pull-up resistor) Serial send data 1
P94 RXD1	1	I/O Input	Port 94: I/O port (with pull-up resistor) Serial receive data 1
P95 SCLK1	1	I/O I/O	Port 95: I/O port (with pull-up resistor) Serial clock I/O 1
$\overline{WDTOUT}$	1	Output	Watchdog timer output pin
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at rising edge by program.
CLK	1	Output	Clock output: Outputs「X1 ÷ 4」clock. Pulled-up during reset.
$\overline{EA}$	1	Input	External access: 0 should be inputted with TMP96C141B. 1, with TMP96CM40 / TMP96PM40.
ALE	1	Output	Address latch enable
$\overline{RESET}$	1	Input	Reset: Initializes LSI. (With pull-up resistor)
X1/X2	2	I/O	Oscillator connecting pin
VCC	2		Power supply pin (+ 5 V) (All Vcc pins should be connected with the power supply pin.)
VSS	3		GND pin (0 V) (All Vss pins should be connected with GND (0 V).)

Note : Pull-up/pull-down resistor can be released from the pin by software (except the $\overline{RESET}$ pin).

3. Operation

This section describes the functions and basic operations of TMP96M40 device. The function of CPU and internal I/O devices are the same function as TMP96C141B.
Check the 「7. Care Points and Restriction of TMP96C141B 」because of the Care described. Regarding the function of TMP96CM40 (not described), see the part of TMP96C141B.

TMP96C141B/TMP96CM40/TMP96PM40 have much the same function but they are different from following points.

Parameter	TMP96C141B	TMP96CM40	TMP96PM40
Interrnal ROM	Not exist	Mask ROM32 Kbyte	PROM32 Kbyte
P00 to P07, AD0 to AD7	Only AD0 to AD7	After reset P00 to P07	
P10 to P17, AD8 to AD15, A8 to A15	Only AD8 to AD15	After reset P10 to P17	
P30, $\overline{RD}$	Only $\overline{RD}$	After reset P30	
P31, $\overline{WR}$	Only $\overline{WR}$	After reset P31	
Pin state at the bus release	TMP96C141B see Table 3.5 (1)	TMP96CM40 see Table 3.3 (1)	

3.1 CPU

TMP96CM40 device has a built-in high-performance 16-bit CPU (900-CPU). (For CPU operation, see TLCS-900 CPU in the previous section.)

3.2 Memory Map

TMP96CM40 has two register modes. One is a minimum mode; in this mode, the area of program memory is 64 Kbytes maximum. The other is a maximum mode; in this mode, The area of program memory is 16 Mbytes maximum.

Both minimum and maximum modes are the data memory area of 16 Mbytes maximum.

That is, the program memory can locate 0H to FFFFH in minimum mode and can locate 0H to FFFFFFH in maximum mode.

(1) Internal ROM

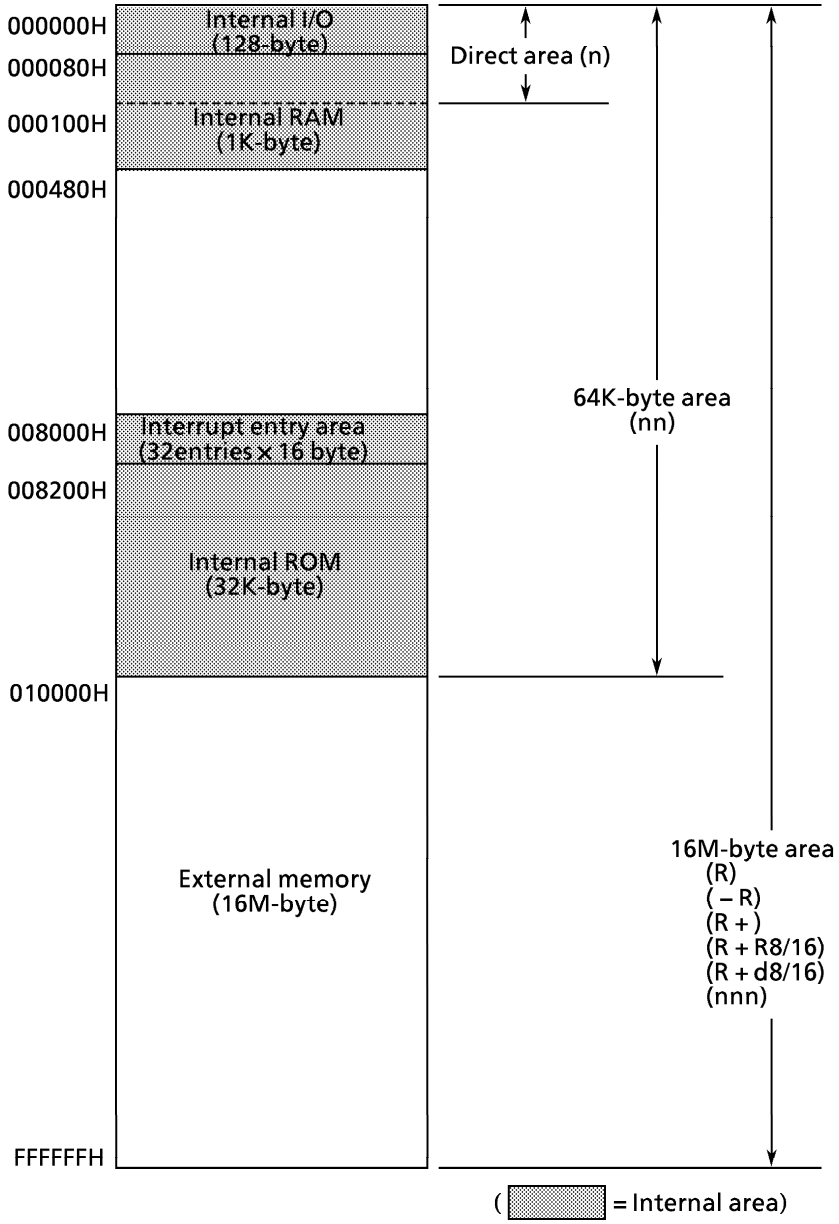
TMP96CM40 has the ROM of 32 Kbytes. This ROM is located to 80000H to FFFFH. After the RESET operation, instruction execution starts from address 8000H.
A part of the internal ROM area (8000H to 81FFH) is interrupt entry area.

(2) Internal RAM

TMP96CM40 has the RAM of 1 Kbytes. This RAM is located to 80H to 47FH. The CPU can access the part of RAM (80H to FFH, 128 bytes) with using the short instruction code of direct addressing mode.

Memory Map

Figure 3.1 is a memory map of the TMP96CM40.



Note : The start address after reset is 8000H. Resetting sets the stack pointer (XSP) on the system mode side to 100H.

Figure3.1 Memory map

3.3 Functions of Ports

The TMP96CM40/TMP96PM40 has 65 bits for I/O ports.

These port pins have I/O functions for the built-in CPU and internal I/Os as well as general-purpose I/O port functions. Table 3.3 lists the function of each port pin.

Table 3.3 Functions of Ports (R: ↑ = With programmable pull-up resistor, ↓ = With programmable pull-down)

Port name	Pin name	Number of pins	Direction	R	Direction setting unit	Pin name for built-in function
Port0	P00 to P07	8	I/O	–	Bit	AD0 to AD7
Port1	P10 to P17	8	I/O	–	Bit	AD8 to AD15/A8 to A15
Port2	P20 to P27	8	I/O	↓	Bit	A0 to A7/A16 to A23
Port3	P30	1	Output	–	(Fixed)	$\overline{RD}$
	P31	1	Output	–	(Fixed)	$\overline{WR}$
	P32	1	I/O	↑	Bit	$\overline{HWR}$
	P33	1	I/O	↑	Bit	$\overline{WAIT}$
	P34	1	I/O	↑	Bit	$\overline{BUSRQ}$
	P35	1	I/O	↑	Bit	$\overline{BUSAK}$
	P36	1	I/O	↑	Bit	R/$\overline{W}$
	P37	1	I/O	↑	Bit	$\overline{RAS}$
Port4	P40	1	I/O	↑	Bit	$\overline{CS0}$ / $\overline{CAS0}$
	P41	1	I/O	↑	Bit	$\overline{CS1}$ / $\overline{CAS1}$
	P42	1	I/O	↓	Bit	$\overline{CS2}$ / $\overline{CAS2}$
Port5	P50 to P53	4	Input	–	(Fixed)	AN0 to AN3
Port6	P60 to P67	8	I/O	↑	Bit	PG00 to PG03, PG10 to PG13
Port7	P70	1	I/O	↑	Bit	TI0
	P71	1	I/O	↑	Bit	TO1
	P72	1	I/O	↑	Bit	TO2
	P73	1	I/O	↑	Bit	TO3
Port8	P80	1	I/O	↑	Bit	TI4/INT4
	P81	1	I/O	↑	Bit	TI5/INT5
	P82	1	I/O	↑	Bit	TO4
	P83	1	I/O	↑	Bit	TO5
	P84	1	I/O	↑	Bit	TI6/INT6
	P85	1	I/O	↑	Bit	TI7/INT7
	P86	1	I/O	↑	Bit	TO6
	P87	1	I/O	↑	Bit	INT0
Port9	P90	1	I/O	↑	Bit	TXD0
	P91	1	I/O	↑	Bit	RXD0
	P92	1	I/O	↑	Bit	$\overline{CTS0}$ / SCLK0
	P93	1	I/O	↑	Bit	TXD1
	P94	1	I/O	↑	Bit	RXD1
	P95	1	I/O	↑	Bit	SCLK1

I/O port Setting

X : Don't care

Port	Pin Name	Port (I/O) or FUnction	I/O Register		
			Pn	PnCR	PnFC
Port 0	P0 (0 : 7)	Input Port	×	0	–
		Output Port	×	1	
		AD (0 : 7) Bus	×	×	
Port 1	P1 (0 : 7)	Input Port	×	0	0
		Output Port	×	1	0
		AD (8 : 15) Bus	×	0	1
		A (8 : 15) Output	×	1	0
Port 2	P2 (0 : 7)	Input Port (No Pull-down)	1	0	0
		Input Port (With Pull-down)	0	0	0
		Output Port	×	1	0
		A (0 : 7) Output	1	0	1
		A (16 : 23) Output	1	1	0
Port 3	P30	Output Port	×	–	0
		$\overline{RD}$ Output (at external access only)	1		1
		$\overline{RD}$ Output (always)	0		1
	P31	Output Port	×	–	0
		$\overline{WR}$ Output (at external access only)	×		1
	P3 (2 : 7)	Input Port (No Pull-up)	0	0	0
		Input Port (With Pull-up)	1	0	0
		Output Port	×	1	0
	P32	$\overline{HWR}$ Output	×	1	1
	P33	$\overline{WAIT}$ Input (No Pull-up)	0	0	–
		$\overline{WAIT}$ Input (With Pull-up)	1	0	
	P34	$\overline{BUSRQ}$ Input (No Pull-up)	0	0	1
		$\overline{BUSRQ}$ Input (With Pull-up)	1	0	1
	P35	$\overline{BUSAK}$ Output	×	1	1
	P36	R/$\overline{W}$ Output	×	1	1
	P37	$\overline{RAS}$ Output	×	1	1
Port 4	P4 (0 : 1)	Input Port (No Pull-up)	0	0	0
		Input Port (With Pull-up)	1	0	0
		Output Port	×	1	0
	P42	Input Port (No Pull-down)	1	0	0
		Input Port (With Pull-down)	0	0	0
		Output Port	×	1	0
	P40	$\overline{CS0}$ Output (Note 1)	×	1	1
	P41	$\overline{CS1}$ Output (Note 1)	×	1	1
	P42	$\overline{CS2}$ Output (Note 1)	×	1	1
Port 5	P5 (0 : 3)	Input Port	×	–	
		AN (0 : 3) Input (Note 2)	×		
Port 6	P6 (0 : 7)	Input Port (No Pull-up)	0	0	0
		Input Port (With Pull-up)	1	0	0
		Output Port	×	1	0
		PGn Output	×	1	1

Note 1: The function of P40 to P42 ($\overline{CS0}$ to $\overline{CS2}$, $\overline{CAS0}$ to $\overline{CAS2}$) is selected using CS/WAIT control register BnCS<BnCAS>.

Note 2: Select the input channels for the A/D converter in ADMOD2<ADCHn>.

Port	Pin Name	Port (I/O) or Function	I/O Register		
			Pn	PnCR	PnFC
Port 7	P7 (0 : 3)	Input Port (No Pull-up)	0	0	0
		Input Port (With Pull-up)	1	0	0
		Output Port	×	1	0
	P70	TI0 Input (No Pull-up)	0	0	–
		TI0 Input (With Pull-up)	1	0	
	P71	TO1Output	×	1	1
	P72	TO2Output	×	1	1
	P73	TO3Output	×	1	1
Port 8	P8 (0 : 7)	Input Port (No Pull-up)	0	0	0
		Input Port (With Pull-up)	1	0	0
		Output Port	×	1	0
	P80	TI4/INT4 Input (No Pull-up)	0	0	–
		TI4/INT4 Input (With Pull-up)	1	0	
	P81	TI5/INT5 Input (No Pull-up)	0	0	–
		TI5/INT5 Input (With Pull-up)	1	0	
	P84	TI6/INT6 Input (No Pull-up)	0	0	–
		TI6/INT6 Input (With Pull-up)	1	0	
	P85	TI7/INT7 Input (No Pull-up)	0	0	–
		TI7/INT7 Input (With Pull-up)	1	0	
	P82	TO4Output	×	1	1
	P83	TO5Output	×	1	1
	P86	TO6Output	×	1	1
	P87 (NOTE 3)	INT0 Input (No Pull-up)	0	0	–
		INT0 Input (With Pull-up)	1	0	
Port 9	P9 (0 : 5)	Input Port (No Pull-up)	0	0	0
		Input Port (With Pull-up)	1	0	0
		Output Port	×	1	0
	P90	TXD0Output	×	1	1
	P93	TXD1Output	×	1	1
	P91	RXD0 Input (No Pull-up)	0	0	–
		RXD0 Input (With Pull-up)	1	0	
	P94	RXD1 Input (No Pull-up)	0	0	–
		RXD1 Input (With Pull-up)	1	0	
	P92	SCLK0Output	×	1	1
		CTS0/SCLK0 Input (No Pull-up)	0	0	0
		CTS0/SCLK0 Input (With Pull-up)	1	0	0
	P95	SCLK1Output	×	1	1
		SCLK1 Input (No Pull-up)	0	0	0
		SCLK1 Input (With Pull-up)	1	0	0

Note 3: When P87 pin is used as INT0 pin, set IIMC<I0IE>to "1" (Input enable) .

Resetting makes the port pins listed below function as general-purpose I/O ports.
I/O pins programmable for input or output function as input ports.
To set port pins for built-in functions, a program is required.

※ Note about the Bus Release and programmable pull-up / down I/O ports.

When the bus is released ($\overline{BUSAK}$="0"), the output buffer of AD0 to 15, A0 to 23, control signal ($\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$, $\overline{CS0}$ / $\overline{CAS0}$ to $\overline{CS2}$ / $\overline{CAS2}$) is off and their state become high-impeadance.

However, the output of built-in programmable pull up / down resistors are kept before the bus is released. These programmable pull up / down resistors can be selected ON/OFF by programmable when they are used as the input ports.

The case of they are used as the output ports, they can not be selected ON/OFF by programmable.

The following is the pin state when the bus is released ($\overline{BUSAK}$="0")

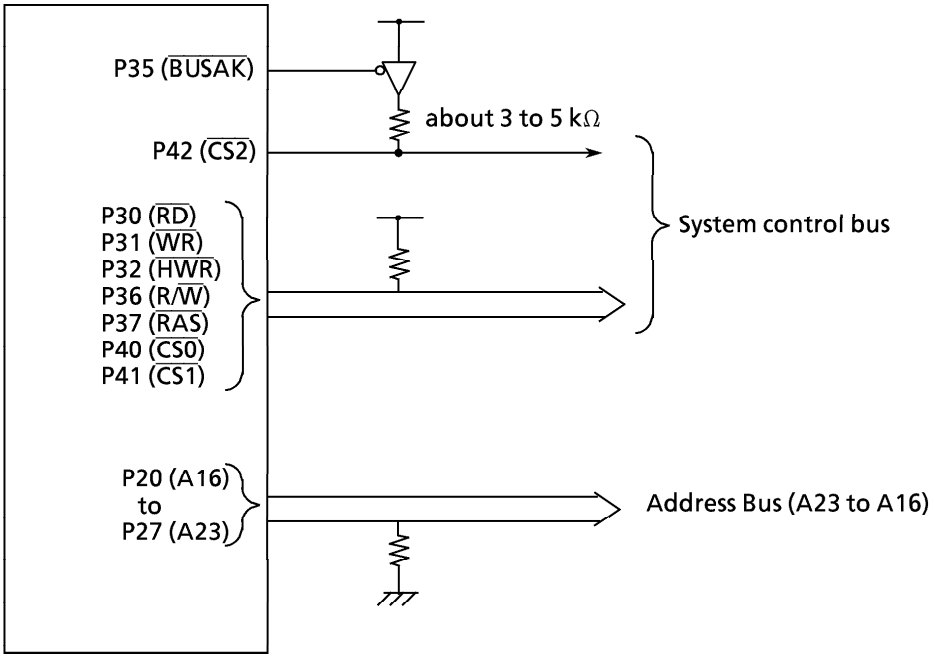
Table 3.3 (1) The condition of pins at the bus release ($\overline{BUSAK}$ = "L")

Pin Name	The Pin State (when the bus is released)	
	Used as the port	Used as the function
P00 to P07 (AD0 to AD7) P10 to P17 (AD8 to 15 / A8 to 15)	The state is not changed. (do not become to high-impedance (HZ).)	become high-impedance (HZ).
P30 ($\overline{RD}$) P31 ($\overline{WR}$)	becomes high-impedance (HZ).	←
P32 ($\overline{HWR}$) P37($\overline{RAS}$)	The output buffer is OFF. The programmable pull up resistor is ON the case of only the output latch is equal to "1".	The output buffer is OFF. The programmable pull up resistor is ON irrespective of the output latch.
P36 (R/$\overline{W}$) P40 ($\overline{CS0}$ / $\overline{CAS0}$) P41 ($\overline{CS1}$ / $\overline{CAS1}$)	↑	The output buffer is OFF. The programmable pull up resistor is undefined.
P42 ($\overline{CS2}$ / $\overline{CAS2}$)	The output buffer is OFF. The programmable pull down resistor is ON the case of only the output latch is equal to "0".	The output buffer is OFF. The programmable pull down resistor is undefined.
P20 to P27 (A16 to 23)	The state is not changed. (do not become to high-impedance (HZ).)	The output buffer is OFF. The programmable pull down resistor is ON the case of only the output latch is equal to "0".

The following are the example of the interface circuit about above pins the case of the bus releasing function is used.

When the bus is released, both internal memory and internal I/O can not be accessed. But the internal I/O continues to operate.

So, the watch dog timer also continues to run. Therefore, be care about bus releasing time and set the detection time of WDT.



Example of the interface circuit (The case of using bus releasing function)

The above circuit is necessary to fix the signal level the case of the bus is released.

Resetting sets P30 ($\overline{RD}$), P31 ($\overline{WR}$) to output, P40 ($\overline{CS0}$), P41 ($\overline{CS1}$), P32 ($\overline{HWR}$), P36 (R/$\overline{W}$), P37 ($\overline{RAS}$), and P35 ($\overline{BUSAK}$) to input with pull up resistor, P42 ($\overline{CS2}$) and P20 to 27 (A16 to 23) to input with pull down resistor.

The above circuit is necessary to fix the signal level after reset because of the external pull up resistor collisions with the internal pull down resistor.

The value of this external pull up resistor must be 3 to 5 kΩ. (the value of the internal pull down resistor is about 50 to 150 kΩ)

P20 to P27 (A16 to 23) also needs circuit like P42 ($\overline{CS2}$) to fix the signal level.

But for the P20 to 27 (A16 to 23) which does not have means (“L” is active), add pull down directly like above circuit.

3.3.1 Port 0 (P00 to P07)

Port 0 is an 8-bit general-purpose I/O port. I/O can be set on a bit basis using the control register P0CR. Resetting resets all bits of P0CR to 0 and sets Port 0 to input mode.

In addition to functioning as a general-purpose I/O port, Port 0 also functions as an address data bus (AD0 to 7). To access external memory, Port 0 functions as an address data bus (AD0 to 7) and all bits of the control register P0CR are cleared to 0.

Don't write 16 bit data in this port for TMP96CM40/TMP96PM40. Execute NOP instruction just after execution of instructions to write data in this port (which include read-modify-write instructions).

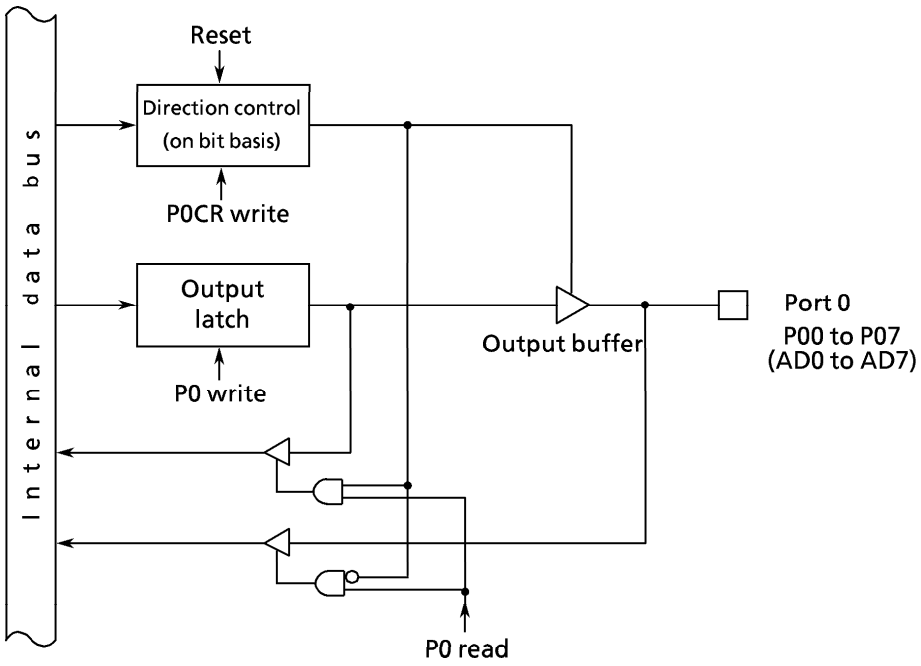


Figure 3.3 (1) Port 0

3.3.2 Port 1 (P10 to P17)

Port 1 is an 8-bit general-purpose I/O port. I/O can be set on a bit basis using control register P1CR and function register P1FC. Resetting resets all bits of output latch P1, control register P1CR, and function register P1FC to 0 and sets Port 1 to input mode.

In addition to functioning as a general-purpose I/O port, Port 1 also functions as an address data bus (AD8 to 15) or an address bus (A8 to 15).

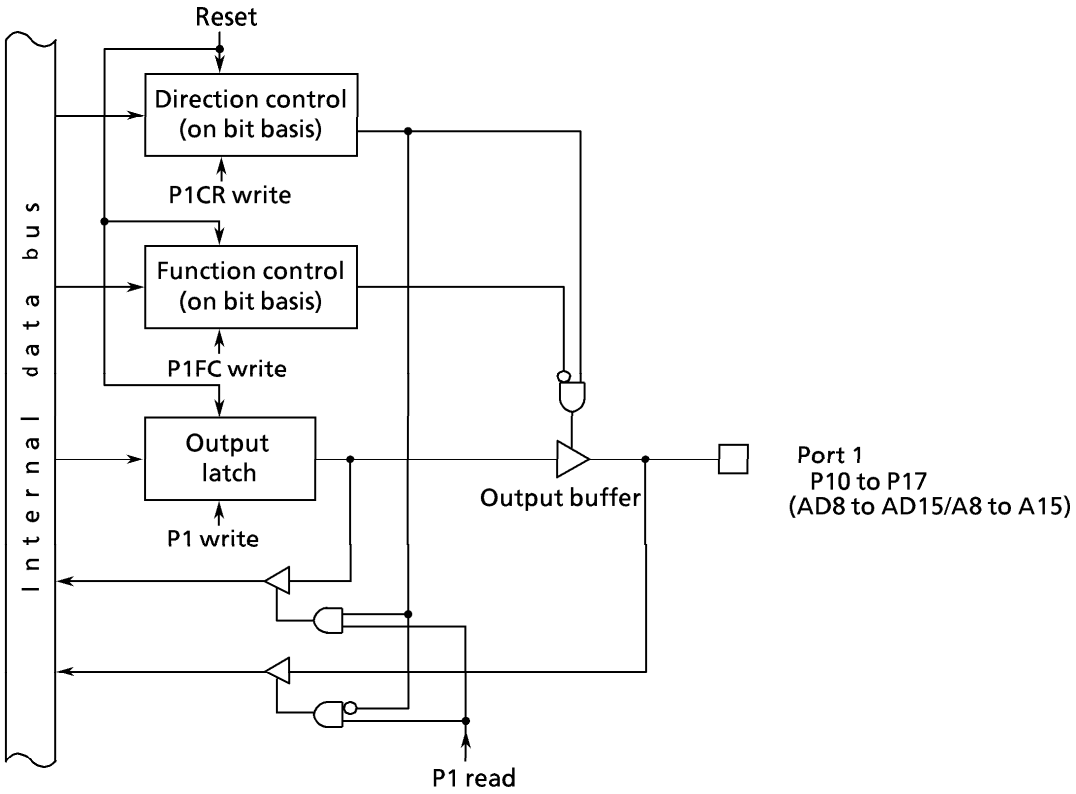


Figure 3.3 (2) Port 1

Port 0 Register

P0 (0000H)

	7	6	5	4	3	2	1	0
bit Symbol	P07	P06	P05	P04	P03	P02	P01	P00
Read/Write	R / W							
After reset	Input mode (Output latch register becomes undefined.)							

Port 0 Control Register

P0CR (0002H)

	7	6	5	4	3	2	1	0
bit Symbol	P07C	P06C	P05C	P04C	P03C	P02C	P01C	P00C
Read/Write	W							
After reset	0	0	0	0	0	0	0	0
Function	0:IN 1:OUT (At external access, Port 0 becomes AD7 to 0 and P0CR is cleared to 0.)							

→ Port 0 I/O setting

0	Input
1	Output

Port 1 Register

P1 (0001H)

	7	6	5	4	3	2	1	0
bit Symbol	P17	P16	P15	P14	P13	P12	P11	P10
Read/Write	R / W							
After reset	Input mode (Output latch register is cleared to "0".)							

Port 1 Control Register

P1CR (0004H)

	7	6	5	4	3	2	1	0
bit Symbol	P17C	P16C	P15C	P14C	P13C	P12C	P11C	P10C
Read/Write	W							
After reset	0	0	0	0	0	0	0	0
Function	<<See P1FC below.>>							

Port 1 Function Register

P1FC (0005H)

	7	6	5	4	3	2	1	0
bit Symbol	P17F	P16F	P15F	P14F	P13F	P12F	P11F	P10F
Read/Write	W							
After reset	0	0	0	0	0	0	0	0
Function	P1FC/P1CR = 00 : IN, 01 : OUT, 10 : AD15 to 8, 11 : A15 to 8							

→ Port 1 function setting

P1CR <P1XC> \ P1FC <P1XF>	0	1
0	Input port	Address data bus (AD15 to 8)
1	Output port	Address bus (A15 to 8)

Read-modify-write is prohibited for registers P0CR, P1CR, and P1FC.

Note : <P1XF> is bit X in register P1FC; <P1XC>, in register P1CR.

Figure 3.3 (3) Registers for Ports 0 and 1

3.3.3 Port 2 (P20 to P27)

Port 2 is an 8-bit general-purpose I/O port. I/O can be set on bit basis using the control register P2CR and function register P2FC. Resetting resets all bits of output latch P2, control register P2CR and function register P2FC to 0. It also sets Port 2 to input mode and connects a pull-down resistor.

In addition to functioning as a general-purpose I/O port, Port 2 also functions as an address data bus (A0 to 7) and an address bus (A16 to 23). Using Port 2 as address bus (A0 to 7 or A16 to 23), write "1" to output latches and off the programmable pull-down resistors. Setting to address bus, set P2CR and P2FC register in a row.

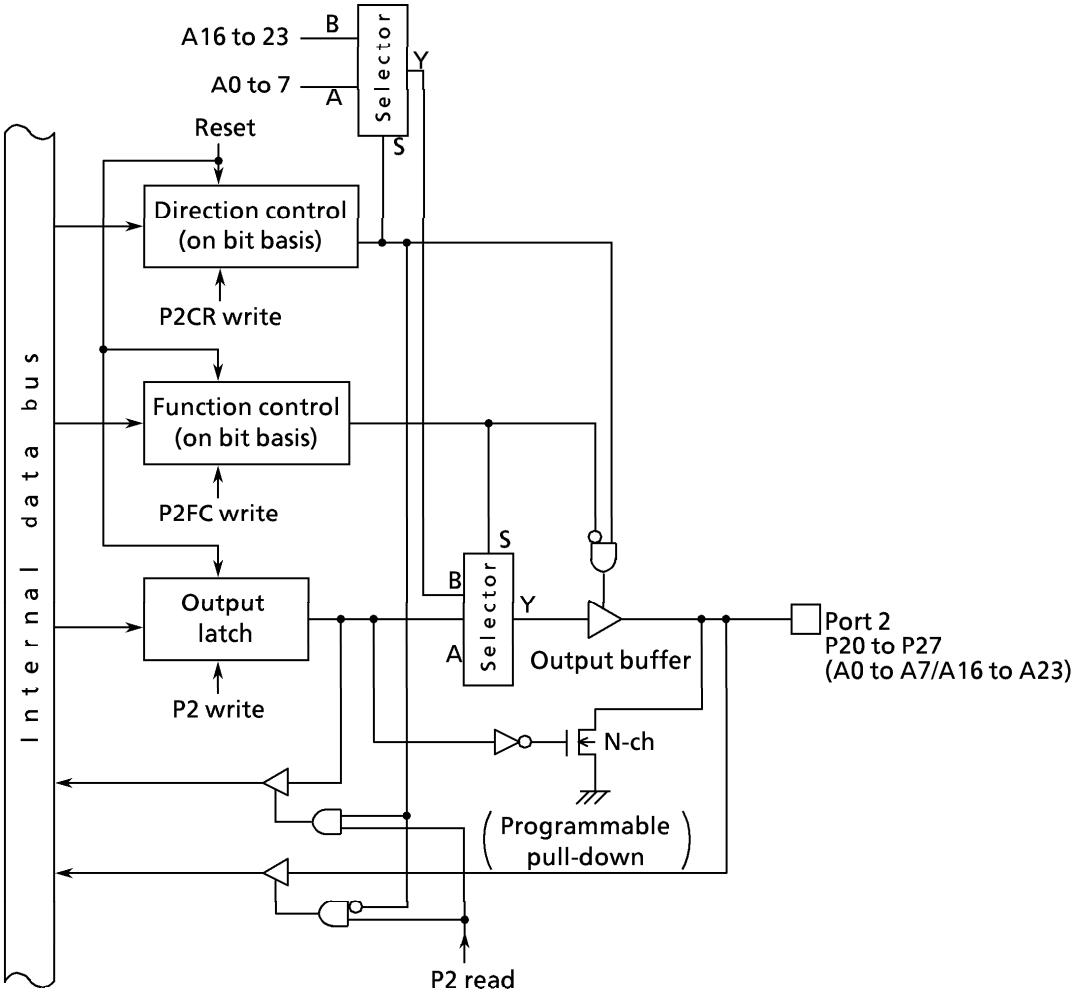


図 3.3 (4) Port 2

Port 2 Register

P2 (0006H)

	7	6	5	4	3	2	1	0
bit Symbol	P27	P26	P25	P24	P23	P22	P21	P20
Read/Write	R / W							
After reset	Input mode (Output latch register is cleared to "0".)							

Port 2 Control Register

P2CR (0008H)

	7	6	5	4	3	2	1	0
bit Symbol	P27C	P26C	P25C	P24C	P23C	P22C	P21C	P20C
Read/Write	W							
After reset	0	0	0	0	0	0	0	0
Function	<<See P2FC below.>>							

Port 2 Function Register

P2FC (0009H)

	7	6	5	4	3	2	1	0
bit Symbol	P27F	P26F	P25F	P24F	P23F	P22F	P21F	P20F
Read/Write	W							
After reset	0	0	0	0	0	0	0	0
Function	P2FC/P2CR = 00 : IN, 01 : OUT, 10 : A7 to 0, 11 : A23 to 16							

- Read-modify-write is prohibited for registers P2CR and P2FC.
- Read-modify-write is prohibited for controlling ON/OFF of the pull-down resistor for register P2.

Port 2 function setting

P2CR <P2XC> \ P2FC<P2XF>	0	1
0	Input	address bus (A7 to 0)
1	Output	address bus (A23 to 16)

Note : <P2XF> is bit X in register P2FC; <P2XC>; in register P2CR.
To set as an address bus A23 to 16, set P2FC after setting P2CR.

Figure 3.3 (5) Registers for Port 2

3.3.4 Port 3 (P30 to P37)

Port 3 is an 8-bit general-purpose I/O port.

I/O can be set on a bit basis, but note that P30 and P31 are used for output only. I/O is set using control register P3CR and function register P3FC. Resetting resets all bits of output latch P3, control register P3CR (bits 0 and 1 are unused), and function register P3FC to 0. Resetting also outputs 1 from P30 and P31, sets P32 to P37 to input mode, and connects a pull-up resistor.

In addition to functioning as a general-purpose I/O port, Port 3 also functions as an I/O for the CPU's control/status signal.

When P30 pin is defined as $\overline{RD}$ signal output mode (<P30F> = 1), clearing the output latch register <P30> to 0 outputs the $\overline{RD}$ strobe (used for the pseudo static RAM) from the P30 pin even when the internal address area is accessed.

If the output latch register <P30> remains 1, the $\overline{RD}$ strobe signal is output only when the external address area is accessed.

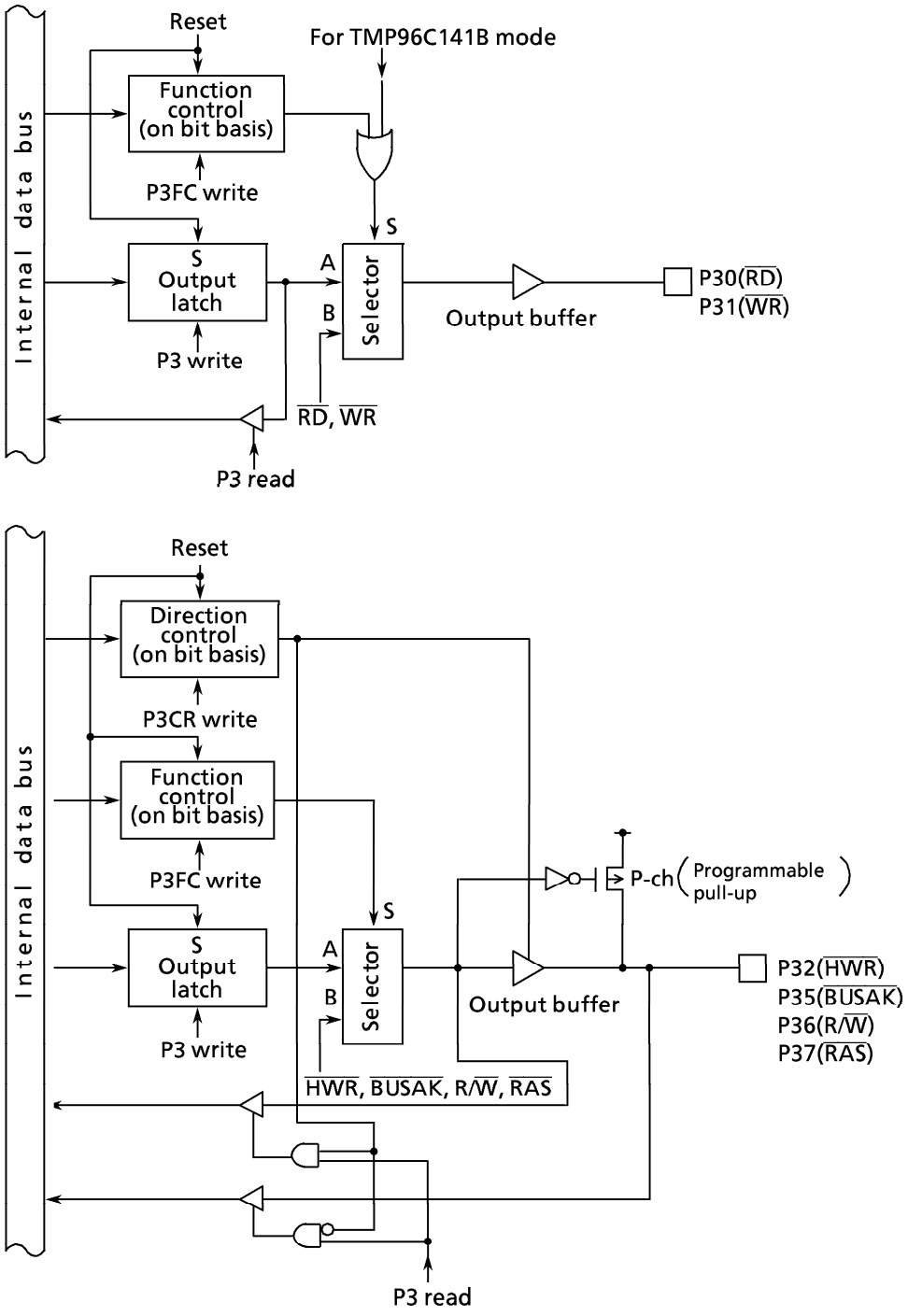


Figure 3.3 (6) Port 3 (P30, P31, P32, P35, P36, P37)

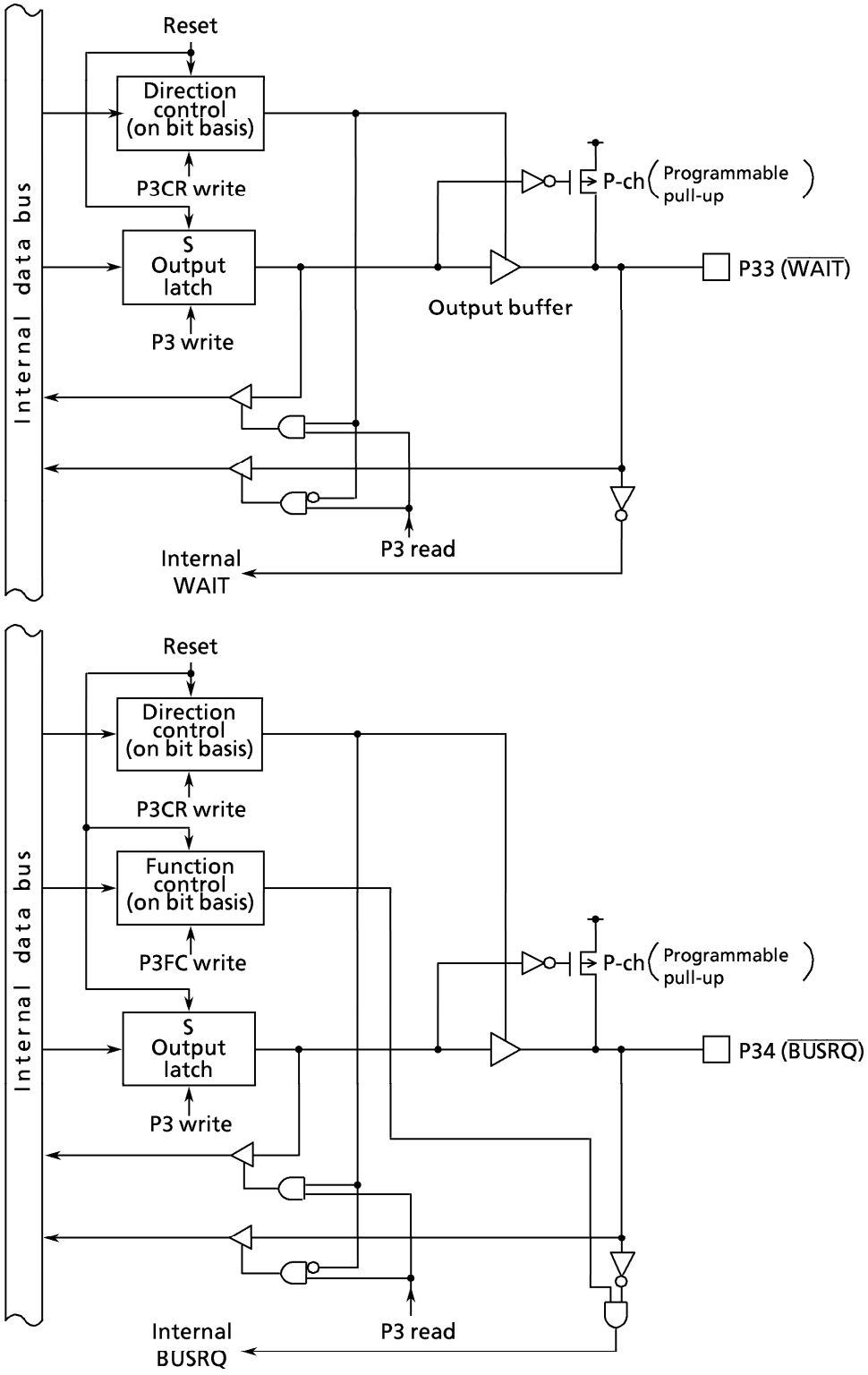


Figure 3.3 (7) Port3 (P33, P34)

Port 3 Register

P3 (0007H)

	7	6	5	4	3	2	1	0
bit Symbol	P37	P36	P35	P34	P33	P32	P31	P30
Read/Write	R/W							
After reset	Input mode (pulled-up)						Output mode	
	1	1	1	1	1	1	1	1

Port 3 Control Register

P3CR (000AH)

	7	6	5	4	3	2	1	0
bit Symbol	P37C	P36C	P35C	P34C	P33C	P32C		
Read/Write	W							
After reset	0	0	0	0	0	0		
	0 : IN 1 : OUT							

I/O setting

0	Input
1	Output

Port 3 Function Register

P3FC (000BH)

	7	6	5	4	3	2	1	0
bit Symbol	P37F	P36F	P35F	P34F		P32F	P31F	P30F
Read/Write	W							
After reset	0	0	0	0		0	0	0
Function	0 : PORT 1 : $\overline{RAS}$	0 : PORT 1 : R/$\overline{W}$	0 : PORT 1 : $\overline{BUSAK}$	0 : PORT 1 : $\overline{BUSRQ}$		0 : PORT 1 : $\overline{HWR}$	0 : PORT 1 : $\overline{WR}$	0 : PORT 1 : $\overline{RD}$

- Read-modify-write is prohibited for registers P3CR and P3FC.
- Read-modify-write is prohibited for controlling ON/OFF of *the pull-up resistor for* register P3.

$\overline{BUSRQ}$ setting

P3FC <P34F>	1
P3CR <P34C>	0

$\overline{BUSAK}$ setting

P3FC <P35F>	1
P3CR <P35C>	1

R/$\overline{W}$ setting

P3FC <P36F>	1
P3CR <P36C>	1

$\overline{RAS}$ setting

P3FC <P37F>	1
P3CR <P37C>	1

P30 ($\overline{RD}$) function setting

<P30> / <P30F>	0	1
0	"0" output	"1" output
1	Always $\overline{RD}$ output (for pseudo SRAM)	$\overline{RD}$ output only for external access

P31 ($\overline{WR}$) function setting

<P31> / <P31F>	0	1
0	"0" output	"1" output
1	$\overline{WR}$ output only for external access	

$\overline{HWR}$ setting

P3FC <P32F>	1
P3CR <P32C>	1

Note : When P33/$\overline{WAIT}$ pin is used as a $\overline{WAIT}$ pin, set P3CR<P33C> to "0" and Chip Select / WAIT control register <BnW1, 0> to "10".

Figure3.3 (8) Registers for Port 3

3.3.5 Port 4 (P40 to P42)

Port 4 is a 3-bit general-purpose I/O port. I/O can be set on a bit basis using control register P4CR and function register P4FC. Resetting does the following:

- Sets the P40 and P42 output latch registers to 1.
- Resets all bits of the P42 output latch register, the control register P4CR, and the function register P4FC to 0.
- Sets P40 and P41 to input mode and connects a pull-up resistor.
- Sets P42 to input mode and connects a pull-down resistor.

In addition to functioning as a general-purpose I/O port, Port 4 also functions as a chip select output signal ($\overline{CS0}$ to $\overline{CS2}$ or $\overline{CAS0}$ to $\overline{CAS2}$).

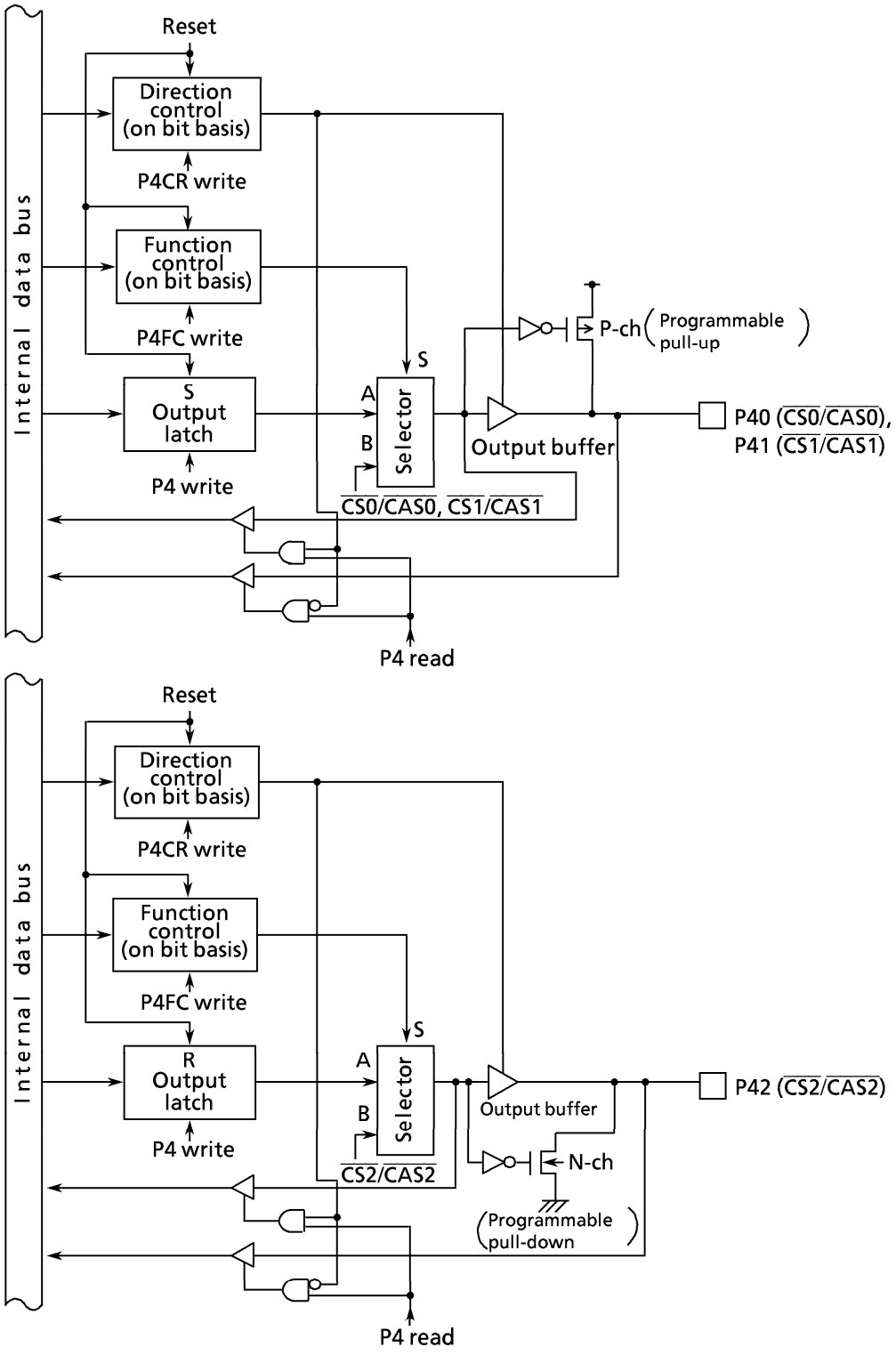


Figure 3.3 (9) Port 4

Port 4 Register

P4 (000CH)

	7	6	5	4	3	2	1	0
bit Symbol						P42C	P41C	P40C
Read/Write						R/W		
After reset						Input mode		
						0 (Pull-down)	1 (Pull-up)	1 (Pull-up)

Port 4 Control Register

P4CR (000EH)

	7	6	5	4	3	2	1	0
bit Symbol						P42C	P41C	P40C
Read/Write						W		
After reset						0	0	0
						0 : IN	1 : OUT	

I/O setting

0	Input
1	Output

Port 4 Function Register

P4FC (0010H)

	7	6	5	4	3	2	1	0
bit Symbol						P42F	P41F	P40F
Read/Write						W		
After reset						0	0	0
Function						0 : PORT	1 : $\overline{CS}/\overline{CAS}$	

- Read-modify-write is not possible for P4CR or P4FC.
- Read-modify-write is prohibited for controlling ON/OFF of the pull-up/pull-down resistor for register P4.

0	Port (P40)
1	$\overline{CS0}$ / $\overline{CAS0}$

0	Port (P41)
1	$\overline{CS1}$ / $\overline{CAS1}$

0	Port (P42)
1	$\overline{CS2}$ / $\overline{CAS2}$

Note : To output chip select signal ($\overline{CS0}/\overline{CAS0}$ to $\overline{CS2}/\overline{CAS2}$), set the corresponding bits of the control register P4CR and the function register P4FC.
The B0CS, B1CS, and B2CS registers of the chip select / wait controller are used to select the $\overline{CS}/\overline{CAS}$ function.

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Figure 3.3 (10) Registers for Port 4

3.3.6 Port 5 (P50 to P53)

Port 5 is a 4-bit input port, also used as an analog input pin.

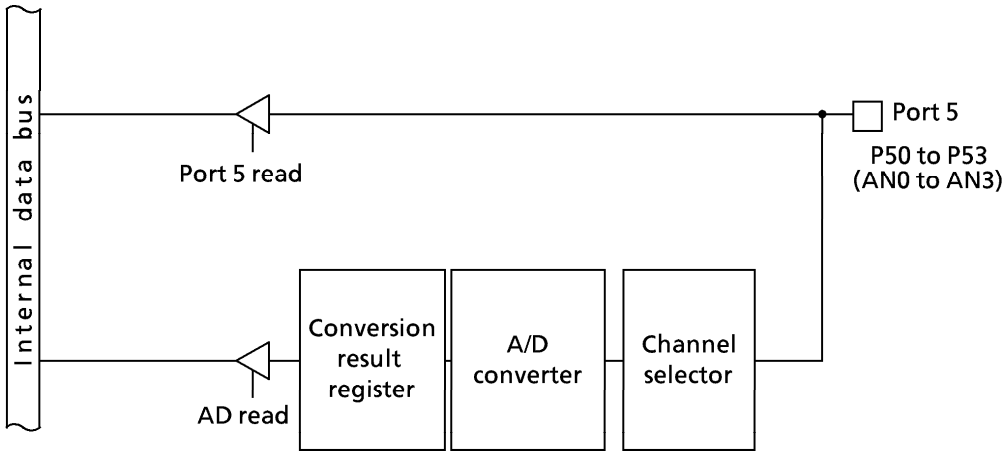


Figure3.3 (11) Port 5

Port 5 Register

		7	6	5	4	3	2	1	0
P5 (000DH)	bit Symbol					P53	P52	P51	P50
	Read/Write					R			
	After reset					Input mode			

Note : The input channel selection of A/D Converter is set by A/D Converter mode register ADMOD.

Figure 3.3 (12) Registers for Port 5

3.3.7 Port 6 (P60 to P67)

Port 6 is an 8-bit general-purpose I/O port. I/O can be set on bit basis. Resetting sets Port 6 as an input port and connects a pull-up resistor. It also sets all bits of the output latch to 1. In addition to functioning as a general-purpose I/O port, Port 6 also functions as a pattern generator PG0/PG1 output. PG0 is assigned to P60 to P63; PG1, to P64 to P67. Writing 1 in the corresponding bit of the port 6 function register (P6FC) enables PG output. Resetting resets the function register P6FC value to 0, and sets all bits to ports.

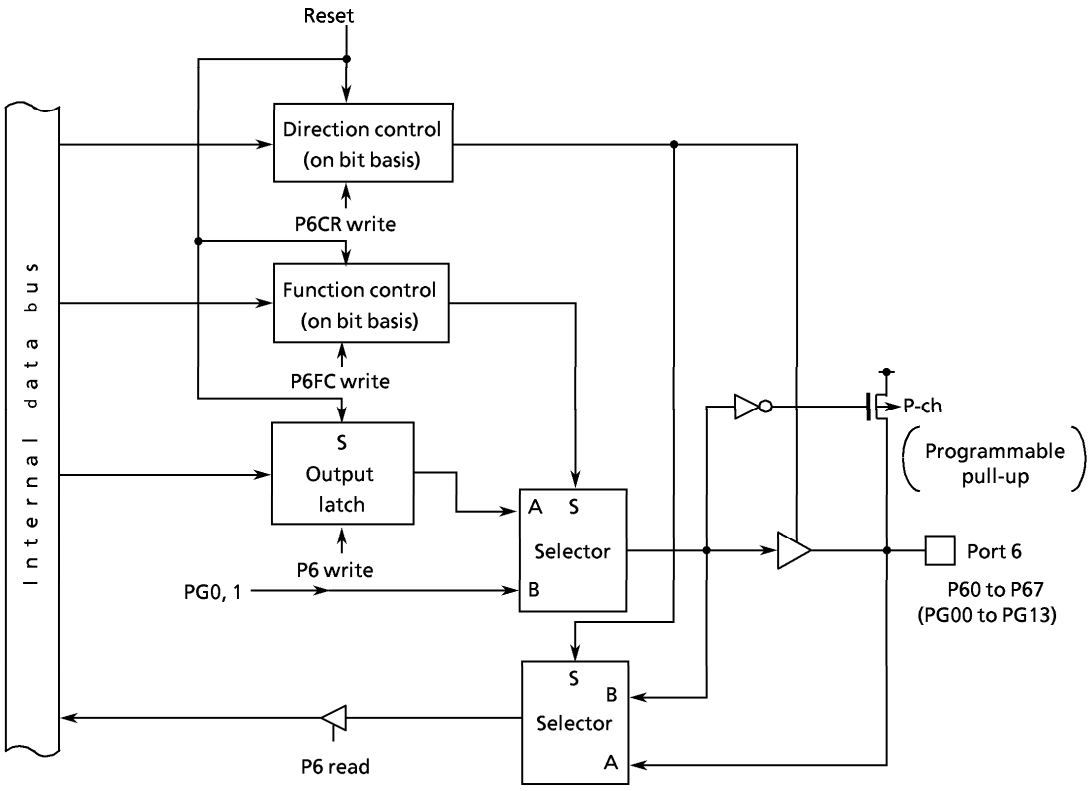


Figure 3.3 (13) Port 6

Port 6 Register

P6 (0012H)

	7	6	5	4	3	2	1	0
bit Symbol	P67	P66	P65	P64	P63	P62	P61	P60
Read/Write	R/W							
After reset	Input mode (Pull-up)							
	1	1	1	1	1	1	1	1

Port 6 Control Register

P6CR (0014H)

	7	6	5	4	3	2	1	0
bit Symbol	P67C	P66C	P65C	P64C	P63C	P62C	P61C	P60C
Read/Write	W							
After reset	0	0	0	0	0	0	0	0
Function	0 : IN				1 : OUT			

Port 6 I/O setting

0	Input
1	Output

Port 6 Function Register

P6FC (0016H)

	7	6	5	4	3	2	1	0
bit Symbol	P67F	P66F	P65F	P64F	P63F	P62F	P61F	P60F
Read/Write	W							
After reset	0	0	0	0	0	0	0	0
Function	0 : PORT		1 : PG1-OUT		0 : PORT		1 : PG0-OUT	

- Read-modify-write is prohibited for registers P6CR and P6FC.
- Read-modify-write is prohibited for controlling ON/OFF of the pull-up resistor for register P6.

Port 6 function setting

0	General-purpose port
1	Stepping motor control / Pattern generation port

Figure3.3 (14) Registers for Port 6

3.3.8 Port 7 (P70 to P73)

Port 7 is a 4-bit general-purpose I/O port. I/O can be set on bit basis. Resetting sets Port 7 as an input port and connects a pull-up resistor. In addition to functioning as a general-purpose I/O port, Port 70 also functions as an input clock pin TI0; Port 71 as an 8-bit timer output (TO1), Port 72 as a PWM0 output (TO2), and Port 73 as a PWM1 output (TO3) pin. Writing 1 in the corresponding bit of the Port 7 function register (P7FC) enables output of the timer. Resetting resets the function register P7FC value to 0, and sets all bits to ports.

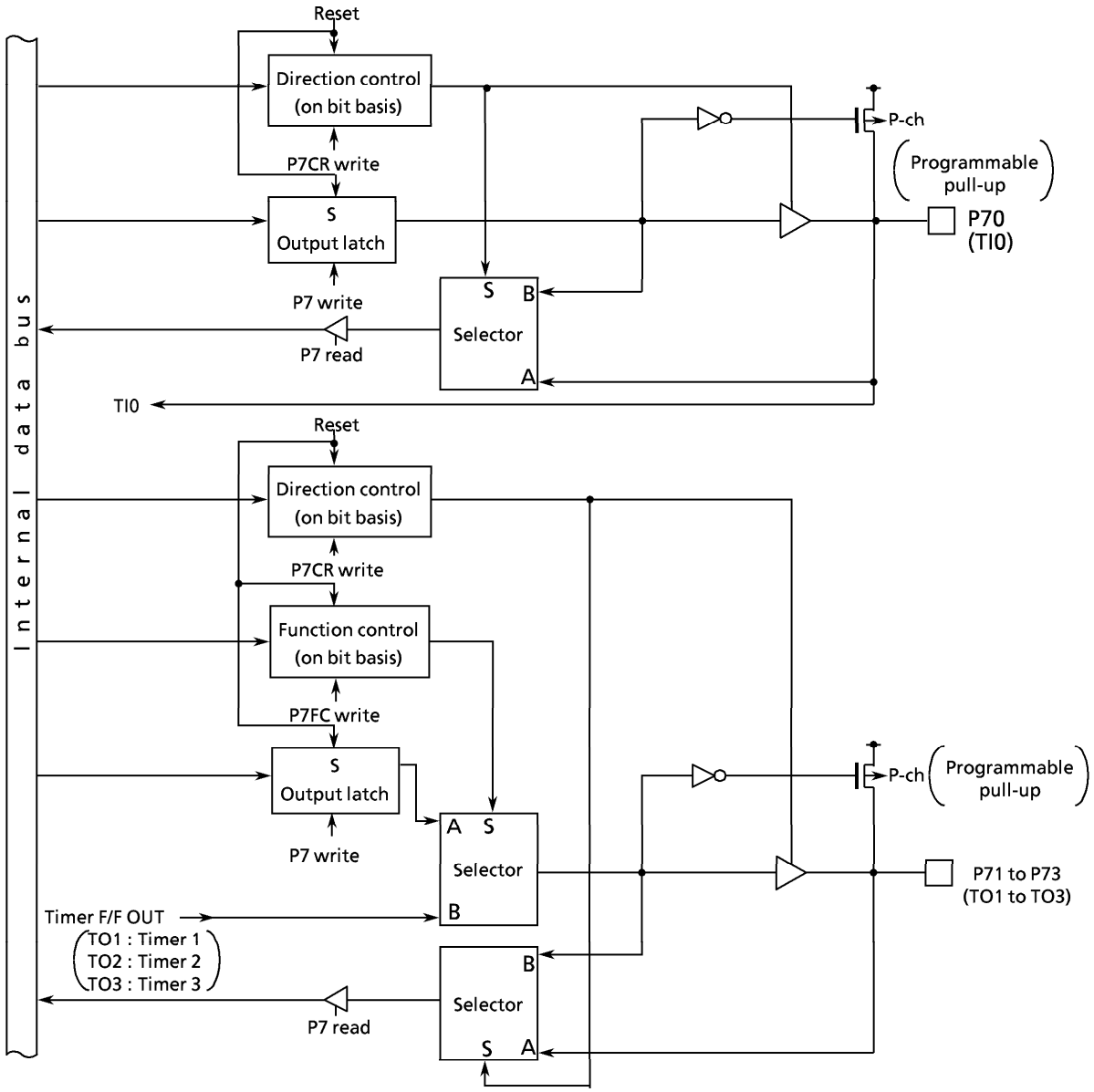


Figure 3.3 (15) Port 7

Port 7 Register

P7 (0013H)	7	6	5	4	3	2	1	0
bit Symbol					P73	P72	P71	P70
Read/Write					R/W			
After reset					Input mode (Pull-up)			
					1	1	1	1

Port 7 Control Register

P7CR (0015H)	7	6	5	4	3	2	1	0
bit Symbol					P73C	P72C	P71C	P70C
Read/Write					W			
After reset					0	0	0	0
Function					0 : IN		1 : OUT	

Port 7 I/O setting

0	Input
1	Output

Port 7 Function Register

P7FC (0017H)	7	6	5	4	3	2	1	0
bit Symbol					P73F	P72F	P71F	
Read/Write					W			
After reset					0	0	0	
Function					0 : PORT 1 : TO3	0 : PORT 1 : TO2	0 : PORT 1 : TO1	

- Read-modify-write is prohibited for registers P7CR and P7FC.
- Read-modify-write is prohibited for controlling ON/OFF of the pull-up resistor for register P7.

Setting P71 as TO1

P7FC <P71F>	1
P7CR <P71C>	1

Setting P72 as TO2

P7FC <P72F>	1
P7CR <P72C>	1

Setting P73 as TO3

P7FC <P73F>	1
P7CR <P73C>	1

Note : P70/TI0 pin does not have a register changing PORT/FUNCTION.
For example, when it is used as an input port (P70), the input signal for P70 is inputted to 8bit Timer 0 as a timer input 0 (TI0).

Figure3.3 (16) Registers for Port 7

3.3.9 Port 8 (P80 to P83)

Port 8 is an 8-bit general-purpose I/O port. I/O can be set on a bit basis. Resetting sets Port 8 as an input port and connects a pull-up resistor. It also sets all bits of the output latch register P8 to 1. In addition to functioning as a general-purpose I/O port, Port 8 also functions as an input for 16-bit timer 4, 5 clocks, an output for 16-bit timer F/F 4, 5, and 6 output, and an input for INT0. Writing 1 in the corresponding bit of the Port 8 function register (P8FC) enables those functions. Resetting resets the function register P8FC value to 0 and sets all bits to ports.

(1) P80 to P86

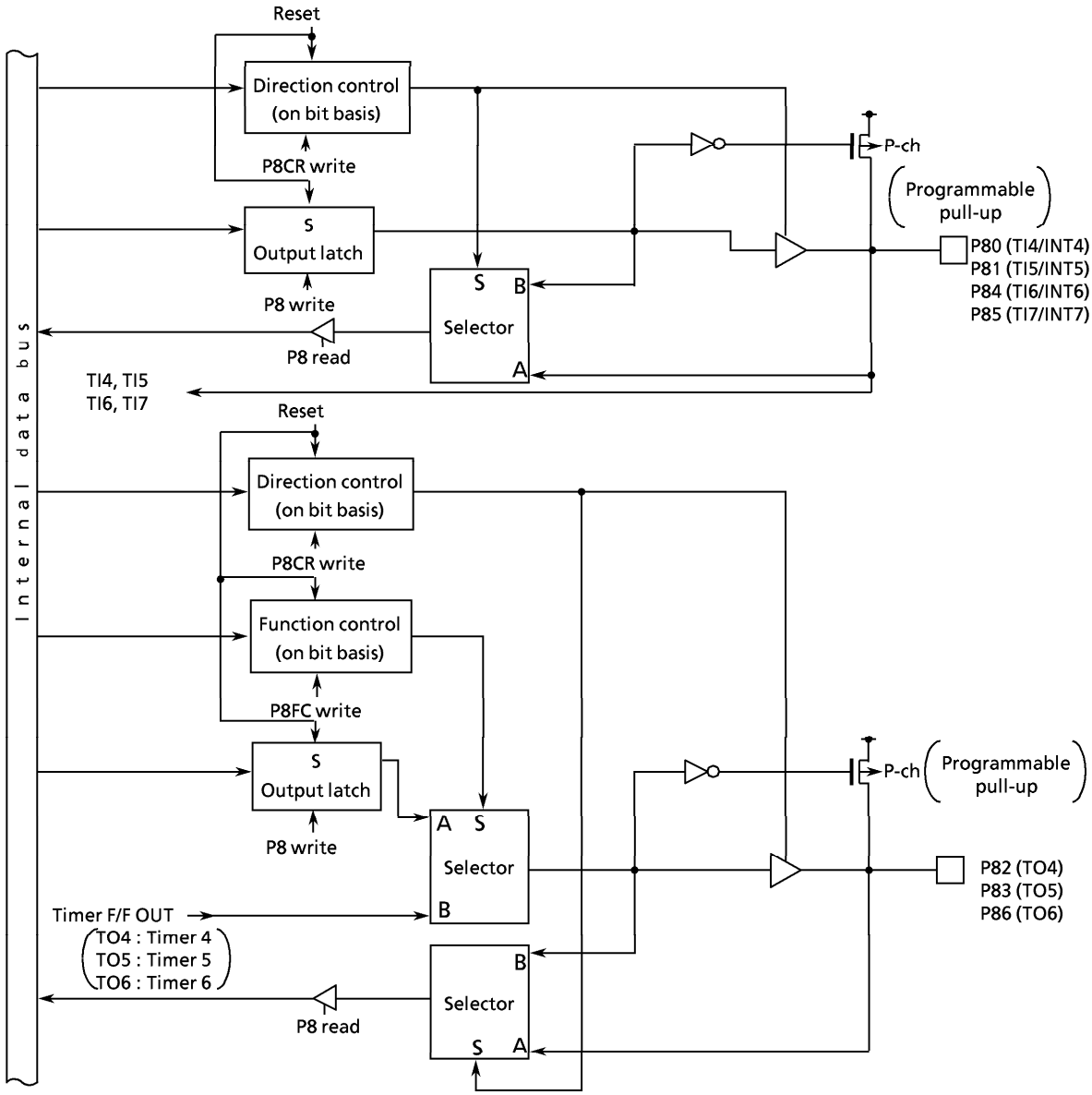


Figure 3.3 (17) Port 8 (P80 to P86)

(2) P87 (INT0)

Port 87 is a general-purpose I/O port, and also used as an INT0 pin for external interrupt request input.

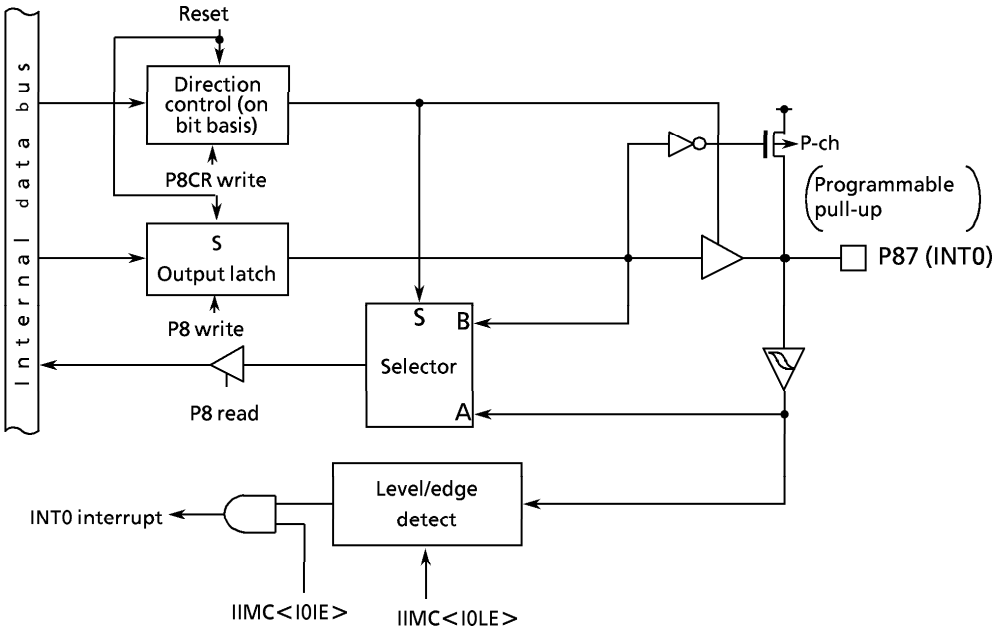


Figure 3.3 (18) Port 87

Port 8 Register

P8 (0018H)

	7	6	5	4	3	2	1	0
bit Symbol	P87	P86	P85	P84	P83	P82	P81	P80
Read/Write	R/W							
After reset	Input mode							
	1	1	1	1	1	1	1	1

Port 8 Control Register

P8CR (001AH)

	7	6	5	4	3	2	1	0
bit Symbol	P87C	P86C	P85C	P84C	P83C	P82C	P81C	P80C
Read/Write	W							
After reset	0	0	0	0	0	0	0	0
Function	0 : IN				1 : OUT			

Port 8 I/O setting

0	Input
1	Output

Port 8 Function Register

P8FC (001CH)

	7	6	5	4	3	2	1	0
bit Symbol		P86F			P83F	P82F		
Read/Write		W			W	W		
After reset		0			0	0		
Function		0 : PORT 1 : TO6			0 : PORT 1 : TO5	0 : PORT 1 : TO4		

- Read-modify-write is prohibited for registers P8CR and P8FC.
- Read-modify-write is prohibited for controlling ON/OFF of the pull-up resistor for register P8.

Setting P82 as TO4

P8FC <P82F>	1
P8CR <P82C>	1

Setting P83 as TO5

P8FC <P83F>	1
P8CR <P83C>	1

Setting P84 as TO6

P8FC <P86F>	1
P8CR <P86C>	1

Note : P80/TI4, P81/TI5, P84/TI6, P85/TI7 pins do not have a register changing PORT/FUNCTION. Therefore this is the same as P70/TI0 pin.
When P87/INT0 pin is used as an INT0 pin, set P8CR<P87C> to "0" and IIMC<I0IE> to "1".

Figure3.3 (19) Registers for Port 8

3.3.10 Port 9 (P90 to P95)

Port 9 is a 6-bit general-purpose I/O port. I/Os can be set on a bit basis.

Resetting sets Port 9 to an input port and connects a pull-up resistor.

It also sets all bits of the output latch register to 1.

In addition to functioning as a general-purpose I/O port, Port 9 can also function as an I/O for serial channels 0 and1. Writing 1 in the corresponding bit of the port 9 function register (P9FC) enables this function.

Resetting resets the function register value to 0 and sets all bits to ports.

(1) Port 90 & 93 (TXD0/TXD1)

Ports 90 and 93 also function as serial channel TXD output pins in addition to I/O ports.

They have a programmable open drain function.

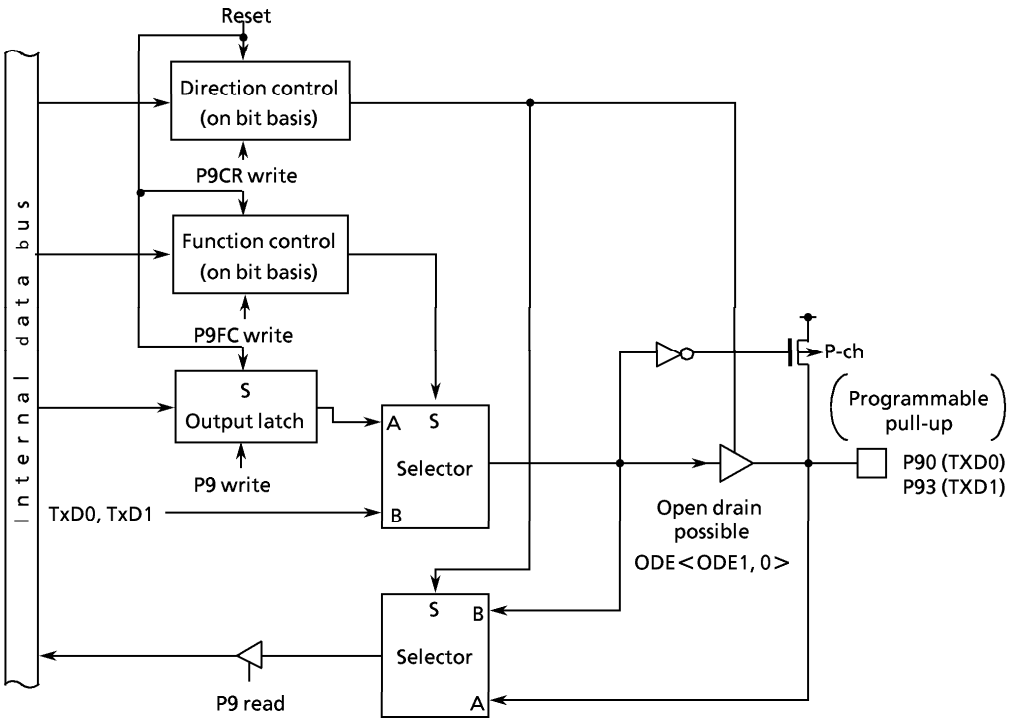


Figure 3.3 (20) Ports 90 and 93

(2) Ports 91 and 94 (RXD0, 1)

Ports 91 and 94 are I/O ports, and also used as RXD input pins for serial channels.

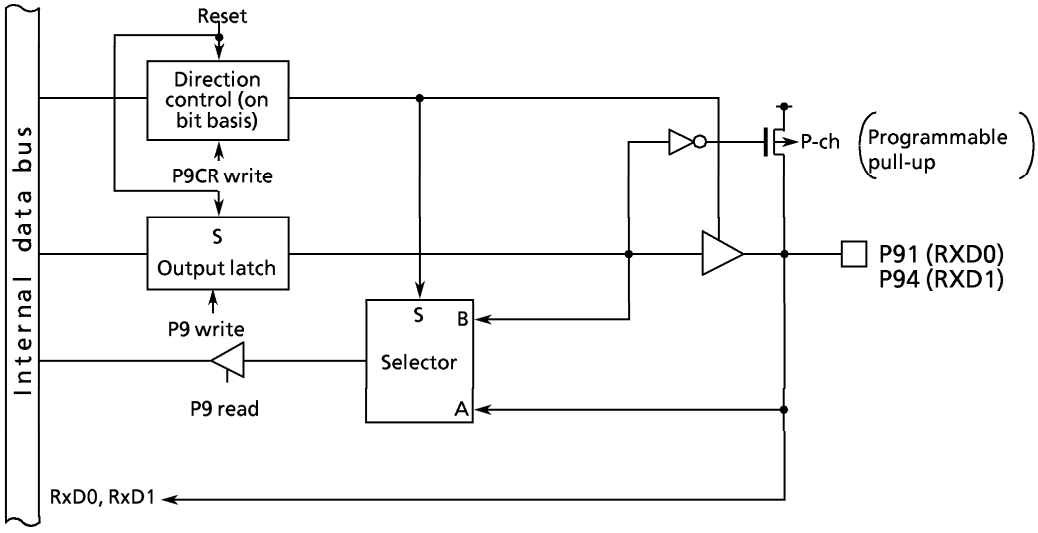


Figure3.3 (21) Ports 91 and 94

(3) Port 92 ($\overline{CTS0}$/SCLK0)

Port 92 is an I/O port, and also used as a $\overline{CTS0}$ input pin for serial channel0. Additionally, the $\overline{CTS0}$ pin, and also as a SCLK0 I/O port.

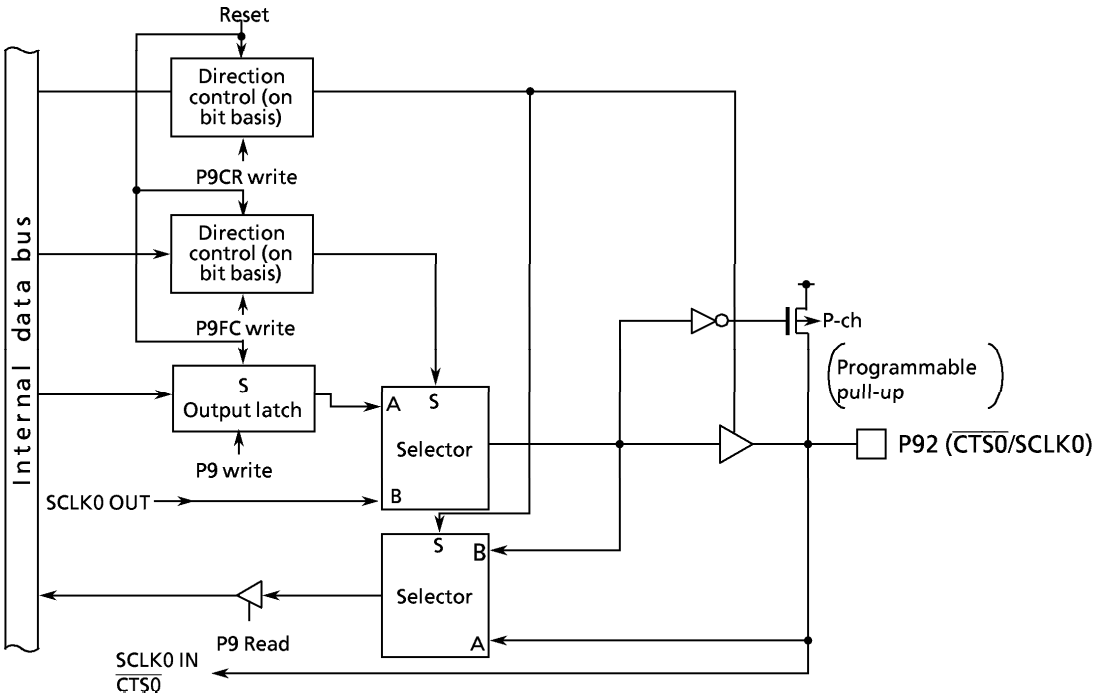


Figure3.3 (22) Ports 92

(4) Port 95 (SCLK1)

Port 95 is a general-purpose I/O port. It is also used as an SCLK1 I/O pin for serial channel 1.

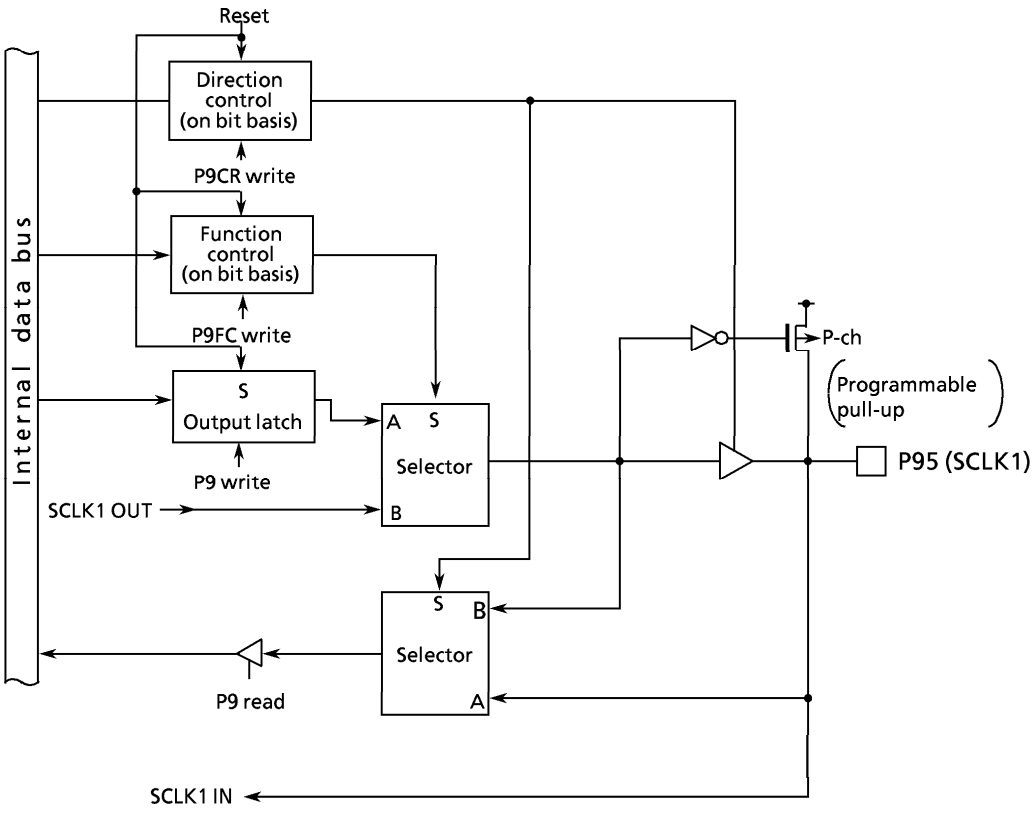


Figure3.3 (23) Port 95

Port 9 Register

P9 (0019H)

	7	6	5	4	3	2	1	0
bit Symbol			P95	P94	P93	P92	P91	P90
Read/Write			R/W					
After reset			Input mode					
			1	1	1	1	1	1

Port 9 Control Register

P9CR (001BH)

	7	6	5	4	3	2	1	0
bit Symbol			P95C	P94C	P93C	P92C	P91C	P90C
Read/Write			W					
After reset			0	0	0	0	0	0
Function			0 : IN			1 : OUT		

Port 9 I/O setting

0	Input
1	Output

Port 9 Function Register

P9FC (001DH)

	7	6	5	4	3	2	1	0
bit Symbol			P95F		P93F	P92F		P90F
Read/Write			W		W	W		W
After reset			0		0	0		0
Function			0 : PORT 1 : SCLK1		0 : PORT 1 : TxD1	0 : PORT 1 : SCLK0		0 : PORT 1 : TxD0

- Read-modify-write is prohibited for registers P9CR, P9FC.
- Read-modify-write is prohibited for controlling ON/OFF of the pull-up resistor for register P9.

P90 TxD0 output setting (Note)

P9FC <P90F>	1
P9CR <P90C>	1

P93 TxD1 output setting (Note)

P9FC <P93F>	1
P9CR <P93C>	1

P95 SCLK output setting

P9FC <P95F>	1
P9CR <P95C>	1

Note : To set the TxD pin to open drain, write 1 in bit 0 (for TxD0 pin) or bit 1 (for TxD1 pin) of the ODE register.
P91/RXD0, P94/RXD1 pins do not have a register changing PORT/FUNCTION.
Therefore this is the same as P70/TI0 pin.

Figure 3.3 (24) Registers for Port 9

4. Electrical Characteristics

4.1 Absolute Maximum Ratings (TMP96CM40)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V cc	– 0.5 to 6.5	V
Input Voltage	V IN	– 0.5 to Vcc + 0.5	V
Output Current (total)	Σ IOL	100	mA
Output Current (total)	Σ IOH	– 100	mA
Power Dissipation (Ta = 85℃)	P D	500	mW
Soldering Temperature (10 s)	T SOLDER	260	℃
Storage Temperature	T STG	– 65 to 150	℃
Operating Temperature	T OPR	– 40 to 85	℃

Note : The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics (TMP96CM40)

Vcc = 5 V ± 10%, TA = – 40 to 85℃ (4 to 16 MHz) TA = – 20 to 70℃ (4 to 20 MHz)

(Typical values are for Ta = 25℃ and Vcc = 5 V)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Low Voltage (AD0 to 15) P2, P3, P4, P5, P6, P7, P8, P9 RESET,NMI,INT0(P87) EA X1	V IL V IL1 V IL2 V IL3 V IL4		– 0.3 – 0.3 – 0.3 – 0.3 – 0.3	0.8 0.3 Vcc 0.25 Vcc 0.3 0.2 Vcc	V V V V V
Input High Voltage (AD0 – 15) P2, P3, P4, P5, P6, P7, P8, P9 RESET, NMI, INT0 (P87) EA X1	V IH V IH1 V IH2 V IH3 V IH4		2.2 0.7 Vcc 0.75 Vcc Vcc – 0.3 0.8 Vcc	Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3	V V V V V
Output Low Voltage	V OL	I OL = 1.6 mA		0.45	V
Output High Voltage	V OH V OH1 V OH2	I OH = – 400 μA I OH = – 100 μA I OH = – 20 μA	2.4 0.75 Vcc 0.9 Vcc		V V V
Darlington Drive Current (8 Output Pins max.)	I DAR	V EXT = 1.5 V R EXT = 1.1 kΩ	– 1.0	– 3.5	mA
Input Leakage Current Output Leakage Current	I LI I LO	0.0 ≦ Vin ≦ Vcc 0.2 ≦ Vin ≦ Vcc – 0.2	0.02 (Typ) 0.05 (Typ)	± 5 ± 10	μA μA
Operating Current (RUN) IDLE STOP (Ta = – 40 to 85℃) STOP (Ta = 0 to 50℃)	I cc	fc = 20 MHz 0.2 ≦ Vin ≦ Vcc – 0.2 0.2 ≦ Vin ≦ Vcc – 0.2	30 (Typ) 2.0 (Typ) 0.2 (Typ)	TBD 10 50 10	mA mA μA μA
Power Down Voltage (@ STOP, RAM Back up)	V STOP	V IL2 = 0.2 Vcc, V IH2 = 0.8 Vcc	2.0	6.0	V
RESET Pull Up Resistor	R RST		50	150	kΩ
Pin Capacitance	C IO	fc = 1 MHz		10	pF
Schmitt Width RESET, NMI, INT0 (P87)	V TH		0.4	1.0 (Typ)	V
Programmable Pull Down Resistor	R KL		10	80	kΩ
Programmable Pull Up Resistor	R KH		50	150	kΩ

Note : I-DAR is guaranteed for a total of up to 8 ports.

4.3 AC Electrical Characteristics (TMP96CM40)

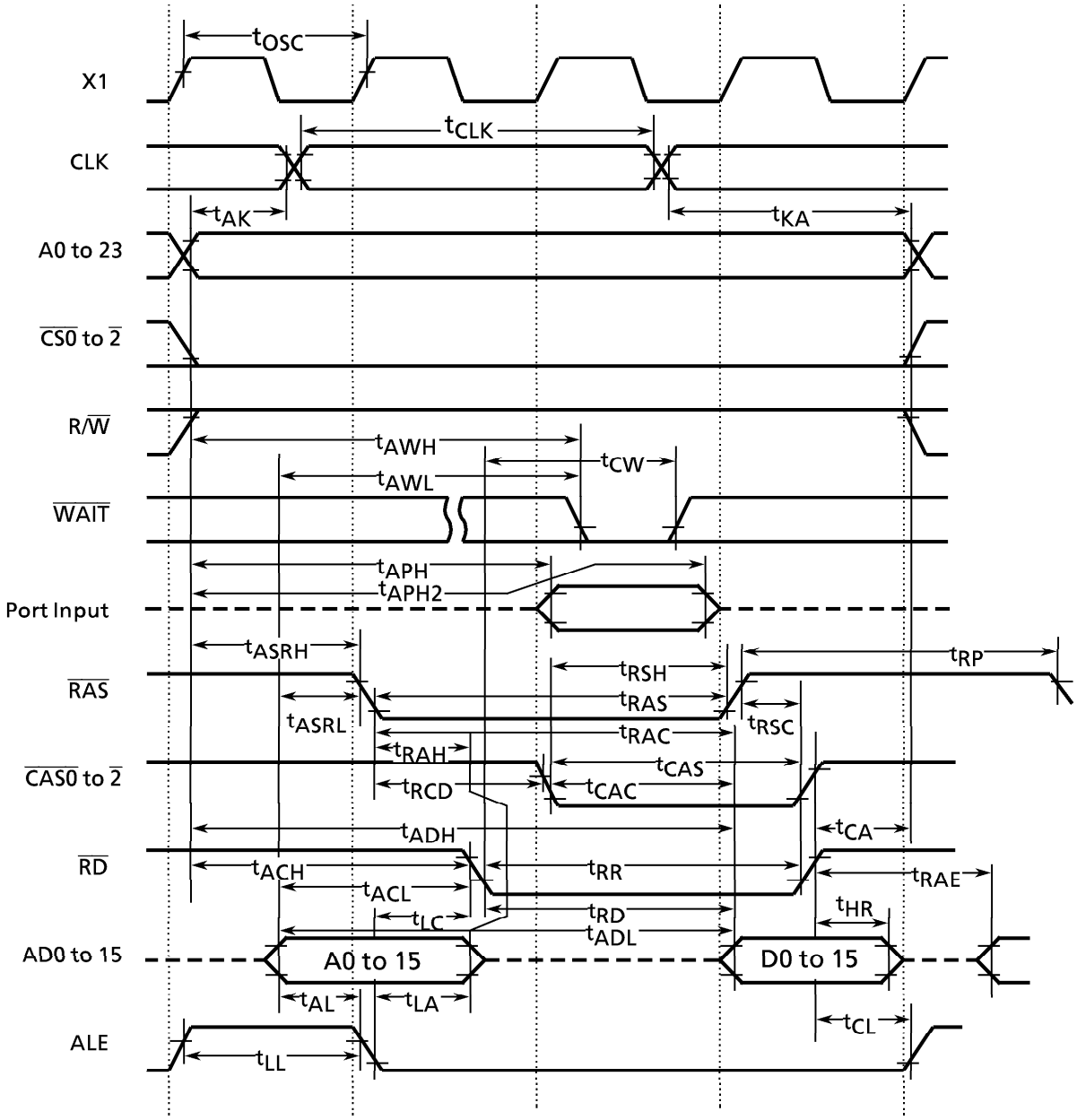
Vcc = 5 V ± 10%, TA = − 40 to 85℃ (4 to 16 MHz) TA = − 20 to 70℃ (4 to 20 MHz)

No.	Parameter	Symbol	Variavle		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Osc. Period (= x)	t_{OSC}	50	250	62.5		50		ns
2	CLK width	t_{CLK}	2x − 40		85		60		ns
3	A0 to 23 Valid → CLK Hold	t_{AK}	0.5x − 20		11		5		ns
4	CLK Valid → A0 to 23 Hold	t_{KA}	1.5x − 70		24		5		ns
5	A0 to 15 Valid → ALE fall	t_{AL}	0.5x − 15		16		10		ns
6	ALE fall → A0 to 15 Hold	t_{LA}	0.5x − 15		16		10		ns
7	ALE High width	t_{LL}	x − 40		23		10		ns
8	ALE fall → $\overline{RD}/\overline{WR}$ fall	t_{LC}	0.5x − 30		1		− 5		ns
9	$\overline{RD}/\overline{WR}$ rise → ALE rise	t_{CL}	0.5x − 20		11		5		ns
10	A0 to 15 Valid → $\overline{RD}/\overline{WR}$ fall	t_{ACL}	x − 25		38		25		ns
11	A0 to 23 Valid → $\overline{RD}/\overline{WR}$ fall	t_{ACH}	1.5x − 50		44		25		ns
12	$\overline{RD}/\overline{WR}$ rise → A0 to 23 Hold	t_{CA}	0.5x − 20		11		5		ns
13	A0 to 15 Valid → D0 to 15 input	t_{ADL}		3.0x − 45		143		105	ns
14	A0 to 23 Valid → D0 to 15 input	t_{ADH}		3.5x − 65		154		110	ns
15	$\overline{RD}$fall → D0 to 15 input	t_{RD}		2.0x − 50		75		50	ns
16	$\overline{RD}$ Low width	t_{RR}	2.0x − 40		85		60		ns
17	$\overline{RD}$rise → D0 to 15 Hold	t_{HR}	0		0		0		ns
18	$\overline{RD}$rise → A0 to 15output	t_{RAE}	x − 15		48		35		ns
19	$\overline{WR}$ Low width	t_{WW}	2.0x − 40		85		60		ns
20	D0 to 15 Valid → $\overline{WR}$ rise	t_{DW}	2.0x − 50		75		50		ns
21	$\overline{WR}$ rise → D0 to 15 Hold	t_{WD}	0.5x − 10		21		15		ns
22	A0 to 23 Valid → $\overline{WAIT}$ input ($\frac{1WAIT}{+n\ mode}$)	t_{AEH}		3.5x − 90		129		85	ns
23	A0 to 15 Valid → $\overline{WAIT}$ input ($\frac{1WAIT}{+n\ mode}$)	t_{AWL}		3.0x − 80		108		70	ns
24	$\overline{RD}/\overline{WR}$ fall → $\overline{WAIT}$ Hold ($\frac{1WAIT}{+n\ mode}$)	t_{CW}	2.0x + 0		125		100		ns
25	A0 to 23 Valid → PORT input	t_{APH}		2.5x − 120		36		5	ns
26	A0 to 23 Valid → PORT Hold	t_{APH2}	2.5x + 50		206		175		ns
27	$\overline{WR}$ rise → PORT Valid	t_{CP}		200		200		200	ns
28	A0 to 23 Valid → $\overline{RAS}$ fall	t_{ASRH}	1.0x − 40		23		10		ns
29	A0 to 15 Valid → $\overline{RAS}$ fall	t_{ASRL}	0.5x − 15		16		10		ns
30	$\overline{RAS}$ fall → D0 to 15 input	t_{RAC}		2.5x − 70		86		55	ns
31	$\overline{RAS}$ fall → A0 to 15 Hold	t_{RAH}	0.5x − 15		16		10		ns
32	$\overline{RAS}$ Low width	t_{RAS}	2.0x − 40		85		60		ns
33	$\overline{RAS}$ High width	t_{RP}	2.0x − 40		85		60		ns
34	$\overline{CAS}$ fall → $\overline{RAS}$ rise	t_{RSH}	1.0x − 35		28		15		ns
35	$\overline{RAS}$ rise → $\overline{CAS}$ rise	t_{RSC}	0.5x − 25		6		0		ns
36	$\overline{RAS}$ fall → $\overline{CAS}$ fall	t_{RCD}	1.0x − 40		23		10		ns
37	$\overline{CAS}$ fall → D0 to 15 input	t_{CAC}		1.5x − 65		29		10	ns
38	$\overline{CAS}$ Low width	t_{CAS}	1.5x − 30		64		40		ns

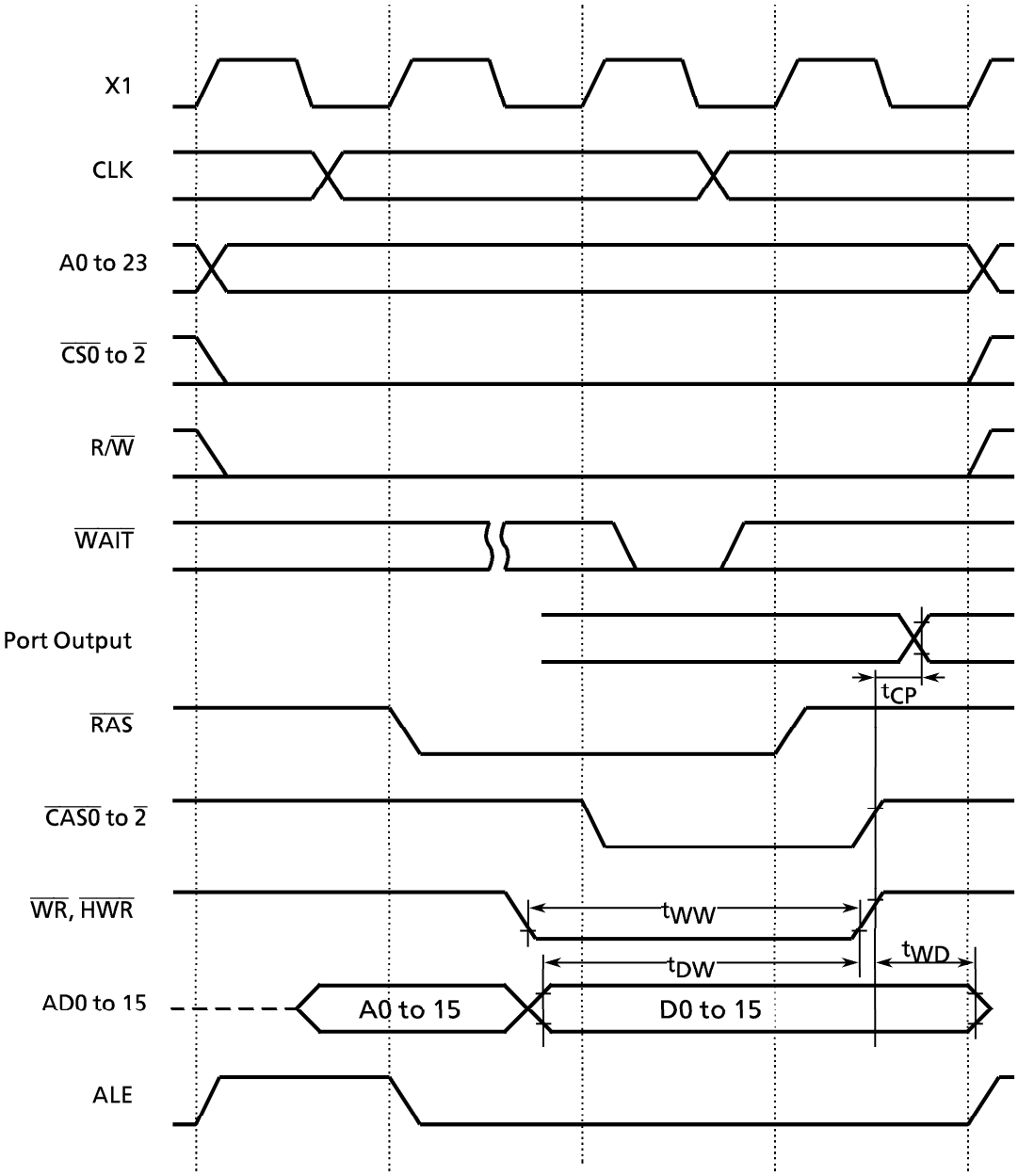
AC Measuring Conditions

- Output Level : High 2.2 V / Low 0.8 V , CL50 pF
  (However CL = 100 pF for AD0 to AD15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, CLK, $\overline{RAS}$, $\overline{CAS0}$ to $\overline{CAS2}$)
- Input Level : High 2.4 V / Low 0.45 V (AD0 to AD15)
  High 0.8 Vcc / Low 0.2 Vcc (Except for AD0 to AD15)

(1) Read Cycle


tOSC
X1
tCLK
CLK
tAK
tKA
A0 to 23
CS0 to 2
R/W
tAWH
tCW
tAWL
WAIT
tAPH
tAPH2
Port Input
tASRH
tRP
tRSH
RAS
tRAS
tASRL
tRSC
tRAC
tRAH
tCAS
CAS0 to 2
tRCD
tCAC
tADH
tCA
RD
tACH
tRR
tRAE
tACL
tHR
tLC
tRD
tADL
AD0 to 15
A0 to 15
D0 to 15
tAL
tLA
tCL
ALE
tLL

(2) Write Cycle



4.4 A/D Conversion Characteristics (TMP96CM40)

Vcc = 5 V ± 10%, TA = − 40 to 85℃ (4 to 16 MHz) TA = − 20 to 70℃ (4 to 20 MHz)

Parameter		Symbol	Min	Typ.	Max	Unit
Analog reference voltage		V_{REF}	Vcc − 1.5		Vcc	V
Analog reference voltage		A_{GND}	Vss		Vss	
Analog input voltage range		V_{AIN}	Vss		Vcc	
Anlog current for analog reference voltage		I_{REF}		0.5	1.5	mA
4 ≦ fc ≦ 16 MHz	Low change mode	Total error (Quantize error of ± 0.5 LSB not included)		± 1.5	± 4.0	LSB
	High change mode			± 3.0	± 6.0	
16 < fc ≦ 20 MHz	Low change mode			± 1.5	± 4.0	
	High change mode			± 4.0	± 8.0	

4.5 Serial Channel Timing – I/O Interface Mode

(1) SCLK Input Mode

Vcc = 5 V ± 10%, TA = − 40 to 85℃ (4 to 16 MHz) TA = − 20 to 70℃ (4 to 20 MHz)

Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle	t_{SCY}	16X		1		0.8		μs
Output Data → Rising edge of SCLK	t_{OSS}	t_{SCY}/2 − 5X − 50		137		100		ns
SCLK rising edge→ Output Data hold	t_{OHS}	5X − 100		212		150		ns
SCLK rising edge→ Input Data hold	t_{HSR}	0		0		0		ns
SCLK rising edge→ effective data input	t_{SRD}		t_{SCY} − 5X − 100		587		450	ns

(2) SCLK Output Mode

Vcc = 5 V ± 10%, TA = − 40 to 85℃ (4 to 16 MHz) TA = − 20 to 70℃ (4 to 20 MHz)

Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle (programmable)	t_{SCY}	16X	8192X	1	512	0.8	409.6	μs
Output Data → SCLK rising edge	t_{OSS}	t_{SCY} − 2X − 150		725		550		ns
SCLK rising edge→ Output Data hold	t_{OHS}	2X − 80		45		20		ns
SCLK rising edge→ Input Data hold	t_{HSR}	0		0		0		ns
SCLK rising edge→ effective data input	t_{SRD}		t_{SCY} − 2X − 150		725		550	ns

4.6 Timer/Counter Input Clock (TI0, TI4, TI5, TI6, TI7)

Vcc = 5 V ± 10%, TA = − 40 to 85℃ (4 to 16 MHz) TA = − 20 to 70℃ (4 to 20 MHz)

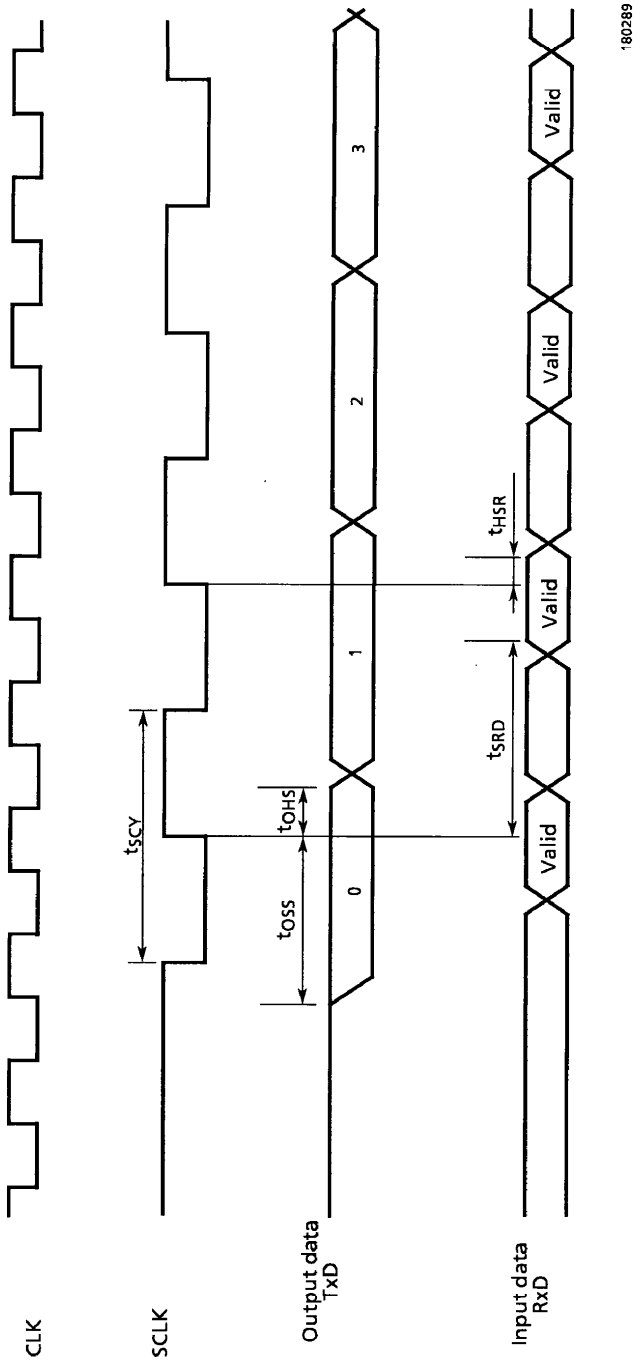
Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock Cycle	t_{VCK}	8X + 100		600		500		ns
Low level clock Pulse width	t_{VCKL}	4X + 40		290		240		ns
High level clock Pulse width	t_{VCKH}	4X + 40		290		240		ns

4.7 Interrupt Operation

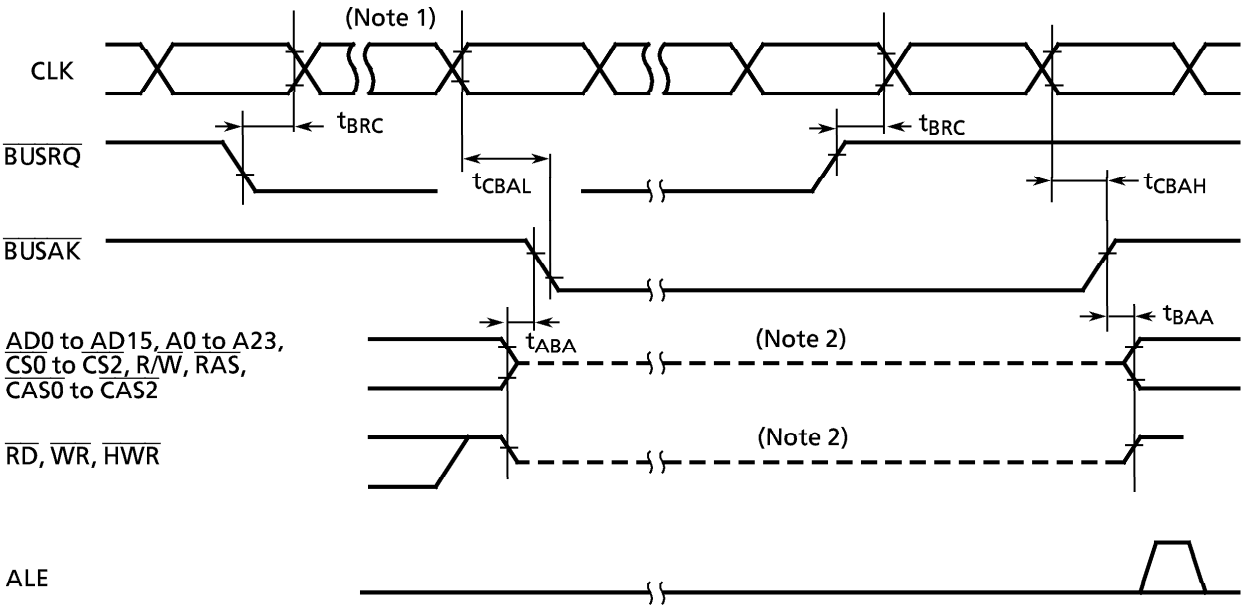
Vcc = 5 V ± 10%, TA = − 40 to 85℃ (4 to 16 MHz) TA = − 20 to 70℃ (4 to 20 MHz)

Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{NMI}$, INT0 Low level Pulse width	t_{INTAL}	4X		250		200		ns
$\overline{NMI}$, INT0 High level Pulse width	t_{INTAH}	4X		250		200		ns
INT4 to INT7 Low level Pulse width	t_{INTBL}	8X + 100		600		500		ns
INT4 to INT7 High level Pulse width	t_{INTBH}	8X + 100		600		500		ns

4.8 Timing Chart for I/O Interface Mode



4.9 Timing Chart for Bus Request ($\overline{BUSRQ}$) / Bus Acknowledge ($\overline{BUSAK}$)



Symbol	Parameter	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{BRC}	$\overline{BUSRQ}$ set-up time for CLK	120		120		120		ns
t_{CBAL}	CLK→ $\overline{BUSAK}$ falling edge		1.5x + 120		214		195	ns
t_{CBAH}	CLK→ $\overline{BUSAK}$ rising edge		0.5x + 40		71		65	ns
t_{ABA}	Output Buffer is off to $\overline{BUSAK}$ ↓	0	80	0	80	0	80	ns
t_{BAA}	$\overline{BUSAK}$ ↑ to Output Buffer is on.	0	80	0	80	0	80	ns

Note 1 : The Bus will be released after the $\overline{WAIT}$ request is inactive, when the $\overline{BUSRQ}$ is set to "0" during "Wait" cycle.

Note 2 : This line only shows the output buffer is off-state.
They don't indicate the signal level is fixed.
After the bus is released, the signal level is kept dynamically before the bus is released by the external capacitance.
Therefore, to fix the signal level by an external resistance under the bus is releasing, the design must be carefully because of the level-fix will be delayed.
The internal programmable pull-up/pull-down resistance is switched active/non-active by the internal signal.

4.10 Typical characteristics

Vcc = 5 V, Ta = 25 °C unless other wise noted.

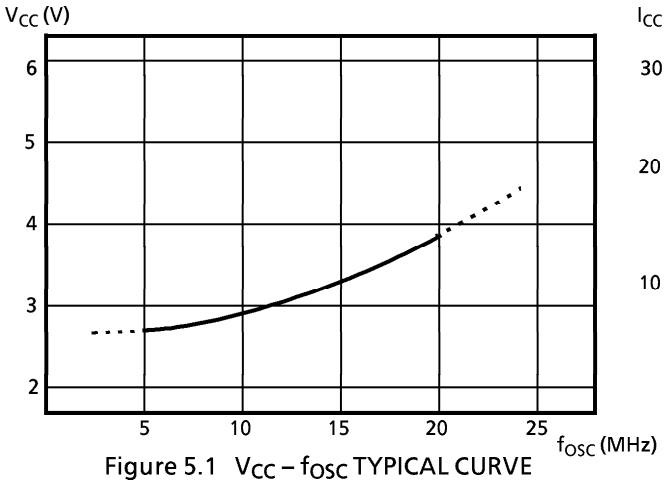


Figure 5.1 V_{CC} – f_{OSC} TYPICAL CURVE

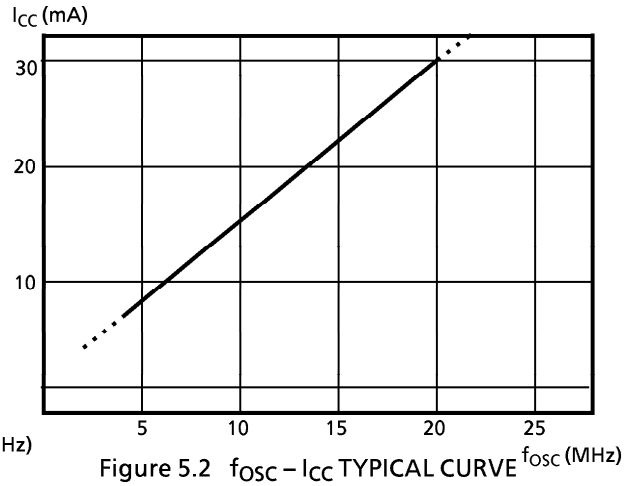


Figure 5.2 f_{OSC} – I_{CC} TYPICAL CURVE

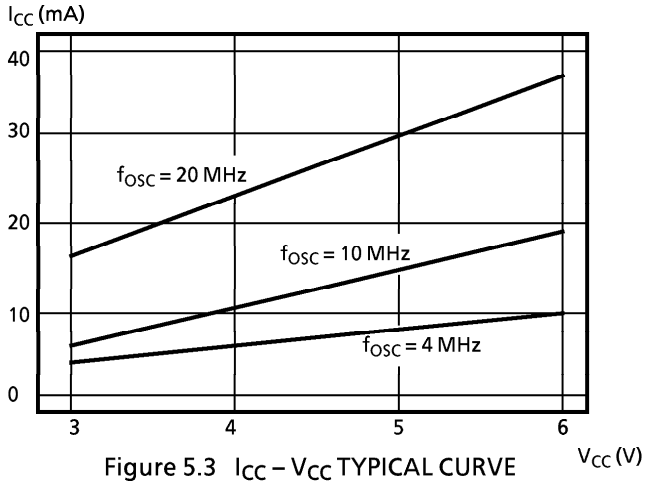


Figure 5.3 I_{CC} – V_{CC} TYPICAL CURVE

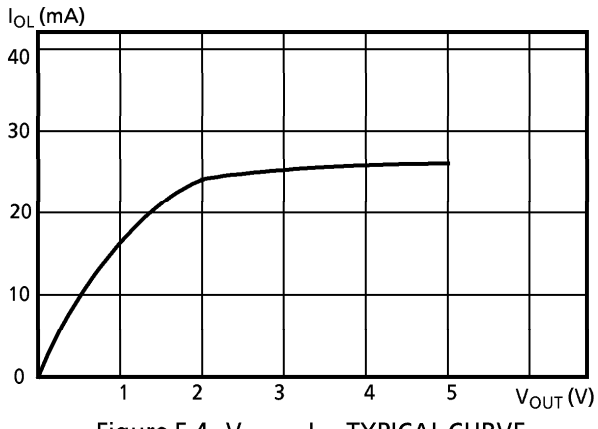


Figure 5.4 V_{OUT} – I_{OL} TYPICAL CURVE

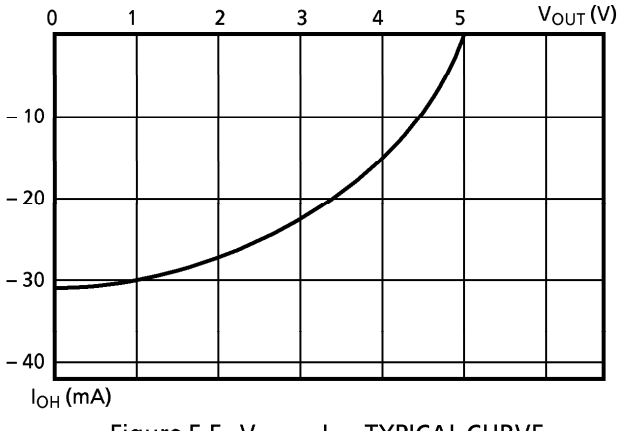


Figure 5.5 V_{OUT} – I_{OH} TYPICAL CURVE