The Embedded I/O Company

TMPE633

Reconfigurable FPGA with Digital I/O PCIe Mini Card

Version 1.0

User Manual

Issue 1.0.0

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TEWS TECHNOLOGIES GmbH

Am Bahnhof 7 25469 Halstenbek, Germany

Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19

e-mail: info@tews.com www.tews.com

TMPE633-10R

26 TTL I/O, Spartan-6 LX25T FPGA

TMPE633-11R

13 RS-485 I/O, Spartan-6 LX25T FPGA

TMPE633-12R

13 M-LVDS I/O, Spartan-6 LX25T FPGA

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
0.0.1	Preliminary Draft	September 2015
1.0.0	Initial Issue	December 2015

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1 Product Description

The TMPE633 is a standard full PCI Express Mini Card, providing a user programmable Xilinx Spartan-6 LX25T FPGA.

The TMPE633-10R provides 26 ESD-protected 5 V-tolerant TTL lines, the TMPE633-11R provides 13 differential I/O lines using EIA 422 / EIA 485 compatible, ESD-protected line transceivers and the TMPE633-12R provides 13 differential I/O lines using Multipoint-LVDS Transceiver.

All I/O lines are individually programmable as input or output. TTL I/O lines can be set to high, low, or tri-state. Each TTL I/O line has a pull-resistor to a common programmable pull voltage that can be set so +3.3 V, +5 V and GND. Differential I/O lines are terminated, RS-485 lines with 120 Ω, M-LVDS lines with 100 Ω.

The I/O signals are accessible through a 30 pin latching connector.

The User FPGA is configured by a SPI flash. An in-circuit debugging option is available via a JTAG header for read back and real-time debugging of the FPGA design (using Xilinx “ChipScope”).

User applications for the TMPE633 with XC6SLX25T-2 FPGA can be developed using the design software ISE WebPACK which can be downloaded free of charge from www.xilinx.com.

TEWS offers a well-documented basic FPGA Example Application design. It includes an .ucf file with all necessary pin assignments and basic timing constraints. The example design covers the main functionalities of the TMPE633. It implements local Bus interface to local Bridge device, register mapping and basic I/O. It comes as a Xilinx ISE project with source code and as a ready-to-download bit stream.

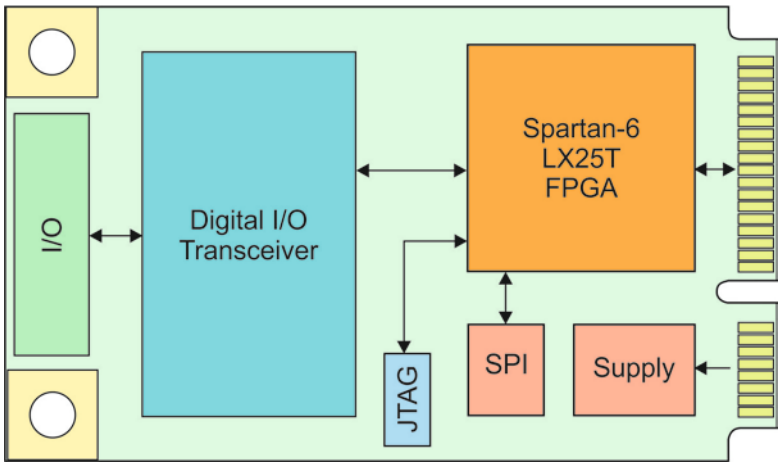


Figure 1-1 : Block Diagram

2 Technical Specification

Interface		
Mechanical Interface	PCI Express Mini Card conforming to PCI Express Mini Card Electromechanical Specification, Revision 2.0 Card Type: Full-Mini Card (50.95 x 30 mm)	
Electrical Interface	PCI Express x1 Link conforming to PCI Express Base Specification, Revision 2.0 The TMPE633 does not support the USB interface	
Main On-Board Devices		
User configurable FPGA	XC6SLX25T-2 (Xilinx)	
SPI-Flash	W25Q64FV (Winbond) 64 Mbit (contains TMPE633 FPGA Example) or compatible	
I/O Interface		
I/O Channels	TMPE633-10R: 26 ESD-protected 5 V-tolerant TTL lines TMPE633-11R: 13 differential RS-485 lines TMPE633-12R: 13 differential M-LVDS lines	
I/O Transceiver	TMPE633-10R: 74LVC2G241 (or compatible) TMPE633-11R: 65HVD75D (or compatible) TMPE633-12R: 65LVDM176D (or compatible)	
I/O Connector	30 pol. Pico-Clasp latching connector	
Physical Data		
Power Requirements	Depends on FPGA design With TMPE633 FPGA Example Design / without external load +3.3Vaux: 100 mA typical +1.5V: 250 mA typical	
Temperature Range	Operating	-40°C to +85°C
	Storage	-40°C to +85°C
MTBF	980.000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	6 g	

Table 2-1 : Technical Specification

3 Handling and Operating Instructions

3.1 ESD Protection

The PCI Express Mini Card module is sensitive to static electricity. Packing, unpacking and all other module handling has to be done in an ESD/EOS protected Area.

3.2 Height Restrictions

The I/O connector will exceed the available PCI Express Mini Card components height. Check carefully if your application provides enough spacing for a TMPE633.

4 Functional Description

This chapter gives a brief overview of the various module functions.

4.1 User FPGA Overview

The FPGA is a Spartan-6 LX25T-2 in a CSG324 package.

Spartan-6	Slices	Flip-Flops	DSP48A1 Slices	Block RAM (Kb)	GTP Transceivers
LX25T	3.758	30.064	32	936	2

Table 4-1 : TMPE633 FPGA Feature Overview

The FPGA is equipped with 4 I/O banks and 2 MGT (multi gigabit transceiver). One of the MGTs can be connected to an Endpoint Block for PCI Express.

Bank	V_{CCO}	V_{REF}	Signals	Remarks
Bank 0	3.3V	none	Optional GPIO	
Bank 1	3.3V	none	I/O Interface	
Bank 2	3.3V	none	I/O Interface	+Configuration
Bank 3	3.3V	none	I/O Interface	
GTP Bank	**Description**			**Remarks**
Bank 101	MGT0: PCIe Endpoint Block MGT1: Not used			

Table 4-2 : FPGA Bank Usage

The FPGA's VCCAUX is connected to the 3.3V supply.

4.2 User FPGA Gigabit Transceiver (GTP)

The TMPE633 provides one MGT as Spartan-6 PCI Express Endpoint Block.

GTP	Signal	FPGA Pins	Connected to
MGT0_101	MGTTX	B4 / A4	used for PCI Express Endpoint Block
	MGTRX	D5 / C5	
MGT1_101	MGTTX	B6 / A6	Not used
	MGTRX	D7 / C7	

Table 4-3 : MGT Connections

The 100 MHz MGT clock MGT0_101 (PCI Express Endpoint Block clock reference) is connected directly to the PCI Express Mini Card reference clock. MGT1_101 is not used on the TMPE633.

GTP	Signal	FPGA Pins	Connected to
MGT0_101	MGTREFCLK	B8 / A8	100 MHz (backplane clock)
MGT1_101	MGTREFCLK	D9 / C9	not connected

Table 4-4 : Multi Gigabit Transceiver Reference Clocks

4.3 User FPGA Configuration

The Spartan-6 FPGA can be configured by the following interfaces:

- Master Serial SPI Flash Configuration Interface
- JTAG Interface via JTAG Header

On delivery the SPI configuration Platform Flash contains the TEWS example application for the TMPE633 Spartan-6 device.

4.3.1 SPI-Flash

The TMPE633 provides a Winbond W25Q64 64-Mbit serial Flash memory, which is used as the default FPGA configuration source. After configuration the flash is accessible from the FPGA, so it also can be used for additional code or user data storage. The SPI-Flash is connected via Quad (x4) SPI interface to Spartan-6 configuration interface.

SPI-Flash Signal	Bank	V_{CCO}	Pin	Description / Spartan-6
CLK	2	3.3V	R15	Serial Clock (CCLK)
CS#	2	3.3V	V3	Chip Select (CS0_B)
DI (bit0)	2	3.3V	T13	Serial Data input (MOSI) / MISO[0]
DO (bit1)	2	3.3V	R13	Serial Data output (DIN) / MISO[1]
WP# (bit2)	2	3.3V	T14	MISO[2]
HOLD# (bit3)	2	3.3V	V14	MISO[3]

Table 4-5 : FPGA SPI-Flash Connections

4.3.2 Configuration via JTAG

For direct FPGA configuration, FPGA read back or in-system diagnostics with ChipScope, the JTAG connector can be used to access the FPGA JTAG port. Also an indirect SPI-Flash programming is possible via the JTAG Chain.

4.3.3 Generate Spartan-6 Configuration Data

To use the maximum configuration speed, the TMPE633 must be configured to use the 40 MHz external master clock as CCLK.

To use this configuration feature, the following configuration option must be set:

‘Enable External Master Clock’ (-g ExtMasterCclk_en) = enable

‘Setup External Master Clock Devision’ (-g ExtMasterCclk_divide) = 1

To use the maximum data transfer speed of the User FPGA SPI Configuration Flash the SPI Configuration Bus Width must be set to the x4.

‘Set SPI Configuration Bus Width’ (-g SPI_buswidth) = 4

Without this option, the configuration time for the Spartan-6 FPGA exceed the maximum PCIe bus setup time.

4.4 Clocking

4.4.1 FPGA Clock Sources

The following table lists the available clock sources on the TMPE633:

FPGA Clock-Pin Name	FPGA Pin Number	Source	Description
MGTREFCLK0_101	B8 / A8	PCI Express Mini Card Slot	100 MHz PCIe Reference clock
IO_L30N_GCLK0_USERCCLK_2	V10	External oscillator	40 MHz Used for external configuration clock (CCLK)

Table 4-6 : Available FPGA clocks

4.5 Digital I/O Interface

Each of the 26 digital I/O channels provides an I/O data signal and an output enable signal to the single ended or differential digital buffers.

The I/O channels are accessible through the I/O bank 1 and 2 of the Spartan-6 FPGA. The subsequent table lists required I/O setting for correct interfacing.

Signal Name	Pin Number	Direction	IO Standard	IO Bank	Drive [mA]	Slew Rate
DIO<0>#	L14	IN/OUT	LVCMOS33	1	8	SLOW
DIO<1>#	N17	IN/OUT	LVCMOS33	1	8	SLOW
DIO<2>#	M16	IN/OUT	LVCMOS33	1	8	SLOW
DIO<3>#	N18	IN/OUT	LVCMOS33	1	8	SLOW
DIO<4>#	L18	IN/OUT	LVCMOS33	1	8	SLOW
DIO<5>#	U17	IN/OUT	LVCMOS33	1	8	SLOW
DIO<6>#	C18	IN/OUT	LVCMOS33	1	8	SLOW
DIO<7>#	G18	IN/OUT	LVCMOS33	1	8	SLOW
DIO<8>#	V12	IN/OUT	LVCMOS33	2	8	SLOW
DIO<9>#	U7	IN/OUT	LVCMOS33	2	8	SLOW
DIO<10>#	R7	IN/OUT	LVCMOS33	2	8	SLOW
DIO<11>#	N6	IN/OUT	LVCMOS33	2	8	SLOW
DIO<12>#	U13	IN/OUT	LVCMOS33	2	8	SLOW
DIO<13>#	N10	IN/OUT	LVCMOS33	2	8	SLOW
DIO<14>#	F18	IN/OUT	LVCMOS33	1	8	SLOW
DIO<15>#	M18	IN/OUT	LVCMOS33	1	8	SLOW
DIO<16>#	N8	IN/OUT	LVCMOS33	2	8	SLOW
DIO<17>#	P8	IN/OUT	LVCMOS33	2	8	SLOW
DIO<18>#	U8	IN/OUT	LVCMOS33	2	8	SLOW
DIO<19>#	V13	IN/OUT	LVCMOS33	2	8	SLOW
DIO<20>#	V5	IN/OUT	LVCMOS33	2	8	SLOW
DIO<21>#	V7	IN/OUT	LVCMOS33	2	8	SLOW
DIO<22>#	N5	IN/OUT	LVCMOS33	2	8	SLOW
DIO<23>#	N7	IN/OUT	LVCMOS33	2	8	SLOW
DIO<24>#	R5	IN/OUT	LVCMOS33	2	8	SLOW
DIO<25>#	T5	IN/OUT	LVCMOS33	2	8	SLOW
OE<0>#	M8	OUTPUT	LVCMOS33	2	8	SLOW
OE<1>#	M11	OUTPUT	LVCMOS33	2	8	SLOW
OE<2>#	P12	OUTPUT	LVCMOS33	2	8	SLOW
OE<3>#	V15	OUTPUT	LVCMOS33	2	8	SLOW
OE<4>#	R11	OUTPUT	LVCMOS33	2	8	SLOW
OE<5>#	U15	OUTPUT	LVCMOS33	2	8	SLOW
OE<6>#	E16	OUTPUT	LVCMOS33	1	8	SLOW

OE<7>#	U11	OUTPUT	LVCMOS33	2	8	SLOW
OE<8>#	V11	OUTPUT	LVCMOS33	2	8	SLOW
OE<9>#	V4	OUTPUT	LVCMOS33	2	8	SLOW
OE<10>#	T7	OUTPUT	LVCMOS33	2	8	SLOW
OE<11>#	T3	OUTPUT	LVCMOS33	2	8	SLOW
OE<12>#	P6	OUTPUT	LVCMOS33	2	8	SLOW
OE<13>#	R10	OUTPUT	LVCMOS33	2	8	SLOW
OE<14>#	F17	OUTPUT	LVCMOS33	1	8	SLOW
OE<15>#	L17	OUTPUT	LVCMOS33	1	8	SLOW
OE<16>#	M10	OUTPUT	LVCMOS33	2	8	SLOW
OE<17>#	N9	OUTPUT	LVCMOS33	2	8	SLOW
OE<18>#	T12	OUTPUT	LVCMOS33	2	8	SLOW
OE<19>#	P11	OUTPUT	LVCMOS33	2	8	SLOW
OE<20>#	T4	OUTPUT	LVCMOS33	2	8	SLOW
OE<21>#	V8	OUTPUT	LVCMOS33	2	8	SLOW
OE<22>#	R3	OUTPUT	LVCMOS33	2	8	SLOW
OE<23>#	U5	OUTPUT	LVCMOS33	2	8	SLOW
OE<24>#	V6	OUTPUT	LVCMOS33	2	8	SLOW
OE<25>#	T6	OUTPUT	LVCMOS33	2	8	SLOW

Table 4-7 : Digital I/O Interface

4.5.1 TTL I/O Interface

Each TTL I/O line is buffered by a 74LVC2G241 tri-state buffer that provides TTL compatible inputs with 5 V-tolerance. The outputs can be set to tri-state with an output enable signal and provide a 47 Ω serial resistor for signal integrity and a 4.7 kΩ pull resistor. A TVS array protects against ESD shocks. The pull resistor guarantees a valid logic level when the outputs are tristate and not driven externally. The pull voltage can be set to 3.3 V, 5 V or GND.

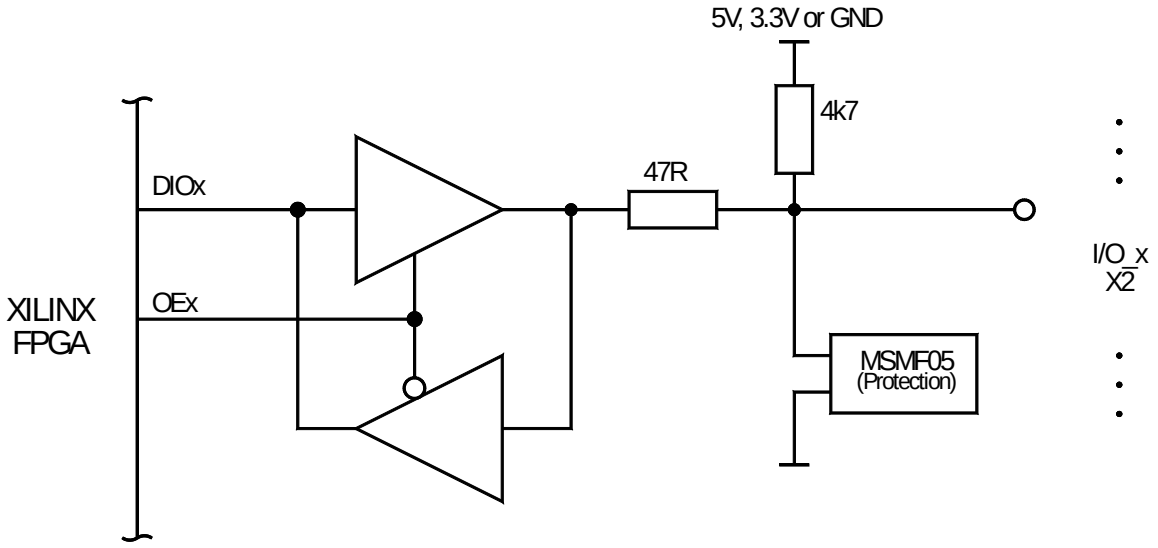


Figure 4-1 : TTL I/O Interface

With the pull voltage set to 5 V, the digital I/O can weakly drive a higher voltage than 3.3 V by setting the output to tri-state. This can be useful when connecting to a standard 5 V CMOS logic input, where a high level of minimum 3.5 V is required. Drive DIO constant low and use OE to toggle the output.

With the pull voltage set to GND, a pull-down functionality is implemented. Drive DIO constant high and use OE to toggle the output.

Pull Option	DIO	OE	Output	Remark
No pull-up or pull-down	0	1	1	
	1	1	1	
Pull-up to 3.3 V	0	1	0	
	1	1	1	Driven to 3.3 V
	-	0	1	Pulled to 3.3 V
Pull-up to 5 V	0	1	0	
	-	0	1	Pulled to 5 V
Pull-down to GND	-	0	0	Pulled to GND
	1	1	1	

Table 4-8 : I/O Pull Options

If the pull resistors float, the user should keep in mind that the I/O Lines are connected via their pull resistors.

The normal behavior is that the User FPGA code controls the I/O Pull Configuration depending on User FPGA I/O Function. The SEL signals are connected to an analog multiplexer. With this multiplexer the desired voltage can be adjusted directly from the User FPGA. The user must ensure that valid signals are always driven.

CNT Lines	Description	Spartan-6 Pins
SEL[1:0]	11 : pull-down 10 : pull-up to 3.3 V 01 : pull-up to 5 V 00 : No pull-up or pull-down	F16, F14

Table 4-9 : I/O Pull Configuration

4.5.1.1 Output Level & Output Current

Because of the 47 ohm series resistor, there is a reduced high-level voltage at the I/O pin when the output buffer sources a noticeable current to the external load while driving a high-level. To maintain a proper TTL high level, the recommended maximum I/O source current is 15 mA.

There is also an increased low-level voltage at the I/O pin when the output buffer sinks a noticeable current from the external load while driving a low-level. To maintain a proper TTL low level, the recommended maximum I/O sink current is 6 mA.

For achieving a 5 V CMOS high-level voltage (V_{OH} >= 3.5 V), the external load should be high impedance. If there would be a low impedance path to ground on the I/O load, this may result in a voltage divider with the on-board pull resistor, significantly reducing the high-level voltage at the I/O pin. To maintain a proper 5 V CMOS high level, the I/O load (leakage) current should not exceed 250 µA.

4.5.2 Differential I/O Interface

Each differential I/O line is buffered by a differential transceiver. The outputs can be set to high impedance with an output enable signal.

RS-485 variants use an ESD-protected SN65HVD75 RS-485/RS-422 transceiver and provide a 120 Ω termination resistor. LVDS variants use a SN65MLVD176 M-LVDS transceiver and provide a 100 Ω termination resistor.

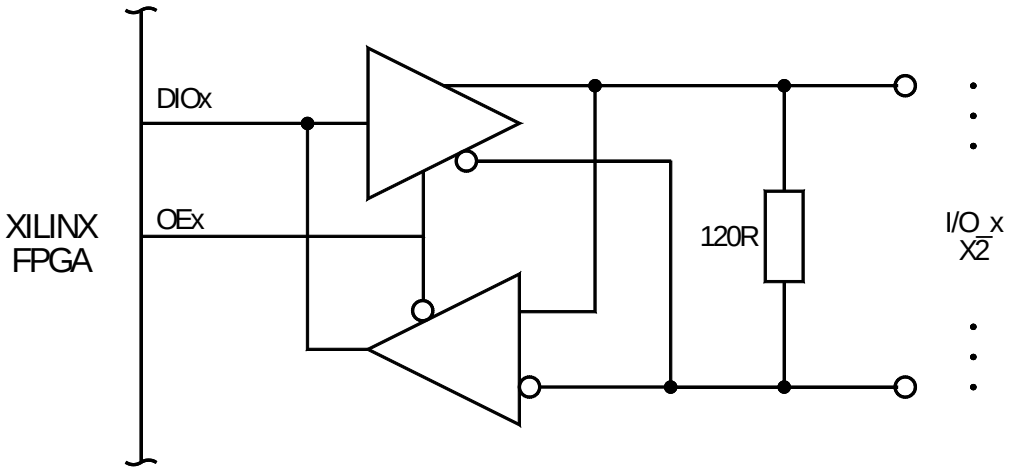


Figure 4-2 : Differential I/O Interface

Please note that each TMPE633 M-LVDS line provides its own termination. If more than four lines are connected together some termination resistors must be removed.

The actual data transmission rate depends on factors like connection, cable length, FPGA design etc.

4.6 User GPIO

The TMPE633 has some optional general purpose I/O and debug signals connected to the FPGA. The required signaling standard is LVCMOS33.

The FPGA is connected to the status indicator of the PCI Express Mini Card Slot:

Signal	Bank	V_{CCO}	Pin	Description
LED_WWAN#	0	3.3 V	E6	WWAN status indicator
LED_WPAN#	0	3.3 V	F7	WPAN status indicator
LED_WLAN#	0	3.3 V	G8	WLAN status indicator

Table 4-10: FPGA General Purpose I/O

4.7 Thermal Management

Power dissipation is design dependent. Main factors are device utilization, frequency and GTP-transceiver usage. Use the Xilinx XPower Estimator (XPE) or XPower Analyzer to determine if additional cooling requirements as forced air cooling apply. Forced air cooling is recommended during operation.

The Spartan-6 FPGA has no heatsink mounted. If additional cooling is required, the TMPE633 can be equipped with a heatsink, for example a Fischer Elektronik ICK S 14 x 14 x 6. Contact factory for this option.

Mounting a heatsink will violate the Mini PCIe Card component envelope. Check carefully if your system provides enough spacing for a TMPE633 with mounted heatsink. In space constrained systems mounting a heatsink may not be possible.

5 Design Help

5.1 Example Design

User applications for the TMPE633 can be developed using the TMPE633 FPGA Example Application design.

TEWS offers this FPGA Example design which consists of well documented basic example. It includes an ucf file with all necessary pin assignments and basic timing constraints. The example design covers the main functionalities of the TMPE633. It implements a PCIe endpoint with register mapping and basic I/O functions. It comes as a Xilinx ISE 14.7 project with source code and as a ready-to-download bit stream. This example design can be used as a starting point for own projects.

The TMPE633 FPGA Example Application design can be developed using the design software ISE Project Navigator (ISE) and Embedded Development Kit (EDK). IDE versions are 14.7. Licenses for both design tools are required.

For details about the TMPE633 FPGA Example Application design refer to the included User Manual.

5.2 FPGA MultiBoot

The Spartan-6 FPGAs provide the “MultiBoot” capability. It allows the FPGA to selectively reconfigure itself with a new bitstream stored in the attached SPI configuration flash. The reconfiguration can be triggered by the FPGA application itself or during the initial FPGA configuration when an error occurs (Fallback Multiboot). The latter can be used to implement safe in-field updates: if an update fails, a “golden” bitstream is loaded that allows to handle the error or to retry the update.

The TMPE633 provides a SPI configuration flash that is large enough to hold multiple FPGA configuration bitstreams. This allows the use of the Spartan-6 MultiBoot feature.

Refer to Xilinx UG380 “Spartan-6 FPGA Configuration User Guide” for more details.

The TMPE633 example design provides a fallback MultiBoot example with “golden” and “multiboot” bitstreams.

6 Installation

To install the PCI Express Mini Card, insert it, slightly slanted, into the connector and fold it down. If the carrier board has spring latches, gently push the card down until the spring latch locks in place. Otherwise secure the card with screws.

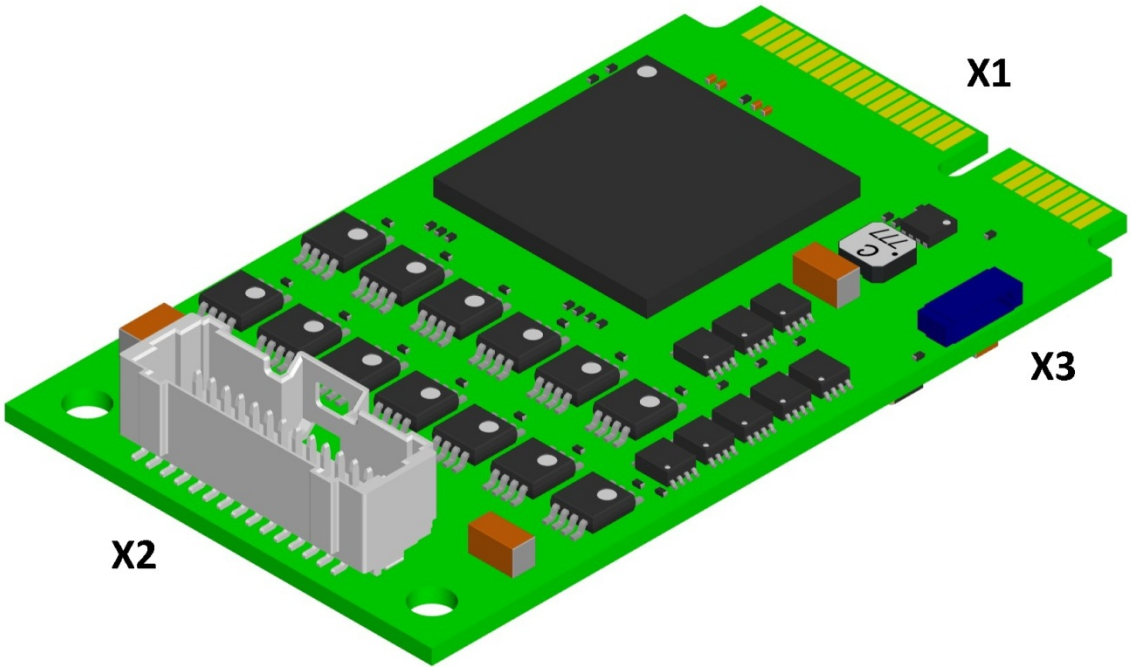
To remove the card, remove the screws or pull the spring latch away from the card until it pops up. The card can then be removed from the connector.

The I/O connector will exceed the available PCI Express Mini Card components height. Check carefully if you application provides enough spacing for a TMPE633.

7 I/O Connectors

This chapter provides information about user accessible on-board connectors

7.1 Overview



X1	System Connector
X2	I/O Connector
X3	JTAG Connector

Figure 7-1 : I/O Connector Overview

7.2 Board Connectors

7.2.1 System Connector (X1)

Pin-Count	52
Connector Type	Card-edge
Source & Order Info	none

Signal names in grey are not used by the card.

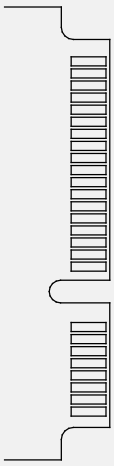
Description	Pin		Pin	Description
W_DISABLE2#	51		52	+3.3Vaux
Reserved	49		50	GND
Reserved	47		48	+1.5V
Reserved	45		46	LEP_WPAN#
GND	43		44	LEP_WLAN#
+3.3Vaux	41		42	LEP_WWAN#
+3.3Vaux	39		40	GND
GND	37		38	USB_D+
GND	35		36	USB_D-
PETp0	33		34	GND
PETn0	31		32	SMB_DATA
GND	29		30	SMB_CLK
GND	27		28	+1.5V
PERp0	25		26	GND
PERn0	23		24	+3.3Vaux
GND	21		22	PERST#
UIM_IC_DP	19		20	W_DISABLE1#
UIM_IC_DM	17		18	GND
Mechanical Key				Mechanical Key
GND	15		16	UIM_SPU
REF_CLK+	13		14	UIM_RESET
REF_CLK-	11		12	UIM_CLK
GND	9		10	UIM_DATA
CLKREQ#	7		8	UIM_PWR
COEX2	5		6	+1.5V
COEX1	3		4	GND
WAKE#	1		2	+3.3Vaux

Figure 7-2 : Preliminary System Connector Pin Assignment

7.2.2 I/O Connector (X2)

Pin-Count	30
Connector Type	Molex Pico-Clasp, dual row straight header, with lock
Source & Order Info	501190-3017
Mating Part	501189-2010

The I/O connector will exceed the available PCI Express Mini Card components height. Check carefully if you application provides enough spacing for a TMPE633.

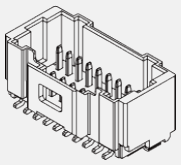
Pin Assignment						
Description		**Pin**		**Pin**	**Description**	
TTL (-10R)	**Diff. (-11R/-12R)**				**TTL (-10R)**	**Diff. (-11R/-12R)**
GND	GND	1		2	GND	GND
I/O_0	I/O_0+	3		4	I/O_1	I/O_0-
I/O_2	I/O_1+	5		6	I/O_3	I/O_1-
I/O_4	I/O_2+	7		8	I/O_5	I/O_2-
I/O_6	I/O_3+	9		10	I/O_7	I/O_3-
I/O_8	I/O_4+	11		12	I/O_9	I/O_4-
I/O_10	I/O_5+	13		14	I/O_11	I/O_5-
I/O_12	I/O_6+	15		16	I/O_13	I/O_6-
I/O_14	I/O_7+	17		18	I/O_15	I/O_7-
I/O_16	I/O_8+	19		20	I/O_17	I/O_8-
I/O_18	I/O_9+	21		22	I/O_19	I/O_9-
I/O_20	I/O_10+	23		24	I/O_21	I/O_10-
I/O_22	I/O_11+	25		26	I/O_23	I/O_11-
I/O_24	I/O_12+	27		28	I/O_25	I/O_12-
GND	GND	29		30	GND	GND

Figure 7-3 : I/O Connector Pin Assignment

I/O_x signals correspond to the DIOx/OEx FPGA pins.

The DIOx/OEx FPGA pins for the I/O_x signals that are not shown in the table are not connected on this build option (i.e. I/O_13 to I/O_25 are not connected for differential board variants like TMPE633-11R or TMPE633-12R).

7.2.3 JTAG Connector (X3)

Pin-Count	10
Connector Type	JST XRS 10pol 0,6 mm Pitch IDC Connector
Source & Order Info	SM10B-XSRS-ETB
Mating Part	10XSR-36S

The TMPE633 provides a JTAG connector to access the FPGA's JTAG port.

TEWS provides a "Programming Kit" (TA308) which includes a XSR cable and an adapter module that provides a Xilinx USB Programmer II compatible 2 mm shrouded header.

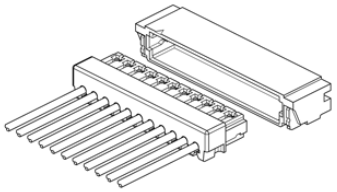
	Pin	Description
	1	GND
	2	TCK
	3	TMS
	4	TDI
	5	TDO
	6	GND
	7	GPIO0
	8	GPIO1
	9	PRESENT#
	10	V_{REF}

Figure 7-4 : XRS Connector Pin Assignment

GPIO0 is connected to FPGA DONE

GPIO1 is connected to Power Good (covers FPGA V_{CORE})

PRESENT# is not used by the TMPE633.

V_{REF} is 3.3 V

8 Appendix A

This appendix contains the signal to pin assignments for the Spartan-6 FPGA.

```
## ########################################################################## ##
##                              TEWS TECHNOLOGIES                             ##
## ########################################################################## ##
##
##   Project Name    : TMPE633 UCF
##   File Name       : tmpe633.ucf
##   Target Device   : XC6SLXxxT-xCSG324
##   Design Tool     : Xilinx ISE Design Suite Embedded 14.7
##   Simulation Tool : -
##
##   Description     : The file lists all FPGA pins that are connected on the
##                     TMPE633
##
##   Owner           : TEWS TECHNOLOGIES GmbH
##                     Am Bahnhof 7
##                     D-25469 Halstenbek
##
##                     Tel.: +49 / (0)4101 / 4058-0
##                     Fax.: +49 / (0)4101 / 4058-19
##                     e-mail: support@tews.com
##
##                     Copyright (c) 2015
##                     TEWS TECHNOLOGIES GmbH
##
##   History         :
##       Version   1 : (RR, 14.10.2015)
##                     Initial Version
##
##   Comments        : none
##
## ########################################################################## ##


## ########################################################################## ##
## Section: Miscellaneous
## ########################################################################## ##

# Set VCC aux power supply values (necessary for Spartan-6 architecture)
config vccaux = 3.3;

# Additional Bank Supply Information find below:
#
#    Bank No.       Supply
# ----------------------------
#       0            3.3 V
#       1            3.3 V
#       2            3.3 V
#       3            3.3 V
#
# Since all banks are supplied by 3.3 V, all signals get the same default
# IOSTANDARD
net "*"               iostandard = LVCMOS33;
```

```
# Prohibit usage of pins that are not allowed for user I/O

config prohibit                    = "T15";       # Bank 2, M0
config prohibit                    = "N12";       # Bank 2, M1
config prohibit                    = "U3";        # Bank 2, INIT_B
config prohibit                    = "B2";        # Bank 0, HSWAPEN


## ########################################################################## ##
## Section: GTP Transceiver
## ########################################################################## ##

# Location Constraints
net "PER0_P"                  loc = "B4";        # Bank 101, PCI Express TX_P
net "PER0_N"                  loc = "A4";        # Bank 101, PCI Express TX_N
net "PET0_P"                  loc = "D5";        # Bank 101, PCI Express RX_P
net "PET0_N"                  loc = "C5";        # Bank 101, PCI Express RX_N

net "REFCLK_P"                loc = "B8";        # Bank 101, 100 MHz PCI Express
                                                   Reference Clock (CLK_P)
net "REFCLK_N"                loc = "A8";        # Bank 101, 100 MHz PCI Express
                                                   Reference Clock (CLK_N)

# Additional Constraints
NET "*/gt_refclk_out(0)" TNM_NET = GT_REFCLK_OUT;
TIMESPEC TS_GT_REFCLK_OUT = PERIOD GT_REFCLK_OUT 10 ns HIGH 50 %;


## ########################################################################## ##
## Section: Clocking
## ########################################################################## ##

# Location Constraints
net "USER_CLK"                loc = "V10";       # Bank 3


# Additional Constraints
net "USER_CLK"            tnm_net = "USER_CLK";
timespec "TS_USER_CLK"            = period "USER_CLK" 40 MHz high 50 %;


## ########################################################################## ##
## Section: I/O Lines
## ########################################################################## ##

# Location Constraints
net "DIO[0]"                  loc = "L14";       # Bank 1
net "DIO[1]"                  loc = "N17";       # Bank 1
net "DIO[2]"                  loc = "M16";       # Bank 1
net "DIO[3]"                  loc = "N18";       # Bank 1
net "DIO[4]"                  loc = "L18";       # Bank 1
net "DIO[5]"                  loc = "U17";       # Bank 1
net "DIO[6]"                  loc = "C18";       # Bank 1
net "DIO[7]"                  loc = "G18";       # Bank 1
net "DIO[8]"                  loc = "V12";       # Bank 2
net "DIO[9]"                  loc = "U7";        # Bank 2
net "DIO[10]"                 loc = "R7";        # Bank 2
```

```
net "DIO[11]"                   loc = "N6";        # Bank 2
net "DIO[12]"                   loc = "U13";       # Bank 2
net "DIO[13]"                   loc = "N10";       # Bank 2
net "DIO[14]"                   loc = "F18";       # Bank 1
net "DIO[15]"                   loc = "M18";       # Bank 1
net "DIO[16]"                   loc = "N8";        # Bank 2
net "DIO[17]"                   loc = "P8";        # Bank 2
net "DIO[18]"                   loc = "U8";        # Bank 2
net "DIO[19]"                   loc = "V13";       # Bank 2
net "DIO[20]"                   loc = "V5";        # Bank 2
net "DIO[21]"                   loc = "V7";        # Bank 2
net "DIO[22]"                   loc = "N5";        # Bank 2
net "DIO[23]"                   loc = "N7";        # Bank 2
net "DIO[24]"                   loc = "R5";        # Bank 2
net "DIO[25]"                   loc = "T5";        # Bank 2

net "OE[0]"                     loc = "M8";        # Bank 2
net "OE[1]"                     loc = "M11";       # Bank 2
net "OE[2]"                     loc = "P12";       # Bank 2
net "OE[3]"                     loc = "V15";       # Bank 2
net "OE[4]"                     loc = "R11";       # Bank 2
net "OE[5]"                     loc = "U15";       # Bank 2
net "OE[6]"                     loc = "E16";       # Bank 1
net "OE[7]"                     loc = "U11";       # Bank 2
net "OE[8]"                     loc = "V11";       # Bank 2
net "OE[9]"                     loc = "V4";        # Bank 2
net "OE[10]"                    loc = "T7";        # Bank 2
net "OE[11]"                    loc = "T3";        # Bank 2
net "OE[12]"                    loc = "P6";        # Bank 2
net "OE[13]"                    loc = "R10";       # Bank 2
net "OE[14]"                    loc = "F17";       # Bank 1
net "OE[15]"                    loc = "L17";       # Bank 1
net "OE[16]"                    loc = "M10";       # Bank 2
net "OE[17]"                    loc = "N9";        # Bank 2
net "OE[18]"                    loc = "T12";       # Bank 2
net "OE[19]"                    loc = "P11";       # Bank 2
net "OE[20]"                    loc = "T4";        # Bank 2
net "OE[21]"                    loc = "V8";        # Bank 2
net "OE[22]"                    loc = "R3";        # Bank 2
net "OE[23]"                    loc = "U5";        # Bank 2
net "OE[24]"                    loc = "V6";        # Bank 2
net "OE[25]"                    loc = "T6";        # Bank 2


##
##############################################################################
############# ##
## Section: SPI
##
##############################################################################
############# ##

# Define Location Constraints
net "CCLK"                      loc = "R15";       # Bank 2, CCLK
net "CSO_B"                     loc = "V3";        # Bank 2, CSO_B

net "MOSI"                      loc = "T13";       # Bank 2, MOSI
net "MISO"                      loc = "R13";       # Bank 2, D0
```

```
net "WP_n"                    loc = "T14";       # Bank 2, D1
net "HOLD_n"                  loc = "V14";       # Bank 2, D2


## ########################################################################## ##
## Section: Module Management
## ########################################################################## ##


# Location Constraints
net "PULL_SEL[0]"             loc = "F14";       # Bank 1
net "PULL_SEL[1]"             loc = "F16";       # Bank 1

net "PERST_n"                 loc = "E8";        # Bank 0, PCI Express Reset


## ########################################################################## ##
## Section: General Purpose I/O
## ########################################################################## ##

# Location Constraints
config prohibit                   = "C15";       # Bank 0, SMB_CLK
config prohibit                   = "A15";       # Bank 0, SMB_DAT

net "LED_WWAN"                loc = "E6";        # Bank 0
net "LED_WPAN"                loc = "F7";        # Bank 0
net "LED_WLAN"                loc = "G8";        # Bank 0
```