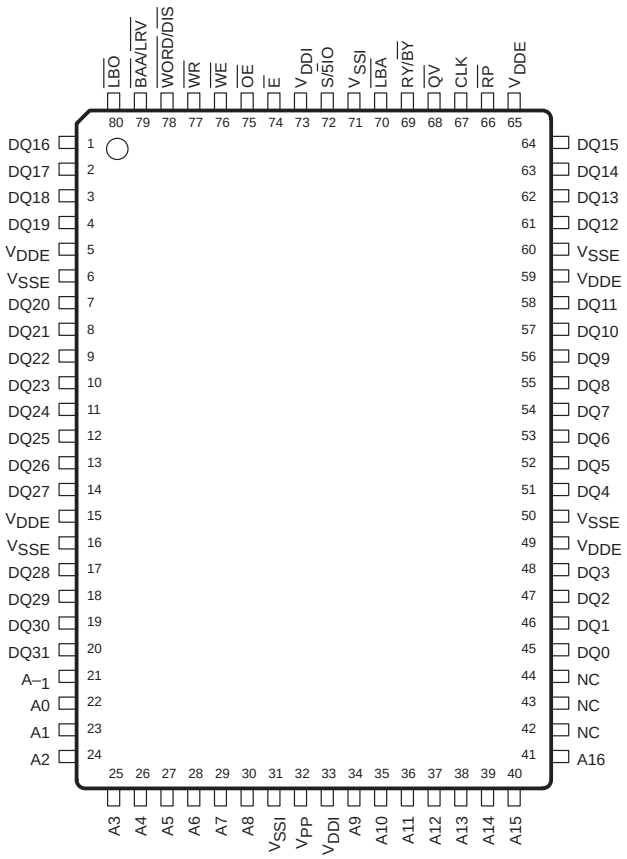
- **Organization**
  - **512K-Byte Main Array**
  - **24K-Byte Protected Overlay-Block**
- **User-Defined x16 or x32 Data Bus**
- **Read Transfer Data Rates Up to 100 MBytes/s at Bus Frequencies Up to 40 MHz**
- **Burstable Pipelined Read Interface With Programmable Latency, Length, and Order**
- **10000 Program/Erase Cycles**
- **Three Temperature Ranges**
  - **Commercial . . . 0°C to 70°C**
  - **Extended . . . – 40°C to 85°C**
  - **Automotive . . . – 40°C to 125°C**
- **80-Pin Plastic Quad Flatpack (PQFP) (PAF Suffix)**
- **Fully Automated On-Chip Erase and Program Operations**
- **Three Separate Voltage Supplies**
  - **I/O Supply – Configurable 3.3 V/5 V**
  - **Read Supply – 5 V**
  - **Programming Supply – 12 V**
- **All Inputs/Outputs TTL-Compatible**

PAF
80-PIN PACKAGE
(T0P VIEW)



description

The TMS28F033 is the first synchronous nonvolatile flash memory device to offer a configurable burst interface to 16/32-bit microprocessors and microcontrollers operating at frequencies up to 40 MHz.

The TMS28F033 contains 4M bits of main memory that is user-configurable as either three or four independently erasable blocks. In addition to the main memory array, there is a protected overlay memory block that is normally hidden from the memory address map. The following table shows the three- and four-block main-memory-array configurations for both 16-bit and 32-bit data bus widths.

Table 1. Memory Configurations

DATA BUS WIDTH	3-BLOCK MAIN ARRAY	4-BLOCK MAIN ARRAY	PROTECTED OVERLAY BLOCK
16 bits	32K, 160K, and 64K	32K, 96K, 64K, and 64K	12K
32 bits	16K, 80K, and 32K	16K, 48K, 32K, and 32K	6K

Embedded program and block-erase functions are fully automated by an on-chip write state machine (WSM), which simplifies these operations and relieves the system microcontroller of these secondary tasks. WSM status can be monitored by the on-chip status register to determine the progress of program/erase tasks.

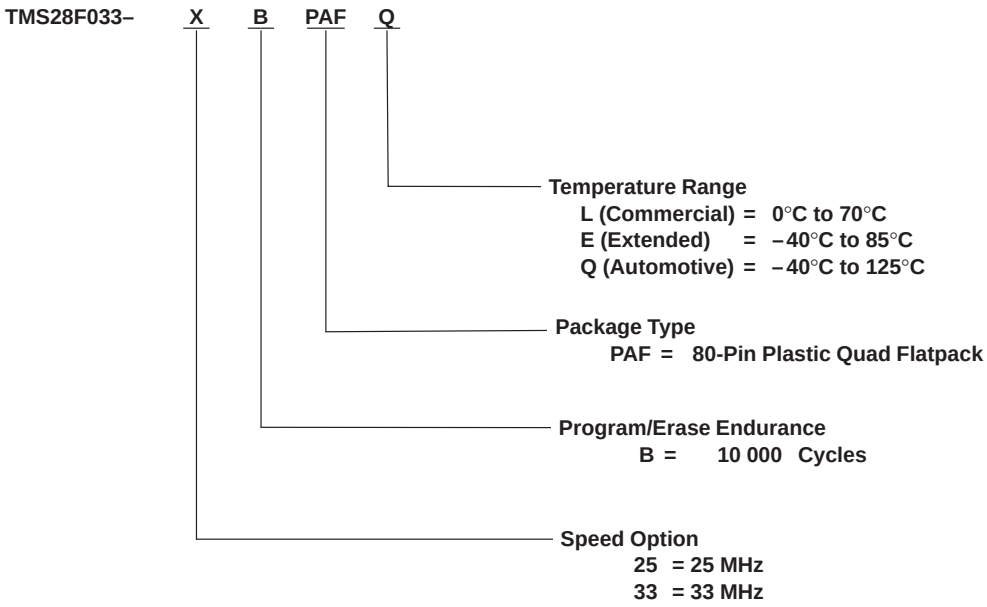
ADVANCE INFORMATION

description (continued)

The TMS28F033 flash memory requires 12 V for erasure and programming, and 5 V for memory-array access while interfacing with either a 3.3-V or 5-V bus.

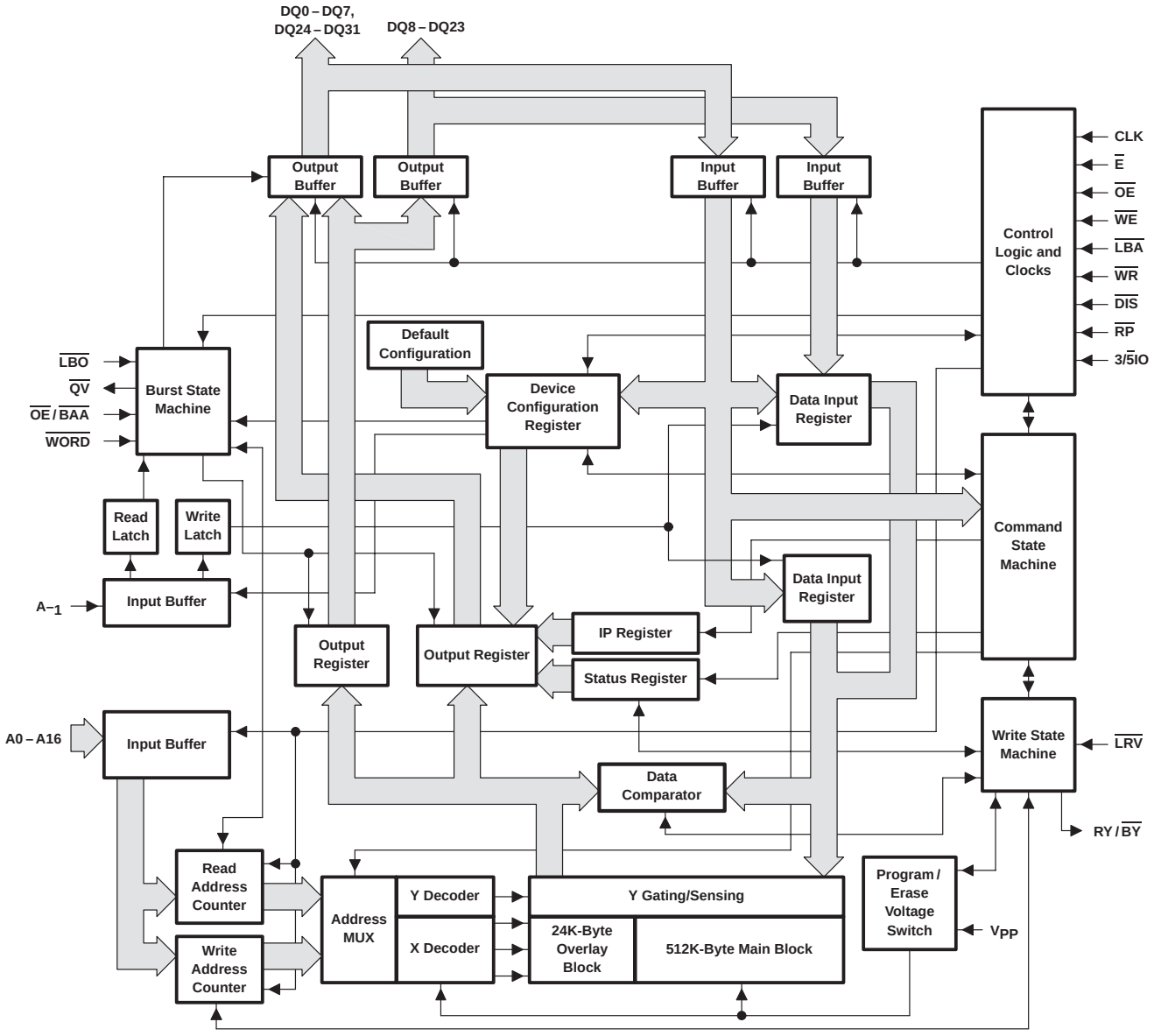
The TMS28F033 flash memory is fabricated using CMOS technology and is packaged in an 80-pin plastic quad flatpack (PQFP) (PAF suffix).

device symbol nomenclature



ADVANCE INFORMATION

functional block diagram



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Terminal Functions

TERMINAL NAME	TERMINAL TYPE†	DESCRIPTION
A_{-1}	I	Word select address. A_{-1} is the low-order address for the 16-bit data bus, and selects between the high and low word. A_{-1} is not used for the 32-bit data bus.
A0 – A16	I	Address bus. A0 – A16 select one of the 131072 32-bit segments (double-words), or, with A_{-1}, selects one of the 262144 16-bit segments (words). A0 is the low-order address for the 32-bit data bus.
DQ0 – DQ31	I/O	Data bus. Bidirectional data bus, where for both 16-bit and 32-bit data bus widths, DQ31 is the most significant bit (MSB) and DQ0 is the least significant bit (LSB). The 16-bit data bus uses DQ0 – DQ7 and DQ24 – DQ31.
$\overline{LBA}$	I	Load-burst address. For synchronous operation, when $\overline{LBA} = V_{IL}$ on a rising CLK edge, the address is latched for the beginning of a read or write operation.
$\overline{BAA}$	I	Burst-address advance. When $\overline{BAA} = V_{IL}$, the burst state machine increments the burst address for each required data beat on the rising CLK edge. For $\overline{BAA}$ usage, see Table 8 and Table 9.
$\overline{RP}$	I	Reset/power-down. When $\overline{RP} = V_{IL}$, the device terminates any current-state-machine activity and does not respond to read requests and does not accept write commands. On the rising edge of $\overline{RP}$, the device sets/clears the OBEB status register bit (SB1) based on the status of V_{PP}. When $V_{PP} \geq V_{PPH}$, OBEB is set; if $V_{PP} \leq V_{PPL}$, OBEB is cleared (see Table 3).
$\overline{E}$	I	Chip enable. When $\overline{E} = V_{IL}$, the device is enabled for read or write operations. When $\overline{E} = V_{IH}$, the device is in standby mode. $\overline{E}$ is an asynchronous signal. For $\overline{E}$ usage, see Table 8 and Table 9.
$\overline{OE}$	I	Output enable. $\overline{OE}$ is used for read operations and can be either synchronous or asynchronous (see Table 8 and Table 9). For synchronous $\overline{OE}$, when $\overline{OE} = V_{IL}$ on a rising CLK edge, the output data is latched and becomes valid prior to the next rising CLK edge. $\overline{OE} = V_{IH}$ during write operations.
$\overline{LBO}$	I	Linear-burst order. When $\overline{LBO} = V_{IL}$, the address counter is set for linear burst. When $\overline{LBO} = V_{IH}$, the address counter is set for interleaved burst. For $\overline{LBO}$ usage, see Table 9 and Table 12.
$\overline{WR}$	I	Write. $\overline{WR}$ is a synchronous signal that controls the read and write operations. If $\overline{WR} = V_{IL}$ when the address is latched ($\overline{LBA} = V_{IL}$), then the cycle is a write cycle . If $\overline{WR} = V_{IH}$ when the address is latched, then the cycle is a read cycle.
$\overline{WE}$	I	Write enable. $\overline{WE}$ is used for write/erase operations and can be either synchronous or asynchronous (see Table 8 and Table 9). For synchronous $\overline{WE}$ usage, with the first occurrence of $\overline{WE} = V_{IL}$ (after the address is latched with $\overline{LBA}$ and $\overline{WR} = V_{IL}$) on a rising CLK edge, the input data/command is latched. For asynchronous writes, the data and address are latched on the $\overline{WE}$ rising edge.
$\overline{WORD}$	I	Word enable. $\overline{WORD}$ is used for selection of the data bus width. When $\overline{WORD} = V_{IL}$, the device has a 16-bit data bus, and data is input or output on DQ0 – DQ7 and DQ24 – DQ31, and address A_{-1} selects between the high and low word. When $\overline{WORD} = V_{IH}$, the device has a 32-bit data bus and turns off the A_{-1} input buffer. For $\overline{WORD}$ usage, see Table 8 and Table 9.
$\overline{DIS}$	I	Disable output. When $\overline{DIS} = V_{IL}$, the synchronous $\overline{OE}$, DQ's, and $\overline{QV}$ signals are disabled. $\overline{DIS}$ functions as an additional synchronous output enable (opposite in logic to $\overline{OE}$). For $\overline{DIS}$ usage, see Table 8 and Table 9.
$\overline{LRV}$	I	Low regulator voltage. When $\overline{LRV} = V_{IL}$ during a write/erase operation, the LRVS status register bit (SB4) is set (see Table 7). $\overline{LRV}$ is an asynchronous signal. For $\overline{LRV}$ usage, see Table 8 and Table 9.
$\overline{QV}$	OD O	Data valid. $\overline{QV}$ is used for read operations. $\overline{QV} = V_{IL}$ when output data is valid on the data bus for either a single or burst-read operation. When $\overline{QV} = V_{IH}$, there is no valid data on the data bus. For $\overline{QV}$ usage, see Table 8 and Table 9.
RY/$\overline{BY}$	OD O	Ready/busy. RY/$\overline{BY}$ indicates the status of the WSM. When $\overline{RY}/\overline{BY} = V_{IL}$, the WSM is currently active performing an operation. When RY/$\overline{BY} = V_{IH}$, the WSM is ready for a new operation. For RY/$\overline{BY}$ usage, see Table 8 and Table 9.
CLK	I	Clock. Signals on both the address and data buses are transmitted and received relative to this system clock. All synchronous inputs must meet setup and hold times relative to the rising CLK edge.
3/5$\overline{IO}$	I	3.3/5.0 I/O select. 3/5$\overline{IO}$ is used to select the external power supply, V_{DDE}, as either 3.3 V or 5 V. Set 3/5$\overline{IO} = V_{IH}$ for V_{DDE} = 3.3 V operation, and set 3/5$\overline{IO} = V_{IL}$ for V_{DDE} = 5 V operation. For 3/5$\overline{IO}$ usage, see Table 8 and Table 9.

† I = input, O = output, OD = open drain, S = power supply

Terminal Functions (Continued)

TERMINAL NAME	TYPE†	DESCRIPTION
V_{PP}	S	Write/erase power supply. V_{PP} is the 12-V power supply for the write/erase operations.
V_{DDI}	S	Internal power supply. V_{DDI} is the 5-V power supply for the internal logic.
V_{DDE}	S	External power supply. V_{DDE} is the 3.3-V/5-V power supply for the inputs and outputs.
V_{SSE}	S	Output ground. V_{SSE} is the ground for the outputs DQ0–DQ31, RY/$\overline{BY}$, and $\overline{QV}$.
V_{SSI}	S	Input ground. V_{SSI} is the ground for both the inputs and internal logic.
NC		No connect. These pins are left unconnected inside the memory chip.

† I = input, O = output, OD = open drain, S = power supply

architecture

The TMS28F033 uses a blocked architecture to allow independent erasure of selected memory blocks. The block to be erased is selected by using any valid address within the block. Figure 1 and Figure 2 show the memory maps for the two configurations.

main memory

The TMS28F033 main memory is configurable to either three blocks (DCR5 = 0) or four blocks (DCR5 = 1), see Table 1, and Figure 1 and Figure 2.

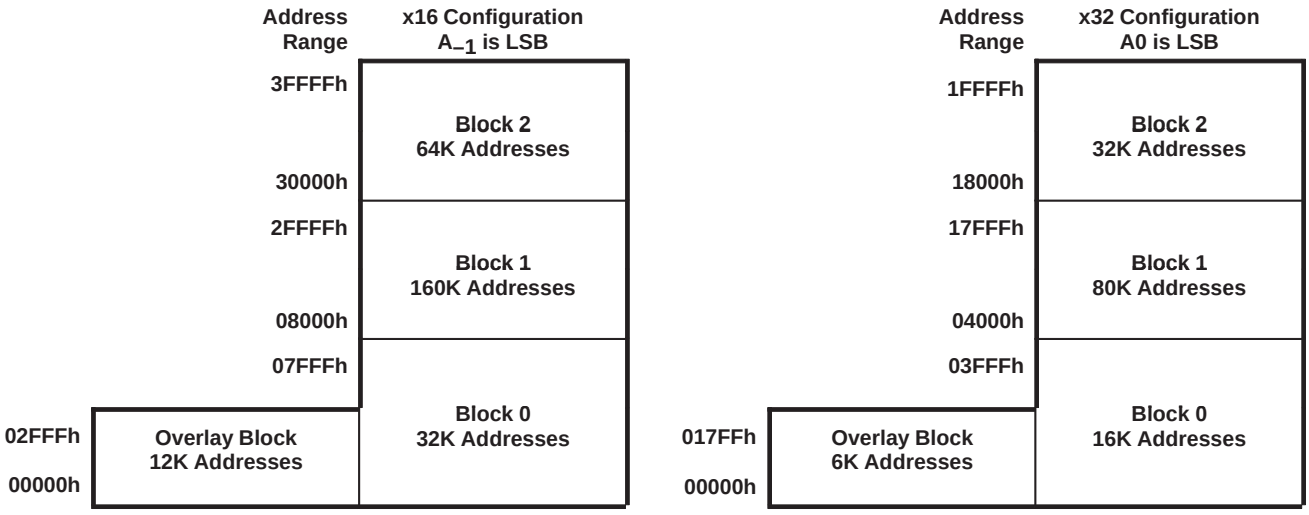

Figure 1. TMS28F033 With Three-Block Main-Array Memory Map (DCR5=0)

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main memory (continued)

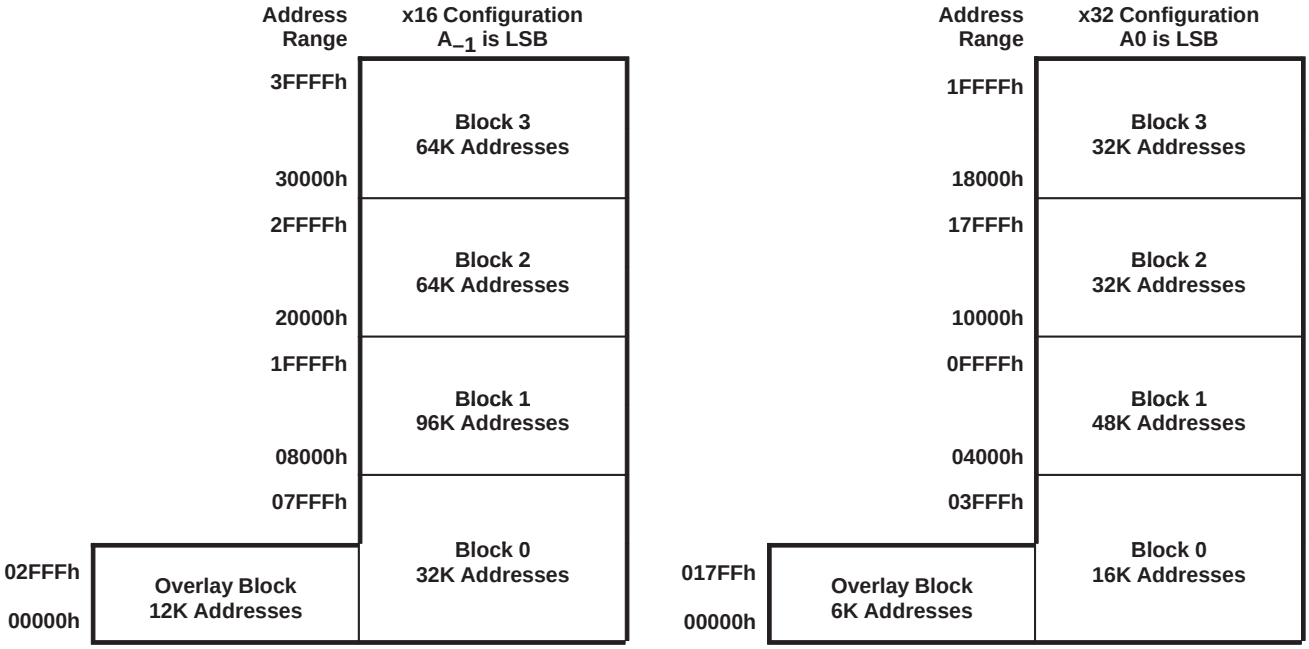

Figure 2. TMS28F033 With Four-Block Main-Array Memory Map (DCR5 = 1)

overlay block

The overlay block is a protected memory region that is programmed or erased using special command state machine (CSM) commands (see Table 4 and Table 5). When enabled, the overlay memory block exists from addresses 00000h to 017FFh for x32 addressing, or from 00000h to 02FFFh for x16 addressing. Two status register bits, OBEB and OBS, are available to monitor the overlay block enable/disable process (see Table 7). The overlay block status (OBS) bit indicates whether the overlay block is enabled (OBS = 1) or disabled (OBS = 0) for reading. See Table 2 for the state of the OBS bit for memory-read accessing. The status of the overlay-block-enable bit (OBEB) does not necessarily indicate that the overlay block is enabled, instead OBEB reflects the state of the overlay block control switch. When OBEB = 1, the switch is set, and when OBEB = 0, the switch is not set (see the overlay-block-control functional diagram in Figure 3). See Table 3 for a listing of methods that set/clear the OBEB.

Table 2. Read-Accessing of the Overlay Block or Main Array

STATE OF OBEB (SB1)	V_{PP} STATUS	STATE OF OBS (SB0)	READ ACCESS
1	$V_{PP} \geq V_{PPH}$	1	Overlay Block
1	$V_{PP} \leq V_{PPL}$	0	Main Array
0	X†	0	Main Array
1	$V_{PPL} < V_{PP} < V_{PPH}$	Not guaranteed	Unknown

† X is a don't care.

overlay block (continued)

Table 3. Methods of Setting/Clearing the Overlay-Block-Enable Bit (OBEB)

METHOD	PRIOR STATE OF OBEB	NEXT STATE OF OBEB
Toggle $\overline{RP}$ with $V_{PP} \geq V_{PPH}$	X†	1
Toggle $\overline{RP}$ with $V_{PP} \leq V_{PPL}$	X†	0
Power-on-reset of V_{DDI} with $V_{PP} \geq V_{PPH}$	X†	1
Power-on-reset of V_{DDI} with $V_{PP} \leq V_{PPL}$	X†	0
Issue CSM command 06h	0	1
Enable/disable overlay block for reads	1	0

† X is a don't care.

The enable/disable-overlay-block CSM command (06h) is used to enable the overlay block for a read operation, or to disable the overlay block after a read operation. When 06h is issued for overlay-block access, both the overlay-block latch and OBEB are set whether $V_{PP} \geq V_{PPH}$ or not. However, only the overlay block is enabled (and only OBS is set) if $V_{PP} \geq V_{PPH}$.

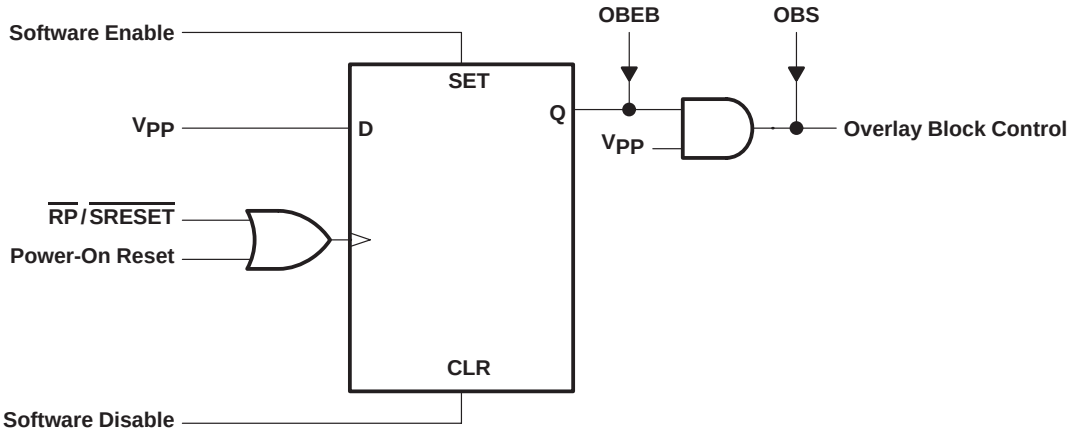

Figure 3. Overlay-Block-Control Functional Diagram

command state machine (CSM)

Commands are issued to the CSM using standard microprocessor write timings. The CSM acts as an interface between the external microprocessor and the internal WSM. The available commands are listed in Table 4 and the corresponding descriptions are in Table 5. When a program or erase command is issued to the CSM, the WSM controls the internal sequences and the CSM responds only to status reads. A command is valid only if the exact sequence of writes is completed. After the WSM completes its task, the WSM status bit (SB7) is set to a logic-high level, allowing the CSM to respond to the full command set again. In addition, Ready/Busy (RY/$\overline{BY}$) is an optional output that is available to monitor the WSM status.

operation

Device operations are selected by entering standard JEDEC 8-bit command codes with conventional microprocessor timing into an on-chip CSM through I/O pins DQ0–DQ7. When the device is powered up, internal reset circuitry initializes the chip to a read-array mode of operation. Changing the mode of operation requires a command code to be entered into the CSM.

The on-chip status register allows the progress of various operations to be monitored. The status register is interrogated by entering a read-status-register command into the CSM (cycle 1) and reading the register data on I/O pins DQ0–DQ7 (cycle 2). Status register bits SB0 through SB7 correspond to DQ0 through DQ7.

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operation (continued)

Table 4. Command-State-Machine Codes for Device Mode Selection

COMMAND CODE ON DQ0 – DQ7†	DEVICE MODE
02h	Block-erase setup of overlay block
04h	Program setup of overlay block
06h	Enable/disable overlay block for reads
0Dh	Block-erase confirm of overlay block
20h	Block-erase setup of main array
40h	Program setup of main array
50h	Clear status register
60h	Enable/disable low-power programming
70h	Read status register
90h	Silicon signature selection
96h	Load device-configuration register
D0h	Block-erase confirm of main array
F0h	Reduced power
FFh	Read array

† DQ0 is the least significant bit. DQ8 – DQ31 can be any valid 2-state level.

command definition

Once a specific command code has been entered, the WSM executes an internal algorithm that generates the necessary timing signals to program, erase, and verify data. See Table 5 for the CSM command definitions and the data for each of the bus cycles. See Table 6 for the addresses required to access the algorithm selection codes.

command definition (continued)

Table 5. Command Definitions

COMMAND	DATA BUS WIDTH	FIRST BUS CYCLE			SECOND BUS CYCLE			THIRD BUS CYCLE		
		OPERATION	ADDRESS	CSM INPUT	OPERATION	ADDRESS	DATA IN/OUT	OPERATION	ADDRESS	DATA IN/OUT
READ OPERATIONS										
Read Array	x16/x32	Write	00000h†	FFh	Read	RA	DO			
Read Algorithm Selection Code (see Note 1, and Table 6)	x16/x32	Write	00000h†	90h	Read	A1A0	M/D DCR			
Read Status Register	x16/x32	Write	00000h†	70h	Read	X	SRB			
PROGRAM OPERATIONS										
Program Setup/Program of Main Array (see Note 1)	x16	Write	00000h†	40h	Write	A_{-1}	PD(L,H)	Write	PA	PD(H,L)
	x16/x32	Write	00000h†	40h	Write	PA	PD			
Program Setup/Program of Overlay Block (see Note 1)	x16	Write	00000h†	04h	Write	A_{-1}	PD(L,H)	Write	PA	PD(H,L)
	x16/x32	Write	00000h†	04h	Write	PA	PD			
Load DCR	x16/x32	Write	00000h†	96h	Write	X	CV			
ERASE OPERATIONS										
Block-Erase Setup/ Block-Erase Confirm of Main Array	x16/x32	Write	00000h†	20h	Write	BBA	D0h			
Block-Erase Setup/ Block-Erase Confirm of Overlay Block	x16/x32	Write	00000h†	02h	Write	BBA	0Dh			
OTHER OPERATIONS										
Reduced-Power Mode	x16/x32	Write	00000h†	F0h						
Enable/Disable Low-Power Programming	x16/x32	Write	00000h†	60h						
Clear Status Register	x16/x32	Write	00000h†	50h						
Enable/Disable Overlay Block for Read	x16/x32	Write	00000h†	06h						

† Address is a don't care for asynchronous writes.

NOTE 1: When using x16 (DCR3 = 1 and $\overline{WORD} = V_{IL}$), programming can be performed in either two or three cycles by configuring the DCR31 bit (see Table 8).

Legend:

ADDRESS

BBA = Block base address
PA = Address to be programmed
RA = Read address
X = Don't care

DATA

CV = Configuration value
DO = Read data out
M/D/DCR = Manufacturer code/device configuration register value
SRB = Status-register data byte on DQ0–DQ7
PD(L,H) = Data to be programmed at PA (low word, high word)

ADVANCE INFORMATION

command definition (continued)

Table 6. Algorithm Selection Codes (See Note 2)

DATA BUS WIDTH	ADDRESS (A0–A16)	A1	A0	A_{-1}	DATA OUT
	X0h	V_{IL}	V_{IL}	X	Manufacturer Code 0097h
16-Bit (see Note 3)	X1h	V_{IL}	V_{IH}	X	Device Code 0068h
	X2h	V_{IH}	V_{IL}	X	DCR Value DDDDh
	X0h	V_{IL}	V_{IL}	—	Manufacturer Code 00000097h
32-Bit (see Note 4)	X1h	V_{IL}	V_{IH}	—	Device Code 00000068h
	X2h	V_{IH}	V_{IL}	—	DCR Value DD0000DDh

NOTES: 2. X is a don't care.
3. When using the 16-bit data bus, the data lines are DQ0–DQ7 and DQ23–DQ31.
4. When using the 32-bit data bus, the data lines are DQ0–DQ31.

status register

The status register allows the user to determine whether the state of a program/erase operation is pending or complete. The status register is monitored by writing a read-status command to the CSM and reading the resulting status code on I/O pins DQ0–DQ7. This operation is valid in either the word-wide (x16) or double-word-wide (x32) mode. The high-order I/Os (DQ8–DQ31) are set to 000000h internally.

After a read-status command has been given, the data appearing on DQ0–DQ7 remains as status register data until a new command is issued to the CSM. To return the device to other modes of operation, a new command must be issued to the CSM. Status register data is updated on every clock cycle. During periods when the WSM is active, the status register can be read to determine the WSM status. Table 7 defines the status-register bits and their functions.

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status register (continued)

Table 7. Status-Register Bit Definitions and Functions

STATUS BIT	FUNCTION	DATA	COMMENTS
SB7	Write-State-Machine (WSM) Status	1 = Ready 0 = Busy	If SB7 = 0 (busy), the WSM has not completed an erase or programming operation. If SB7 = 1 (ready), other operations can be performed.
SB6	Reserved	0	
SB5 (DCR4 = 0)	Operation Status (OS)	1 = Commands/operations not successful 0 = Commands/operations successful	The WSM sets the OS bit high (SB5 = 1) after an illegal command has been issued, an error has occurred while erasing a block, or as the result of an error while programming a word. If all past operations have completed successfully, then the OS bit remains low (SB5 = 0); however, the WSM cannot clear this bit.
SB5 (DCR4 = 1)	Erase Status (ES)	1 = Block-erase error 0 = Block-erase good	SB5 = 0 indicates that a block-erase has been successful. SB5 = 1 indicates that an erase error has occurred. In this case, the WSM has completed the maximum erase pulses determined by the internal algorithm, but this was insufficient to completely erase the device.
SB4 (DCR4 = 0)	Low Regulator Voltage Status (LRVS)	1 = $\overline{\text{LRV}}$ asserted 0 = $\overline{\text{LRV}}$ not asserted	The LRVS bit is set high (SB4 = 1) when the $\overline{\text{LRV}}$ input is asserted during an erase or program command. The clear-status-register command clears the LRVS bit (SB4 = 0).
SB4 (DCR4 = 1)	Program Status (PS)	1 = Program error 0 = Program good	SB4 = 0 indicates successful programming has occurred at the addressed location. SB4 = 1 indicates that the WSM was unable to correctly program the addressed location.
SB3	V_{PP} Status (VPPS)	1 = Program abort: V_{PP} range error 0 = V_{PP} good	SB3 provides information on the status of V_{PP} during programming and erasing. If V_{PP} is lower than V_{PPL} after a program or erase command has been issued, SB3 is set to a 1 to indicate that the operation is aborted.
SB2	Low-Power Mode (LPM)	1 = Byte-program 0 = Word-program	When the LPM bit is set high (SB2 = 1), the WSM programs each word in byte increments. When the LPM bit is low (SB2 = 0), the WSM programs in word (x32 or x16) increments.
SB1	Overlay-Block-Enable Bit (OBEB)	1 = Overlay block can be enabled 0 = Overlay block disabled	When the OBEB bit, which is V_{PP}-independent, is set (SB1 = 1), the overlay block can be enabled for reads. When the OBEB bit is low (SB1 = 0), the overlay block is disabled for reads.
SB0	Overlay-Block Status (OBS)	1 = Overlay block enabled 0 = Overlay block disabled	When the OBS bit, with $V_{PP} \geq V_{PPH}$, is set (SB0 = 1), the overlay block is enabled for reads. When the OBS bit is cleared (SB0 = 0), the overlay block is disabled for reads.

device configuration register (DCR)

The DCR is a user-loaded register that determines many of the device functions (see Table 8). Sixteen configurable bits (DCR0–DCR7 and DCR24–DCR31 with DCR26–27 reserved) can be set by using the load-DCR CSM command (96h) (see Table 5). The current value of the DCR can be read with CSM command 90h, provided A1 is set to V_{IH} and A0 is set to V_{IL} (see Table 6).

device configuration defaults

The term “default” denotes the state of a bit in the DCR when the device is first powered up or when a power-on reset is performed. These defaults are set at the factory after fabrication. After the CSM command that loads the DCR (96h) is executed, the defaults no longer define the device operation; instead, the new configuration takes effect. To restore the default state, either perform a power-on reset or load the DCR with the reset-state settings using the 96h command sequence.

The TMS28F033 has two types of defaults: a fuse-bit-option default and a standard default. The difference between the two types is that a fuse-bit-option default can be optionally set (0 or 1) at the factory, whereas a standard default is always set to 0 at the factory. The DCR has eight fuse-bit-option defaults, DCR0–DCR7, and eight standard defaults, DCR24–DCR31. The X-latency bits DCR28–DCR29 are the only exceptions to these two types of defaults. These bits default to 00 (standard defaults), except when the device is in x16 mode ($\overline{WORD} = V_{IL}$) or when $\overline{OE}$ is asynchronous (DCR1 = 1). In these exceptions, the DCR28–DCR29 bits function as 10 (see Table 8). It is important to note that even though DCR28–DCR29 functions as 10 for these exceptions, they are still read (with the DCR read command 90h) as 00, instead of 10.

Table 8. Device Configuration Register Bit Definitions and Functions

DCR BIT	FUNCTION	DATA	COMMENTS
DCR0	Control pin configuration	0 = Basic Control Pin Set 1 = Enhanced Control Pin Set (see Note 5 and Note 6)	When DCR0 = 0, the device functions with the basic pin set, and the internal pullups are enabled for the $\overline{RP}$, $\overline{BAA}/\overline{LRV}$, and $\overline{WORD}/\overline{DIS}$ pins. When DCR0 = 1, the device functions with the enhanced pin set. See the Terminal Functions table and Table 9
DCR1	$\overline{OE}$ functionality	0 = Synchronous $\overline{OE}$ 1 = Asynchronous $\overline{OE}$ (see Note 5 and Note 6)	When DCR1 = 0, $\overline{OE}$ functions as a synchronous output enable. When DCR1 = 1, $\overline{OE}$ functions asynchronously. See the Terminal Functions table and Table 9
DCR2	$\overline{WE}$ functionality	0 = Synchronous $\overline{WE}$ 1 = Asynchronous $\overline{WE}$ (see Note 5 and Note 6)	When DCR2 = 0, $\overline{WE}$ functions as a synchronous write enable. When DCR2 = 1, $\overline{WE}$ functions asynchronously. See the Terminal Functions table and Table 9
DCR3	$\overline{WORD}/\overline{DIS}$ functionality	0 = $\overline{DIS}$, and x32 mode 1 = $\overline{WORD}$ (see Note 5 and Note 6)	When DCR3 = 0, pin 78 functions as output disable ($\overline{DIS}$) and the device is forced into x32 mode. When DCR3 = 1, pin 78 functions as $\overline{WORD}$ (for x16 mode, set $\overline{WORD} = V_{IL}$; and for x32 mode, set $\overline{WORD} = V_{IH}$). See the Terminal Functions table and Table 9
DCR4	$\overline{BAA}/\overline{LRV}$ functionality	0 = $\overline{LRV}$ 1 = $\overline{BAA}$ (see Note 5 and Note 6)	When DCR4 = 0, pin 79 functions as low regulator voltage ($\overline{LRV}$) and its status can be monitored in SB4. When DCR4 = 1, pin 79 functions as burst address advance ($\overline{BAA}$). See the Terminal Functions table and Table 9
DCR5	Main block control	0 = 3 Main Blocks 1 = 4 Main Blocks (see Note 5 and Note 6)	When DCR5 = 0, the main memory array has three blocks, as seen in Figure 1. When DCR5 = 1, the main memory array has four blocks, as seen in Figure 2. See Table 1.
DCR7, DCR6	Internal timing control	Refer to switching characteristics for t_{CHCH1} and t_{CHQV} (see Note 5 and Note 6)	These bits are used to optimize device performance (see switching characteristics table).

NOTES: 5. The default setting for these bits is set at the factory prior to shipping.
6. These bits return to the default setting after a power-on reset is performed; therefore, it is necessary to program these bits to the desired configuration.

device configuration defaults (continued)

Table 8. Device Configuration Register Bit Definitions and Functions (Continued)

DCR BIT	FUNCTION	DATA	COMMENTS
DCR8–DCR23	Reserved for Texas Instruments (TI™) and should not be used	0000h	
DCR25, DCR24	Burst length	00 = MOD4 (default) 01 = MOD8 10 = MOD16 11 = MOD32 (see Note 6)	There are four available burst length settings. The MOD4 burst is a modulo burst of four words/double-words for x16/x32, respectively. The other available burst lengths are MOD8, MOD16, and MOD32 (see Table 12).
DCR27, DCR26	Reserved for TI and should not be used	00 – (default) (see Note 6)	
DCR29, DCR28	Burst latency (X)	00 = $\overline{OE}$-controlled (default if in x32 mode and when $\overline{OE}$ is synchronous) 01 = 3 cycles 10 = 4 cycles (default if in x16 mode or when $\overline{OE}$ is asynchronous) 11 = 5 cycles (see Note 6)	The four X latency possibilities are $\overline{OE}$-controlled burst, and 3, 4, or 5 clock cycles for $\overline{BAA}$-controlled burst. X latency denotes the number of clock cycles required to access the first word from memory (see Table 10 and Table 11).
DCR30	Burst latency (Y)	0 = 1 cycle (default) 1 = 2 cycles (see Note 6)	The two Y latency possibilities are one clock cycle and two clock cycles. Y latency denotes the number of clock cycles required to access the subsequent words to complete the cache fill (see Table 10 and Table 11).
DCR31	One- or two-word write option for x16 mode	0 = Program one word (two-cycle write) (default) 1 = Program two words (three-cycle write) (see Note 6)	Applicable for x16 mode only. When DCR31 = 0, only one word (16 bits) is programmed in two cycles for each program command received by the CSM. When DCR31 = 1, two words (32 bits) are programmed in three cycles for each program command received by the CSM (see Table 5).

NOTES: 5. The default setting for these bits is set at the factory prior to shipping.
6. These bits return to the default setting after a power-on reset is performed; therefore, it is necessary to program these bits to the desired configuration.

control pin functions

The DCR0 bit is the control pin configuration bit that selects between the basic or enhanced pin set (see Table 8 and Table 9). With the enhanced pin set (DCR0 = 1), five additional pins are available: chip enable ($\overline{E}$), data valid ($\overline{QV}$), ready/busy (RY/$\overline{BY}$), 3.3-V/5-V IO voltage select (3/5$\overline{IO}$), and linear burst order ($\overline{LBO}$). With the basic pin set (DCR0 = 0), neither $\overline{QV}$ nor RY/$\overline{BY}$ are available, both $\overline{E}$ and $\overline{LBO}$ are effectively tied low (V_{IL}), and 3/5$\overline{IO}$ is effectively tied high (V_{IH}). The DCR1 and DCR2 bits determine the synchronous or asynchronous operation of output enable ($\overline{OE}$) and write enable ($\overline{WE}$), respectively. DCR3 determines the function of pin 78 as either output disable ($\overline{DIS}$) or word enable ($\overline{WORD}$) (see the Terminal Functions table). When DCR3 = 0 (for $\overline{DIS}$ usage) the device is forced into using the 32-bit data bus (see Figure 21). When DCR3 = 1, both the 16-bit and 32-bit data buses are available. The DCR4 bit determines the function of pin 79 as either low-regulator-voltage detection ($\overline{LRV}$) or burst-address advance ($\overline{BAA}$).

control pin functions (continued)

Table 9. DCR-Controlled Pin Functions

PIN NUMBER	DCR BIT (x)	DCRx = 0	DCRx = 1
68	0	Hi-Z	$\overline{QV}$
69	0	Hi-Z	RY/$\overline{BY}$
72	0	3.3-V IO	3/5$\overline{IO}$
74	0	Chip Enabled	$\overline{E}$
75	1	Synchronous $\overline{OE}$	Asynchronous $\overline{OE}$
76	2	Synchronous $\overline{WE}$	Asynchronous $\overline{WE}$
78	3	$\overline{DIS}$	$\overline{WORD}$
79	4	$\overline{LRV}$	$\overline{BAA}$
80	0	Linear Burst	$\overline{LBO}$

burst length

The burst length, as determined by DCR24–DCR25, is the length of the data sequence (or number of memory locations) to be read for each entered address. When using $\overline{BAA}$ (DCR4 = 1), there are four possibilities for burst length: modulo 4 addressing (MOD4), MOD8, MOD16, and MOD32. For MOD4, when the initial address is XXXX0h, the internal burst address order is 0–1–2–3 for linear burst ($\overline{LBO}$ = V_{IL}). MOD8, MOD16, and MOD32 function as 0–1–2 . . . 6–7, 0–1–2 . . . 14–15, and 0–1–2 . . . 30–31, respectively. Burst delivery is critical word first with wrap around.

burst access and burst performance

The notation X–Y– . . . –Y is used to denote the X and Y burst latency for the data sequence to be burst. X-latency (DCR28–DCR29) denotes the number of clock cycles required to access the first word/double-word from memory, and Y-latency (DCR30) denotes the number of clock cycles required to access the subsequent words/double-words to complete the cache fill (see Table 10). The four X-latency possibilities are: $\overline{OE}$-controlled, and 3, 4, or 5 clock cycles. The two Y-latency possibilities are 1 and 2 clock cycles. The burst performance for <25 MHz, <33 MHz, and <40 MHz for linear and interleave burst order is listed in Table 11.

Table 10. Burst Access Combinations (see Note 7)

DEVICE CONFIGURATION REGISTER BITS			BURST ACCESS (CLOCK CYCLES TO READ)
DCR30	DCR29	DCR28	
0	0	0	X–1– . . . –1 (see Note 8)
0	0	1	3–1– . . . –1
0	1	0	4–1– . . . –1
0	1	1	5–1– . . . –1
1	0	0	X–2– . . . –2 (see Note 8)
1	1	0	4–2– . . . –2

NOTES: 7. These burst access combinations are available for MOD4, MOD8, MOD16, and MOD32.
8. For both DCR30–DCR28 = 000 and DCR30–DCR28 = 100, the X-latency is $\overline{OE}$-controlled.

burst access and burst performance (continued)

Table 11. Burst Performance (Clock Cycles to Read)

FREQUENCY (MHz)	x16 Mode			x32 Mode
	LINEAR†		INTERLEAVE	LINEAR
	A_{-1} = 0	A_{-1} = 1		
< 25 (see Note 9)	4–2– . . . –2	4–2– . . . –2	4–2– . . . –2	4–2– . . . –2
< 33 (see Note 9)	4–2– . . . –2	5–1– . . . –1	4–1– . . . –1	4–2– . . . –2
< 40 (see Notes 9 and 10)	—	—	—	5–2– . . . –2

† The state of A_{-1} when the address is latched (at CLK 1 in Figure 14)

NOTES: 9. The Y-latency notation for MOD4 has three 1s/2s (–1–1–1/–2–2–2). For MOD8, there are seven 1s/2s (–1–1–1–1–1–1–1/–2–2–2–2–2–2–2). MOD16 has fifteen 1's/2's, and MOD32 has 31 1's/2's.

10. To obtain 5–2– . . . –2 (40 MHz), the required DCR settings are 4–2– . . . –2, and asynchronous $\overline{OE}$ with $\overline{BAA}$-controlled burst.

burst suspend/resume

Burst suspension is the ability to hold the address advance and the data on the output I/Os DQ0–DQ7 and DQ24–DQ31 if in x16 mode, or on DQ0–DQ31 if in x32 mode. For DCR4 = 1, the suspension of a burst sequence is possible by bringing $\overline{BAA}$ high. To resume the burst, bring $\overline{BAA}$ low again (see Figure 18). When DCR4 = 0, the suspension of the burst is possible by bringing $\overline{OE}$ high. To resume the burst, bring $\overline{OE}$ low again.

linear burst order ($\overline{LBO}$)

When performing a burst read, a single starting address is entered into the device and then the TMS28F033 internally accesses a sequence of locations based on that starting address. The burst sequence is determined by the linear burst order ($\overline{LBO}$) setting (see the Terminal Functions table). When $\overline{LBO}$ = V_{IL}, the burst order is linear 0–1–2–3 . . . .; and when $\overline{LBO}$ = V_{IH}, the burst order is interleave (see Table 12). Linear burst order is available with MOD4, MOD8, MOD16, and MOD32. Interleave burst order is available only with MOD4, and only with the 16-bit data bus.

Table 12. 2-Bit Linear and Interleaved-Burst Sequences (MOD4)

BURST SEQUENCE	ADDRESS A1 – A0 For x32 Mode, AND A0 – A_{-1} For x16 Mode							
	DECIMAL				BINARY			
	START	2ND	3RD	4TH†	START	2ND	3RD	4TH†
Linear (see Note 11)	0	1	2	3	00	01	10	11
	1	2	3	0	01	10	11	00
	2	3	0	1	01	10	11	00
	3	0	1	2	11	00	01	10
Interleave (see Note 12)	0	1	2	3	00	01	10	11
	1	0	3	2	01	00	11	10
	2	3	0	1	10	11	00	01
	3	2	1	0	11	10	01	00

† Burst sequence continues until $\overline{OE}$ or $\overline{BAA}$ is brought high.

NOTES: 11. Linear burst is available with both x16 and x32 for MOD4, MOD8, MOD16, and MOD32. For linear burst set $\overline{LBO}$=V_{IL}.

12. Interleaved burst is available only with MOD4, and only with the 16-bit data bus. For interleave burst set $\overline{LBO}$ =V_{IH}.

word (X16) write option

DCR31 determines the number of write cycles for word-wide programming. For DCR31 = 0, the device performs two-cycle writes, or with DCR31 = 1, the device performs three-cycle writes (see Table 5). See Figure 22 and Figure 24 for synchronous two- and three-cycle writes, respectively. For asynchronous two-cycle writes, see Figure 23.

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operation modes for word-wide (x16) or double-word-wide (x32) mode selection

In x32 configuration, the memory array is divided into two parts: a lower half that outputs data through I/O pins DQ0–DQ7 and DQ24–DQ31, and an upper half that outputs data through DQ8–DQ23. Device operation in either x16 mode or x32 mode is user-selectable by configuring DCR3 = 1. This allows the input $\overline{\text{WORD}}$ logic state to determine either x16 or x32 mode. When $\overline{\text{WORD}}$ is at a logic-high level, the device is in the double-word-wide (x32) mode and data is written to or read from I/O pins DQ0–DQ31. When $\overline{\text{WORD}}$ is at a logic-low level, the device is in the word-wide (x16) mode and data is written to or read from I/O pins DQ0–DQ7 and DQ24–DQ31. In the word-wide mode, I/O pins DQ8–DQ23 are placed in the high-impedance state and A_{-1} becomes the low-order address pin that selects either the upper or lower half of the array. Array data from the upper half (DQ0–DQ7, DQ24–DQ31) and the lower half (DQ8–DQ23) are multiplexed in order to appear on DQ0–DQ7 and DQ24–DQ31. The operation modes for word-wide and double-word-wide configurations are summarized in Table 13 and Table 14, respectively.

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operation modes for word-wide (x16) or double-word-wide (x32) mode selection (continued)

Table 13. Operation Modes for Word-Wide Mode (x16) (See Note 2 and Note 14)

MODE	CLK	A (Addr Bus)	$\overline{E}$	$\overline{WR}$	$\overline{WE}$	$\overline{LBA}$	$\overline{BAA}$	$\overline{OE}$	DQ (Data Bus) (see Note 14)	$\overline{QV}$	RY/$\overline{BY}$	V_{PP}	$\overline{RP}$
READ OPERATION MODES													
Latch non-pipelined read address	L–H	Address	V_{IL}	V_{IH}	X	V_{IL}	X	V_{IH}	Hi-Z	Hi-Z	Hi-Z	X	V_{IH}
Latch pipelined read address	L–H	Address	V_{IL}	V_{IH}	X	V_{IL}	X	V_{IH}	Data out	V_{OL}	Hi-Z	X	V_{IH}
Latch pipelined read address with early overlap	L–H	Address	V_{IL}	V_{IH}	X	V_{IL}	X	V_{IL}	Hi-Z	Hi-Z	Hi-Z	X	V_{IH}
Wait (prior to first data read)	L–H	X	V_{IL}	X	X	V_{IH}	X	V_{IH}	Hi-Z	Hi-Z	Hi-Z	X	V_{IH}
Latch read data	L–H	X	V_{IL}	X	X	V_{IH}	X	V_{IL}	Hi-Z	Hi-Z	Hi-Z	X	V_{IH}
Drive read data	L–H	X	V_{IL}	X	X	V_{IH}	X	X	Data out	V_{OL}	Hi-Z	X	V_{IH}
Burst read	L–H	X	V_{IL}	X	X	V_{IH}	V_{IL}	V_{IL}	Data out	V_{OL}	Hi-Z	X	V_{IH}
Burst terminate	L–H	X	V_{IL}	X	X	V_{IH}	V_{IH}	V_{IH}	Data out	V_{OL}	Hi-Z	X	V_{IH}
Burst suspend (see Note 15)	L–H	X	V_{IL}	X	X	V_{IH}	V_{IH}	X	Data out	V_{OL}	Hi-Z	X	V_{IH}
Update status during algorithm	L–H	X	V_{IL}	X	X	X	X	V_{IL}	X	X	X	X	V_{IH}
Read status during algorithm	L–H	X	V_{IL}	X	X	X	X	X	Status out	V_{OL}	X	X	V_{IH}
Read overlay	L–H	X	V_{IL}	X	X	X	X	V_{IL}	Overlay data out	V_{OL}	Hi-Z	V_{PPH}	V_{IH}
SYNCHRONOUS WRITE OPERATION MODES													
Latch write address	L–H	Address	V_{IL}	V_{IL}	X	V_{IL}	X	V_{IH}	X	X	Hi–Z	X	V_{IH}
Latch write address/data	L–H	Address	V_{IL}	V_{IL}	V_{IL}	V_{IL}	X	V_{IH}	Data in	Hi-Z	Hi-Z	X	V_{IH}
Latch write data	L–H	X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	V_{IH}	Data in	Hi-Z	Hi-Z	X	V_{IH}
ASYNCHRONOUS WRITE OPERATION MODES													
Latch write address/data	X	Address	V_{IL}	X	L–H	X	X	V_{IH}	Data in	Hi-Z	Hi-Z	X	V_{IH}
OTHER OPERATION MODES													
Standby	X	X	V_{IH}	X	X	X	X	X	Hi-Z	Hi-Z	X	X	V_{IH}
Reset/deep power down	X	X	X	X	X	X	X	X	Hi-Z	Hi-Z	V_{OH}	X	V_{IL}

NOTES: 13. X is a don't care.
14. For x16 mode ($\overline{WORD}$ = V_{IL} when DCR3 = 1), the data lines are DQ0–DQ7 and DQ24–DQ31.
15. This mode freezes the burst counter and holds the current data line values.

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operation modes for word-wide (x16) or double-word-wide (x32) mode selection (continued)

Table 14. Operation Modes for Double-Word-Wide Mode (x32) (See Note 13 and Note 16)

MODE	CLK	A (Addr Bus)	$\overline{E}$	$\overline{WR}$	$\overline{WE}$	$\overline{LBA}$	$\overline{BAA}$	$\overline{OE}$	DQ (Data Bus) (see Note 16)	$\overline{QV}$	RY/$\overline{BY}$	V_{PP}	$\overline{RP}$
READ OPERATION MODES													
Latch non-pipelined read address	L–H	Address	V_{IL}	V_{IH}	X	V_{IL}	X	V_{IH}	Hi-Z	Hi-Z	Hi-Z	X	V_{IH}
Latch pipelined read address	L–H	Address	V_{IL}	V_{IH}	X	V_{IL}	X	V_{IH}	Data out	VOL	Hi-Z	X	V_{IH}
Latch pipelined read address with early overlap	L–H	Address	V_{IL}	V_{IH}	X	V_{IL}	X	V_{IL}	Hi-Z	Hi-Z	Hi-Z	X	V_{IH}
Wait (prior to first data read)	L–H	X	V_{IL}	X	X	V_{IH}	X	V_{IH}	Hi-Z	Hi-Z	Hi-Z	X	V_{IH}
Latch read data	L–H	X	V_{IL}	X	X	V_{IH}	X	V_{IL}	Hi-Z	Hi-Z	Hi-Z	X	V_{IH}
Drive read data	L–H	X	V_{IL}	X	X	V_{IH}	X	X	Data out	VOL	Hi-Z	X	V_{IH}
Burst read	L–H	X	V_{IL}	X	X	V_{IH}	V_{IL}	V_{IL}	Data out	VOL	Hi-Z	X	V_{IH}
Burst terminate	L–H	X	V_{IL}	X	X	V_{IH}	V_{IH}	V_{IH}	Data out	VOL	Hi-Z	X	V_{IH}
Burst suspend (see Note 15)	L–H	X	V_{IL}	X	X	V_{IH}	V_{IH}	X	Data out	VOL	Hi-Z	X	V_{IH}
Update status during algorithm	L–H	X	V_{IL}	X	X	X	X	V_{IL}	X	X	X	X	V_{IH}
Read status during algorithm	L–H	X	V_{IL}	X	X	X	X	X	Status out	VOL	X	X	V_{IH}
Read overlay	L–H	X	V_{IL}	X	X	X	X	V_{IL}	Overlay data out	VOL	Hi-Z	V_{PPH}	V_{IH}
SYNCHRONOUS WRITE OPERATION MODES													
Latch write address	L–H	Address	V_{IL}	V_{IL}	X	V_{IL}	X	V_{IH}	X	X	Hi-Z	X	V_{IH}
Latch write address/data	L–H	Address	V_{IL}	V_{IL}	V_{IL}	V_{IL}	X	V_{IH}	Data in	Hi-Z	Hi-Z	X	V_{IH}
Latch write data	L–H	X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	V_{IH}	Data in	Hi-Z	Hi-Z	X	V_{IH}
ASYNCHRONOUS WRITE OPERATION MODES													
Latch write address/data	X	Address	V_{IL}	X	L–H	X	X	V_{IH}	Data in	Hi-Z	Hi-Z	X	V_{IH}
OTHER OPERATION MODES													
Standby	X	X	V_{IH}	X	X	X	X	X	Hi-Z	Hi-Z	X	X	V_{IH}
Reset/deep power down	X	X	X	X	X	X	X	X	Hi-Z	Hi-Z	VOH	X	V_{IL}

NOTES: 13. X is a don't care.
15. This mode freezes the burst counter and holds the current data line values.
16. For x32 mode ($\overline{WORD}=V_{IH}$ when DCR3=1, or DCR3=0) the data lines are DQ0 – DQ31.

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clear status register

For DCR4 = 0 ($\overline{\text{LRV}}$ usage), the WSM can set the V_{PP} status bit (SB3), the low-regulator-voltage status bit (SB4), and the operation status bit (SB5). For DCR4 = 1, the WSM can set the V_{PP} status bit (SB3), the program status bit (SB4), and the erase status bit (SB5) of the status register. The clear-status-register command (50h) allows the external microprocessor to clear SB3, SB4, and SB5. When the status bits are cleared, the device returns to the read-array mode.

load device configuration register

The load DCR command is a two-bus-cycle command that loads the device configuration register. When the DCR load command (96h) is written to the CSM, the CSM will set up the device configuration register to be loaded on the next write cycle. On the second cycle, the configuration data DDDDh loads the two bytes of the device configuration register DCR0–DCR7 and DCR24–DCR31 (see Table 5 and Table 6). DCR8–DCR23 and DCR26–DCR27 are reserved and should be loaded with 0s.

read operations

There are three read operations available: read array, read algorithm-selection code, and read status register. See Table 13 and Table 14 for the required control signals needed with synchronous reads.

- Read array

  The read-array command consists of two bus cycles, and is listed in Table 5. For synchronous reads on the first bus cycle, the CSM command code FFh on DQ0–DQ7 and the address 00000h are entered.

  The second bus cycle begins with the address phase where, for synchronous operation, $\overline{\text{LBA}}$ goes low on a rising clock edge. On the same clock (CLK 1 of Figure 14 for burst reads, or CLK 1 of Figure 27 for single reads), the address is latched and $\overline{\text{WR}}$ is sampled. For a read, $\overline{\text{WR}}$ is set high, and the device is ready for the read-data phase. The data phase follows the address phase by one or more clock cycles, where $\overline{\text{OE}}$ goes low on a rising clock edge and the data is driven onto the bus DQ0–DQ31 for x32, and DQ0–DQ7 with DQ24–DQ31 for x16. For single reads, the data is valid for CLK 3 (see Figure 27). For burst reads, on CLK 3 of Figure 14, $\overline{\text{BAA}}$ is brought low to burst the second data segment. $\overline{\text{OE}}$ is kept low for four clock cycles (CLKs 2–5) and $\overline{\text{BAA}}$ is kept low for three CLKs (CLKs 3–5), which bursts four words for MOD4. Burst reads for burst lengths MOD8, MOD16, or MOD32 are accomplished by holding $\overline{\text{OE}}$ and $\overline{\text{BAA}}$ low for each data segment in the same way (see Figure 14 through Figure 21). The optional output valid ($\overline{\text{QV}}$) goes low when valid data is output from the device (see the Terminal Functions table, Figure 14 through Figure 21, and Figure 27).

- Read algorithm-selection code

  As listed in Table 5, CSM command code 90h is written on DQ0–DQ7. Two bus cycles are required for this operation: the first to enter the command code and a second to read the manufacturer/device code or DCR value by loading the required A1A0 address bits (see Table 5 and Table 6). By loading a new address, the manufacturer-equivalent code is obtained on DQ0–DQ7 with both A1 and A0 at a logic-level V_{IL}. Similarly, the device-equivalent code is obtained when A1 is set to V_{IL} and A0 is set to V_{IH}. The device configuration register value is obtained when A1 is set to V_{IH} and A0 is set to V_{IL}.

- Read status register

  The status register is read by entering the command code 70h on DQ0–DQ7. Two bus cycles are required for this operation: one to enter the command code and a second to read the status register (see Table 5). The status register contents are updated on every clock cycle.

The device interface is synchronous but supports asynchronous read timings, which hold the address valid and $\overline{\text{LBA}}$ low throughout the address and data phases as required by some microprocessors after power-up (see Figure 13).

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programming operations

There are two program operations available: program-setup/program to main array and program-setup/program to overlay block. Both are available with synchronous or asynchronous writes.

Both the x16 and x32 data bus configurations have a two-bus-cycle write capability, where in two bus cycles, either one 16-bit word or one 32-bit word is programmed, respectively. In addition, three-cycle writes are available with the 16-bit data bus by configuring DCR31(see Table 8). On the first cycle, which is the command cycle, the CSM command code 40h or 04h is loaded to set up the device for programming either to the main array or to the overlay block array, respectively. On the second cycle, which is the write-data cycle, the data is loaded. After the desired command code and data are loaded, the WSM takes over and correctly sequences the device to complete the program operation. During this time, the CSM responds only to status reads until the program operation has been completed, after which all commands to the CSM become valid again. Once a program command has been issued, the WSM cannot normally be interrupted until the program algorithm is completed. Monitoring of the write operation is possible through the status register or the ready/busy (RY/$\overline{BY}$) pin (see Figure 22 and Figure 24). See Figure 22 and Figure 24 for two- and three-cycle synchronous writes respectively. For asynchronous writes, the address and command/data are latched on the rising edge of $\overline{WE}$ (see Figure 23 for asynchronous write).

Taking $\overline{RP}$ to V_{IL} during programming aborts the program operation. During programming, V_{PP} must remain $V_{PP} \geq V_{PPH}$ (see Figure 22 and Figure 23). Only 0s are written and compared during a program operation. If 1s are programmed, the memory cell contents do not change and no error occurs.

A program-setup command can be aborted by writing FFFFh on DQ0–D7 and DQ24–DQ31 (in word-wide mode), or FFFFFFFFh (in double-word-wide mode) during the second cycle. After writing all 1s during the second cycle, the CSM responds only to status reads. When the WSM status bit (SB7) is set to a logic-high level, signifying the nonprogram operation is terminated, all commands to the CSM become valid again.

erase operations

There are two erase operations that can be performed: block-erase-setup/confirm main array (20h/D0h) and block-erase-setup/confirm overlay block (02h/0Dh). An erase operation must be used to initialize all bits in an array block to 1s. After block-erase confirm is issued, the CSM responds only to status reads until the WSM completes its task. Both of these erase operations are available with synchronous and asynchronous writes.

Block erasure inside the memory array sets all bits within the addressed block to logic 1s. Erasure is accomplished only by blocks; data at single address locations within the array cannot be individually erased. The block to be erased is selected by using any valid address within that block. Block erasure is initiated by a command sequence to the CSM: block-erase setup (20h/02h) followed by block-erase confirm (D0h/0Dh) (see Figure 25 and Figure 26). This two-command erase sequence protects against accidental erasure of memory contents.

Asynchronous erase-setup and confirm commands are latched on the rising edge of $\overline{WE}$, and block addresses are latched during the block-erase-confirm command on the rising edge of $\overline{WE}$. For both synchronous and asynchronous operations, when the block-erase-confirm command is complete, the WSM automatically executes a sequence of events to complete the block erasure. During this sequence, the block is programmed with logic 0s, data is verified, all bits in the block are erased, and verification is performed to ensure that all bits are correctly erased. Monitoring of the erase operation is possible through the status register or the ready/busy (RY/$\overline{BY}$) pin (see Figure 25 and Figure 26).

Taking $\overline{RP}$ to V_{IL} during erasing aborts the erase operation. During erasing, V_{PP} must remain $V_{PP}>=V_{PPH}$ as seen in Figure 25 and Figure 26.

reduced power mode

The command F0h, when written to the CSM, puts TMS28F033 in reduced-power mode (not to be confused with $\overline{RP}$). This mode is used when the chip-enable, $\overline{E}$, input is not used and reduced power consumption is needed. However, the device does not have its outputs disabled; instead, it can respond to any CSM command at any time and then its power comes back up. When in reduced power mode, the outputs are still $\overline{OE}$-controlled.

$\overline{RP}$ input (reset/deep power-down mode)

When $\overline{RP}$ is high, the memory functions normally. When $\overline{RP}$ goes low, any CSM activity is terminated immediately. While $\overline{RP}$ is low, the memory does not respond to read requests and does not accept write commands. When $\overline{RP}$ goes high, the memory is reinitialized and prepared for normal operation (read mode), and sets/clears OBEB based on V_{PP} (see Table 3).

low-power-program mode

Low-power-program mode is activated by entering the command code 60h. The low-power-programming mode enable/disable is a single-cycle command that toggles the state of the LPM bit in the status register. Depending on the LPM status register bit (see Table 7), the WSM programs by bytes (low-power mode) or by words (normal mode) (see Table 5 for CSM command).

low regulator voltage ($\overline{LRV}$)

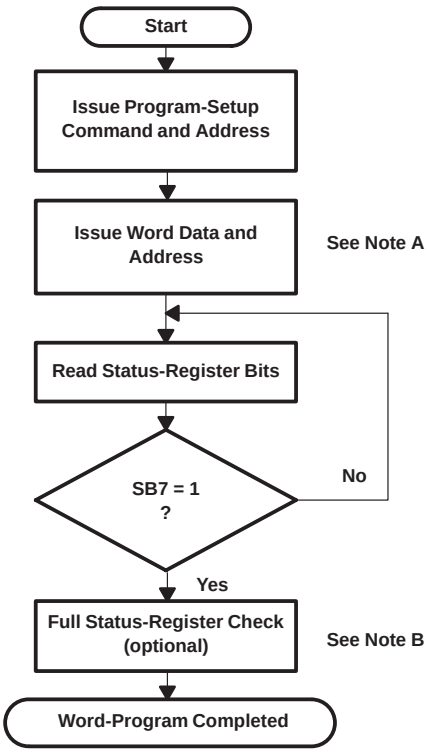
$\overline{LRV}$ is selected for use by setting DCR4 = 0. This signal can be generated by an external power supply monitor and should go low when V_{PP} is out of regulation ($V_{PP} \leq V_{PPH}$). The WSM periodically samples the $\overline{LRV}$ input during erasing and programming. When $\overline{LRV}$ goes low, the status register SB4 is set, providing a more accurate monitor of V_{PP} than the V_{PP} status bit (SB3).

pipelining

This device supports efficient bus usage by latching the address on the first clock cycle of a read operation, and then delaying the data phase (delay bringing $\overline{OE}$ low), thereby allowing the address and data buses to be used by other parts of the system.

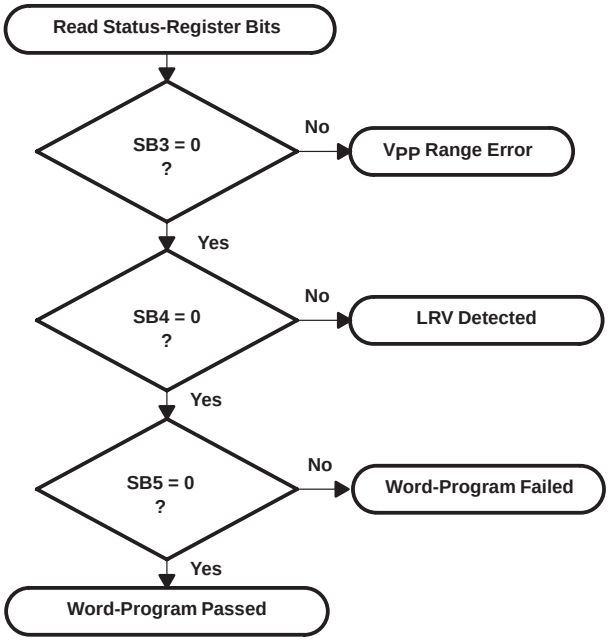
overlapping data and address phases

The address and data phases of consecutive synchronous read or write operations can be overlapped by one or more clock cycles. This is done by bringing $\overline{LBA}$ low to latch a new address before the completion of the data phase of the current cycle. For overlapping synchronous single reads, and overlapping synchronous single reads with writes, see Figure 27. For overlapping burst reads, see Note C in Figure 14 and Figure 15. For overlapping synchronous write cycles, see Figure 24.



BUS OPERATION	COMMAND	COMMENTS
Write	Write program setup	Data = 40h for main array or 04h for overlay block Addr = 00000h for synchronous $\overline{WE}$ or XXXXXh for asynchronous $\overline{WE}$
Write	Write	Data = Word to be programmed Addr = Address of word to be programmed
Read		Status-register data. Status register is updated on each rising clock.
Wait		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent words. Write read-array command after the last word-program operation to reset the device to read-array mode.		

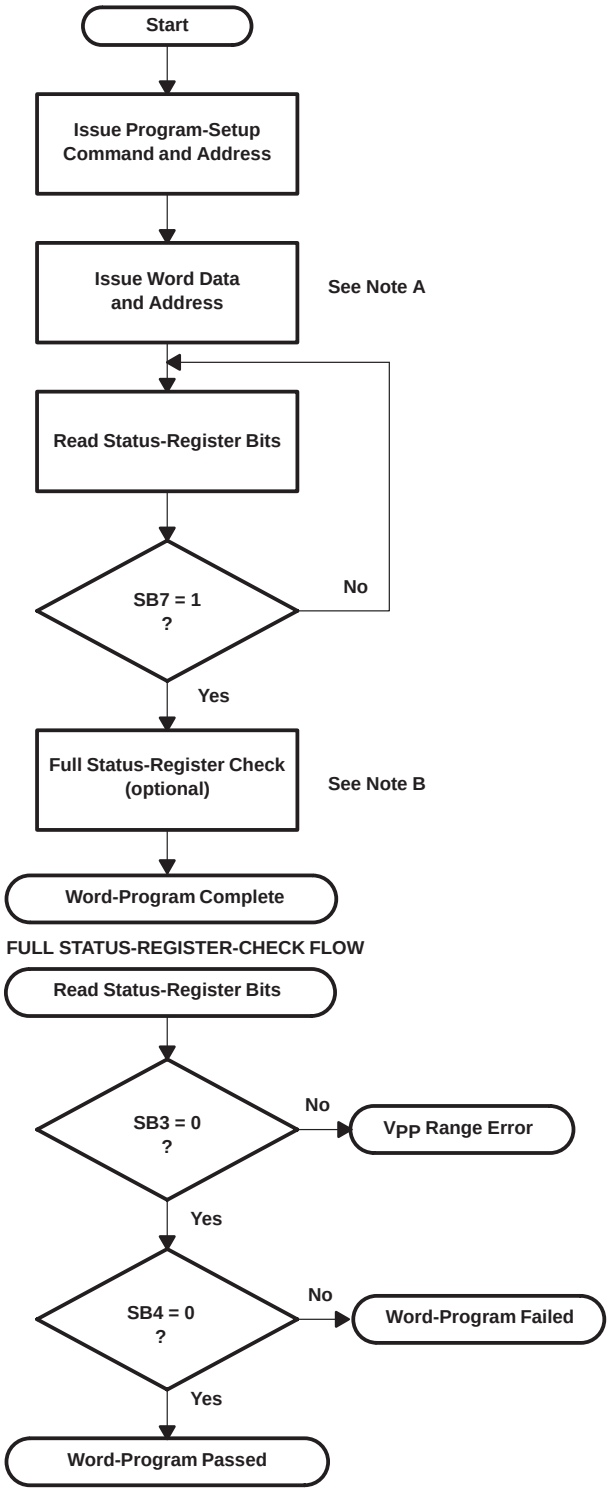
FULL STATUS-REGISTER-CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
Wait		Check SB3 1 = Detect V_{PP} low (see Note C)
Wait		Check SB4 1 = Detect $\overline{LRV}$ low (see Note D)
Wait		Check SB5 1 = Word-program error (see Note D)

NOTES: A. In this flowchart, the use of “word” refers to both 16-bit and 32-bit data-bus widths.
B. Full status-register check can be done after each word or after a sequence of words.
C. SB3 must be cleared before attempting additional program/erase operations.
D. SB4 and SB5 are cleared only by the clear-status-register command, but this does not prevent additional program operation attempts.

Figure 4. Automated Programming Flowchart (DCR4 = 0)



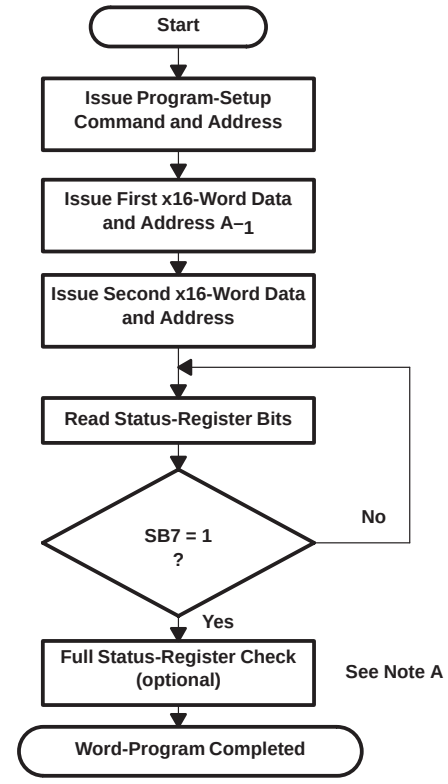
BUS OPERATION	COMMAND	COMMENTS
Write	Write program setup	Data = 40h for main array or 04h for overlay block Addr = 00000h for synchronous $\overline{WE}$ or XXXXXh for asynchronous $\overline{WE}$
Write	Write	Data = Word to be programmed Addr = Address of word to be programmed
Read		Status-register data. Status register is updated on each rising clock.
Wait		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent words. Write read-array command after the last word-program operation to reset the device to read-array mode.		

BUS OPERATION	COMMAND	COMMENTS
Wait		Check SB3 1 = Detect V_{PP} low (see Note C)
Wait		Check SB4 1 = Word-program error (see Note D)

NOTES: A. In this flowchart, the use of “word” refers to both 16-bit and 32-bit data-bus widths.
B. Full status-register check can be done after each word or after a sequence of words.
C. SB3 must be cleared before attempting additional program/erase operations.
D. SB4 is cleared only by the clear-status-register command, but this does not prevent additional program operation attempts.

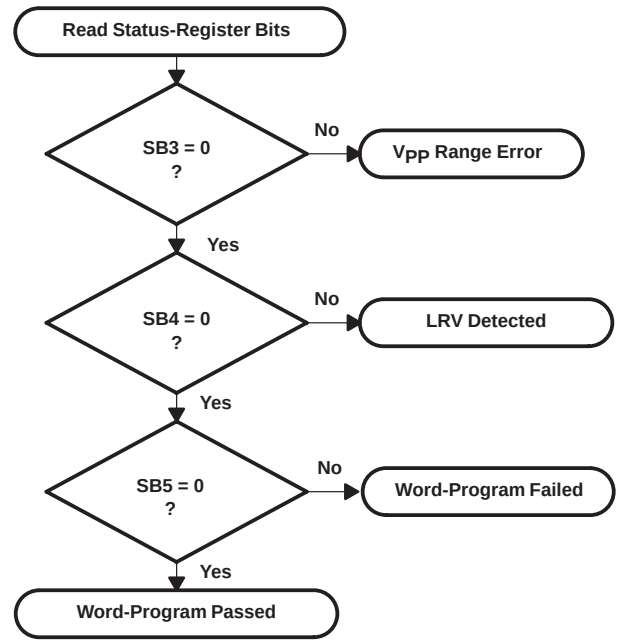
Figure 5. Automated Programming Flowchart (DCR4 = 1)

ADVANCE INFORMATION



FULL STATUS-REGISTER-CHECK FLOW

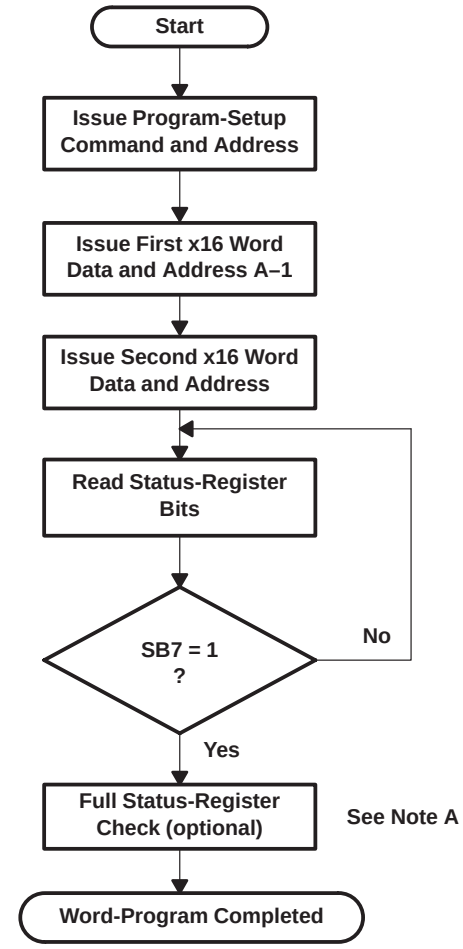
BUS OPERATION	COMMAND	COMMENTS
Write	Write program setup	Data = 40h for main array or 04h for overlay block Addr = 00000h for synchronous $\overline{WE}$ or XXXXXh for asynchronous $\overline{WE}$
Write	Write	Data = First x16 word to be programmed Addr = A_{-1} (see Table 3)
Write	Write	Data = Second x16 word to be programmed Addr = Address of x16 word to be programmed
Read		Status-register data. Status register is updated on each rising clock.
Wait		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent words. Write read-array command after the last word-program operation to reset the device to read-array mode.		



BUS OPERATION	COMMAND	COMMENTS
Wait		Check SB3 1 = Detect V_{PP} low (see Note B)
Wait		Check SB4 1 = Detect $\overline{LRV}$ low (see Note C)
Wait		Check SB5 1 = Word-program error (see Note C)

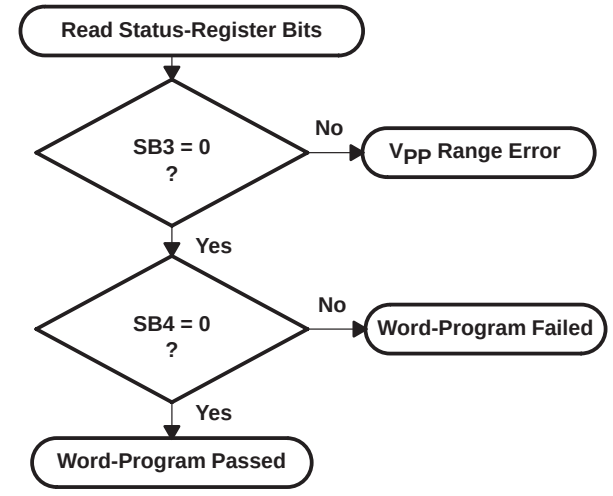
NOTES: A. Full status-register check can be done after each word or after a sequence of words.
B. SB3 must be cleared before attempting additional program/erase operations.
C. SB4 and SB5 are cleared only by the clear-status-register command, but this does not prevent additional program operation attempts.

Figure 6. Automated x16 Word-Programming Flowchart With Three-Cycle Write (DCR4 = 0)



BUS OPERATION	COMMAND	COMMENTS
Write	Write program setup	Data = 40h for main array or 04h for overlay block Addr = 00000h for synchronous $\overline{WE}$ or XXXXXh for asynchronous $\overline{WE}$
Write	Write	Data = First x16 word to be programmed Addr = A_{-1} (see Table 3)
Write	Write	Data = Second x16 word to be programmed Addr = Address of x16 word to be programmed
Read		Status-register data. Status register is updated on each rising clock.
Wait		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent words. Write read-array command after the last word-program operation to reset the device to read-array mode.		

FULL STATUS-REGISTER-CHECK FLOW

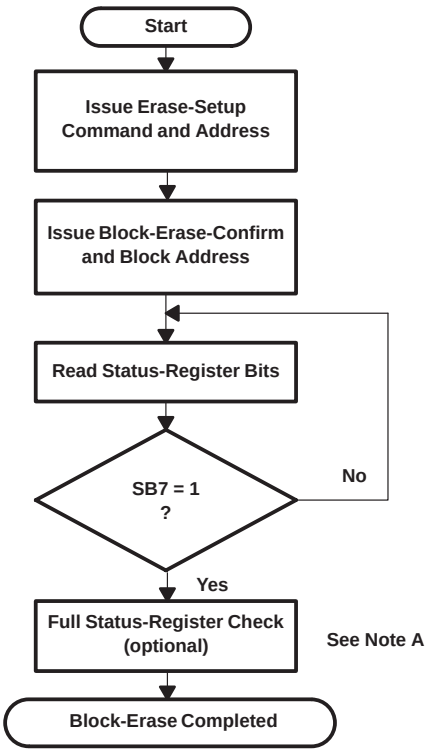


BUS OPERATION	COMMAND	COMMENTS
Wait		Check SB3 1 = Detect V_{PP} low (see Note B)
Wait		Check SB4 1 = Word-program error (see Note C)

NOTES: A. Full status-register check can be done after each word or after a sequence of words.
B. SB3 must be cleared before attempting additional program/erase operations.
C. SB4 is cleared only by the clear-status-register command, but this does not prevent additional program operation attempts.

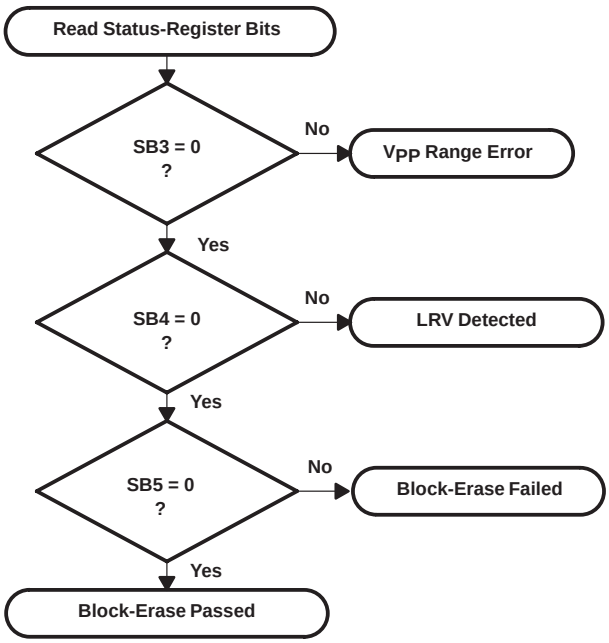
Figure 7. Automated x16 Word-Programming Flowchart With Three-Cycle Write (DCR4 = 1)

ADVANCE INFORMATION



BUS OPERATION	COMMAND	COMMENTS
Write	Write erase setup	Data = 20h for main array or 02h for overlay block Addr = 00000h for synchronous $\overline{WE}$ or XXXXXh for asynchronous $\overline{WE}$
Write	Erase	Data = D0h for main array or 0Dh for overlay block Block Addr = Address within block to be erased
Read		Status-register data. Status register is updated on each rising clock.
Wait		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent words. Write read-array command after the last word-program operation to reset the device to read-array mode.		

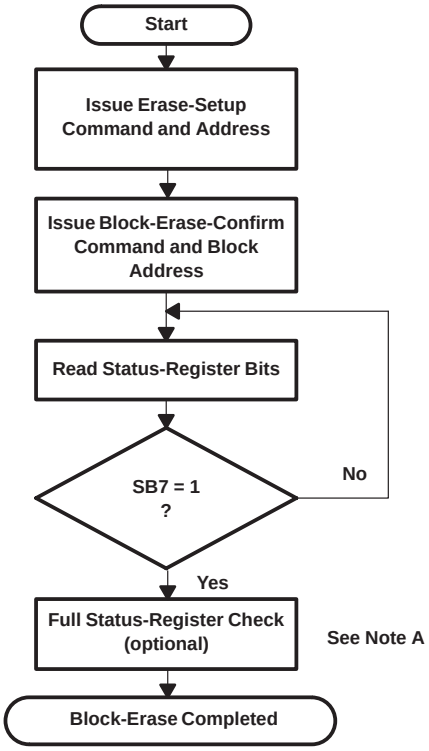
FULL STATUS-REGISTER-CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
Wait		Check SB3 1 = Detect V_{PP} low (see Note B)
Wait		Check SB4 1 = Detect $\overline{LRV}$ low (see Note C)
Wait		Check SB5 1 = Block-erase error (see Note C)

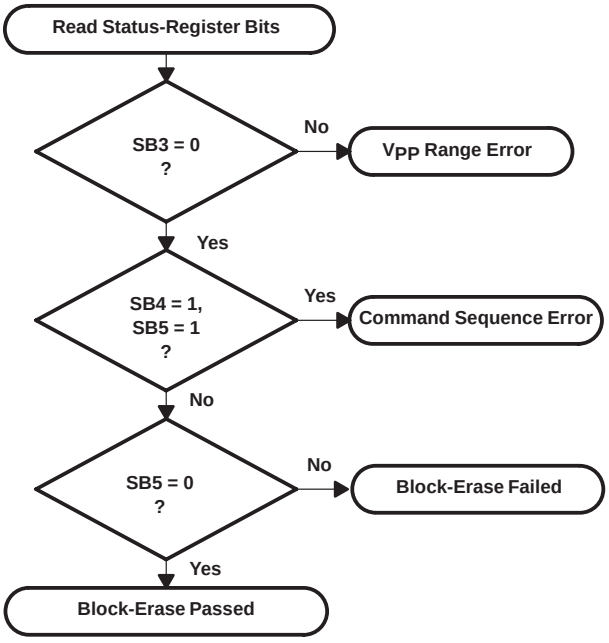
NOTES: A. Full status-register check can be done after each block or after a sequence of blocks.
B. SB3 must be cleared before attempting additional program/erase operations.
C. SB4 and SB5 are cleared only by the clear-status-register command, but this does not prevent additional erase operation attempts.

Figure 8. Automated Block-Erase Flowchart (DCR4 = 0)



BUS OPERATION	COMMAND	COMMENTS
Write	Write erase setup	Data = 20h for main array or 02h for overlay block Addr = 00000h for synchronous $\overline{WE}$ or XXXXXh for asynchronous $\overline{WE}$
Write	Erase	Data = D0h for main array or 0Dh for overlay block Block Addr = Address within block to be erased
Read		Status-register data. Status register is updated on each rising clock.
Wait		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent words. Write read-array command after the last word-program operation to reset the device to read-array mode.		

FULL STATUS-REGISTER-CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
Wait		Check SB3 1 = Detect V_{PP} low (see Note B)
Wait		Check SB4 and SB5 1 = Block-erase command error
Wait		Check SB5 1 = Block-erase error (see Note C)

NOTES: A. Full status-register check can be done after each block or after a sequence of blocks.
B. SB3 must be cleared before attempting additional program/erase operations.
C. SB5 is cleared only by the clear-status-register command, but this does not prevent additional erase operation attempts.

Figure 9. Automated Block-Erase Flowchart (DCR4 = 1)

ADVANCE INFORMATION

absolute maximum ratings over ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{DDI} (5 V) (see Note 17) . . . . . –0.5 V to 7 V
Supply voltage range, V_{DDE} (3.3 V) (see Note 17) . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (except V_{PP}) . . . . . –0.5 V to V_{DDE} + 0.5 V
Input voltage range, V_I (V_{PP}) . . . . . –0.5 V to 14 V
Biased junction Temperature, T_J . . . . . 150°C
Ambient temperature, T_A . . . . .
(L) . . . . . 0 V to 70°C
(E) . . . . . –40 V to 85°C
(Q) . . . . . –40 V to 125°C
Storage temperature range, T_{stg} . . . . . –55°C to 150°C
Soldering temperature, T_{SO} (IR reflow for 180 seconds) . . . . . 225°C
Soldering temperature (maximum ramp rate) . . . . . 6°C/s
Thermal resistance, Q_{JA} (junction-to-ambient) . . . . . 50°C/W
Data retention (at 55°C ambient) . . . . . 20 Years (minimum)
Number of erase/write cycles . . . . . 10000 Cycles

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 17: All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DDI}	Supply voltage		4.5	5	5.5	V
V_{DDE}	Output buffer supply voltage	$3/5\overline{IO} = V_{IH}$	3.0	3.3	3.6	V
		$3/5\overline{IO} = V_{IL}$	4.5	5.0	5.5	
V_{IL}	Input low voltage		–0.3		0.8	V
V_{IH}	Input high voltage		2.0		V_{DDE} + 0.3	V
V_{PP}	Programming supply voltage		11.4	12	12.6	V
V_{PPL}	Programming voltage low				7	V
V_{PPH}	Programming voltage high		11.4			V
T_A	Ambient temperature during read/erase/program	L Suffix	0		70	°C
		E Suffix	–40		85	°C
		Q Suffix	–40		125	°C

double-word/word typical write and block-erase duration (see Notes 18 and 19)

BLOCK SIZE	ERASE OPERATION		WRITE OPERATION						UNIT
	ERASE	LPP MODE	PROGRAMMING			LOW-POWER PROGRAMMING MODE			
x32 / x16	x16 or x32	x16 or x32	x32	x16		x32	x16		
				2-CYCLE	3-CYCLE		2-CYCLE	3-CYCLE	
6K/12K	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	s
16K/32K	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	s
32K/64K	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	s
48K/96K	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	s
80K/160K	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	s

NOTES: 18. Excludes system-level overhead
19. Typical values shown are at T_A = 25°C

electrical characteristics over recommended ranges of supply voltage and ambient temperature, V_{DDE} = 3.3 V (see Notes 20 through 23)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OL}†	Output low voltage	V_{DDI}/V_{DDE} = MIN, I_{OL} = 100 µA		0.2	V
V_{OH}†	Output high voltage	V_{DDI}/V_{DDE} = MIN, I_{OH} = –100 µA	V_{DDE}–0.2		V
I_{DDI_pwdn}	I_{DDI} power-down current	V_{DDI}/V_{DDE} = MAX, $\overline{RP}$= V_{IL}		TBD	µA
I_{LI}	Input leakage	V_{IN} = GND to V_{DDE} MAX, V_{DDI} = V_{DDI} MAX		± 5	µA
I_{LO}	Output leakage	V_O = GND to V_{DDE} MAX, $\overline{DIS}$ = V_{IL} , V_{DDI} = V_{DDI} MAX		± 10	µA
I_{PU}	Internal pullup current ($\overline{DIS}$, $\overline{RP}$, $\overline{LRV}$ pins)	(V_{DDI}/V_{DDE} = MIN, V_{PIN} = 2.0 V) or (V_{DDI}/V_{DDE} = MAX, V_{PIN} = 0 V)	20	600	µA
I_{DDI}	Supply current, internal	V_{DDI}/V_{DDE} = MAX, $\overline{OE}$ = V_{IL}, at 25 MHz		100	mA
I_{DDE}	Supply current, external	V_{DDI}/V_{DDE} = MAX, $\overline{OE}$ = V_{IL}, at 25 MHz, MOD4, x32		65	mA
I_{PPS}	Supply current, for slow programming (low-power programming mode)	$V_{DDI}/V_{PP}/V_{DDE}$ = MAX		50	mA
I_{ERSS}	Supply current, for slow erasing (low-power programming mode)	$V_{DDI}/V_{PP}/V_{DDE}$ = MAX		50	mA
I_{PPF}	Supply current, for fast programming	$V_{DDI}/V_{PP}/V_{DDE}$ = MAX		120	mA
I_{ERSF}	Supply current, for fast erasing	$V_{DDI}/V_{PP}/V_{DDE}$ = MAX		120	mA

† Dependent on JEDEC standard 8–1A.

NOTES: 20. Test results of erasing and programming with $V_{PPL} < V_{PP} < V_{PPH}$ are undefined.
21. Positive current flow is into the device.
22. Test supply voltage range: (4.5-V dc ≤ V_{DDI} ≤ 5.5-V dc) and (3-V dc ≤ V_{DDE} ≤ 3.6-V dc).
23. Device in read mode with $\overline{OE}$ enabled.

ADVANCE INFORMATION

electrical characteristics over recommended ranges of supply voltage and ambient temperature, V_{DDE} = 5 V (see Notes 20, 21, 23, and 24)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OL}†	Output low voltage	V_{DDI}/V_{DDE} = MIN, I_{OL} = TBD		0.2	V
V_{OH}†	Output high voltage	V_{DDI}/V_{DDE} = MIN, I_{OH} = TBD	V_{DDE} – 0.2		V
I_{DDI_pwdn}	I_{DDI} power-down current	V_{DDI}/V_{DDE} = MAX, $\overline{RP}$= V_{IL}		TBD	μA
I_{LI}	Input leakage	V_{IN} = GND to V_{DDE} MAX, V_{DDI} = V_{DDI} MAX		± 5	μA
I_{LO}	Output leakage	$\overline{V_O}$ = GND to V_{DDE} MAX, $\overline{DIS}$ = V_{IL} , V_{DDI} = V_{DDI} MAX		± 10	μA
I_{PU}	Internal pullup current ($\overline{DIS}$, $\overline{RP}$, $\overline{LRV}$ pins)	(V_{DDI}/V_{DDE} = MIN, V_{PIN} = 2.0 V) or (V_{DDI}/V_{DDE} = MAX, V_{PIN} = 0 V)	TBD	TBD	μA
I_{DDI}	Supply current, internal	V_{DDI}/V_{DDE} = MAX, $\overline{OE}$ = V_{IL}, at 25 MHz		100	mA
I_{DDE}	Supply current, external	V_{DDI}/V_{DDE} = MAX, $\overline{OE}$ = V_{IL}, at 25 MHz, MOD4, x32		TBD	mA
I_{PPS}	Supply current, for slow programming (low-power programming mode)	$V_{DDI}/V_{PP}/V_{DDE}$ = MAX		50	mA
I_{ERSS}	Supply current, for slow erasing (low-power programming mode)	$V_{DDI}/V_{PP}/V_{DDE}$ = MAX		50	mA
I_{PPF}	Supply current, for fast programming	$V_{DDI}/V_{PP}/V_{DDE}$ = MAX		120	mA
I_{ERSF}	Supply current, for fast erasing	$V_{DDI}/V_{PP}/V_{DDE}$ = MAX		120	mA

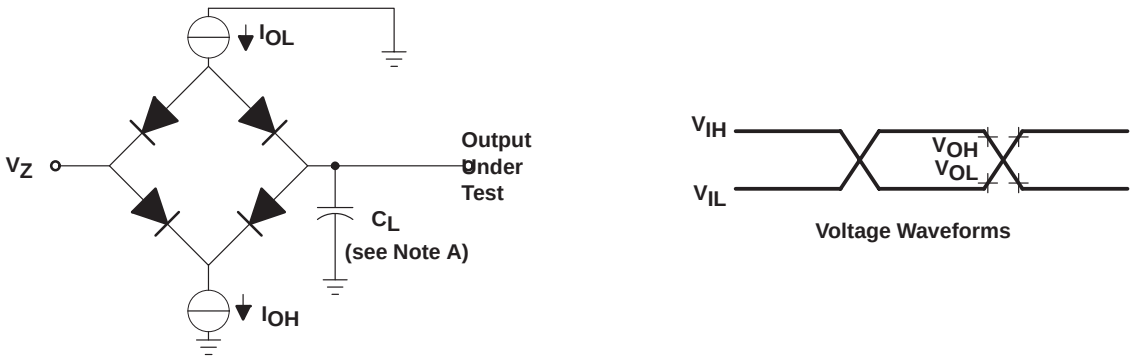
† Dependent on JEDEC standard 8–1A.

NOTES: 20. Test results of erasing and programming with $V_{PPL} < V_{PP} < V_{PPH}$ are undefined.
21. Positive current flow is into the device.
23. Device in read mode with $\overline{OE}$ enabled.
24. Test supply voltage range: (4.5-V dc ≤ V_{DDI} ≤ 5.5-V dc) and (4.5-V dc ≤ V_{DDE} ≤ 5.5-V dc).

capacitance over recommended ranges of supply voltage and ambient temperature, f = 1 MHz, V_I = 0 V

PARAMETER		TEST CONDITION	MIN	MAX	UNIT
C_i	Input capacitance			8	pF
C_o	Output capacitance	V_O = 0 V		12	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and fixture capacitance.
B. AC test conditions are driven at V_{IH} and V_{IL}. Timing measurements are made at V_{OH} and V_{OL} levels on both inputs and outputs. Refer to Table 16 for values based on V_{DDE} operating range.

Figure 10. Load Circuit and Voltage Waveforms

Table 15. AC Test Conditions

V_{DDE} RANGE	I_{OL} (mA)	I_{OH} (mA)	V_Z† (V)	V_{OL} (V)	V_{OH} (V)	V_{IL} (V)	V_{IH} (V)	C_L (pF)	t_f (ns)	t_r (ns)
5 V ± 10%	1.0	–1.0	1.4	0.8	2.0	0.45	2.4	70	< 5	< 5
3.3 V ± 0.3V	1.0	–1.0	1.4	0.8	2.0	0.45	2.4	70	< 5	< 5

† V_Z is the measured value used to detect the high-impedance state.

Table 16. Timing Nomenclature

SYMBOL	PIN CHARACTERS	SYMBOL	PIN CONDITION
A	Address Inputs	H	High
C	Clock (CLK)	L	Low
D	Data Inputs	X	Not valid
Q	Data Outputs	Z	High impedance
E	$\overline{E}$ (Chip Enable)	V	Valid
G	$\overline{OE}$ (Output Enable)	D	Driven
W	$\overline{WE}$ (Write Enable)		
P	$\overline{RP}$ (Reset/Power-Down)		
Y	RY/$\overline{BY}$ (Ready/Busy)		
L	$\overline{LBA}$ (Load Burst Address)		
B	$\overline{BAA}$ (Burst Address Advance)		
S	$\overline{DIS}$ (Disable Output)		
R	$\overline{WR}$ (Write)		
V	V_{PP} (Write/Erase Power Supply)		
5	V_{DDI} (Internal Power Supply)		

ADVANCE INFORMATION

switching characteristics over recommended ranges of supply voltage and ambient temperature range, synchronous read operations (see Figure 11, Figure 14, and Figure 21)

PARAMETER			3.3-V V_{DDE} RANGE		5-V V_{DDE} RANGE		UNITS
			MIN	MAX	MIN	MAX	
t_{CLK}	CLK period (see Note 25)						ns
t_{CH}	High time, clock		10		10		ns
t_{CL}	Low time, clock		10		10		ns
t_{CLCH}	Rise time, CLK			3		4	ns
t_{CHCL}	Fall time, CLK			3		4	ns
t_{CHAX}	Hold time, address from CLK high		3		3		ns
t_{CHRL}	Hold time, $\overline{WR}$ from CLK high		3		3		ns
t_{CHLH}	Hold time, $\overline{LBA}$ from CLK high		5		5		ns
t_{CHBH}	Hold time, $\overline{BAA}$ from CLK high		TBD		TBD		ns
t_{CHGH}	Hold time, $\overline{OE}$ from CLK high		2		2		ns
t_{CHSH}	Hold time, $\overline{DIS}$ from CLK high		2		2		ns
t_{ELCH}	Setup time, $\overline{E}$ to CLK high		TBD		TBD		ns
t_{AVCH}	Setup time, address to CLK high		10		10		ns
t_{RHCH}	Setup time, $\overline{WR}$ to CLK high		0		0		ns
t_{LLCH}	Setup time, $\overline{LBA}$ to CLK high		6		6		ns
t_{BLCH}	Setup time, $\overline{BAA}$ to CLK high		TBD		TBD		ns
t_{GLCH}	Setup time, $\overline{OE}$ to CLK high		9		9		ns
t_{SLCH}	Setup time, $\overline{DIS}$ to CLK high		12		12		ns
t_{CHCH1}	$\overline{LBA}$/CLK high to data latched ($\overline{OE}$/CLK), for one wait-state access	DCR7:6 = 00		47		47	ns
		DCR7:6 = 01		43		43	ns
		DCR7:6 = 1X		40		40	ns
t_{CHQD}	$\overline{OE}$/CLK high to data bus driven		0		0		ns
t_{CHQV}	$\overline{OE}$/CLK high to data valid	DCR7:6 = 00		22		TBD	ns
		DCR7:6 = 01		26		TBD	ns
		DCR7:6 = 1X		29		TBD	ns
t_{CHQX}	CLK high to data invalid		5		5		ns
t_{CHQZ}	CLK high to data high Z (see Note 26)			40		40	ns
t_{CHQL}	CLK high to $\overline{QV}$ low			TBD		TBD	ns
t_{CHQH}	CLK high to $\overline{QV}$ high			TBD		TBD	ns

NOTES: 25. t_{CLK} min = max ((t_{CHCH1}/#ws), $t_{CHQV} + t_{dsu,cpu} + t_{sys}$)
where: $t_{dsu,cpu}$ = data setup time for CPU
t_{sys} = system margin
#ws = number of wait states (CLKs) from address latched to data latched

26. $I_{OL}/I_{OH} = \pm 4$ mA, value dependent on loading conditions

switching characteristics over recommended ranges of supply voltage and ambient temperature range, synchronous reads with asynchronous $\overline{OE}$ operations (see Figure 20)

PARAMETER			3.3-V V_{DDE} RANGE		5-V V_{DDE} RANGE		UNITS
			MIN	MAX	MIN	MAX	
t_{GLQD}	$\overline{OE}$ low to data bus driven		0		0		ns
t_{GLQV}	$\overline{OE}$ low to data valid	DCR[7:6] = 00		TBD		TBD	ns
		DCR[7:6] = 01		TBD		TBD	ns
		DCR[7:6] = 1X		TBD		TBD	ns
t_{GHQX}	$\overline{OE}$ high to data invalid		TBD		TBD		ns
t_{GHQZ}	$\overline{OE}$ high to data high Z			TBD		TBD	ns

timing requirements over recommended ranges of supply voltage and ambient temperature range, synchronous write/erase operations (see Figure 22, Figure 24, and Figure 25)

		3.3-V V_{DDE} RANGE		5-V V_{DDE} RANGE		UNITS
		MIN	MAX	MIN	MAX	
t_{CHEH}	Hold time, $\overline{E}$ from CLK high	TBD		TBD		ns
t_{CHRH}	Hold time, $\overline{WR}$ from CLK high	3		3		ns
t_{CHWH}	Hold time, $\overline{WE}$ from CLK high	2		2		ns
t_{CHDX}	Hold time, CLK high to data	3		3		ns
t_{YHVL}	Hold time, V_{PP} from RY/$\overline{BY}$ high	0		0		ns
t_{CHYH1}	Duration of double-word/word write operation	TBD	TBD	TBD	TBD	ns
t_{CHYH2}	Duration of double-word/word write operation in low-power programming (LPP) mode	TBD	TBD	TBD	TBD	ns
t_{CHYH3}	Duration of block-erase operation	TBD	TBD	TBD	TBD	ns
t_{CHYH4}	Duration of block-erase operation in LPP mode	TBD	TBD	TBD	TBD	ns
t_{ELCH}	Setup time, $\overline{E}$ to CLK high	TBD		TBD		ns
t_{RLCH}	Setup time, $\overline{WR}$ to CLK high	10		10		ns
t_{WLCH}	Setup time, $\overline{WE}$ to CLK high	9		9		ns
t_{DVCH}	Setup time, data to CLK high	10		10		ns
t_{VHCH}	Setup time, V_{PP} to $\overline{LBA}$/CLK high	TBD		TBD		ns
t_{CHYL}	CLK high to RY/$\overline{BY}$ low	TBD		TBD		ns

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timing requirements over recommended ranges of supply voltage and ambient temperature range, asynchronous write/erase operations (see Figure 23 and Figure 26)

		3.3-V V_{DDE} RANGE		5-V V_{DDE} RANGE		UNITS
		MIN	MAX	MIN	MAX	
t_{WHWH}	Cycle time, write	TBD		TBD		ns
t_{WHAX}	Hold time, address from $\overline{WE}$ high	TBD		TBD		ns
t_{YHVL}	Hold time, V_{PP} from RY/$\overline{BY}$ high	0		0		ns
t_{WHEH}	Hold time, $\overline{E}$ from $\overline{WE}$ high	TBD		TBD		ns
t_{AVWH}	Setup time, address to $\overline{WE}$ high	TBD		TBD		ns
t_{ELWL}	Setup time, $\overline{E}$ to $\overline{WE}$ low	TBD		TBD		ns
t_{VHWH}	Setup time, V_{PP} to $\overline{WE}$ high	TBD		TBD		ns
t_{WL}	Pulse duration, $\overline{WE}$ low	TBD		TBD		ns
t_{WH}	Pulse duration, $\overline{WE}$ high	TBD		TBD		ns
t_{DVWH}	Data valid to $\overline{WE}$ high	TBD		TBD		ns
t_{WHDX}	$\overline{WE}$ high to data invalid	TBD		TBD		ns
t_{WHYH1}	Duration of double-word/word operation	TBD		TBD		ns
t_{WHYH2}	Duration of double-word/word operation in low-power programming (LPP) mode	TBD		TBD		ns
t_{WHYH3}	Duration of block-erase operation	TBD		TBD		ns
t_{WHYH4}	Duration of block-erase operation in LPP mode	TBD		TBD		ns
t_{WHYL}	$\overline{WE}$ high to RY/$\overline{BY}$ low	TBD		TBD		ns

V_{DDI} power-up and reset/power-down ($\overline{RP}$) characteristics over recommended ranges of supply voltage and ambient temperature range (see Figure 12)

	PARAMETER	MIN	MAX	UNITS
t_{5HPH}	Power (V_{DDI}) applied to $\overline{RP}$ high	1		ms
t_{PHCH}	$\overline{RP}$ high to $\overline{LBA}$/CLK high	200		ns
t_{PL5L}	$\overline{RP}$ low to power (V_{DDI}) low	0		ns
t_{5HVH}	V_{DDI} high to V_{PP} high		500	ns
t_{VHPH}	V_{PP} high to $\overline{RP}$ high	100		ns

PARAMETER MEASUREMENT INFORMATION

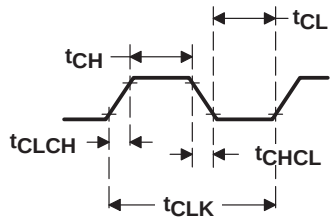


Figure 11. Clock (CLK) Waveform

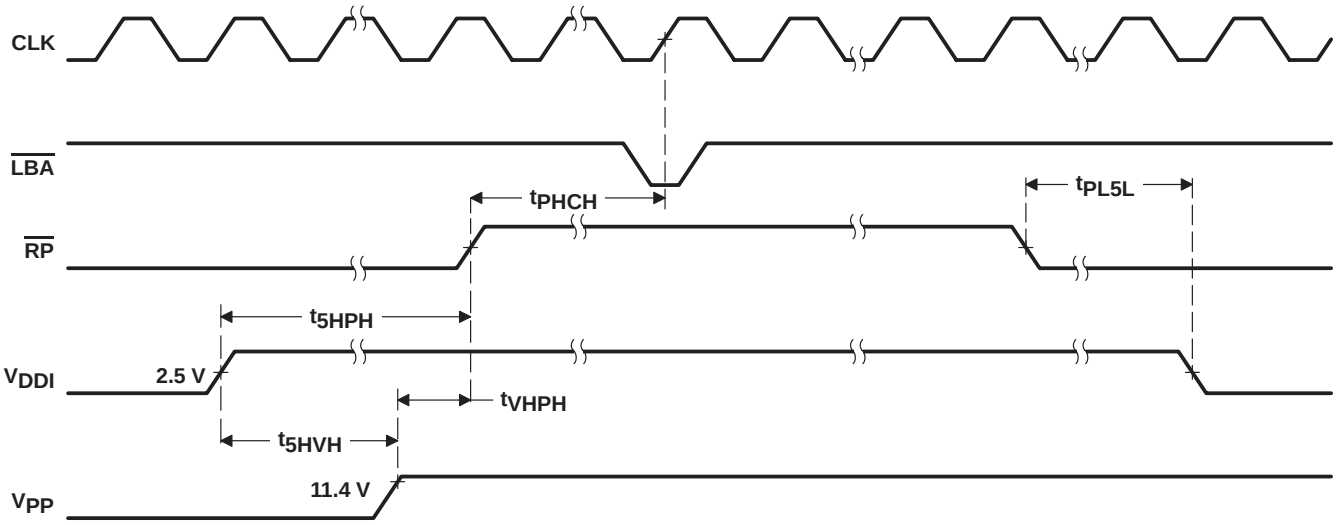
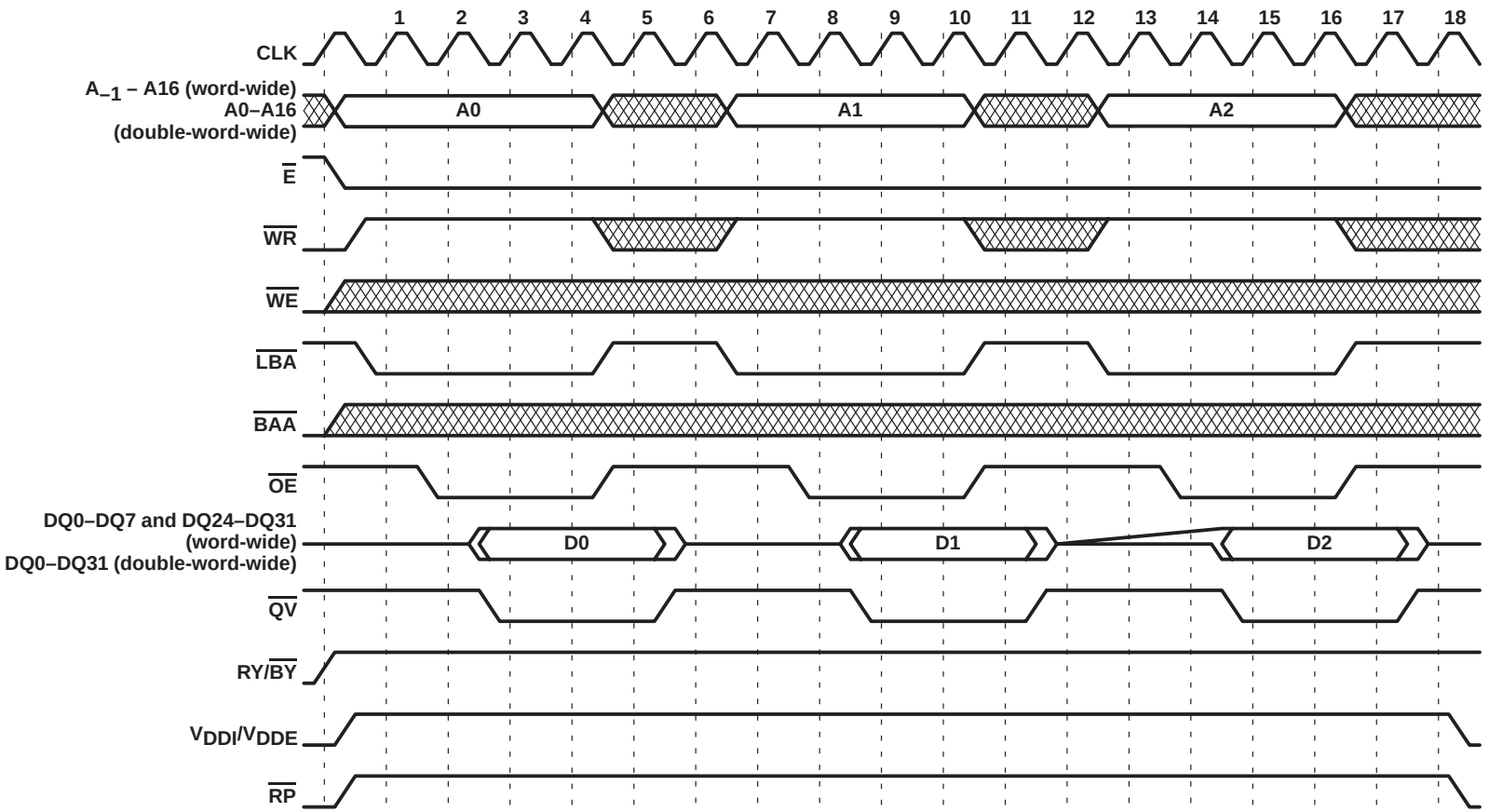


Figure 12. V_{PP}/V_{DDI} Power-Up and Reset/Power-Down ($\overline{RP}$) Waveforms

ADVANCE INFORMATION



BASIC/ENHANCED PIN SET DCR0	$\overline{OE}$ MODE DCR1	$\overline{WE}$ MODE DCR2	$\overline{DIS}$/WORD DCR3	$\overline{LRV}$/$\overline{BAA}$ DCR4	BURST LENGTH DCR25,24	BURST LATENCY (X) DCR29,28	BURST LATENCY (Y) DCR30	x16 WRITE OPTION DCR31
Basic pin set (DCR0 = 0)	0 (see Note D)	X	Optional (see Note E)	X	X	X	X	X
Enhanced pin set (DCR0 = 1)	0 (see Note D)	X	Optional (see Note E)	X	X	X	X	X

NOTES: A. X is a don't care.
B. See Table 8 through Table 12 for DCR setting descriptions.
C. Burst doesn't occur while $\overline{LBA}$ is low.
D. Synchronous and asynchronous $\overline{OE}$ are available (see Figure 20); DCR1 = 0 and DCR1 = 1, respectively.
E. For $\overline{DIS}$ usage, see Figure 21.

Figure 13. Asynchronous Read Cycles With Device Configuration Register Settings

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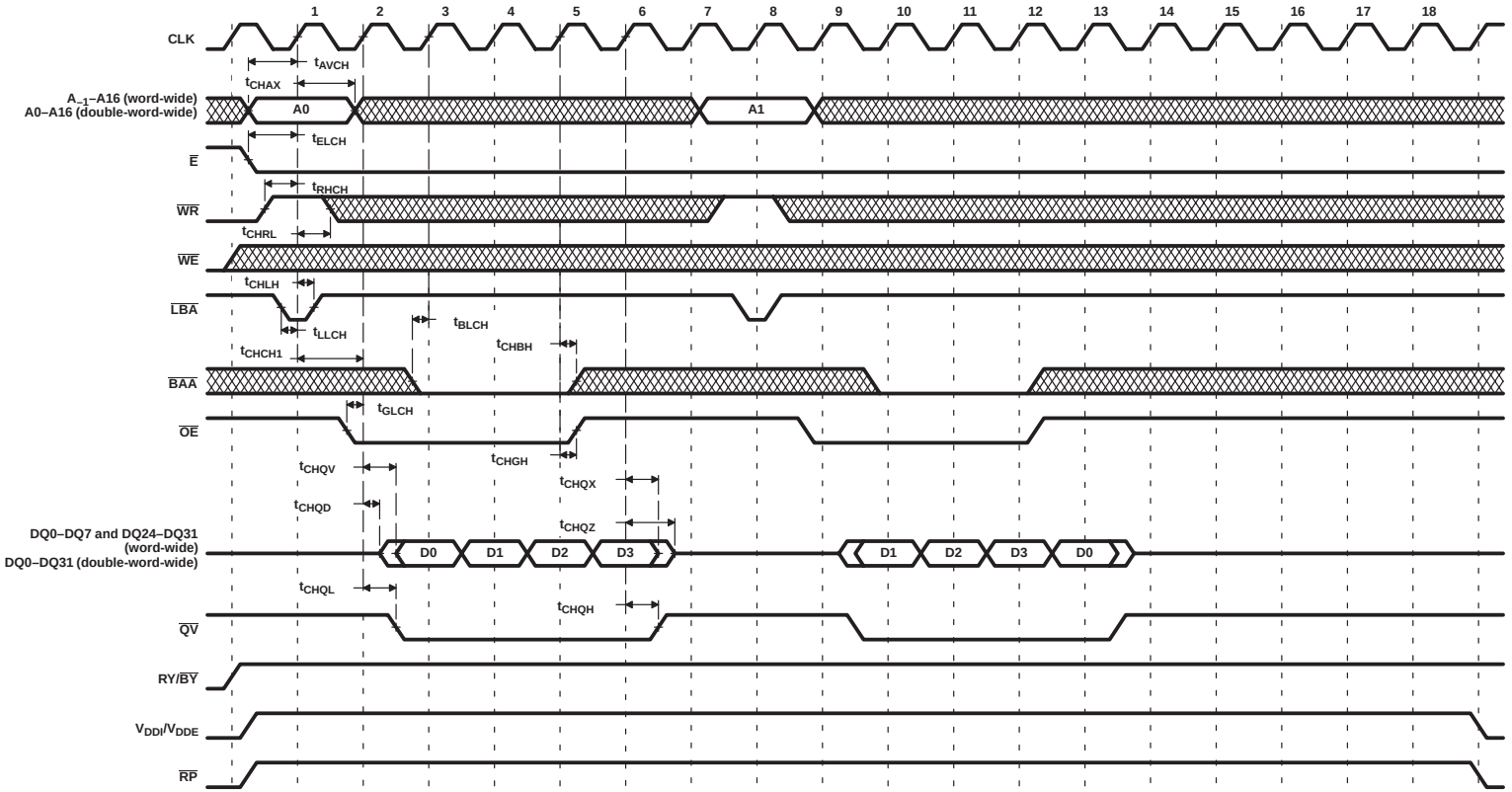
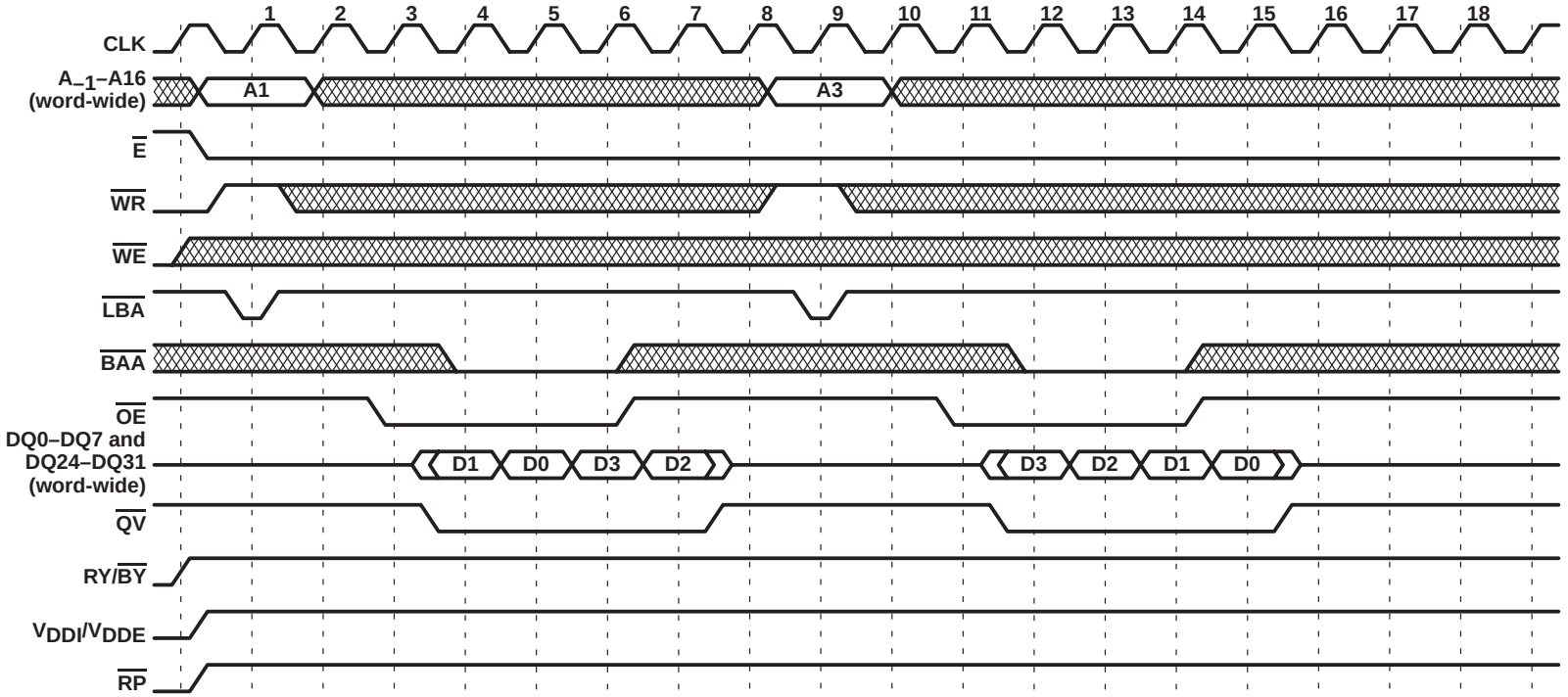


BASIC/ENHANCED PIN SET DCR0	OE MODE DCR1	WE MODE DCR2	DIS/ WORD DCR3	LRV/ BAA DCR4	BURST LENGTH DCR25,24	BURST LATENCY (X) DCR29,28	BURST LATENCY (Y) DCR30	x16 WRITE OPTION DCR31
Basic pin set (DCR0=0)	0 (see Note E)	X	Optional (see Note F)	1 (see Note G)	00 (see Note H)	01 (see Note I)	0 (see Note I)	X
Enhanced pin set (DCR0=1)	0 (see Note E	X	Optional (see Note F)	1 (see Note G)	00 (see Note H)	01 (see Note I)		X

NOTES: A. X is a don't care.
B. See Table 8 through Table 12 for DCR setting descriptions.
C. Address A1 can be loaded as early as clock 5 for overlapped burst reads.
D. Linear burst with the enhanced pin set requires $\overline{LBO} = V_{IL}$.
E. Synchronous and asynchronous $\overline{OE}$ are available (see Figure 20); DCR1 = 0 and DCR1 = 1, respectively.
F. For $\overline{DIS}$ usage, see Figure 21.
G. For synchronous $\overline{OE}$ (DCR1 = 0), $\overline{BAA}$ is not required to burst if $\overline{OE}$ is used to control the burst (DCR[29:28] = 00).
H. 3–1– . . . –1 is available with MOD4, MOD8, MOD16 (see Figure 17), and MOD32.
I. Linear MOD4 burst is available with 3–1–1–1, 4–1–1–1, 5–1–1–1, and 4–2–2–2 (see Figure 19).

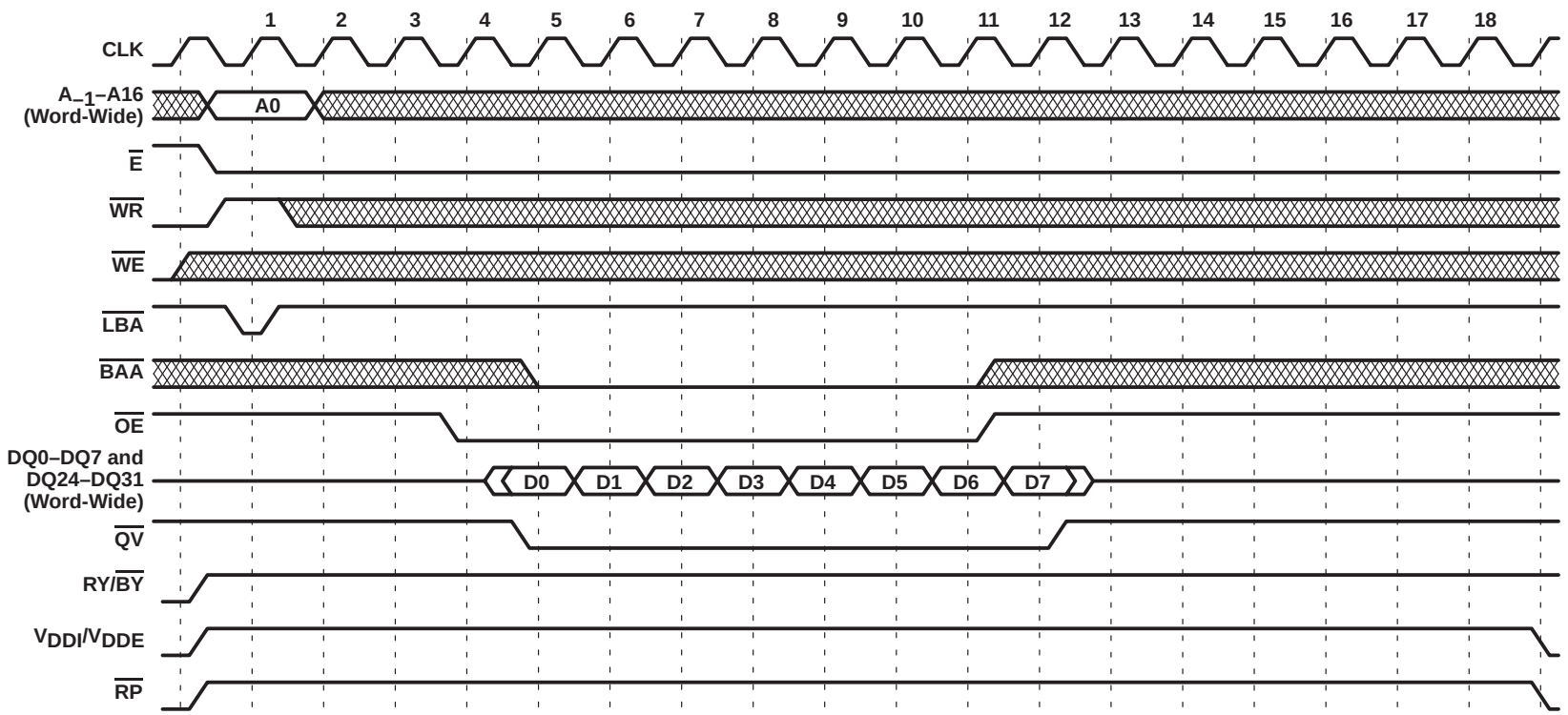
Figure 14. 3–1–1–1 MOD4 Linear Burst With Device Configuration Register Settings



BASIC/ENHANCED PIN SET DCR0	$\overline{OE}$ MODE DCR1	$\overline{WE}$ MODE DCR2	$\overline{DIS}/\overline{WORD}$ DCR3	$\overline{LRV}/\overline{BAA}$ DCR4	BURST LENGTH DCR25,24	BURST LATENCY (X) DCR29,28	BURST LATENCY (Y) DCR30	x16 WRITE OPTION DCR31
See Note E	—	—	—	—	—	—	—	—
Enhanced pin set (DCR0 = 1)	0	X	1 (see Note F)	1 (see Note G)	00 (see Note H)	10 (see Note I)	0	X

NOTES: A. X is a don't care.
B. See Table 8 through Table 12 for DCR setting descriptions.
C. Address A3 can be loaded as early as clock 6 for overlapped burst reads.
D. Interleave burst requires $\overline{LBO}$ = V_{IH}.
E. Interleave burst is available only with the enhanced pin set.
F. Interleave burst is available only with the 16-bit data bus, which requires DCR3 = 1 with $\overline{WORD}$ = V_{IL}.
G. For synchronous $\overline{OE}$ (DCR1 = 0), $\overline{BAA}$ is not required to burst if $\overline{OE}$ is used to control the burst (DCR[29:28] = 00).
H. Interleave burst is available only with MOD4.
I. Interleave MOD4 burst is available with 3–1–1–1 and 4–1–1–1.

Figure 15. 4–1–1–1 MOD4 Interleave Burst Read With Device Configuration Register Settings



BASIC/ENHANCED PIN SET DCR0	$\overline{OE}$ MODE DCR1	$\overline{WE}$ MODE DCR2	$\overline{DIS}/\overline{WORD}$ DCR3	$\overline{LRV}/\overline{BAA}$ DCR4	BURST LENGTH DCR25,24	BURST LATENCY (X) DCR29,28	BURST LATENCY (Y) DCR30	x16 WRITE OPTION DCR31
Basic pin set (DCR0 = 0)	0	X	1 (see Note D)	1 (see Note E)	01 (see Note F)	11 (see Note G)	0 (see Note G)	X
Enhanced pin set (DCR0 = 1)	0	X	1 (see Note D)	1 (see Note E)	01 (see Note F)	11 (see Note G)	0 (see Note G)	X

NOTES: A. X is a don't care.
B. See Table 8 through Table 12 for DCR setting descriptions.
C. Linear burst with the enhanced pin set requires $\overline{LBO}$ = V_{IL}.
D. 5–1– . . . –1 is available only with the 16-bit data bus, which requires DCR3 = 1 and $\overline{WORD}$=V_{IL}.
E. For synchronous $\overline{OE}$ (DCR1 = 0), $\overline{BAA}$ is not required to burst if required to burst if $\overline{OE}$ is used to control the burst (DCR[29:28] = 00).
F. 5–1– . . . –1 is available with MOD4, MOD8, MOD16, and MOD32.
G. Linear MOD8 burst is available with 3–1– . . . –1, 4–1– . . . –1, 5–1– . . . –1, and 4–2– . . . –2.

Figure 16. 5–1– . . . –1 MOD8 Linear Burst With Device Configuration Register Settings

BASIC/ENHANCED PIN SET DCR0	OE MODE DCR1	WE MODE DCR2	DIS/WORD DCR3	LRV/BAA DCR4	BURST LENGTH DCR25,24	BURST LATENCY (X) DCR29,28	BURST LATENCY (Y) DCR30	x16 WRITE OPTION DCR31
Basic pin set (DCR0 = 0)	0	X	Optional	1 (see Note D)	10 (see Note E)	01 (see Note F)	0 (see Note F)	X
Enhanced pin set (DCR0 = 1)	0	X	Optional	1 (see Note D)	10 (see Note E)	01 (see Note F)	0 (see Note F)	X

NOTES: A. X is a don't care.
B. See Table 8 through Table 12 for DCR setting descriptions.
C. Linear burst with the enhanced pin set requires $\overline{LBO}$ = V_{IL}.
D. For synchronous $\overline{OE}$ (DCR1 = 0), $\overline{BAA}$ is not required to burst if $\overline{OE}$ is used to control the burst (DCR[29:28] = 00).
E. 3–1– . . . –1 is available with MOD4 (see Figure 14), MOD8, MOD16, and MOD32.
F. Linear MOD16 burst is available with 3–1– . . . –1, 4–1– . . . –1, 5–1– . . . –1, and 4–2– . . . –2.

Figure 17. 3–1– . . . –1 MOD16 Linear Burst With Device Configuration Register Settings

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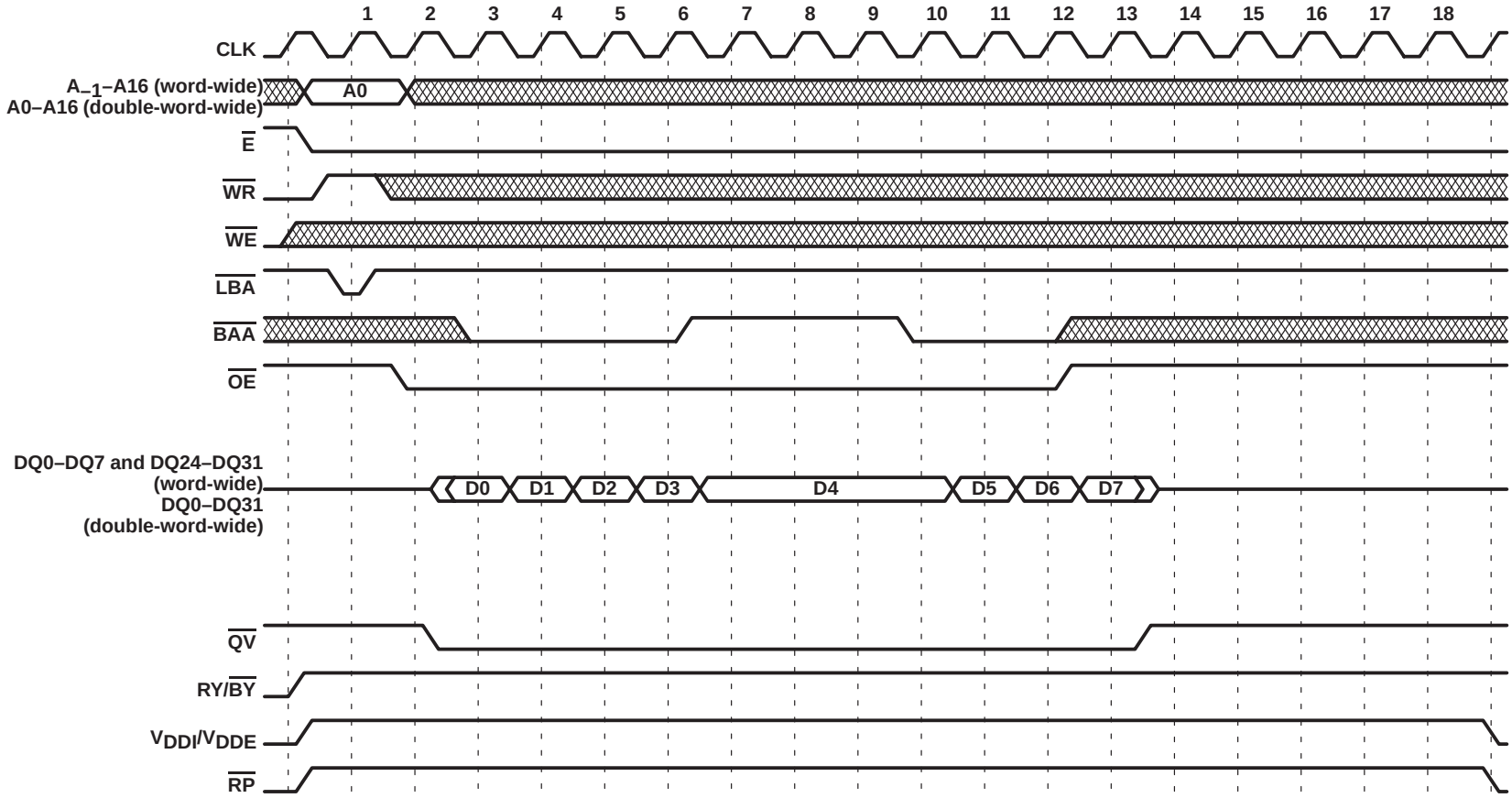
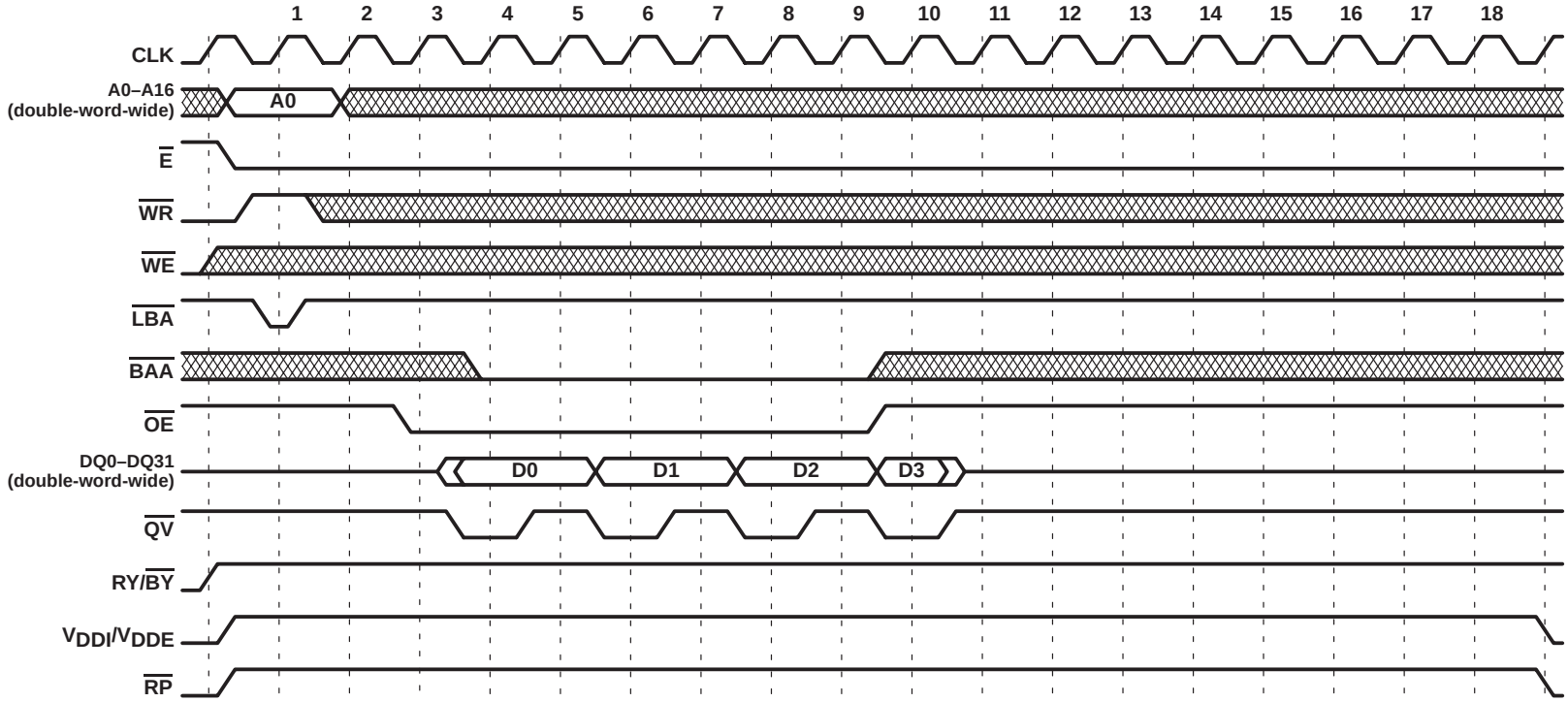


BASIC/ENHANCED PIN SET DCR0	OE MODE DCR1	WE MODE DCR2	DIS/WORD DCR3	LRV/BAA DCR4	BURST LENGTH DCR25,24	BURST LATENCY (X) DCR29,28	BURST LATENCY (Y) DCR30	x16 WRITE OPTION DCR31
Basic pin set (DCR0 = 0)	0	X	Optional	1 (see Note D)	01 (see Note E)	01 (see Note F)	0 (see Note F)	X
Enhanced pin set (DCR0 = 1)	0	X	Optional	1 (see Note D)	01 (see Note E)	01 (see Note F)	0 (see Note F)	X

NOTES: A. X is a don't care.
B. See Table 8 through Table 12 for DCR setting descriptions.
C. Linear burst with the enhanced pin set requires $\overline{LBO}=V_{IL}$.
D. $\overline{BAA}$ is required to hold the current data and corresponding address for a burst suspend/resume.
E. $\overline{BAA}$ suspend/resume is available with MOD4, MOD8, MOD16, and MOD32.
F. $\overline{BAA}$ suspend/resume is available with 3–1– . . . –1, 4–1– . . . –1, 5–1– . . . –1, and 4–2– . . . –2.

Figure 18. $\overline{BAA}$ Suspend/Resume on 3–1– . . . –1 MOD8 Linear Burst With Device Configuration Register Settings



BASIC/ENHANCED PIN SET DCR0	OE MODE DCR1	WE MODE DCR2	DIS/WORD DCR3	LRV/BAA DCR4	BURST LENGTH DCR25,24	BURST LATENCY (X) DCR29,28	BURST LATENCY (Y) DCR30	x16 WRITE OPTION DCR31
Basic pin set (DCR0 = 0)	0	X	Optional (see Note D)	1 (see Note E)	00 (see Note F)	10 (see Note G)	1 (see Note G)	X
Enhanced pin set (DCR0 = 1)	0	X	Optional (see Note D)	1 (see Note E)	00 (see Note F)	10 (see Note G)	1 (see Note G)	X

NOTES: A. X is a don't care.
B. See Table 8 through Table 12 for DCR setting descriptions.
C. Linear burst with the enhanced pin set requires $\overline{LBO}$ = V_{IL}.
D. 4–2–2–2 is available only with the 32-bit data bus. With DCR3 = 0, the 32-bit data bus is automatically in use. With DCR3 = 1, set $\overline{WORD}$=V_{IH}.
E. For synchronous $\overline{OE}$ (DCR1 = 0), $\overline{BAA}$ is not required to burst if $\overline{OE}$ is used to control the burst (DCR[29:28] = 00).
F. 4–2– . . . –2 is available with MOD4, MOD8, MOD16, and MOD32.
G. Linear MOD4 burst is available with 3–1–1–1 (see Figure 14), 4–1–1–1, 5–1–1–1, and 4–2–2–2.

Figure 19. 4–2–2–2 MOD4 Linear Burst With Device Configuration Register Settings

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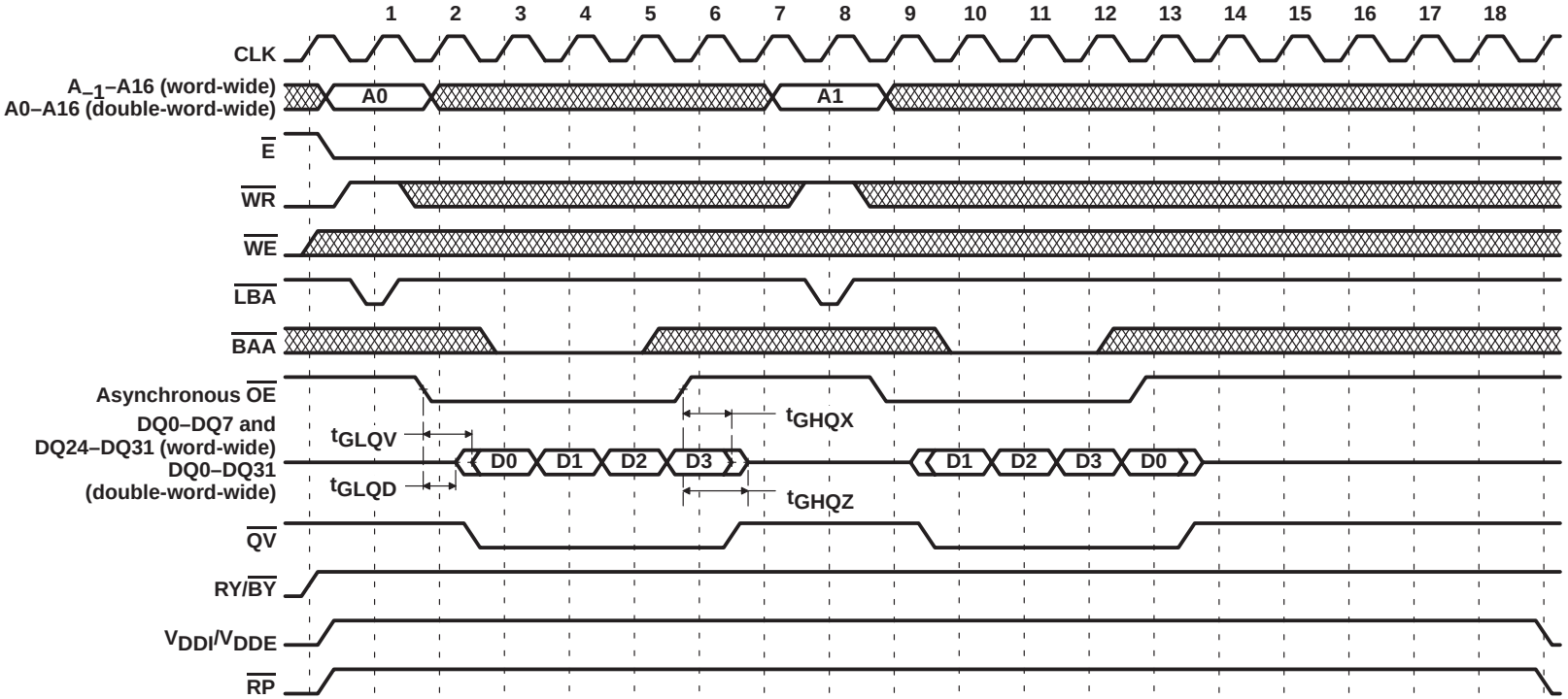
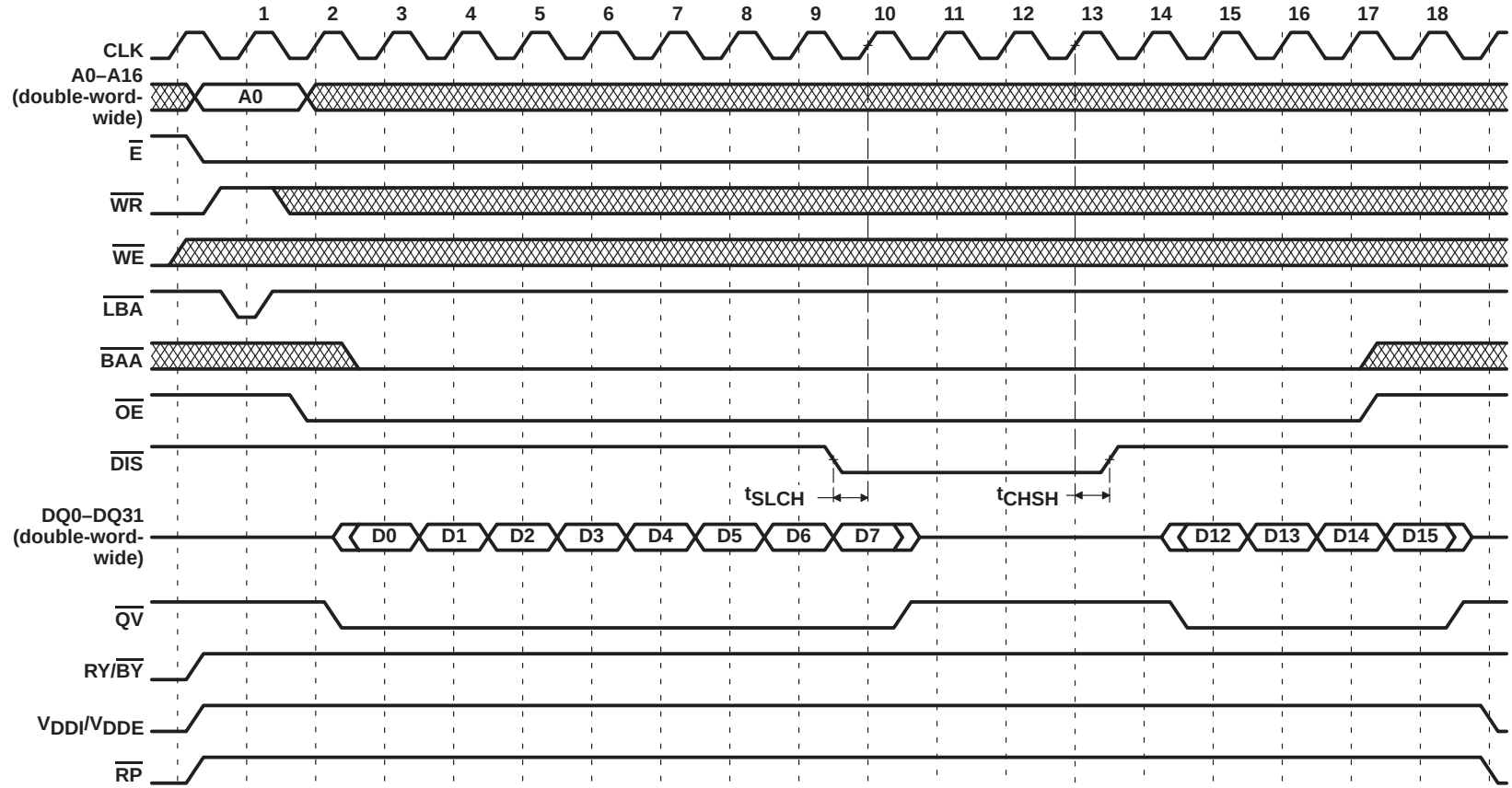


BASIC/ENHANCED PIN SET DCR0	OE MODE DCR1	WE MODE DCR2	DIS/WORD DCR3	LRV/BAA DCR4	BURST LENGTH DCR25,24	BURST LATENCY (X) DCR29,28	BURST LATENCY (Y) DCR30	x16 WRITE OPTION DCR31
Basic pin set (DCR0 = 0)	1 (see Note E)	X	Optional	1 (see Note F)	00 (see Note G)	01 (see Note H)	0 (see Note H)	X
Enhanced pin set (DCR0 = 1)	0 (see Note E)	X	Optional	1 (see Note F)	00 (see Note G)	01 (see Note H)	0 (see Note H)	X

NOTES: A. X is a don't care.
B. See Table 8 through Table 12 for DCR setting descriptions.
C. Address A1 can be loaded as early as clock 5 for overlapped burst reads.
D. Linear burst with the enhanced pin set requires $\overline{LBO}=V_{IL}$.
E. For synchronous $\overline{OE}$ burst reads see Figure 14 through Figure 19, and Figure 21.
F. For asynchronous $\overline{OE}$ (DCR1 = 1), $\overline{BAA}$ is required to burst.
G. 3–1– . . . –1 is available with MOD4, MOD8, MOD16 (see Figure 17), and MOD32.
H. Linear MOD4 burst is available with 3–1–1–1, 4–1–1–1, 5–1–1–1, and 4–2–2–2 (see Figure 19).

Figure 20. 3–1–1–1 MOD4 Linear Burst (Asynchronous $\overline{OE}$) With Device Configuration Register Settings



BASIC/ENHANCED PIN SET DCR0	OE MODE DCR1	WE MODE DCR2	DIS/WORD DCR3	LRV/BAA DCR4	BURST LENGTH DCR25,24	BURST LATENCY (X) DCR29,28	BURST LATENCY (Y) DCR30	x16 WRITE OPTION DCR31
Basic pin set (DCR0 = 0)	0	X	0 (see Note D)	1 (see Note E)	10 (see Note F)	01 (see Note G)	0 (see Note G)	X
Enhanced pin set (DCR0 = 1)	0	X	0 (see Note D)	1 (see Note E)	10 (see Note F)	01 (see Note G)	0 (see Note G)	X

NOTES: A. X is a don't care.
B. See Table 8 through Table 12 for DCR setting descriptions.
C. Linear burst with the enhanced pin set requires $\overline{LBO}$=V_{IL}.
D. $\overline{DIS}$ requires DCR3 =0, available only with the 32-bit data bus.
E. For synchronous $\overline{OE}$ (DCR1 =0), $\overline{BAA}$ is not required to burst if $\overline{OE}$ is used to control the burst (DCR[29:28] = 00).
F. 3–1– . . . –1 is available with MOD4 (see Figure 14), MOD8, MOD16, and MOD32.
G. Linear MOD16 burst is available with 3–1– . . . –1, 4–1– . . . –1, 5–1– . . . –1, and 4–2– . . . –2.

Figure 21. $\overline{DIS}$ Usage on 3–1– . . . –1 MOD16 Linear Burst With Device Configuration Register Settings

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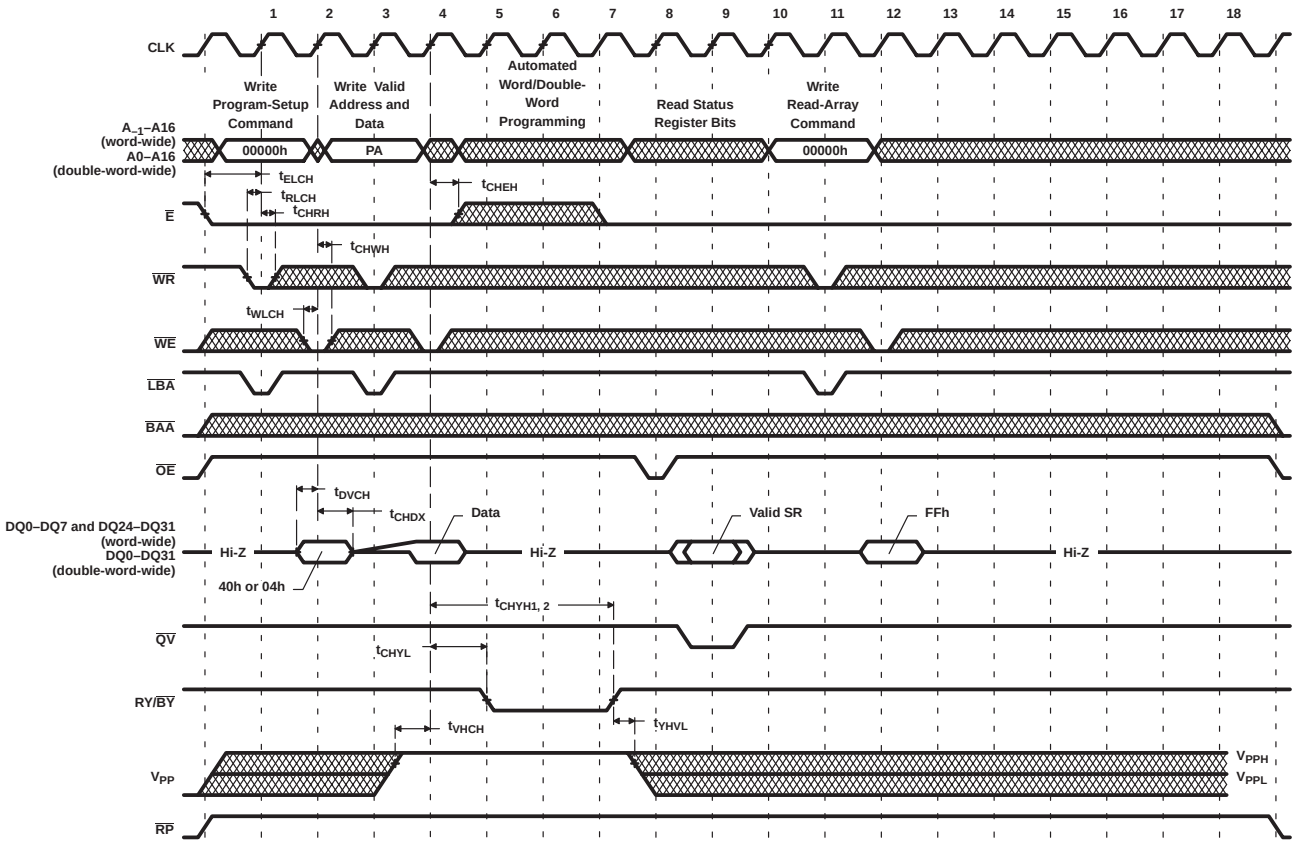

BASIC/ENHANCED PIN SET DCR0	OE MODE DCR1	WE MODE DCR2	DIS/WORD DCR3	LRV/BAA DCR4	BURST LENGTH DCR25,24	BURST LATENCY (X) DCR29,28	BURST LATENCY (Y) DCR30	x16 WRITE OPTION DCR31
Basic pin set (DCR0 = 0)	0	0 (see Note D)	Optional	X (see Note E)	XX	XX	X	0 (see Note F)
Enhanced pin set (DCR0 = 1)	0	0 (see Note D)	Optional	X (see Note E)	XX	XX	X	0 (see Note F)

NOTES: A. X is a don't care. PA is the address to be programmed.
B. See Table 8 for DCR setting descriptions.
C. Wait states can be inserted between the address and data phases of a command or write-data cycle. In addition, the address phase of the write-data cycle can occur on the same CLK as the data phase of the command cycle (see Figure 24).
D. For asynchronous two-cycle write timing (DCR2 = 1), see Figure 23.
E. For LRV usage (DCR4 = 0), see Figure 3, and for DCR4 = 1, see Figure 5.
F. When using the 16-bit data bus (DCR3 = 1 and WORD = V_{IL}), both two-cycle writes (DCR31 = 0) and three-cycle writes (DCR31 = 1) are available. For synchronous three-cycle write timing, see Figure 24.

Figure 22. Synchronous Write-Cycle Timing (Two-Cycle Write) With Device Configuration Register Settings

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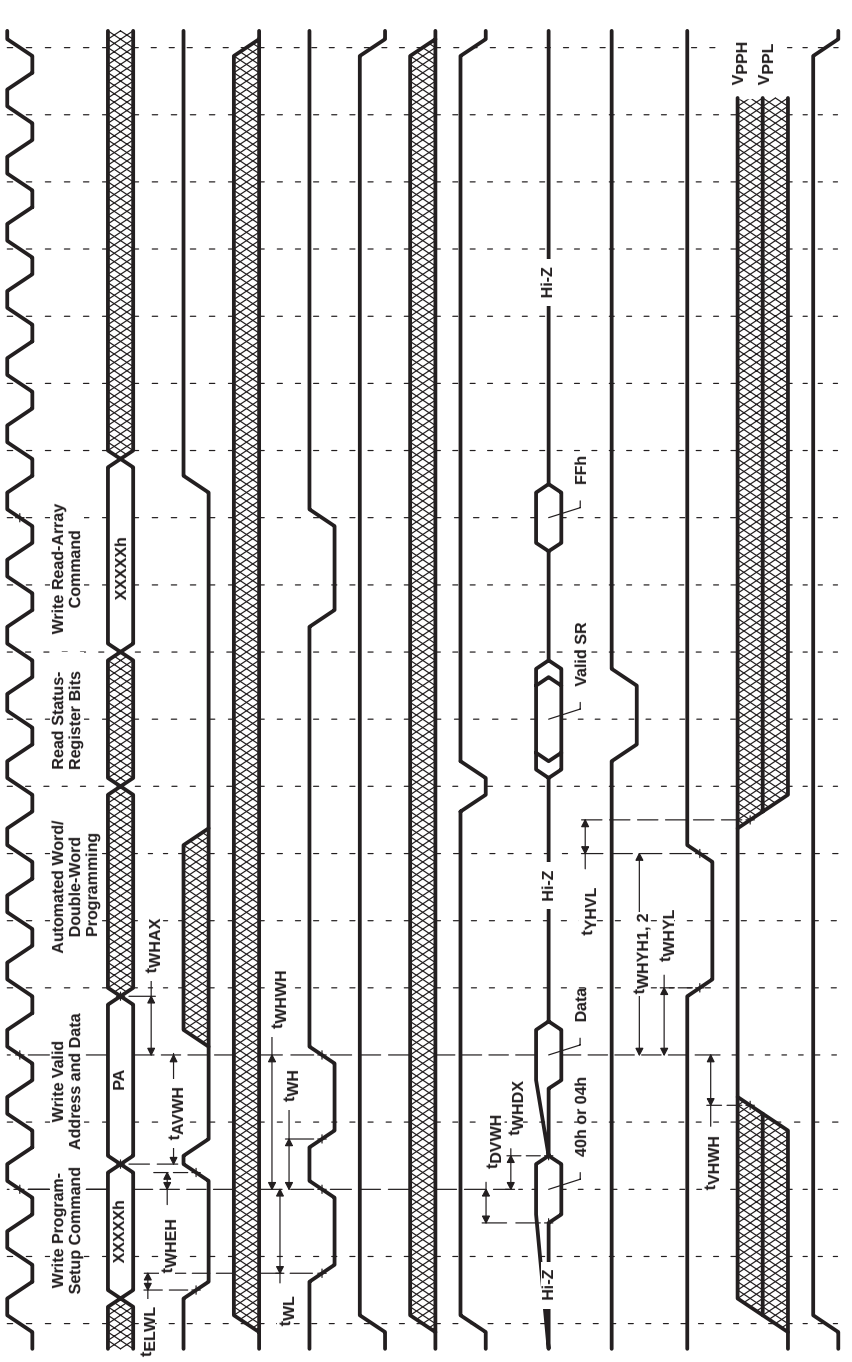
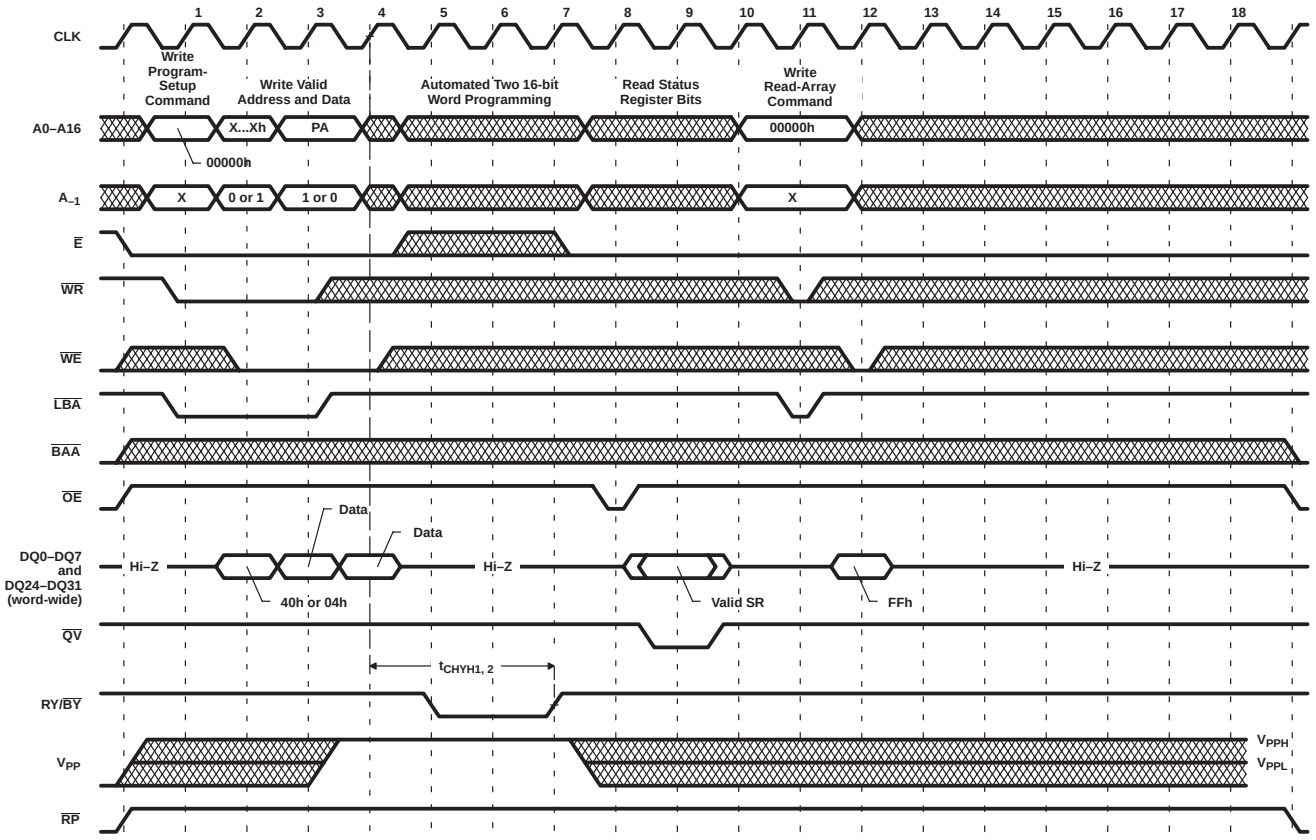


BASIC/ENHANCED PIN SET DCR0	OE MODE DCR1	WE MODE DCR2	DIS/WORD DCR3	LRV/BAA DCR4	BURST LENGTH DCR25,24	BURST LATENCY (X) DCR29,28	BURST LATENCY (Y) DCR30	x16 WRITE OPTION DCR31
Basic pin set (DCR0 = 0)	0	1 (see Note D)	Optional	X (see Note E)	XX	XX	X	0 (see Note F)
Enhanced pin set (DCR0 = 1)	0	1 (see Note D)	Optional	X (see Note E)	XX	XX	X	0 (see Note F)

NOTES: A. X is a don't care. PA is the address to be programmed.
B. See Table 8 for DCR setting descriptions.
C. For asynchronous writes, the address and data/command are latched on the $\overline{WE}$ rising edge.
D. For synchronous two-cycle write timing (DCR2 = 0), see Figure 22.
E. For $\overline{LRV}$ usage (DCR4 = 0), see Figure 4; and for $\overline{DCR4}$ = 1, see Figure 5.
F. When using the 16-bit data bus (DCR3 = 1 and $\overline{WORD}$ = V_{IL}), both two-cycle writes (DCR31 = 0) and three-cycle writes (DCR31 = 1) are available. For asynchronous three-cycle writes, the "write valid address and data" cycle is repeated for the second 16-bit data segment.

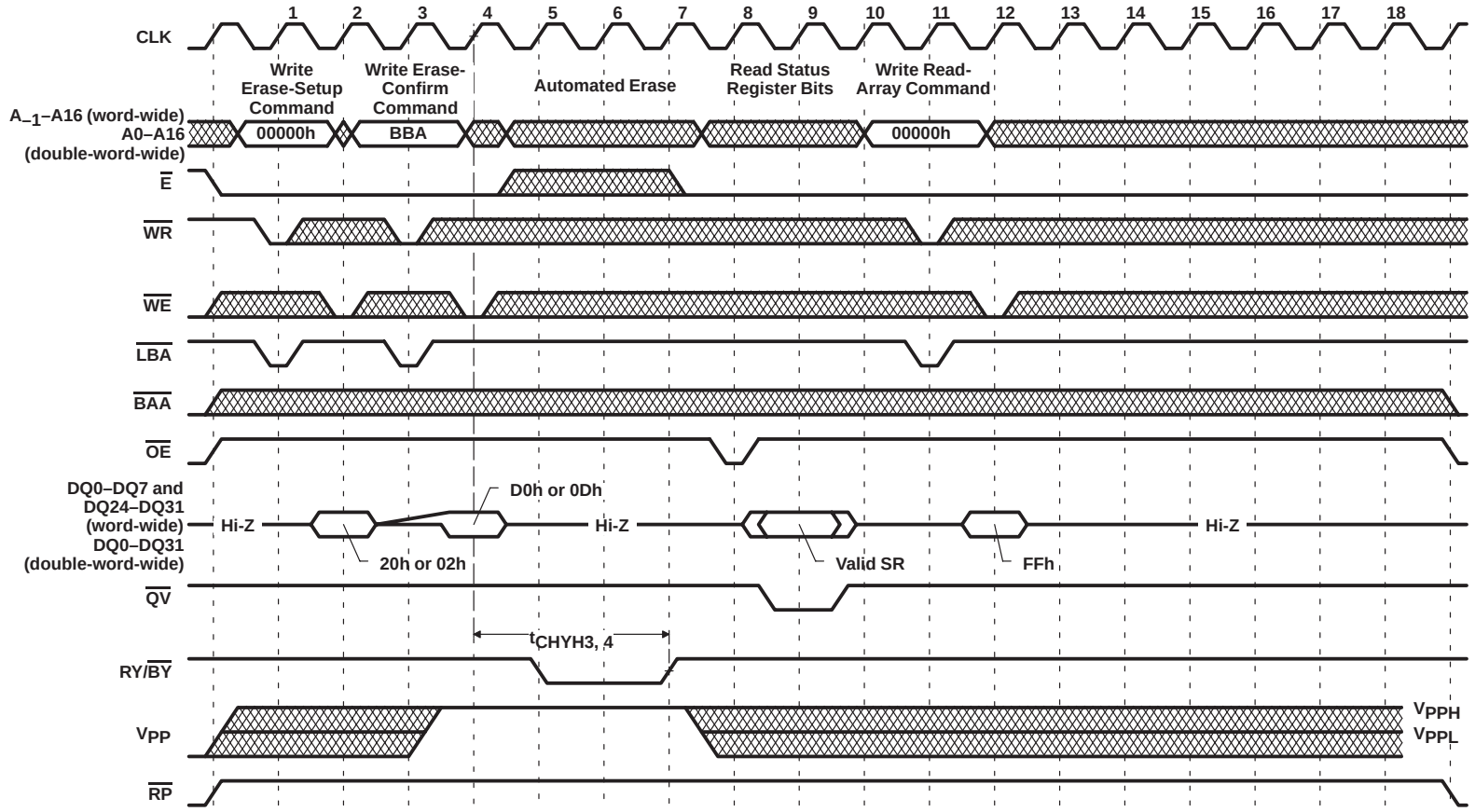
Figure 23. Asynchronous Write-Cycle Timing (Two-Cycle Write) With Device Configuration Register Settings



BASIC/ENHANCED PIN SET DCR0	$\overline{OE}$ MODE DCR1	$\overline{WE}$ MODE DCR2	$\overline{DIS}/\overline{WORD}$ DCR3	$\overline{LRV}/\overline{BAA}$ DCR4	BURST LENGTH DCR25,24	BURST LATENCY (X) DCR29,28	BURST LATENCY (Y) DCR30	x16 WRITE OPTION DCR31
Basic pin set (DCR0 = 0	0	0	1 (see Note D)	X (see Note E)	XX	XX	X	1 (see Note F)
Enhanced pin set (DCR0 = 1)	0	0	1 (see Note D)	X (see Note E)	XX	XX	X	1 (see Note F)

NOTES: A. X is a don't care. PA is the address to be programmed.
B. See Table 8 for DCR setting descriptions.
C. Wait states can be inserted between the address and data phases of a command or write-data cycle. In addition, wait states can be inserted between the data phase of the current cycle and the address phase of the next cycle (see Figure 22).
D. Three-cycle write is available only with the 16-bit data bus, which requires DCR3 = 1 and $\overline{WORD}=V_{IL}$.
E. For $\overline{LRV}$ usage (DCR4 = 0) see Figure 6, and for DCR4 = 1 see Figure 7.
F. When using the 16-bit data bus (DCR3 = 1 and $\overline{WORD} = V_{IL}$), both two-cycle writes (DCR31 = 0) and three-cycle writes (DCR31 = 1) are available. For synchronous two-cycle write timing, see Figure 22.

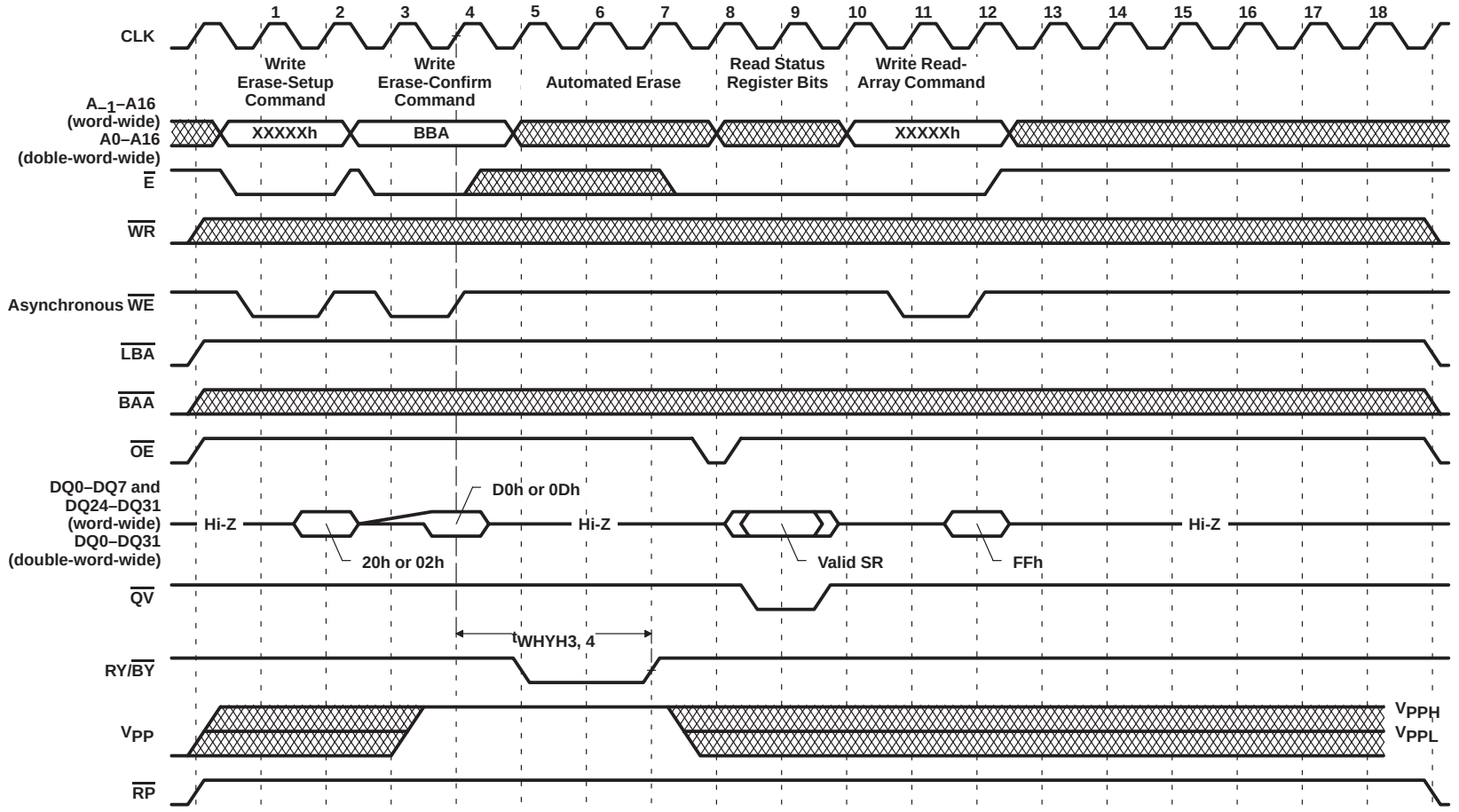
Figure 24. Synchronous Write-Cycle Timing (Three-Cycle Write) with Device Configuration Register Settings



BASIC/ENHANCED PIN SET DCR0	OE MODE DCR1	WE MODE DCR2	DIS/WORD DCR3	LRV/BAA DCR4	BURST LENGTH DCR25,24	BURST LATENCY (X) DCR29,28	BURST LATENCY (Y) DCR30	x16 WRITE OPTION DCR31
Basic pin set (DCR0 = 0)	0	0 (see Note D)	Optional	X (see Note E)	XX	XX	X	X
Enhanced pin set (DCR0 = 1)	0	0 (see Note D)	Optional	X (see Note E)	XX	XX	X	X

NOTES: A. X is a don't care. BBA is the block base address.
B. See Table 8 for DCR setting descriptions.
C. Wait states can be inserted between the address and data phases of a command or erase-confirm cycle. In addition, the address phase of the erase-confirm cycle can occur on the same CLK as the data phase of the command cycle.
D. For asynchronous erase-cycle timing (DCR2 = 1), see Figure 26.
E. For LRV usage (DCR4 = 0), see Figure 8; and for DCR4 = 1, see Figure 9.

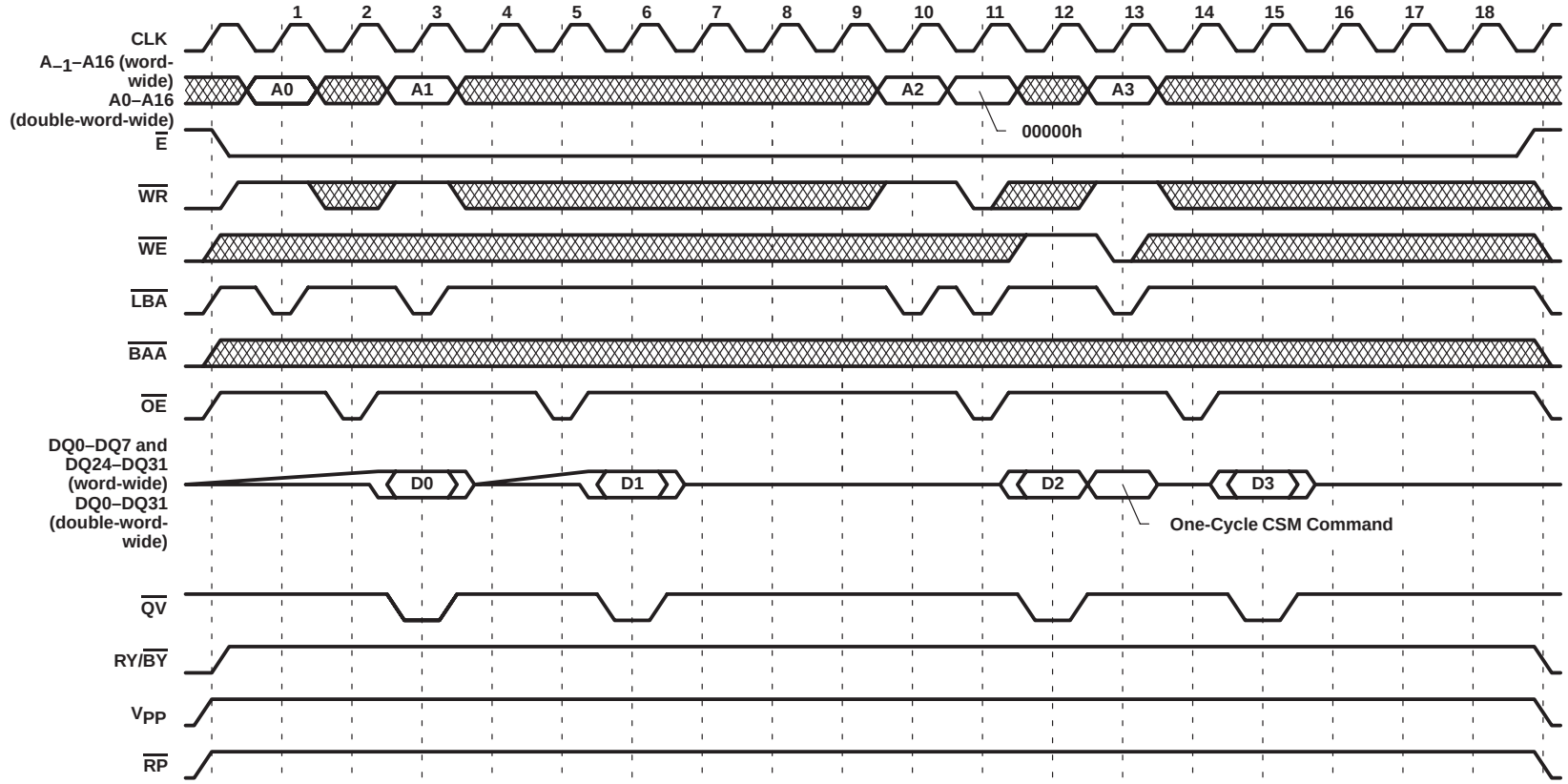
Figure 25. Synchronous Erase-Cycle Timing With Device Configuration Register Settings



BASIC/ENHANCED PIN SET DCR0	$\overline{OE}$ MODE DCR1	$\overline{WE}$ MODE DCR2	$\overline{DIS}/\overline{WORD}$ DCR3	$\overline{LRV}/\overline{BAA}$ DCR4	BURST LENGTH DCR25,24	BURST LATENCY (X) DCR29,28	BURST LATENCY (Y) DCR30	x16 WRITE OPTION DCR31
Basic pin set (DCR0 = 0)	0	1 (see Note D)	Optional	X (see Note E)	XX	XX	X	X
Enhanced pin set (DCR0 = 1)	0	1 (see Note D)	Optional	X (see Note E)	XX	XX	X	X

NOTES: A. X is a don't care. BBA is the block base address.
B. See Table 8 for DCR setting descriptions.
C. For asynchronous erase, the address and command are latched on the $\overline{WE}$ rising edge.
D. For asynchronous erase-cycle timing (DCR2 = 1), see Figure 25.
E. For $\overline{LRV}$ usage (DCR4 = 0), see Figure 8; and for DCR4 = 1, see Figure 9.

Figure 26. Asynchronous Erase-Cycle Timing With Device Configuration Register Settings



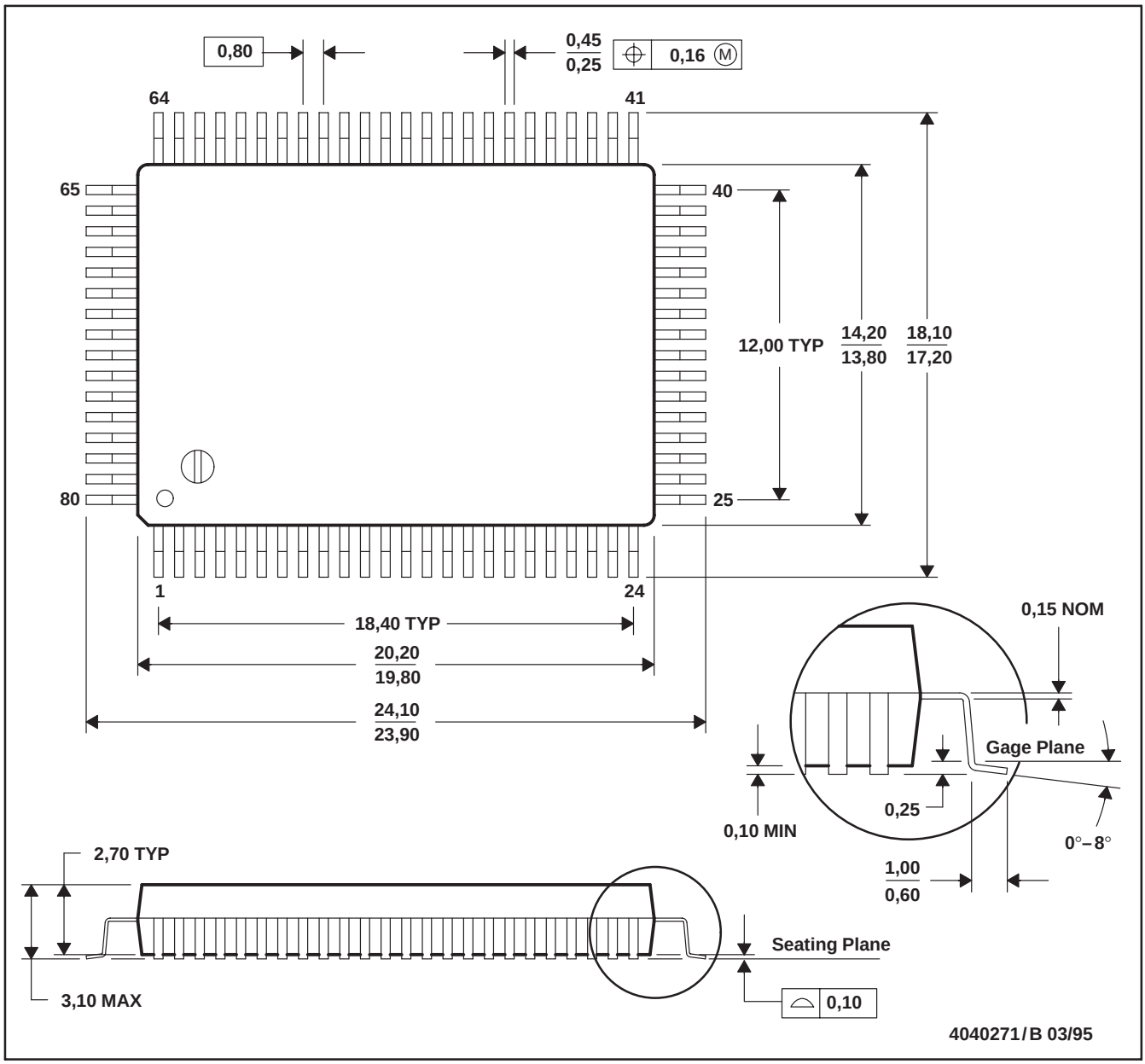
BASIC/ENHANCED PIN SET DCR0	OE MODE DCR1	WE MODE DCR2	DIS/WORD DCR3	LRV/BAA DCR4	BURST LENGTH DCR25,24	BURST LATENCY (X) DCR29,28	BURST LATENCY (Y) DCR30	x16 WRITE OPTION DCR31
Basic pin set (DCR0 = 0)	0 (see Note D)	0 (see Note E)	Optional	1 (see Note F)	X	Optional (see Note G)	X	X
Enhanced pin set (DCR0 = 1)	0 (see Note D)	0 (see Note E)	Optional	1 (see Note F)	X	Optional (see Note G)	X	X

NOTES: A. X is a don't care.
B. See Table 8 for DCR setting descriptions.
C. LBA (for A1) can go low as early as CLK2.
D. Synchronous and asynchronous OE are available (see Figure 20); DCR1 = 0 and DCR1 = 1, respectively.
E. Synchronous WE is required to perform overlapping writes.
F. For single reads, the number of wait states can be set by selecting BAA usage (DCR4 = 1) and by setting DCR[29:28] = (number of wait states). BAA usage is not required to perform single reads.
G. In the timing diagram above, both 1 wait state (CLK 1 to CLK 2) and 2 wait states (CLK 3 to CLK 5) are shown, corresponding to DCR[29:28] = 01 and 10, respectively. OE can be used to control the number of wait states for single reads by setting DCR[29:28] = 00.

Figure 27. Overlapping Read/Write Cycles With Device Configuration Register Settings

MECHANICAL DATA

PAF (R-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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