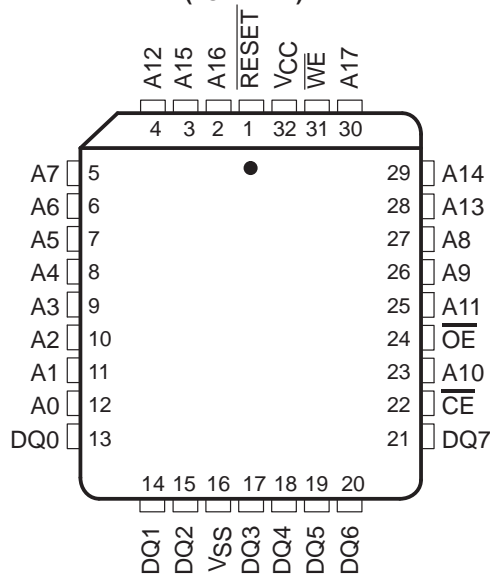


# TMS29F002RT, TMS29F002RB 262144 BY 8-BIT FLASH MEMORIES

SMJS849B – MARCH 1997 – REVISED JUNE 1998

- **Single Power Supply Supports 5-V  $\pm$  10% Read/Write Operation**
- **Organization : . . . 262 144 by 8 Bits**
- **Array-Blocking Architecture**
  - One 16K-Byte Boot Sector
  - Two 8K-Byte Parameter Sectors
  - One 32K-Byte Sector
  - Three 64K-Byte Sectors
  - Any Combination of Sectors Can Be Erased. Support Full-Chip Erase
  - Any Combination of Sectors Can Be Marked as Read-Only
- **Boot-Code Sector Architecture**
  - T = Top Sector
  - B = Bottom Sector
- **Sector Protection**
  - Hardware Protection Method That Disables Any Combination of Sectors From Write or Erase Operations Using Standard Programming Equipment
- **Embedded Program/Erase Algorithms**
  - Automatically Pre-Programs and Erases Any Sector
  - Automatically Programs and Verifies the Program Data at Specified Address
- **JEDEC Standards**
  - Compatible With JEDEC Byte Pinouts
  - Compatible With JEDEC EEPROM Command Set
- **Fully Automated On-Chip Erase and Program Operations**
- **100 000 Program/Erase Cycles**
- **Low Power Dissipation**
- **Low Current Consumption**
  - 25-mA Typical Active Read
  - 30-mA Typical Program/Erase Current
  - Less Than 100- $\mu$ A Standby Current
- **All Inputs/Outputs TTL-Compatible**
- **Erase Suspend/Resume**
  - Supports Reading Data From, or Programming Data to, a Sector Not Being Erased
- **Hardware-Reset Pin Initializes the Internal-State Machine to the Read Operation**

FM PACKAGE  
32-PIN PLCC  
(TOP VIEW)



PIN NOMENCLATURE

A[0:17]	Address Inputs
DQ[0:7]	Data In/Data out
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{RESET}$	Reset/Deep Power Down
VCC	Power Supply
VSS	Ground
WE	Write Enable

- **32-Pin Plastic Leaded Chip Carrier (PLCC) (FM Suffix)**
- **Detection Of Program/Erase Operation**
  - Data Polling and Toggle Bit Feature of Program/Erase Cycle Completion
- **High-Speed Data Access at 5-V  $V_{CC} \pm 10\%$** 
  - 90 ns Commercial . . . 0°C to 70°C
  - 100 ns Extended . . . –40°C to 85°C



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

Copyright © 1998, Texas Instruments Incorporated

# TMS29F002RT, TMS29F002RB

## 262144 BY 8-BIT

### FLASH MEMORIES

SMJS849B – MARCH 1997 – REVISED JUNE 1998

---

#### description

The TMS29F002RT/B is a 262 144 by 8-bit (2097 152-bit), 5-V single-supply, programmable read-only memory device that can be electrically erased and reprogrammed. This device is organized as 262 144 by 8 bits, divided into seven sectors:

- One 16K-byte boot sector
- Two 8K-byte sectors
- One 32K-byte sector
- Three 64K-byte sectors

Any combination of sectors can be marked as read-only or erased. Full-chip erasure is also supported.

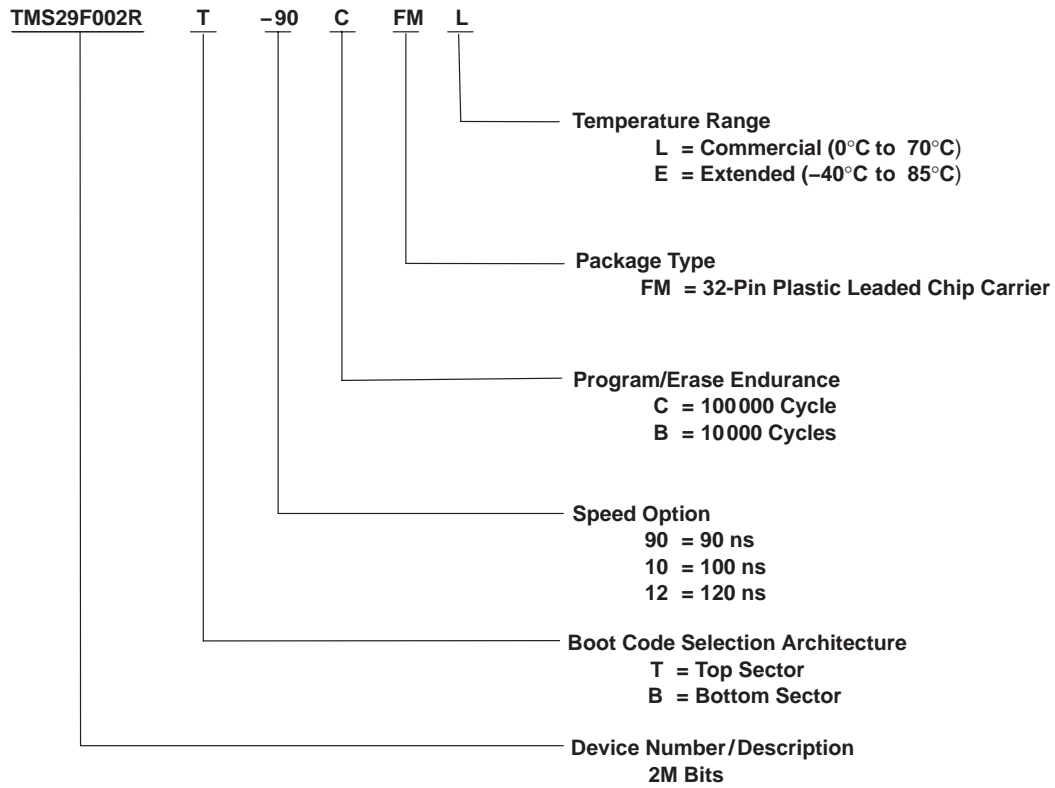
Sector data protection is afforded by methods that can disable any combination of sectors from write or read operations using standard programming equipment. An on-chip state machine provides an on-board algorithm that automatically pre-programs and erases any sector before it automatically programs and verifies program data at any specified address. The command set is compatible with the JEDEC 2M-bit electrically erasable, programmable read-only memory (EEPROM) command set. A suspend/resume feature allows access to unaltered memory blocks during a section-erase operation. All outputs of this device are TTL-compatible. Additionally, an erase/suspend/resume feature supports reading data from, or programming data to, a sector that is not being erased.

Device operations are selected by writing JEDEC-standard commands into the command register using standard microprocessor write timings. The command register acts as an input to an internal-state machine which interprets the commands, controls the erase and programming operations, outputs the status of the device, outputs the data stored in the device, and outputs the device algorithm-selection code. On initial power up, the device defaults to the read mode. A hardware-reset pin initializes the internal-state machine to the read operation.

The device has low power dissipation with a 25-mA typical active read for the byte mode, 30-mA typical program/erase current mode, and less than 100- $\mu$ A standby current with a 15- $\mu$ A deep-power-down mode. These devices are offered with 90-, 100-, and 120-ns access times. Table 1 and Table 2 show the sector-address ranges. The TMS29F002RT/B is offered in a 32-pin plastic leaded chip carrier (PLCC) (FM suffix).



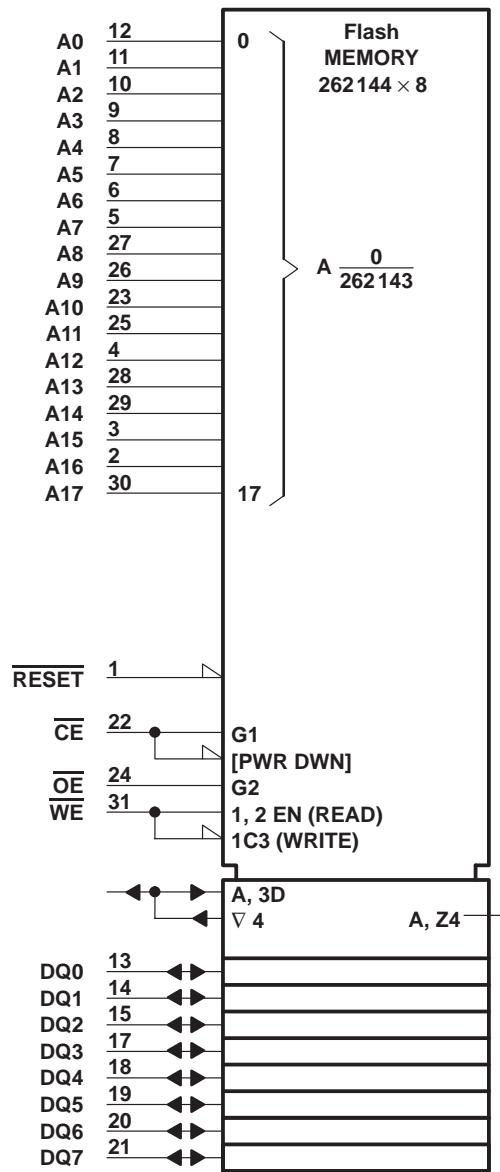
**device symbol nomenclature**



**TMS29F002RT, TMS29F002RB**  
**262144 BY 8-BIT**  
**FLASH MEMORIES**

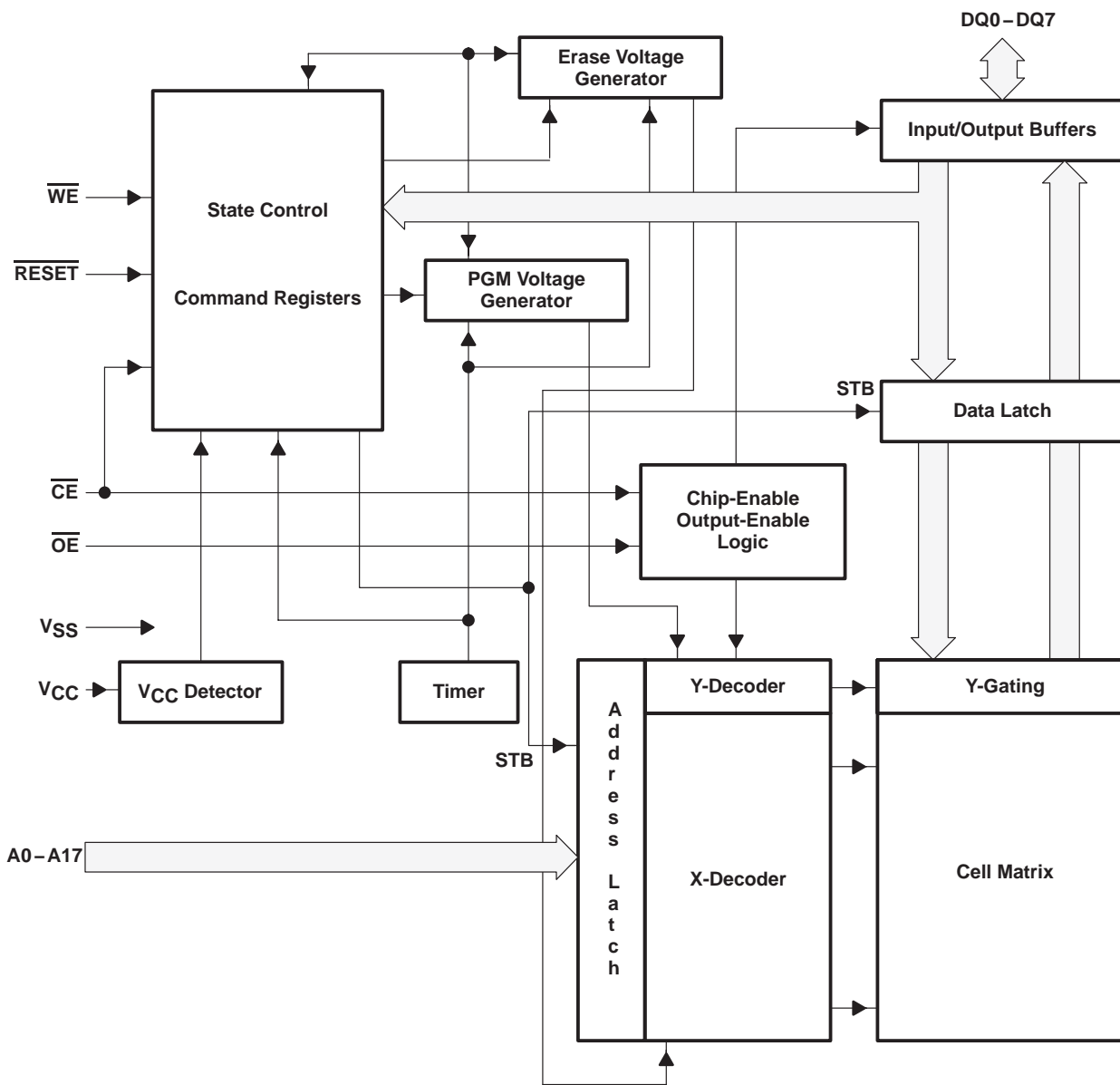
SMJS849B – MARCH 1997 – REVISED JUNE 1998

**logic symbol†**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

block diagram



**TMS29F002RT, TMS29F002RB**  
**262144 BY 8-BIT**  
**FLASH MEMORIES**

SMJS849B – MARCH 1997 – REVISED JUNE 1998

**operation**

See Table 1 and Table 2 for the sector-address ranges of the TMS29F002RT/B.

**Table 1. Top-Boot Sector-Address Ranges†‡**

	A17	A16	A15	A14	A13	SECTOR SIZE	(x8) ADDRESS RANGE
SA6	1	1	1	1	X	16K-Byte	3C000H–3FFFFH
SA5	1	1	1	0	1	8K-Byte	3A000H–3BFFFH
SA4	1	1	1	0	0	8K-Byte	38000H–39FFFH
SA3	1	1	0	X	X	32K-Byte	30000H–37FFFH
SA2	1	0	X	X	X	64K-Byte	20000H–2FFFFH
SA1	0	1	X	X	X	64K-Byte	10000H–1FFFFH
SA0	0	0	X	X	X	64K-Byte	00000H–0FFFFH

† The address range is A0–A17

‡ X can be 0 or 1.

**Table 2. Bottom-Boot Sector-Address Ranges†‡**

	A17	A16	A15	A14	A13	SECTOR SIZE	(x8) ADDRESS RANGE
SA6	1	1	X	X	X	64K-Byte	30000H–3FFFFH
SA5	1	0	X	X	X	64K-Byte	20000H–2FFFFH
SA4	0	1	X	X	X	64K-Byte	10000H–1FFFFH
SA3	0	0	1	X	X	32K-Byte	08000H–0FFFFH
SA2	0	0	0	1	1	8K-Byte	06000H–07FFFH
SA1	0	0	0	1	0	8K-Byte	04000H–05FFFH
SA0	0	0	0	0	X	16K-Byte	00000H–03FFFH

† The address range is A0–A17

‡ X can be 0 or 1.



**operation (continued)**

See Table 3 for the operation modes of the TMS29F002RT/B.

**Table 3. Operation Modes**

MODE	FUNCTIONS†								DQ0–DQ7
	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A0	A1	A6	A9	$\overline{\text{RESET}}$	
Algorithm-selection mode	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>ID</sub>	V <sub>IH</sub>	Manufacturer-Equivalent Code 01h (TMS29F002RT/B – Byte)
5-V power supply	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>ID</sub>	V <sub>IH</sub>	Device-Equivalent Code B0h (TMS29F002RT – Byte)
	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>ID</sub>	V <sub>IH</sub>	Device-Equivalent Code 34h (TMS29F002RB – Byte)
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	A0	A1	A6	A9	V <sub>IH</sub>	Data out
Output disable	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	X	X	X	X	V <sub>IH</sub>	Hi-Z
Standby and write inhibit	V <sub>IH</sub>	X	X	X	X	X	X	V <sub>IH</sub>	Hi-Z
Write‡	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	A0	A1	A6	A9	V <sub>IH</sub>	Data in
Temporary sector unprotect	X	X	X	X	X	X	X	V <sub>ID</sub>	X
Verify sector protect	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>ID</sub>	V <sub>IH</sub>	Data out
Hardware reset	X	X	X	X	X	X	X	V <sub>IL</sub>	Hi-Z

Legend:

V<sub>IL</sub> = Logic 0

V<sub>IH</sub> = Logic 1

V<sub>ID</sub> = 12.0 V ± 0.5 V

† X can be V<sub>IL</sub> or V<sub>IH</sub>.

‡ See Table 5 for valid address and data during write.

**read mode**

A logic-low signal applied to the  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  pins allows the output of the TMS29F002RT/B to be read. When two or more '29F002RT/B devices are connected in parallel, the output of any one device can be read without interference. The  $\overline{\text{CE}}$  pin is for power control and must be used for device selection. The  $\overline{\text{OE}}$  pin is for output control, and is used to gate the data output onto the bus from the selected device.

The address-access time (t<sub>AVQV</sub>) is the delay from stable address to valid output data. The chip-enable ( $\overline{\text{CE}}$ ) access time (t<sub>ELQV</sub>) is the delay from  $\overline{\text{CE}}$  low and stable addresses to valid output data. The output-enable access time (t<sub>GLQV</sub>) is the delay from  $\overline{\text{OE}}$  low to valid output data when  $\overline{\text{CE}}$  equals logic low and addresses are stable for at least the duration of t<sub>AVQV</sub>–t<sub>GLQV</sub>.

**standby mode**

I<sub>CC</sub> supply current is reduced by applying a logic-high level on  $\overline{\text{CE}}$  and  $\overline{\text{RESET}}$  to enter the standby mode. In the standby mode, the outputs are placed in the high-impedance state. Applying a CMOS logic-high level on  $\overline{\text{CE}}$  and  $\overline{\text{RESET}}$  reduces the current to 100 µA. Applying a TTL logic-high level on  $\overline{\text{CE}}$  and  $\overline{\text{RESET}}$  reduces the current to 1 mA. If the '29F002RT/B is deselected during erasure or programming, the device continues to draw active current until the operation is complete.

**output disable**

When  $\overline{\text{OE}}$  equals V<sub>IH</sub> or  $\overline{\text{CE}}$  equals V<sub>IH</sub>, output from the device is disabled and the output pins (DQ0–DQ7) are placed in the high-impedance state.

# TMS29F002RT, TMS29F002RB

## 262144 BY 8-BIT

### FLASH MEMORIES

SMJS849B – MARCH 1997 – REVISED JUNE 1998

#### automatic-sleep mode

The '29F002RT/B has a built-in feature called automatic-sleep mode to minimize device energy consumption. The automatic-sleep mode, which is independent of  $\overline{CE}$ ,  $\overline{WE}$ , and  $\overline{OE}$ , is enabled when addresses remain stable for 300 ns. Typical sleep-mode current is 100  $\mu$ A. Sleep mode does not affect output data, which remains latched and available to the system.

#### algorithm selection

The algorithm-selection mode provides access to a binary code that matches the device with its proper programming and erase command operations. This mode is activated when  $V_{ID}$  (11.5 V to 12.5 V) is placed on address pin A9. Address pins A1 and A6 must be logic low. Two bytes of code are accessed by toggling address pin A0 from  $V_{IL}$  to  $V_{IH}$ . Address pins other than A0, A1, and A6 can be at logic low or at logic high.

The algorithm-selection mode can also be read by using the command register, which is useful when  $V_{ID}$  is not available to be placed on address pin A9. Table 4 shows the binary algorithm-selection codes.

**Table 4. Algorithm-Selection Codes (5-V Single Power Supply)<sup>†</sup>**

	CODE	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer-equivalent code	01H	0	0	0	0	0	0	0	1
TMS29F002RT	B0H	1	0	1	1	0	0	0	0
TMS29F002RB	34H	0	0	1	1	0	1	0	0
Sector protection	01H	0	0	0	0	0	0	0	1

<sup>†</sup> A1 =  $V_{IL}$ , A6 =  $V_{IL}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{OE} = V_{IL}$

#### erase and programming

Erase and programming of the '29F002RT/B are accomplished by writing a sequence of commands using standard microprocessor write timing. The commands are written to a command register and input to the command-state machine (CSM). The CSM interprets the command entered and initiates program, erase, suspend, and resume operations as instructed. The CSM acts as the interface between the write-state machine (WSM) and external chip operations. The WSM controls all voltage generation, pulse generation, preconditioning, and verification of memory contents. Program and block-/chip-erase functions are fully automatic. Once the end of a program or erase operation has been reached, the device resets internally to the read mode. If  $V_{CC}$  drops below the low-voltage-detect level ( $V_{LKO}$ ), any programming or erase operation is aborted and subsequent writes are ignored until the  $V_{CC}$  level is greater than  $V_{LKO}$ . The control pins must be logically correct to prevent unintentional command writes or programming or erasing.

#### command definitions

Device operating modes are selected by writing specific address and data sequences into the command register. Table 5 defines the valid command sequences. Writing incorrect address and data values or writing them in the incorrect sequence causes the device to reset to the read mode. The command register does not occupy an addressable memory location. The register is used to store the command sequence, along with the address and data needed by the memory array. Commands are written by setting  $\overline{CE} = V_{IL}$ ,  $\overline{OE} = V_{IH}$ , and bringing  $\overline{WE}$  from logic high to logic low. Addresses are latched on the falling edge of  $\overline{WE}$  and data is latched on the rising edge of  $\overline{WE}$ . Holding  $\overline{WE} = V_{IL}$  and toggling  $\overline{CE}$  is an alternative method. See the switching characteristics of the write/erase/program-operations section for specific timing information.



**command definitions (continued)**

**Table 5. Command Definitions**

COMMAND	BUS CYCLES	1ST CYCLE		2ND CYCLE		3RD CYCLE		4TH CYCLE		5TH CYCLE		6TH CYCLE	
		ADDR	DATA	ADDR	DATA	ADDR	DATA	ADDR	DATA	ADDR	DATA	ADDR	DATA
Read/reset	1	XXXH	F0H										
	3	555H	AAH	2AAH	55H	555H	F0H	RA	RD				
Algorithm selection	3	555H	AAH	2AAH	55H	555H	90H	01H	B0H				
									T				
									34H				
									B				
Program	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD				
Chip erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Sector erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
Sector-erase suspend	1	XXXH	B0H	Erase suspend valid during sector-erase operation									
Sector-erase resume	1	XXXH	30H	Erase resume valid only after erase-suspend operation									

**LEGEND:**

- RA = Address of the location to be read
- PA = Address of the location to be programmed
- SA = Address of the sector to be erased  
Addresses A13–A17 select one to seven sectors.
- RD = Data to be read at selected address location
- PD = Data to be programmed at selected address location

**read/reset command**

The read or reset mode is activated by writing either of the two read/reset command sequences into the command register. The device remains in this mode until another valid command sequence is input in the command register. Memory data is available in the read mode and can be read with standard microprocessor read-cycle timing.

On power up, the device defaults to the read/reset mode. A read/reset command sequence is not required and memory data is available.

**algorithm-selection command**

The algorithm-selection command allows access to a binary code that matches the device with the proper programming and erase command operations. After writing the three-bus-cycle command sequence, the first byte of the algorithm-selection code can be read from address XX00h. The second byte of the code can be read from address XX01h (see Table 5). This mode remains in effect until another valid command sequence is written to the device.

**program command**

Programming is a four-bus-cycle command sequence. The first three bus cycles put the device into the program-setup state. The fourth bus cycle loads the address location and the data to be programmed into the device. The addresses are latched on the falling edge of  $\overline{WE}$  and the data is latched on the rising edge of  $\overline{WE}$  in the fourth bus cycle. The rising edge of  $\overline{WE}$  starts the program operation. The embedded programming function automatically provides needed voltage and timing to program and verify the cell margin. Any further commands written to the device during the program operation are ignored.

# TMS29F002RT, TMS29F002RB

## 262144 BY 8-BIT

### FLASH MEMORIES

SMJS849B – MARCH 1997 – REVISED JUNE 1998

---

#### program command (continued)

Programming can be performed at any address location in any sequence. When erased, all bits are in a logic-high state. Logic lows are programmed into the device and only an erase operation can change bits from logic lows to logic highs. Attempting to program a 1 into a bit that has been programmed previously to a 0 causes the internal-pulse counter to exceed the pulse-count limit, which sets the exceed-time-limit indicator (DQ5) to a logic-high state. The automatic-programming operation is complete when the data on DQ7 is equivalent to the data written to this bit, at which time the device returns to the read mode and addresses are no longer latched. Figure 1 shows a flow chart of the typical device-programming operation.

#### chip-erase command

Chip erase is a six-bus-cycle command sequence. The first three bus cycles put the device into the erase-setup state. The next two bus cycles unlock the erase mode. The sixth bus cycle loads the chip-erase command. This command sequence is required to ensure that the memory contents are not erased accidentally. The rising edge of  $\overline{WE}$  starts the chip-erase operation. Any further commands written to the device during the chip-erase operation are ignored.

The embedded chip-erase function automatically provides the voltage and timing needed to program and to verify all the memory cells prior to electrical erase. It then erases and verifies the cell margin automatically without programming the memory cells prior to erase.

Figure 2 shows a flow chart of the typical chip-erase operation.

#### sector-erase command

Sector-erase is a six-bus-cycle command sequence. The first three bus cycles put the device into the erase-setup state. The next two bus cycles unlock the erase mode and the sixth bus cycle loads the sector-erase command and the sector-address location to be erased. Any address location within the desired sector can be used. The addresses are latched on the falling edge of  $\overline{WE}$  and the sector-erase command (30h) is latched on the rising edge of  $\overline{WE}$  in the sixth bus cycle. After a delay of 50  $\mu$ s from the rising edge of  $\overline{WE}$ , the sector-erase operation begins on the selected sector(s).

Additional sectors can be selected to be erased concurrently during the sector-erase command sequence. For each additional sector to be selected for erase, another bus cycle is issued. The bus cycle loads the next sector-address location and the sector-erase command. The time between the end of the previous bus cycle and the start of the next bus cycle must be less than 50  $\mu$ s; otherwise, the new sector location is not loaded. A time delay of 50  $\mu$ s from the rising edge of the last  $\overline{WE}$  starts the sector-erase operation. If there is a falling edge of  $\overline{WE}$  within the 50- $\mu$ s time delay, the timer is reset.

One to seven sector-address locations can be loaded in any sequence. The state of the delay timer can be monitored using the sector-erase delay indicator (DQ3). If DQ3 is at logic low, the time delay has not expired. See the operation status section for a description.

Any command other than erase suspend (B0h) or sector erase (30h) written to the device during the sector-erase operation causes the device to exit the sector-erase mode and the contents of the sector(s) selected for erase are no longer valid. To complete the sector-erase operation, reissue the sector-erase command sequence.

The embedded sector-erase function automatically provides needed voltage and timing to program and to verify all of the memory cells prior to electrical erase and then erases and verifies the cell margin automatically. Programming the memory cells prior to erase is not required.

See the operation status section for a full description. Figure 3 shows a flow chart of the typical sector-erase operation.



### **erase-suspend command**

The erase-suspend command (B0h) allows interruption of a sector-erase operation to read data from unaltered sectors of the device. Erase-suspend is a one-bus-cycle command. The addresses can be  $V_{IL}$  or  $V_{IH}$  and the erase-suspend command (B0h) is latched on the rising edge of  $\overline{WE}$ . Once the sector-erase operation is in progress, the erase-suspend command requests the internal write-state machine to halt operation at predetermined breakpoints. The erase-suspend command is valid only during the sector-erase operation and is invalid during programming and chip-erase operations. The sector-erase delay timer expires immediately if the erase-suspend command is issued while the delay is active.

After the erase-suspend command is issued, the device takes between 0.1  $\mu$ s and 15  $\mu$ s to suspend the operation. The toggle bit must be monitored to determine when the suspend has been executed. When the toggle bit stops toggling, data can be read from sectors that are not selected for erase. Reading from a sector selected for erase can result in invalid data. See the operation status section for a full description.

Once the sector-erase operation is suspended, reads or programs to a sector that is not being erased can be performed. This command is applicable only during sector-erase operations. Any other command written during the erase-suspend mode to the suspended sector is ignored.

### **erase-resume command**

The erase-resume command (30h) restarts a suspended sector-erase operation from the point where it was halted. Erase resume is a one-bus-cycle command. The addresses can be  $V_{IL}$  or  $V_{IH}$  and the erase-resume command (30h) is latched on the rising edge of  $\overline{WE}$ . When an erase-suspend/erase-resume command combination is written, the internal-pulse counter (exceed timing limit) is reset. The erase-resume command is valid only in the erase-suspend state. After the erase-resume command is executed, the device returns to the valid sector-erase state and further writes of the erase-resume command are ignored. After the device has resumed the sector-erase operation, another erase-suspend command can be issued to the device.

### **operation status**

The status of the device during an automatic-programming algorithm, chip-erase command, or sector-erase command can be determined in two ways:

- DQ6: Toggle bit
- DQ7: Data polling

### **status-bit definitions**

During operation of the automatic embedded program and erase functions, the status of the device can be determined by reading the data state of designated outputs. The data-polling bit (DQ7) and toggle bit (DQ6) require multiple successive reads to observe a change in the state of the designated output. Table 6 defines the values of the status flags.

**TMS29F002RT, TMS29F002RB**  
**262144 BY 8-BIT**  
**FLASH MEMORIES**

SMJS849B – MARCH 1997 – REVISED JUNE 1998

**status-bit definitions (continued)**

**Table 6. Operation Status Flags†**

	DEVICE OPERATION‡	DQ7	DQ6	DQ5	DQ3	DQ2	
In progress	Programming	$\overline{\text{DQ7}}$	T	0	0	No Tog	
	Program/erase in auto-erase mode	0	T	0	1	§	
	Erase-suspend mode	Erase-sector address	1	1	0	0	T
		Non-erase sector address	D	D	D	D	D
	Program in erase-suspend mode	$\overline{\text{DQ7}}^{\parallel}$	T	0	0	1§	
Exceeded time limits	Programming	$\overline{\text{DQ7}}$	T	1	0	No Tog	
	Program/erase in auto-erase mode	0	T	1	1	#	
	Program in erase-suspend mode	$\overline{\text{DQ7}}$	T	1	0	No Tog	
Successful operation complete	Programming complete	D	D	D	D	D	
	Sector-/chip-erase complete	1	1	1	1	1	

† T = toggle, D = data, No Tog = no toggle

‡ DQ4, DQ1, DQ0 are reserved for future use.

§ DQ2 can be toggled when the sector address applied is an erasing sector. DQ2 cannot be toggled when the sector address applied is a non-erasing sector. DQ2 is used to determine which sectors are erasing and which are not.

¶ Status flags apply when outputs are read from the address of a non-erase-suspend operation.

# If DQ5 is high (exceeded timing limits), successive reads from a problem sector causes DQ2 to toggle.

**data-polling (DQ7)**

The data-polling-status function outputs the complement of the data latched into the DQ7 data register while the write-state machine is engaged in a program or erase operation. Data bit DQ7 changes from complement to true to indicate the end of an operation. Data-polling is available only during programming, chip-erase, sector-erase, and sector-erase-timing delay. Data-polling is valid after the rising edge of WE in the last bus cycle of the command sequence loaded into the command register. Figure 4 shows a flow chart of data-polling.

During a program operation, reading DQ7 outputs the complement of the DQ7 data to be programmed at the selected address location. Upon completion, reading DQ7 outputs the true DQ7 data loaded into the program-data register. During the erase operations, reading DQ7 outputs a logic low. Upon completion, reading DQ7 outputs a logic high. Also, data-polling must be performed at a sector address that is within a sector that is being erased. Otherwise, the status is invalid. When using data-polling, the address should remain stable throughout the operation.

During a data-polling read, while  $\overline{\text{OE}}$  is logic low, data bit DQ7 can change asynchronously. Depending on the read timing, the system can read valid data on DQ7, while other DQ pins are still invalid. A subsequent read of the device is valid. See Figure 17 for the data-polling timing diagram.

**toggle bit (DQ6)**

The toggle-bit status function outputs data on DQ6, which toggles between logic high and logic low while the write-state machine is engaged in a program or erase operation. When DQ6 stops toggling at a logic high after two consecutive reads to the same address, the operation is complete. The toggle bit is available only during programming, chip erase, sector erase, and sector-erase-timing delay. Toggle bit data is valid after the rising edge of WE in the last bus cycle of the command sequence loaded into the command register. Figure 5 shows a flow chart of the toggle-bit status-read algorithm. Depending on the read timing, DQ6 can stop toggling while other DQ pins are still invalid and a subsequent read of the device is valid. See Figure 18 for the toggle-bit timing diagram.



---

### toggle bit (DQ6) (continued)

In instances where program operation is issued to a protected sector, toggle bit (DQ6) toggles for approximately 2  $\mu$ s, after which it reverts back to read mode. On the other hand, if an erase operation is attempted on protected sectors, DQ6 toggles for approximately 100  $\mu$ s, then returns to read mode. Both instances do not alter the contents of the protected sectors.

### exceed time limit (DQ5)

The program and erase operations use an internal-pulse counter to limit the number of pulses applied. If the pulse-count limit is exceeded, DQ5 is set to a logic-high data state. This indicates that the program or erase operation has failed. DQ7 does not change from complemented data to true data and DQ6 does not stop toggling when read. To continue operation, the device must be reset.

The exceed-time-limit condition occurs when attempting to program a logic-high state into a bit that has been programmed previously to a logic low. Only an erase operation can change bits from logic low to logic high. After reset, the device is functional and can be erased and reprogrammed.

### sector-load-timer (DQ3)

The sector-load-timer status bit, DQ3, is used to determine whether the time to load additional sector addresses has expired. This indicates that another sector-erase command sequence can be issued. If DQ3 is at a logic high, it indicates that the delay has expired and attempts to issue additional sector-erase commands are ignored. See the sector-erase command section for a description.

The data-polling and toggle bit are valid during the 50- $\mu$ s time delay and can be used to determine if a valid sector-erase command has been issued. To ensure additional sector-erase commands have been accepted, the status of DQ3 should be read before and after each additional sector-erase command. If DQ3 is at a logic low on both reads, the additional sector-erase command was accepted.

### toggle bit 2 (DQ2)

The state of DQ2 determines whether the device is in algorithmic-erase mode or erase-suspend mode. DQ2 toggles if successive reads are issued to the erasing or erase-suspended sector, assuming in case of the latter that the device is in erase-suspend-read mode. It also toggles when DQ5 becomes a logic high due to the timer-exceed limit, and reads are issued to the failed sector. DQ2 does not toggle in any other sector due to DQ5 failure. When the device is in erase-suspend-program mode, successive reads from the non-erase-suspended sector causes a logic high on DQ2.

### hardware-reset bit ( $\overline{\text{RESET}}$ )

When the  $\overline{\text{RESET}}$  pin is driven to a logic low, it forces the device out of the currently active mode and into a reset state. It also avoids bus contention by placing the outputs into the high-impedance state for the duration of the  $\overline{\text{RESET}}$  pulse.

During any operation, if  $\overline{\text{RESET}}$  is asserted to logic low, the on-going operation is terminated and it can take from 1  $\mu$ s– to 20  $\mu$ s to sense reset completion; or the user can allow a maximum reset completion time of 20  $\mu$ s.

The  $\overline{\text{RESET}}$  pin also can be used to drive the device into deep power-down (standby) mode by applying  $V_{SS} \pm 0.3$  V to it.  $I_{CC4}$  reads  $<1$   $\mu$ A typical, and 15  $\mu$ A maximum for CMOS inputs. Standby mode can be entered anytime, regardless of the condition on  $\overline{\text{CE}}$ .

Asserting  $\overline{\text{RESET}}$  during program or erase can leave erroneous data in the address locations. These locations need to be updated after the device resumes normal operations.

# TMS29F002RT, TMS29F002RB

## 262144 BY 8-BIT

### FLASH MEMORIES

SMJS849B – MARCH 1997 – REVISED JUNE 1998

---

#### temporary hardware-sector unprotect feature

This feature temporarily enables both programming and erase operations on any combination of one to seven sectors that were previously protected. This feature is enabled using high voltage  $V_{ID}$  (11.5 V to 12.5 V) on the RESET pin, using standard command sequences.

Normally, the device is delivered with all sectors unprotected.

#### sector-protect programming

The sector-protect programming mode is activated when A6, A0, and  $\overline{CE}$  are at  $V_{IL}$ , and address pin A9 and control pin  $\overline{OE}$  are forced to  $V_{ID}$ . Address pin A1 is set to  $V_{IH}$ . The sector-select address pins A13 – A17 are used to select the sector to be protected. Address pins A0–A12 and the I/O pins must be stable and can be either  $V_{IL}$  or  $V_{IH}$ . Once the addresses are stable,  $\overline{WE}$  is pulsed low for 100  $\mu$ s, causing programming to begin on the falling edge of  $\overline{WE}$  and to terminate on the rising edge of  $\overline{WE}$ . Figure 6 is a flow chart of the sector-protect algorithm and Figure 19 shows a timing diagram of the sector-protect operation.

Commands to program or erase a protected sector do not change the data contained in the sector. Attempts to program and erase a protected sector cause the data-polling bit (DQ7) and toggle bit (DQ6) to operate from 2  $\mu$ s to 100  $\mu$ s and then return to valid data.

#### sector-protect verify

Verification of the sector-protection programming is activated when  $\overline{WE} = V_{IH}$ ,  $\overline{OE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ , and address pin A9 =  $V_{ID}$ . Address pins A0 and A6 are set to  $V_{IL}$ , and A1 is set to  $V_{IH}$ . Sector-address pins A13–A17 select the sector that is to be verified. The other addresses can be  $V_{IH}$  or  $V_{IL}$ . If the sector that was selected is protected, the DQs output 01h. If the sector is not protected, the DQs output 00h.

Sector-protect verify can also be read using the algorithm-selection command. After issuing the three-bus-cycle command sequence, the sector-protection status can be read on DQ0. The sector address pins A13–A17 select the sector to be verified when address pins A0 =  $V_{IL}$ , A1 =  $V_{IH}$ , and A6 =  $V_{IL}$  are set. The remaining addresses are set to  $V_{IL}$ . If the sector selected is protected, DQ0 outputs a logic-high state. If the sector selected is not protected, DQ0 outputs a logic-low state. This mode remains in effect until another valid command sequence is written to the device. Figure 6 is a flow chart of the sector-protect algorithm and Figure 19 shows a timing diagram of the sector-protect operation.

#### sector unprotect

Prior to sector unprotect, all sectors must be protected using the sector-protect programming mode. The sector unprotect is activated when address pin A9 and control pin  $\overline{OE}$  are forced to  $V_{ID}$ . Address pins A1 and A6 are set to  $V_{IH}$  while  $\overline{CE}$  and A0 are set to  $V_{IL}$ . Sector-select address pins A13–A17 can be  $V_{IL}$  or  $V_{IH}$ . All sectors are unprotected in parallel and once the inputs are stable,  $\overline{WE}$  is pulsed low for 10 ms, causing the unprotect operation to begin on the falling edge of  $\overline{WE}$  and to terminate on the rising edge of  $\overline{WE}$ . Figure 7 is a flow chart of the sector-unprotect algorithm and Figure 20 shows a timing diagram of the sector-unprotect operation.

#### sector-unprotect verify

Verification of the sector unprotect is accomplished when  $\overline{WE} = V_{IH}$ ,  $\overline{OE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ , and A9 =  $V_{ID}$ , and then select the sector to be verified. Address pins A1 and A6 are set to  $V_{IH}$ , and A0 is set to  $V_{IL}$ . The other addresses can be  $V_{IH}$  or  $V_{IL}$ . If the sector selected is protected, the DQs output 01h. If the sector is not protected, the DQs output 00h. Sector unprotect can also be read using the algorithm-selection command.

#### low $V_{CC}$ write lockout

During power-up and power-down operations, write cycles are locked out for  $V_{CC}$  less than  $V_{LKO}$ . If  $V_{CC} < V_{LKO}$ , the command input is disabled and the device is reset to the read mode. On power up, if  $\overline{CE} = V_{IL}$ ,  $\overline{WE} = V_{IL}$ , and  $\overline{OE} = V_{IH}$ , the device does not accept commands on the rising edge of  $\overline{WE}$ . The device automatically powers up in the read mode.



**glitching**

Pulses of less than 5 ns (typical) on  $\overline{OE}$ ,  $\overline{WE}$ , or  $\overline{CE}$  do not issue a write cycle.

**power supply considerations**

Each device should have a 0.1- $\mu$ F ceramic capacitor connected between  $V_{CC}$  and  $V_{SS}$  to suppress circuit noise. Printed circuit traces to  $V_{CC}$  should be appropriate to handle the current demand and minimize inductance.

**flow charts**

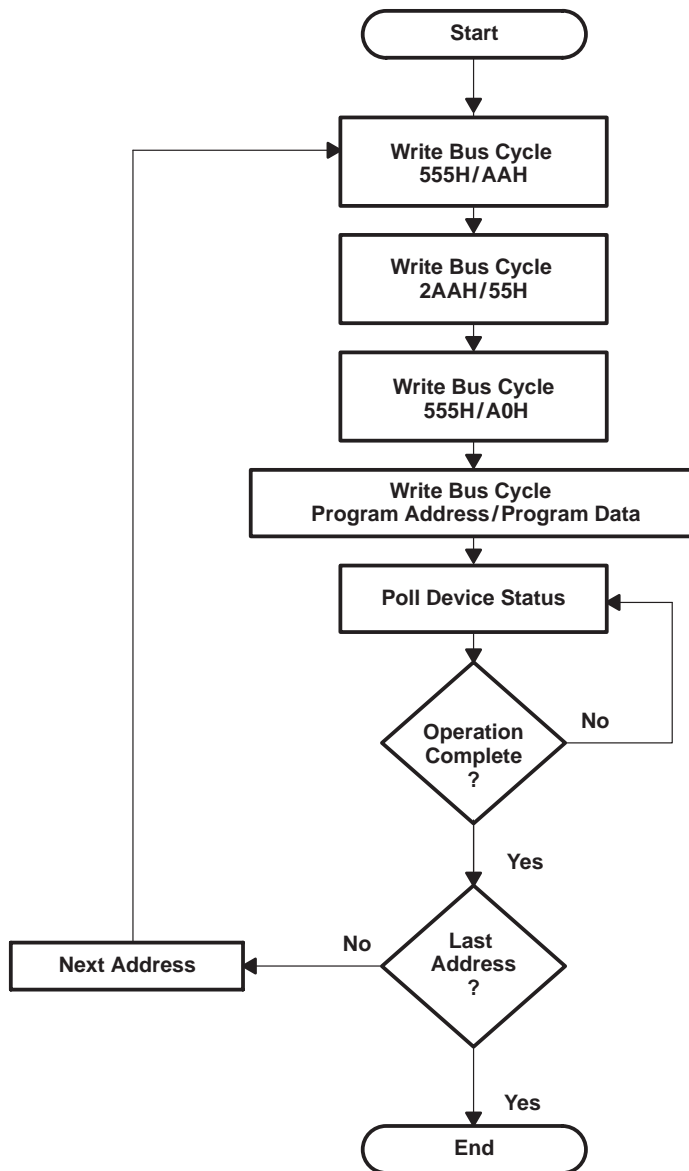


Figure 1. Program Algorithm

flow charts (continued)

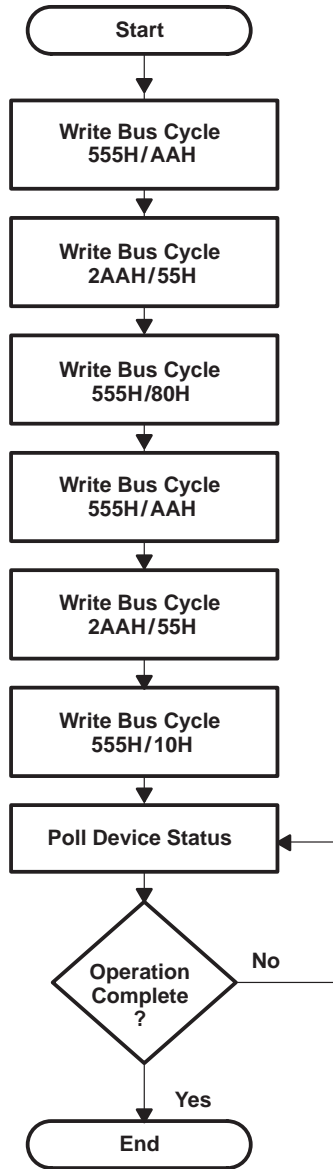


Figure 2. Chip-Erase Algorithm



flow charts (continued)

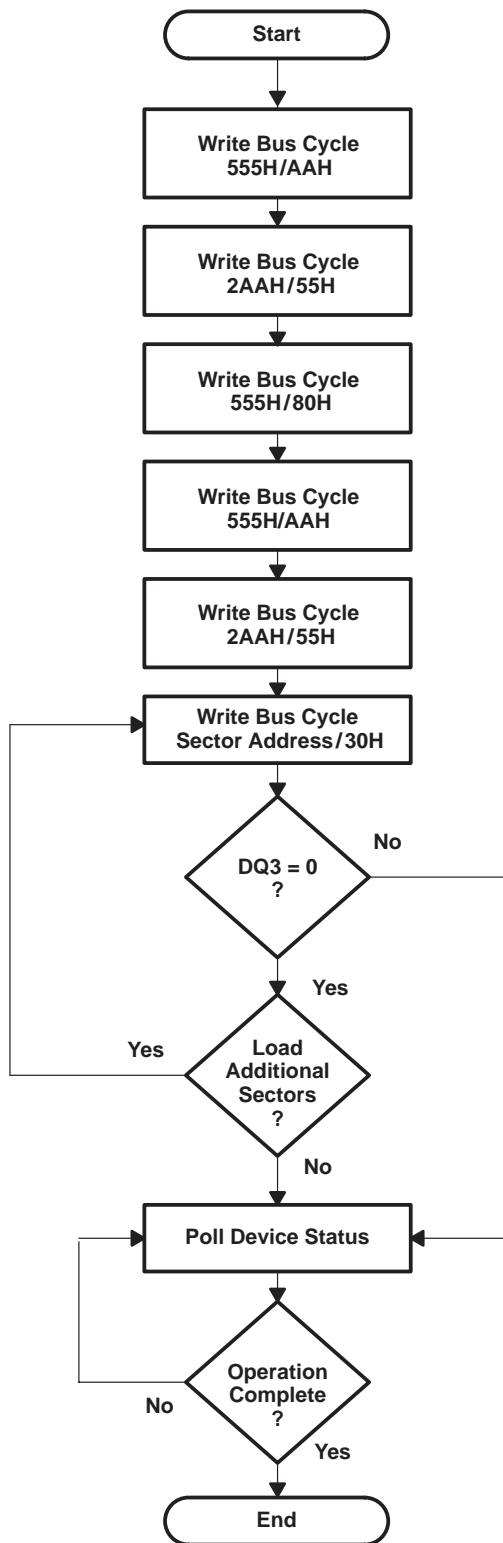
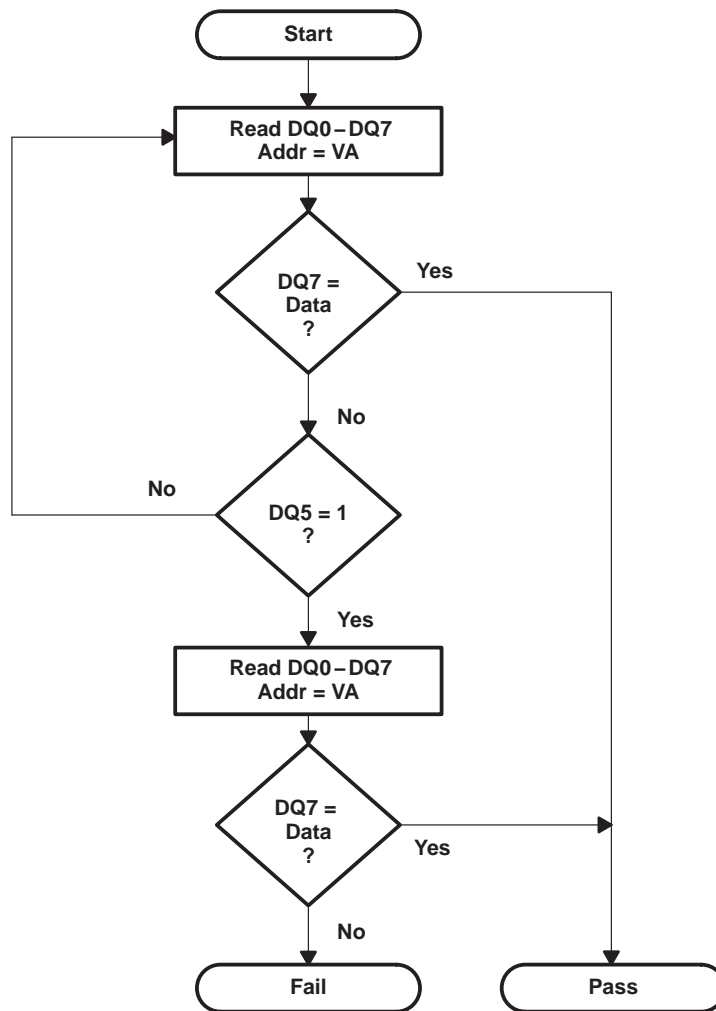


Figure 3. Sector-Erase Algorithm

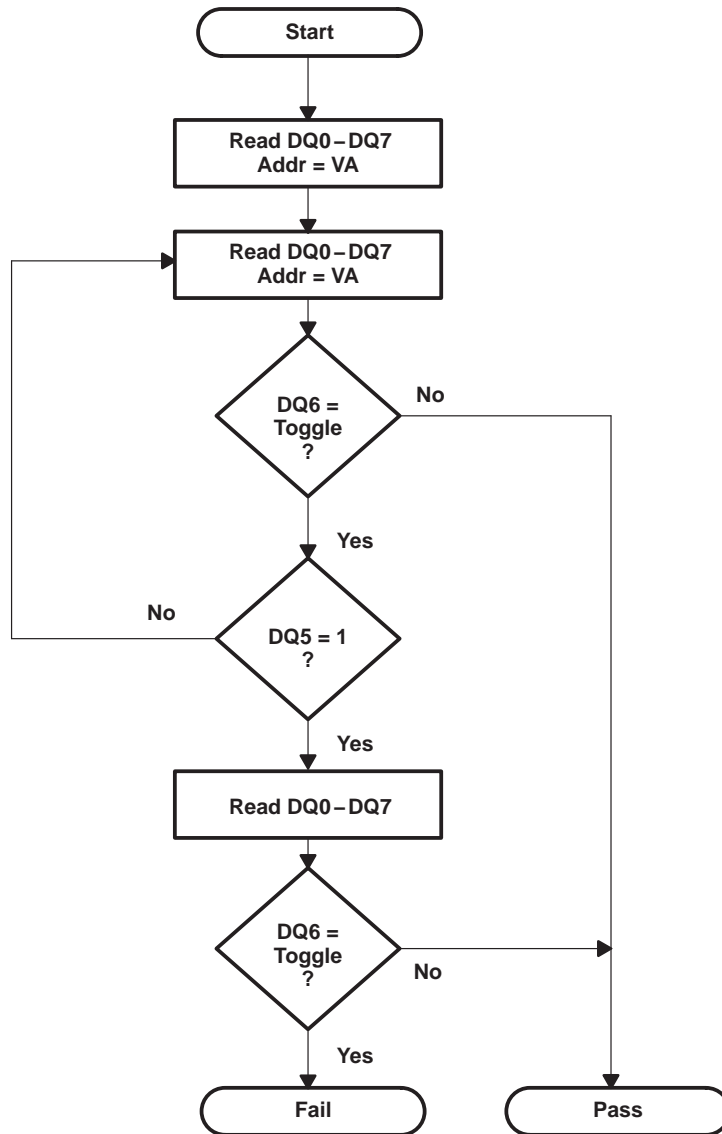
flow charts (continued)



- NOTES: A. Polling status bits DQ7 and DQ5 may change asynchronously.  
Read DQ7 after DQ5 changes states.  
B. VA = Program address for byte-programming  
= Selected sector address for sector erase  
= Any valid address for chip erase

Figure 4. Data-Polling Algorithm

flow charts (continued)



- NOTES: A. Polling status bits DQ6 and DQ5 can change asynchronously. Read DQ6 after DQ5 changes states.  
 B. After an erase operation is complete, DQ6 stops toggling at a logic high state.

Figure 5. Toggle-Bit Algorithm

flow charts (continued)

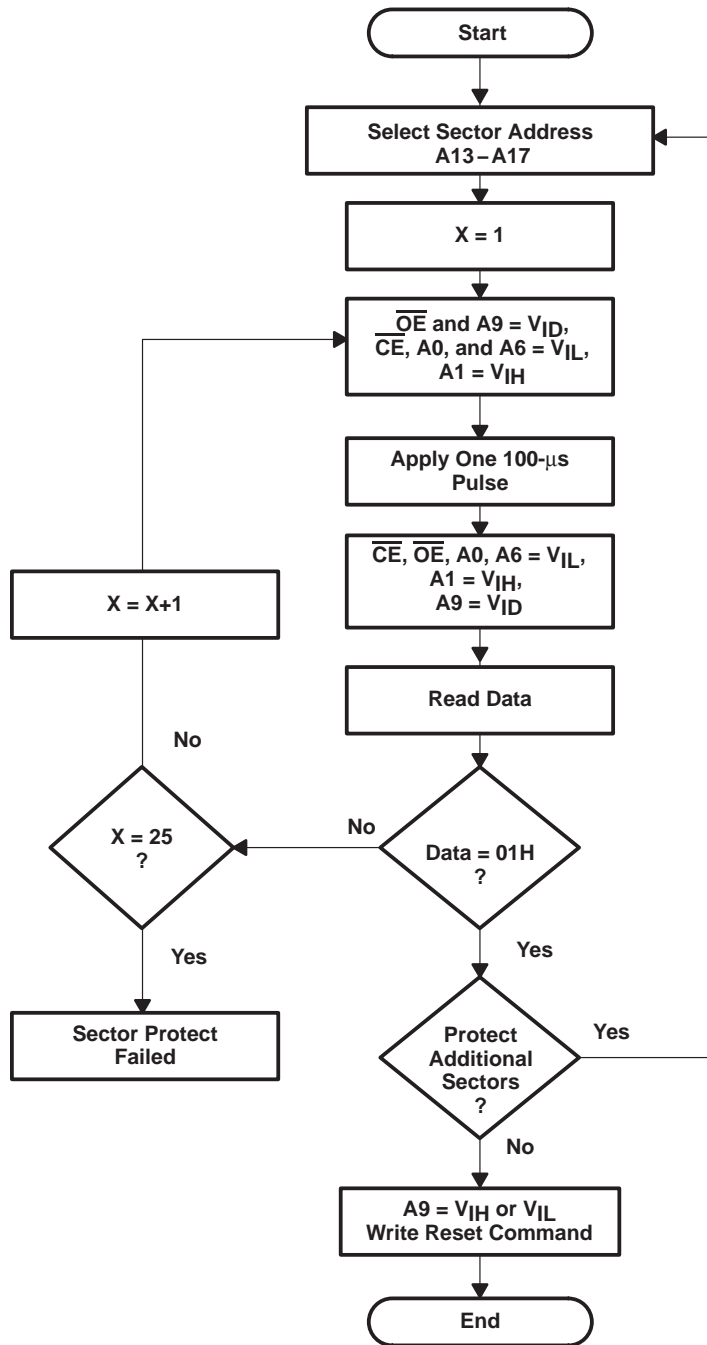


Figure 6. Sector-Protect Algorithm

flow charts (continued)

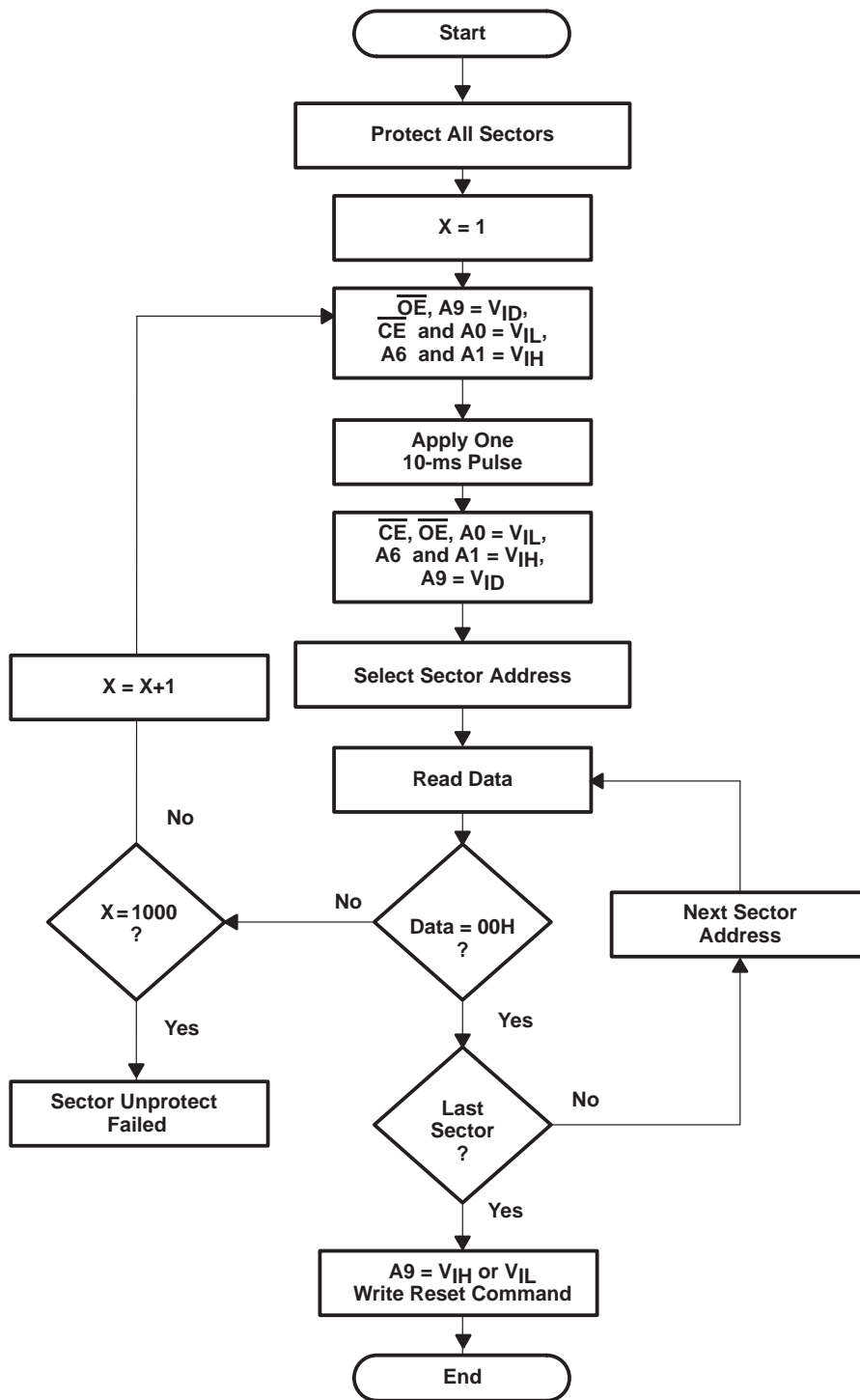
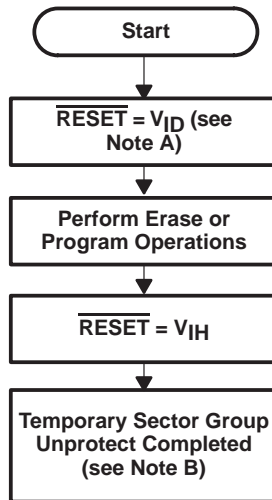


Figure 7. Sector-Unprotect Algorithm

flow charts (continued)



- NOTES: A. All protected sectors unprotected  
B. All previously protected sectors are protected once again

**Figure 8. Temporary Sector-Unprotect Algorithm**

**absolute maximum ratings over ambient temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ (see Note 1)	–0.6 V to 7 V
Input voltage range: All inputs except A9, $\overline{CE}$ , $\overline{OE}$ (see Note 2)	–0.6 V to $V_{CC} + 1$ V
A9, $\overline{CE}$ , $\overline{OE}$	–0.6 V to 13.5 V
Output voltage range (see Note 3)	–0.6 V to $V_{CC} + 1$ V
Ambient temperature range during read/erase/program, $T_A$	
Extended	–40°C to 85°C
Commercial	0°C to 70°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to  $V_{SS}$ .  
 2. The voltage on any input pin can undershoot to –2 V for periods less than 20 ns (see Figure 10).  
 3. The voltage on any output pin can overshoot to  $V_{CC} + 2$  V for periods less than 20 ns (see Figure 11).

**recommended operating conditions**

		MIN	MAX	UNIT	
$V_{CC}$	Supply voltage	4.5	5.5	V	
$V_{IH}$	High-level dc input voltage	TTL	2	$V_{CC}+0.5$	V
		CMOS	$0.7 * V_{CC}$	$V_{CC}+0.5$	
$V_{IL}$	Low-level dc input voltage	TTL	–0.5	0.8	V
		CMOS	–0.5	0.2	
$V_{ID}$	Algorithm-selection and sector-protect input voltage	11.5	12.5	V	
$V_{LKO}$	Low $V_{CC}$ lock-out voltage (see Note 4)	3.2	4.2	V	
$T_A$	Ambient temperature	Extended	–40	85	°C
		Commercial	0	70	

NOTE 4:  $T_A = 25^\circ\text{C}$

**TMS29F002RT, TMS29F002RB**  
**262144 BY 8-BIT**  
**FLASH MEMORIES**

SMJS849B – MARCH 1997 – REVISED JUNE 1998

**electrical characteristics over recommended ranges of supply voltage and ambient temperature**

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	TTL-input level	V <sub>CC</sub> = V <sub>CC</sub> MIN, I <sub>OH</sub> = -2.5 mA	2.4 V	V
		CMOS-input level	V <sub>CC</sub> = V <sub>CC</sub> MIN, I <sub>OH</sub> = -100 μA	V <sub>CC</sub> - 0.4	
		CMOS-input level	V <sub>CC</sub> = V <sub>CC</sub> MIN, I <sub>OH</sub> = -2.5 mA	0.85 * V <sub>CC</sub>	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = V <sub>CC</sub> MIN, I <sub>OL</sub> = 5.8 mA		0.45	V
I <sub>I</sub>	Input current (leakage)	V <sub>CC</sub> = V <sub>CC</sub> MAX, V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>		±1	μA
I <sub>O</sub>	Output current (leakage)	V <sub>O</sub> = V <sub>SS</sub> to V <sub>CC</sub> , $\overline{CE}$ = V <sub>IH</sub>		±1	μA
I <sub>ID</sub>	High-voltage current (standby)	A9 or $\overline{CE}$ or $\overline{OE}$ = V <sub>ID</sub> MAX		35	μA
I <sub>CC1</sub>	V <sub>CC</sub> supply current (standby)	TTL-input level	$\overline{CE}$ = V <sub>IH</sub> , V <sub>CC</sub> = V <sub>CC</sub> MAX	1	mA
		CMOS-input level	$\overline{CE}$ = V <sub>CC</sub> ± 0.2, V <sub>CC</sub> = V <sub>CC</sub> MAX	100	μA
I <sub>CC2</sub>	V <sub>CC</sub> supply current (see Notes 5 and 6)	$\overline{CE}$ = V <sub>IL</sub> , $\overline{OE}$ = V <sub>IH</sub>		40	mA
I <sub>CC3</sub>	V <sub>CC</sub> supply current (see Note 7)	$\overline{CE}$ = V <sub>IL</sub> , $\overline{OE}$ = V <sub>IH</sub>		60	mA
I <sub>CC4</sub>	V <sub>CC</sub> supply current (standby during reset)	V <sub>CC</sub> = V <sub>CC</sub> MAX, RESET = V <sub>SS</sub> ± 0.3 V		15	μA
I <sub>CC5</sub>	Automatic sleep mode (see Notes 6 and 8)	V <sub>IH</sub> = V <sub>CC</sub> ± 0.3 V, V <sub>IL</sub> = V <sub>SS</sub> ± 0.3 V		100	μA

- NOTES: 5. I<sub>CC</sub> current in the read mode, switching at 6 MHz.  
6. I<sub>OUT</sub> = 0 mA  
7. I<sub>CC</sub> current while erase or program operation is in progress.  
8. Automatic sleep mode is entered when addresses remain stable for 300 ns.

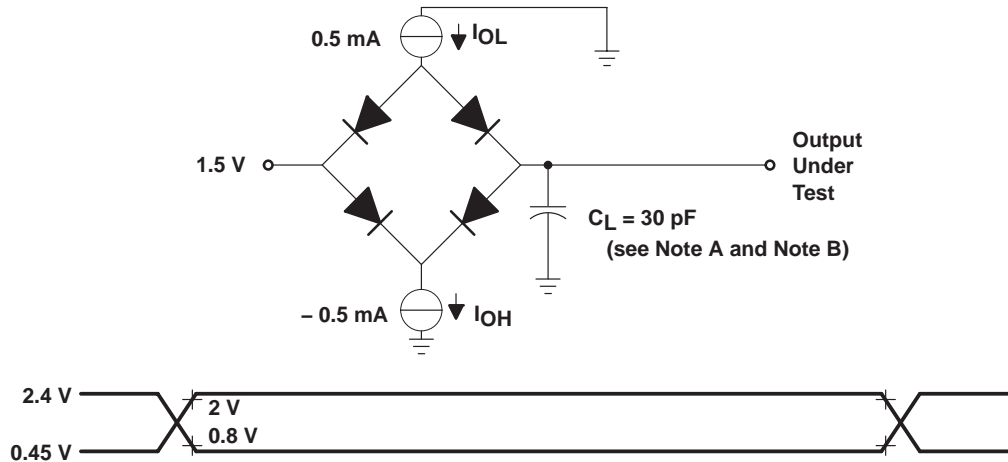
**capacitance over recommended ranges of supply voltage and ambient temperature**

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
C <sub>i1</sub>	Input capacitance (All inputs except A9, $\overline{CE}$ , $\overline{OE}$ )	V <sub>I</sub> = 0 V, f = 1 MHz		7.5	pF
C <sub>i2</sub>	Input capacitance (A9, $\overline{CE}$ , $\overline{OE}$ )	V <sub>I</sub> = 0 V, f = 1 MHz		9	pF
C <sub>o</sub>	Output capacitance	V <sub>O</sub> = 0 V, f = 1 MHz		12	pF





PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and fixture capacitance.  
 B. The ac testing inputs are driven at 2.4 V for logic high and 0.45 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low on both inputs and outputs. Each device should have a 0.1- $\mu\text{F}$  ceramic capacitor connected between  $V_{CC}$  and  $V_{SS}$  as closely as possible to the device pins.

Figure 9. AC Test Output Load Circuit

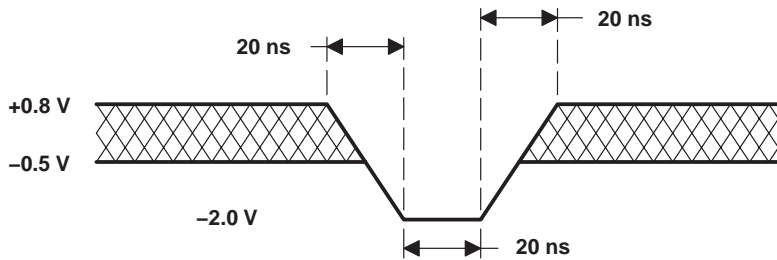


Figure 10. Maximum Negative Overshoot Waveform

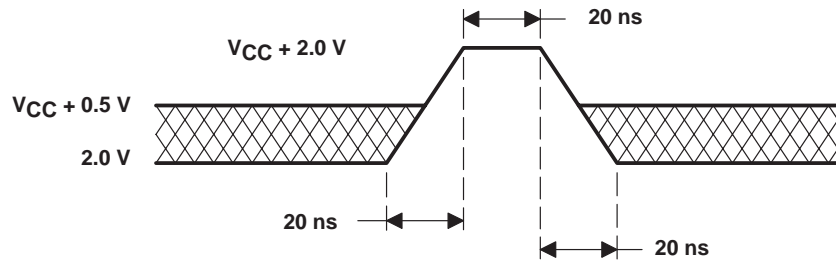


Figure 11. Maximum Positive Overshoot Waveform

**TMS29F002RT, TMS29F002RB**  
**262144 BY 8-BIT**  
**FLASH MEMORIES**

SMJS849B – MARCH 1997 – REVISED JUNE 1998

**PARAMETER MEASUREMENT INFORMATION**

switching characteristics over recommended ranges of supply voltage and ambient temperature, read-only operation (see Figure 12, Figure 17, Figure 18, Figure 19, and Figure 20)

PARAMETER	ALTERNATE SYMBOL	'29F002R-90		'29F002R-100		'29F002R-120		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(R)}$ Cycle time, read	$t_{AVAV}$	90		100		120		ns
$t_{a(A)}$ Access time, address	$t_{AVQV}$		90		100		120	ns
$t_{a(E)}$ Access time, $\overline{CE}$	$t_{ELQV}$		90		100		120	ns
$t_{a(G)}$ Access time, $\overline{OE}$	$t_{GLQV}$		35		45		50	ns
$t_{dis(E)}$ Disable time, $\overline{CE}$ to high impedance	$t_{EHQZ}$		20		25		30	ns
$t_{dis(G)}$ Disable time, $\overline{OE}$ to high impedance	$t_{GHQZ}$		20		25		30	ns
$t_{en(E)}$ Enable time, $\overline{CE}$ to low impedance	$t_{ELQX}$	0		0		0		ns
$t_{en(G)}$ Enable time, $\overline{OE}$ to low impedance	$t_{GLQX}$	0		0		0		ns
$t_{h(D)}$ Hold time, output from address $\overline{CE}$ or $\overline{OE}$ change	$t_{AXQX}$	0		0		0		ns



switching characteristics over recommended ranges of supply voltage and ambient temperature, controlled by  $\overline{WE}$  (see Figure 13, Figure 15, Figure 16, Figure 17, Figure 18, Figure 19, Figure 20, and Figure 21)

PARAMETER	ALTERNATE SYMBOL	'29F002R-90			'29F002R-100			'29F002R-120			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(W)}$ Cycle time, write	$t_{AVAV}$	90			100			120			ns
$t_{su(A)}$ Setup time, address	$t_{AVWL}$	0			0			0			ns
$t_{h(A)}$ Hold time, address	$t_{WLAX}$	45			50			50			ns
$t_{su(D)}$ Setup time, data	$t_{DVWH}$	45			50			50			ns
$t_{h(D)}$ Hold time, data valid after $\overline{WE}$ high	$t_{WHDX}$	0			0			0			ns
$t_{su(E)}$ Setup time, $\overline{CE}$	$t_{ELWL}$	0			0			0			ns
$t_{h(E)}$ Hold time, $\overline{WE}$	$t_{WHEH}$	0			0			0			ns
$t_{h(E)}$ Hold time, $\overline{CE}$	$t_{EHWH}$	0			0			0			ns
$t_{w(WL)}$ Pulse duration, $\overline{WE}$ low	$t_{WLWH1}$	45			45			50			ns
$t_{w(WH)}$ Pulse duration, $\overline{WE}$ high	$t_{WHWL}$	20			20			20			ns
$t_{rec(R)}$ Recovery time, read before write	$t_{GHWL}$	0			0			0			ns
Hold time, $\overline{OE}$ read	$t_{WHGL1}$	0			0			0			ns
Hold time, $\overline{OE}$ toggle, data	$t_{WHGL2}$	10			10			10			ns
Setup time, $V_{CC}$	$t_{VCEL}$	50			50			50			$\mu$ s
Transition time, $V_{ID}$ (see Notes 9 and 10)	$t_{HVT}$	4			4			4			$\mu$ s
$t_{RSP}$ Reset setup time for temporary sector unprotect		4			4			4			$\mu$ s
Pulse duration, $\overline{WE}$ low (see Note 9)	$t_{WLWH2}$	100			100			100			$\mu$ s
Pulse duration, $\overline{WE}$ low (see Note 10)	$t_{WLWH3}$	10			10			10			ms
Setup time, $\overline{CE} V_{ID}$ to $\overline{WE}$ (see Note 10)	$t_{EHVWL}$	4			4			4			$\mu$ s
Setup time, $\overline{OE} V_{ID}$ to $\overline{WE}$ (see Notes 9 and 10)	$t_{GHVWL}$	4			4			4			$\mu$ s
$t_{c(W)PR}$ Cycle time, programming operation	$t_{WHWH1}$		7			7			7		$\mu$ s
$t_{c(W)ER}$ Cycle time, sector-erase operation	$t_{WHWH2}$		7			7			7		s
Cycle time, chip-erase operation	$t_{WHWH3}$		7	30		7	30		7	30	s

NOTES: 9. Sector-protect timing  
10. Sector-unprotect timing

**TMS29F002RT, TMS29F002RB**  
**262144 BY 8-BIT**  
**FLASH MEMORIES**

SMJS849B – MARCH 1997 – REVISED JUNE 1998

switching characteristics over recommended ranges of supply voltage and ambient temperature, controlled by CE (see Figure 14)

PARAMETER	ALTERNATE SYMBOL	'29F002R-90			'29F002R-100			'29F002R-120			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(W)}$ Cycle time, write	$t_{AVAV}$	90			100			120			ns
Cycle time, sector-erase operation	$t_{EHEH2}$	1			1			1			s
Cycle time, chip-erase operation	$t_{EHEH3}$		7	60		7	60		7	60	s
$t_h(A)$ Hold time, address	$t_{ELAX}$	45			50			50			ns
$t_h(D)$ Hold time, data	$t_{EHDX}$	45			50			50			ns
$t_h(W)$ Hold time, $\overline{WE}$	$t_{EHWH}$	0			0			0			ns
$t_h(C)$ Hold time, $\overline{OE}$ read	$t_{EHGL1}$	0			0			0			ns
Hold time, $\overline{OE}$ toggle, data	$t_{EHGL2}$	10			10			10			ns
$t_w(EL)$ Pulse duration, $\overline{CE}$ low	$t_{ELEH1}$	45			45			45			ns
$t_w(EH)$ Pulse duration, $\overline{CE}$ high	$t_{EHEL}$	20			20			20			ns
$t_{rec(R)}$ Recovery time, read before write	$t_{GHLE}$	0			0			0			ns
$t_{su(A)}$ Setup time, address	$t_{AVEL}$	0			0			0			ns
$t_{su(D)}$ Setup time, data	$t_{DVEH}$	45			50			50			ns
$t_{su(W)}$ Setup time, $\overline{WE}$	$t_{WLEL}$	0			0			0			ns
Setup time, $\overline{OE}$	$t_{GLEL}$	0			0			0			ns
Programming operation	$t_{EHEH1}$		7			7			7		$\mu$ s

**erase and program performance†**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sector-erase time	Excludes 00H programming prior to erasure		1‡	15§	s
Program time	Excludes system-level overhead	9	9	3600§	µs
Chip-programming time	Excludes system-level overhead		6‡	50§	s
Erase/program cycles			10 000	100 000	cycles

† The internal algorithms allow for 2.5-ms/byte program time. DQ5 = 1 only after a byte takes the theoretical maximum time to program. A minimal number of bytes can require significantly more programming pulses than the typical byte. The majority of the bytes program within one or two pulses. This is demonstrated by the typical and maximum programming time listed above.

‡ 25°C, 5-V V<sub>CC</sub>, 100 000 cycles, typical pattern

§ Under worst-case conditions: 90°C, 5-V V<sub>CC</sub>, 100 000 cycles

**latchup characteristics (see Note 11)**

PARAMETER	MIN	MAX	UNIT
Input voltage with respect to V <sub>SS</sub> on all pins except I/O pins (including A9 and $\overline{OE}$ )	-1	13	V
Input voltage with respect to V <sub>SS</sub> on all I/O pins	-1	V <sub>CC</sub> + 1	V
Current	-100	100	mA

NOTE 11: Includes all pins except V<sub>CC</sub> test conditions: V<sub>CC</sub> = 5 V, one pin at a time

**pin capacitance, all packages (see Note 12)**

PARAMETER	TEST CONDITIONS	TYP	MAX	UNIT
C <sub>IN</sub> Input capacitance	V <sub>IN</sub> = 0	6	7.5	pF
C <sub>OUT</sub> Output capacitance	V <sub>OUT</sub> = 0	8.5	12	pF
C <sub>IN2</sub> Control pin capacitance	V <sub>IN</sub> = 0	8	10	pF

NOTE 12: Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz

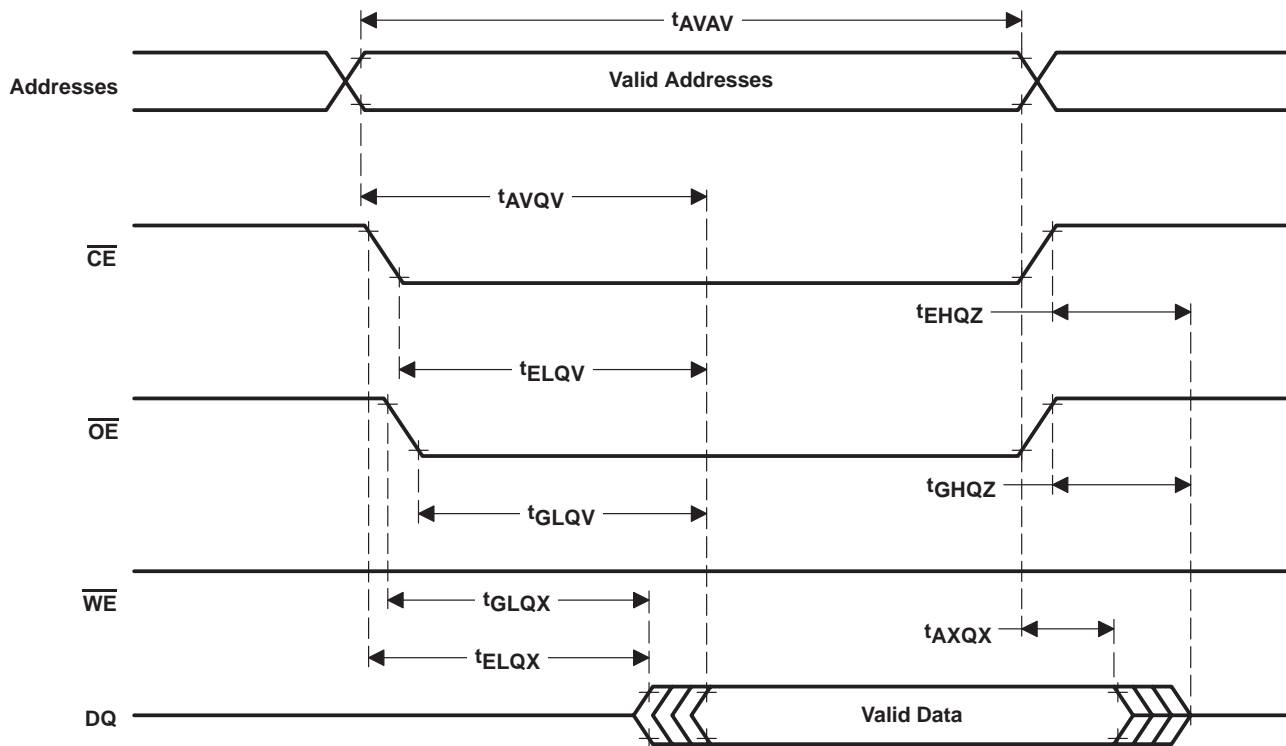
**data retention**

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Minimum pattern data retention time	150°C	10		Years
	125°C	20		

**TMS29F002RT, TMS29F002RB**  
**262144 BY 8-BIT**  
**FLASH MEMORIES**

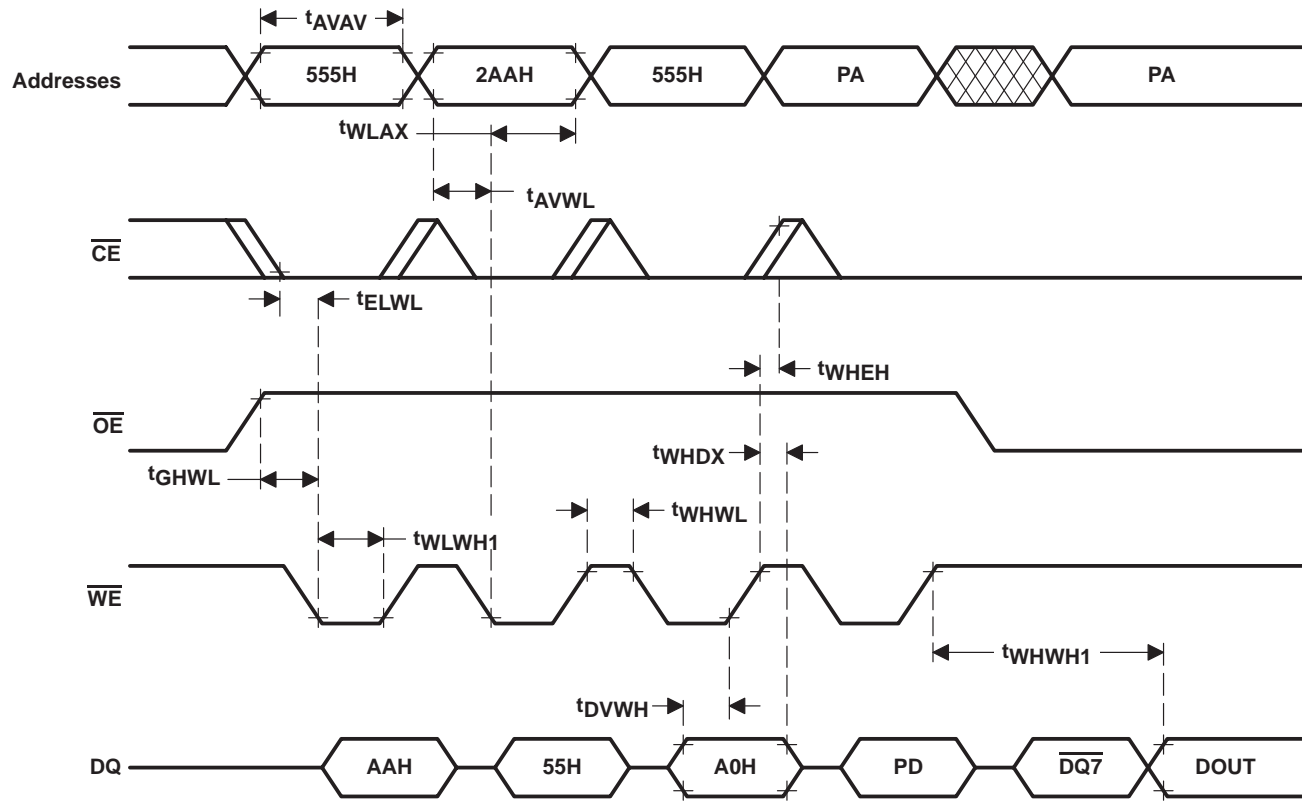
SMJS849B – MARCH 1997 – REVISED JUNE 1998

**read operation**



**Figure 12. AC Waveform for Read Operation**

write operation



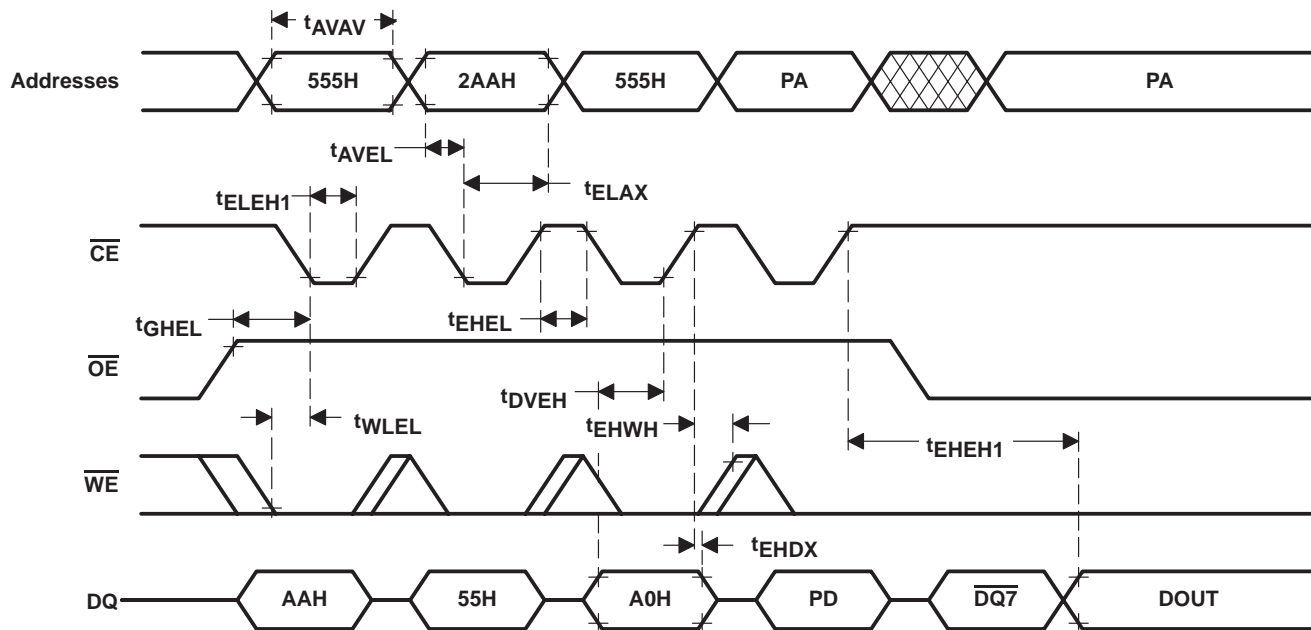
- NOTES: A. PA = Address to be programmed  
 B. PD = Data to be programmed  
 C. DQ7 = Complement of data written to DQ7

Figure 13. AC Waveform for Program Operation

**TMS29F002RT, TMS29F002RB**  
**262144 BY 8-BIT**  
**FLASH MEMORIES**

SMJS849B – MARCH 1997 – REVISED JUNE 1998

**write operation (continued)**

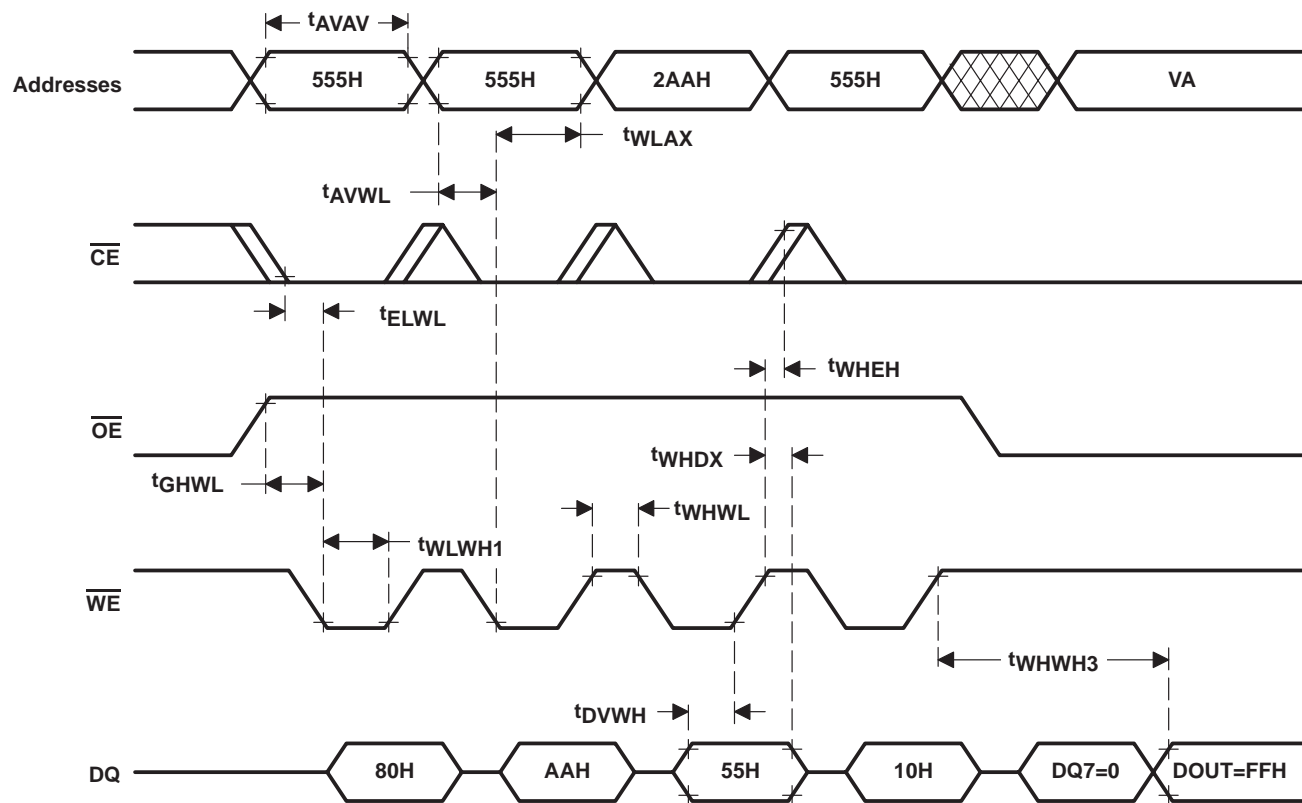


- NOTES: A. PA = Address to be programmed  
 B. PD = Data to be programmed  
 C.  $\overline{DQ7}$  = Complement of data written to DQ7

**Figure 14. AC Waveform for Alternate  $\overline{CE}$ -Controlled Write Operation**



chip-erase operation



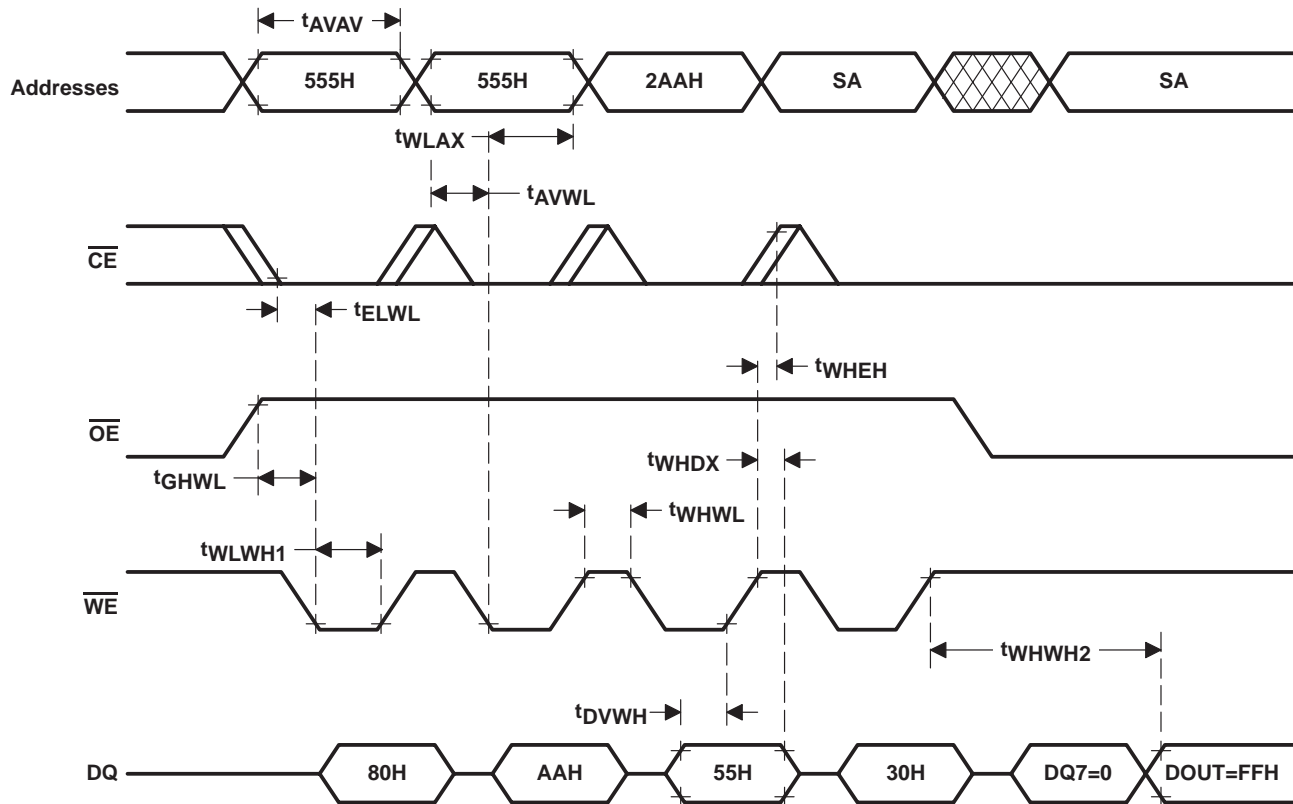
- NOTES: A. VA = any valid address  
 B. Figure details the last four bus cycles in a six-bus-cycle operation.

Figure 15. AC Waveform for Chip-Erase Operation

**TMS29F002RT, TMS29F002RB**  
**262144 BY 8-BIT**  
**FLASH MEMORIES**

SMJS849B – MARCH 1997 – REVISED JUNE 1998

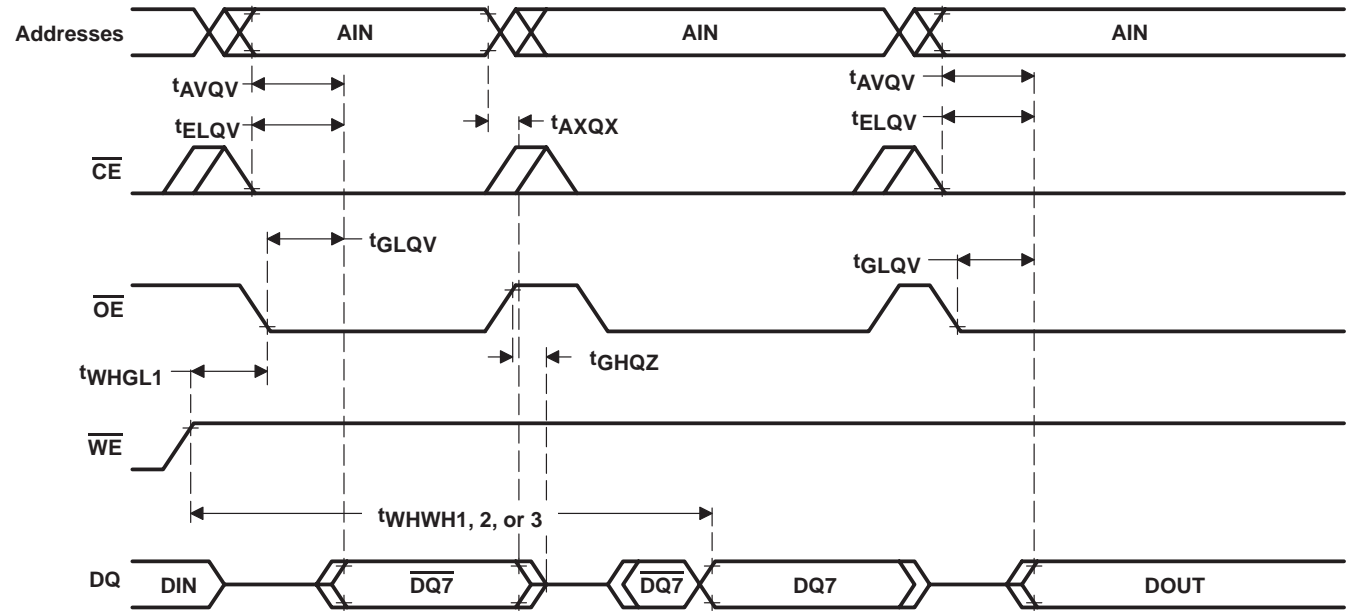
**sector-erase operation**



- NOTES: A. SA = Sector address to be erased  
 B. Figure details the last four bus cycles in a six-bus-cycle operation.

**Figure 16. AC Waveform for Sector-Erase Operation**

data-polling operation



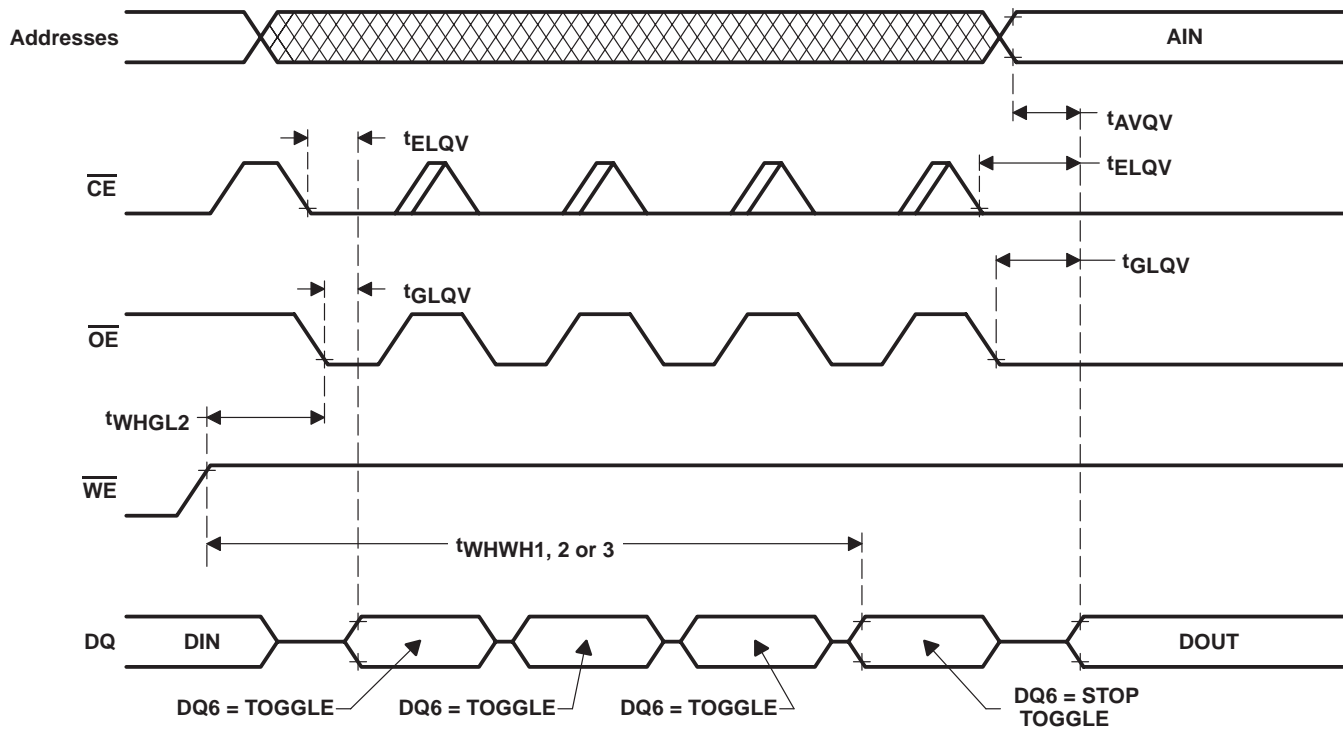
- NOTES: A.  $\overline{\text{DIN}}$  = Last command data written to the device  
 B.  $\overline{\text{DQ7}}$  = Complement of data written to DQ7  
 C. DOUT = Valid data output  
 D. AIN = Valid address for byte-program, sector-erase, or chip-erase operation

Figure 17. AC Waveform for Data-Polling Operation

**TMS29F002RT, TMS29F002RB**  
**262144 BY 8-BIT**  
**FLASH MEMORIES**

SMJS849B – MARCH 1997 – REVISED JUNE 1998

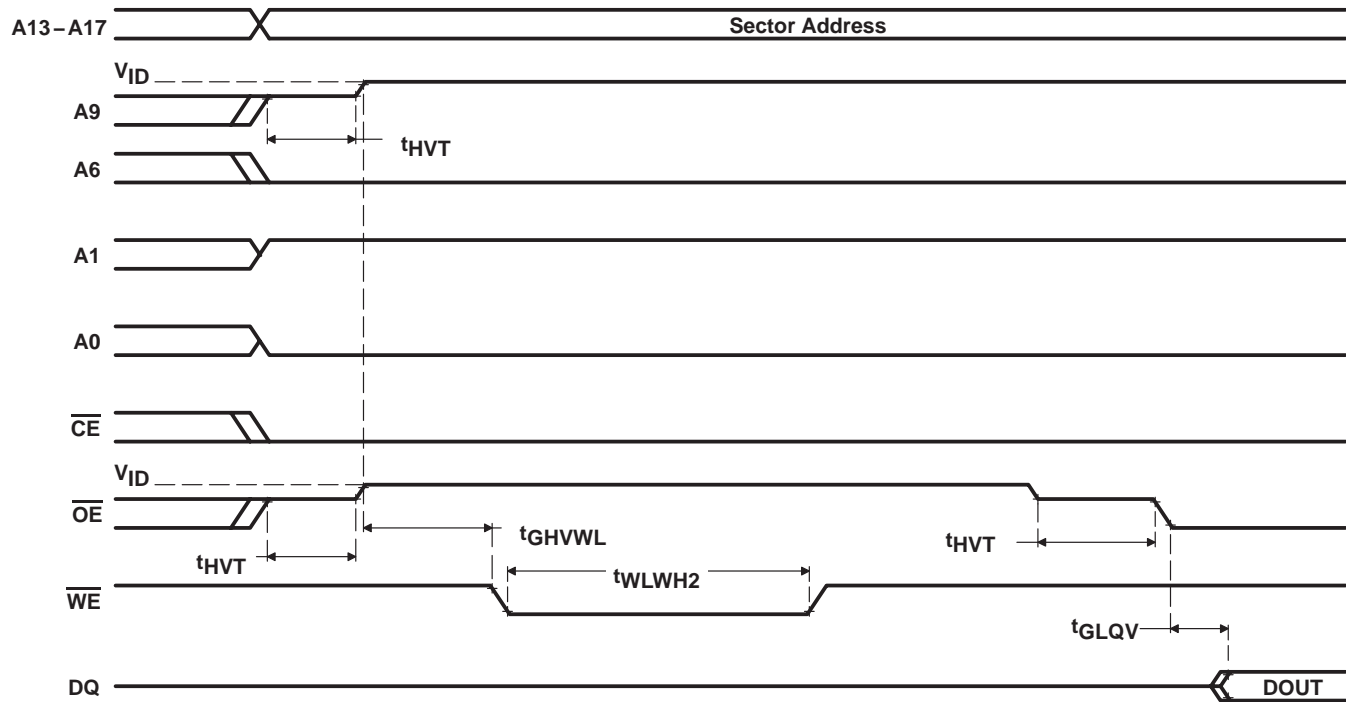
**toggle-bit operation**



- NOTES: A. DIN = Last command data written to the device  
 B. DQ6 = Toggle bit output  
 C. DOUT = Valid data output  
 D. AIN = Valid address for byte-program, sector-erase, or chip-erase operation

**Figure 18. AC Waveforms for Toggle-Bit Operation**

sector-protect operation



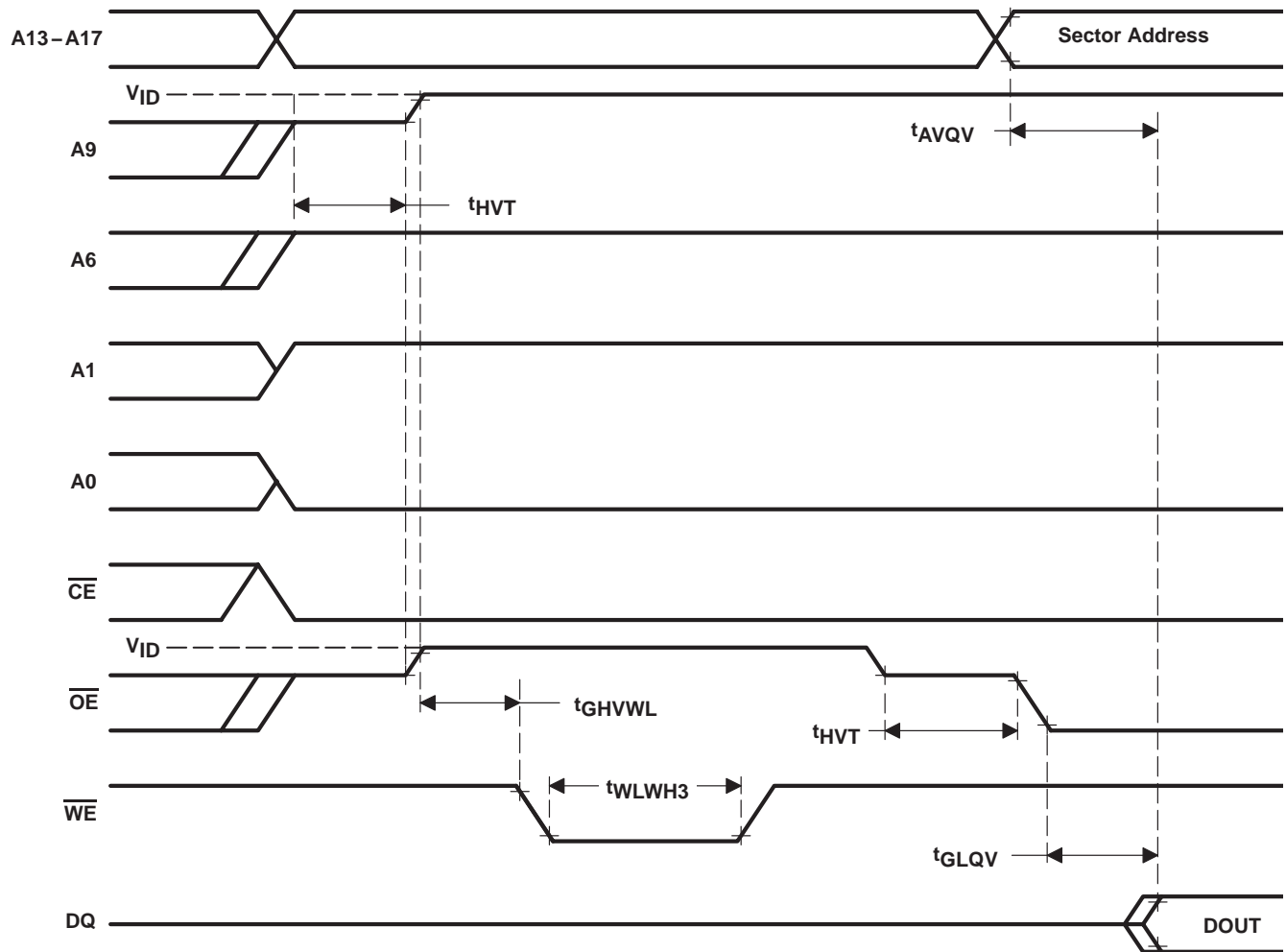
- NOTES: A. DOUT = 00H if the selected sector is not protected,  
 01H if the sector is protected.  
 B.  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

Figure 19. AC Waveform for Sector-Protect Operation

**TMS29F002RT, TMS29F002RB**  
**262144 BY 8-BIT**  
**FLASH MEMORIES**

SMJS849B – MARCH 1997 – REVISED JUNE 1998

**sector-unprotect operation**



- NOTES: A. DOUT = 00H if the selected sector is not protected,  
01H if the sector is protected.  
B.  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

**Figure 20. AC Waveform for Sector-Unprotect Operation**

temporary sector-unprotect operation

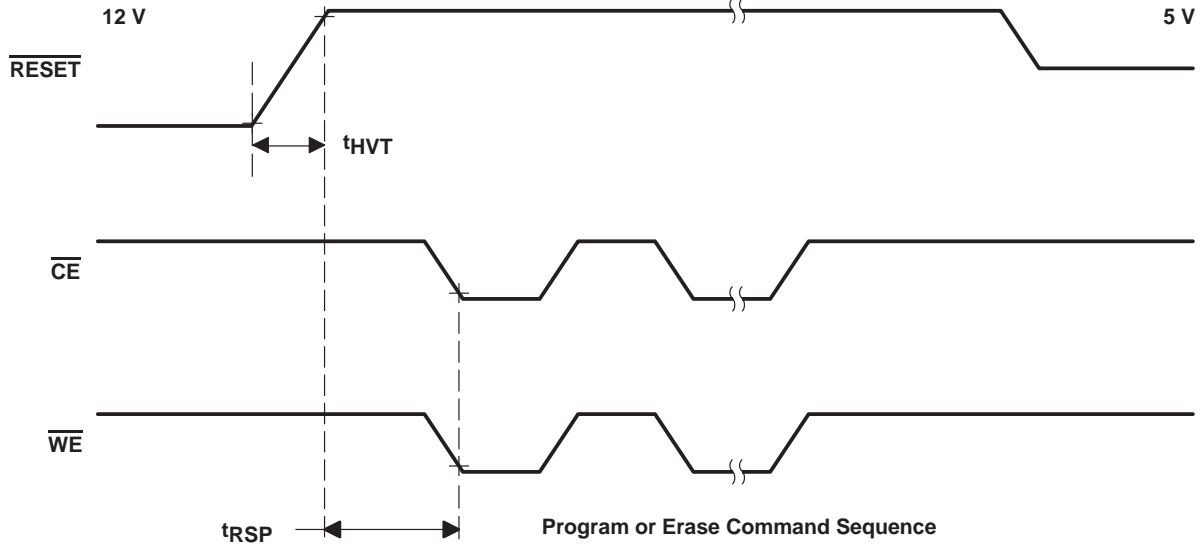


Figure 21. Temporary Sector-Unprotect Timing Diagram

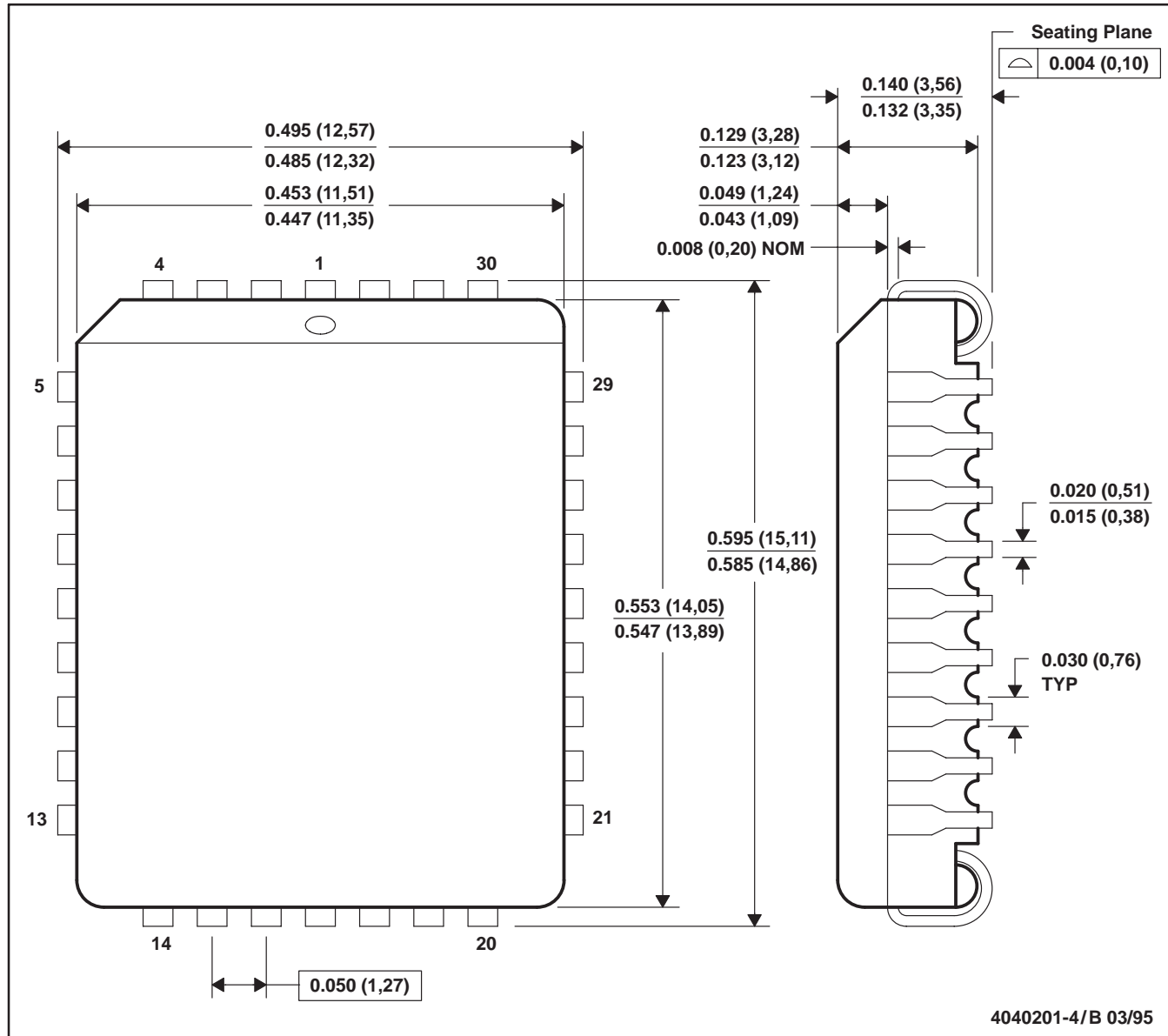
**TMS29F002RT, TMS29F002RB**  
**262144 BY 8-BIT**  
**FLASH MEMORIES**

SMJS849B – MARCH 1997 – REVISED JUNE 1998

**MECHANICAL DATA**

**FM (R-PQCC-J32)**

**PLASTIC J-LEADED CHIP CARRIER**



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-016



## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

### Applications

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2008, Texas Instruments Incorporated