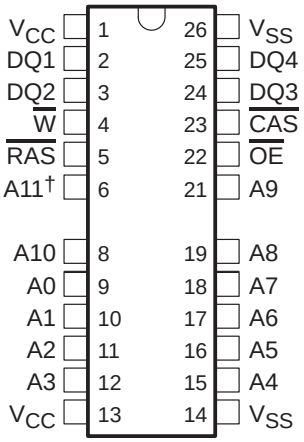
Electrical characteristics for TMS416400/P and TMS417400/P is Production Data. Electrical characteristics for TMS426400/P and TMS427400/P is Product Preview only.

- **Organization . . . 4194304 × 4**
- **Single 5 V Power Supply for TMS41x400/P (±10% Tolerance)**
- **Single 3.3 V Power Supply for TMS42x400/P (±0.3 V Tolerance)**
- **Performance Ranges:**

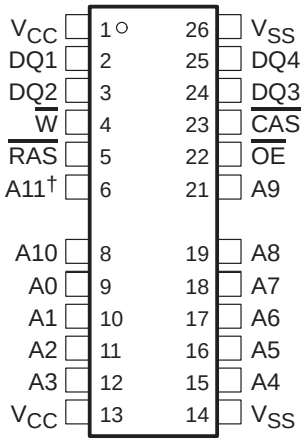
	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR WRITE CYCLE MIN
'4xx400/P-60	60 ns	15 ns	30 ns	110 ns
'4xx400/P-70	70 ns	18 ns	35 ns	130 ns
'4xx400/P-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page-Mode Operation With CAS-Before-RAS (CBR) Refresh**
- **Long Refresh Period and Self-Refresh Option (TMS4xx400P)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **High-Reliability Plastic 24/26-Lead 300-Mil-Wide Surface-Mount Small-Outline J-Lead (SOJ) Package and 24/26-Lead Surface-Mount Thin Small-Outline Package (TSOP)**
- **Operating Free-Air Temperature Range: 0°C to 70°C**
- **EPIC™ (Enhanced Performance Implanted CMOS) Technology**

DJ PACKAGE (TOP VIEW)



DGA PACKAGE (TOP VIEW)



PIN NOMENCLATURE

A0–A11†	Address Inputs
CAS	Column-Address Strobe
DQ1–DQ4	Data In/Data Out
OE	Output Enable
NC	No Internal Connection
RAS	Row-Address Strobe
V_{CC}	5-V or 3.3-V Supply‡
V_{SS}	Ground
W	Write Enable

† A11 is NC for TMS4x7400/P.
‡ See Available Options Table

description

The TMS4xx400 is a set of high-speed, 16777216-bit dynamic random-access memories organized as 4194304 words of 4 bits each. The TMS4xx400P series are high-speed, low-power, self-refresh, 16777216-bit dynamic random-access memories organized as 4194304 words of 4 bits each. The TMS4xx400 and TMS4xx400P employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power.

AVAILABLE OPTIONS

DEVICE	POWER SUPPLY	SELF REFRESH BATTERY BACKUP	REFRESH CYCLES
TMS416400	5 V	—	4096 in 64 ms
TMS416400P	5 V	Yes	4096 in 128 ms
TMS417400	5 V	—	2048 in 32 ms
TMS417400P	5 V	Yes	2048 in 128 ms
TMS426400	3.3 V	—	4096 in 64 ms
TMS426400P	3.3 V	Yes	4096 in 128 ms
TMS427400	3.3 V	—	2048 in 32 ms
TMS427400P	3.3 V	Yes	2048 in 128 ms

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

description (continued)

The TMS4xx400 and TMS4xx400P are each offered in a 24/26-lead plastic surface-mount TSOP (DGA suffix) package and a 24/26-lead plastic surface-mount SOJ (DJ suffix) package. These packages are characterized for operation from 0°C to 70°C.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by t_{RASP}, the maximum $\overline{RAS}$ low time.

Unlike conventional page-mode DRAMs, the column-address buffers in these devices are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses and enables the output. This feature allows the devices to operate at a higher data bandwidth than conventional page-mode parts because data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as enhanced page mode. A valid column address can be presented immediately after row-address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low) if t_{AA} max (access time from column address) and t_{RAC} have been satisfied. In the event that column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CPA} or t_{CAC}.

address: A0 – A11 (TMS4x6400/P) and A0 – A10 (TMS4x7400/P)

Twenty-two address bits are required to decode 1 of 4194304 storage cell locations. For the TMS4x6400 and TMS4x6400P, 12 row-address bits are set up on A0 through A11 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Ten column-address bits are set up on A0 through A9. For TMS4x7400 and TMS4x7400P, 11 row-address bits are set up on inputs A0 through A10 and latched onto the chip by $\overline{RAS}$. Eleven column-address bits are set up on A0 through A10. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable because it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffers and latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through $\overline{W}$. A logic high on $\overline{W}$ selects the read mode, and a logic low selects the write mode. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation with $\overline{OE}$ grounded.

data in (DQ1 – DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$, and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ is already low, and the data is strobed in by $\overline{W}$ with setup and hold time referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to the high-impedance state prior to impressing data on the I/O lines.

data out (DQ1 – DQ4)

Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after the access time interval t_{CAC} (which begins with the negative transition of $\overline{CAS}$) as long as t_{RAC} and t_{AA} are satisfied.

$\overline{\text{RAS}}$-only refresh

TMS4x6400, TMS4x6400P

A refresh operation must be performed at least once every 64 ms (128 ms for TMS4x6400P) to retain data. This can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{\text{RAS}}$-only operation can be used by holding $\overline{\text{CAS}}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{\text{RAS}}$-only refresh.

TMS4x7400, TMS4x7400P

A refresh operation must be performed at least once every 32 ms (128 ms for TMS4x7400P) to retain data. This can be achieved by strobing each of the 2048 rows (A0–A10). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{\text{RAS}}$-only operation can be used by holding $\overline{\text{CAS}}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{\text{RAS}}$-only refresh.

hidden refresh

Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{\text{CAS}}$ at V_{IL} after a read operation and cycling $\overline{\text{RAS}}$ after a specified precharge period, similar to a $\overline{\text{RAS}}$-only refresh cycle. The external address is ignored, and the refresh address is generated internally.

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ (CBR) refresh

CBR refresh is utilized by bringing $\overline{\text{CAS}}$ low earlier than $\overline{\text{RAS}}$ (see parameter t_{CSR}) and holding it low after $\overline{\text{RAS}}$ falls (see parameter t_{CHR}). For successive CBR refresh cycles, $\overline{\text{CAS}}$ can remain low while cycling $\overline{\text{RAS}}$. The external address is ignored, and the refresh address is generated internally.

battery-backup refresh

TMS4x6400P

A low-power battery-backup refresh mode that requires less than 500 μA (5 V) or 350 μA (3.3 V) refresh current is available on the TMS4x6400P. Data integrity is maintained using CBR refresh with a period of 31.25 μs while holding $\overline{\text{RAS}}$ low for less than 1 μs. To minimize current consumption, all input levels must be at CMOS levels ($V_{IL} < 0.2$ V, $V_{IH} > V_{CC} - 0.2$ V).

TMS4x7400P

A low-power battery-backup refresh mode that requires less than 500 μA (5 V) or 350 μA (3.3 V) refresh current is available on the TMS4x7400P. Data integrity is maintained using CBR refresh with a period of 62.5 μs while holding $\overline{\text{RAS}}$ low for less than 1 μs. To minimize current consumption, all input levels must be at CMOS levels ($V_{IL} < 0.2$ V, $V_{IH} > V_{CC} - 0.2$ V).

self refresh (TMS4xx400P)

The self-refresh mode is entered by dropping $\overline{\text{CAS}}$ low prior to $\overline{\text{RAS}}$ going low. Then $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ are both held low for a minimum of 100 μs. The chip is then refreshed internally by an on-board oscillator. No external address is required because the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are brought high to satisfy t_{CHS}. Upon exiting self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. The burst refresh ensures the DRAM is fully refreshed.

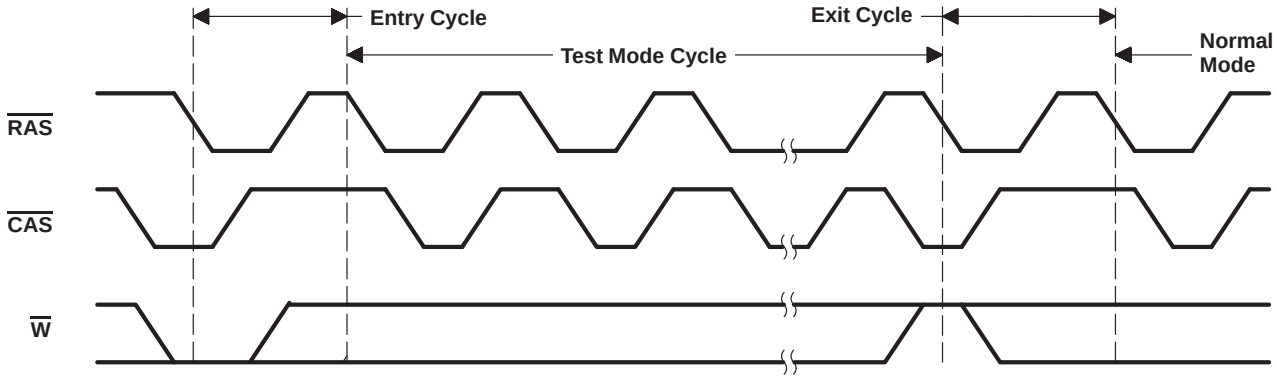
power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after power up to the full V_{CC} level. These eight initialization cycles must include at least one refresh ($\overline{\text{RAS}}$-only or CBR) cycle.

test mode

The test mode is initiated with a CBR-refresh cycle while simultaneously holding the $\overline{W}$ input low. The entry cycle performs an internal refresh cycle while internally setting the device to perform parallel read or write on subsequent cycles. While in the test mode, any data sequence can be performed. The device exits test mode if a CBR refresh cycle with $\overline{W}$ held high or a $\overline{RAS}$-only refresh cycle is performed.

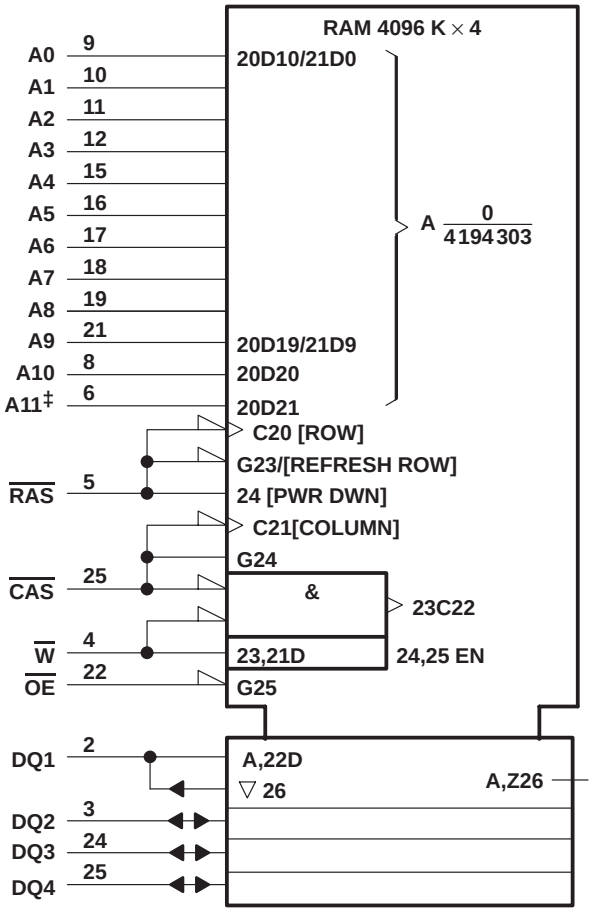
In the test mode, the device is configured as 1024K bits × 4 bits for each DQ. Each DQ pin has a separate 4-bit parallel read and write data bus that ignores column addresses A0 and A1. During a read cycle, the four internal bits are compared for each DQ pin separately. If the four bits agree, DQ goes high; if not, DQ goes low. During a write cycle, the data states of all four DQs must be the same to ensure proper function of the test mode. Test time is reduced by a factor of four for this series.



NOTE A: The states of $\overline{W}$, data in, and address are defined by the type of cycle used during test mode.

Figure 1. Test-Mode Cycle

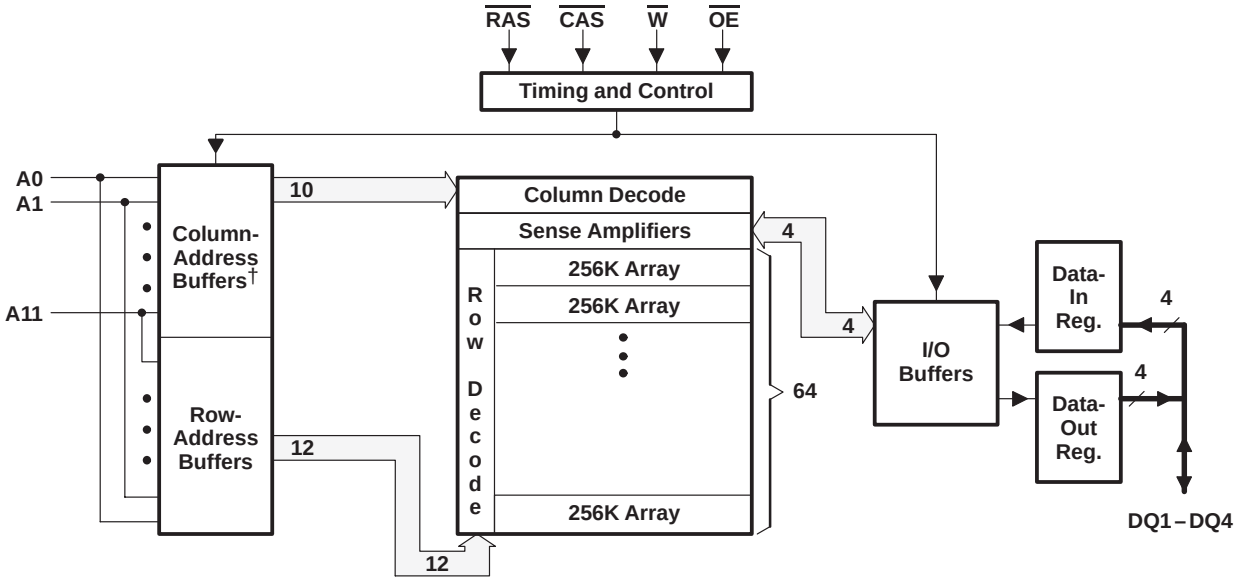
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 647-12.
‡ A11 is NC for TMS4x7400 and TMS4x7400P.

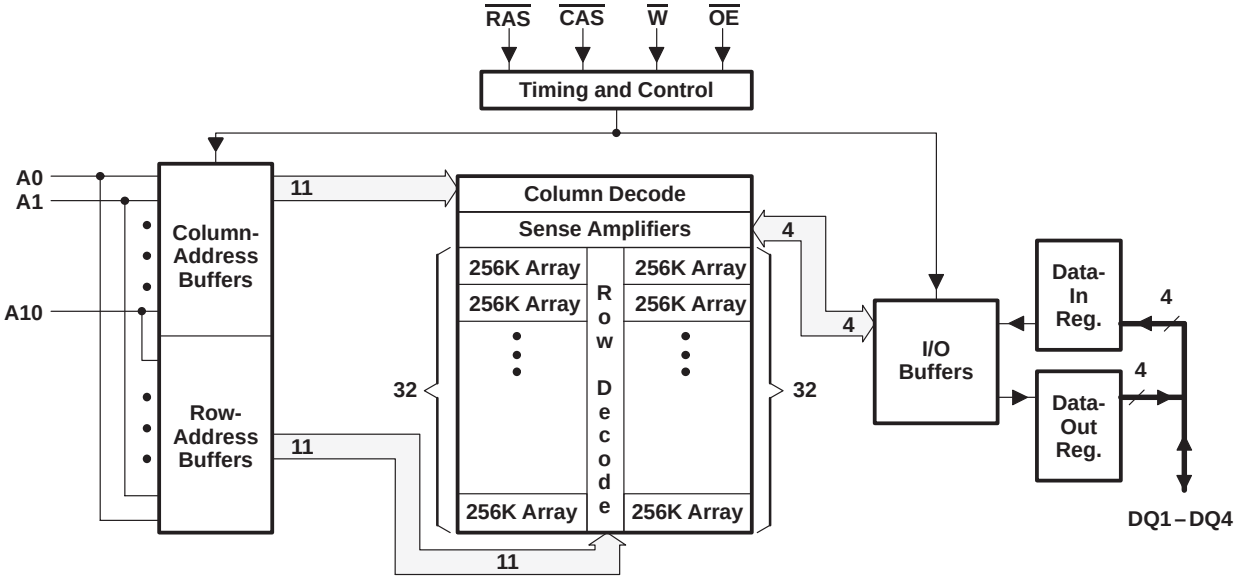
functional block diagram

TMS4x6400/P



† Column addresses A10 and A11 are not used.

TMS4x7400/P



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}: TMS41x400, TMS41x400P . . . . . – 1 V to 7 V
TMS42x400, TMS42x400P . . . . . – 0.5 V to 4.6 V
Voltage range on any pin (see Note 1): TMS41x400, TMS41x400P . . . . . – 1 V to 7 V
TMS42x400, TMS42x400P . . . . . – 0.5 V to 4.6 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		TMS41x400			TMS42x400			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	3	3.3	3.6	V
V_{SS}	Supply voltage		0			0		V
V_{IH}	High-level input voltage	2.4		6.5	2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	– 0.3		0.8	V
T_A	Operating free-air temperature	0		70	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TMS416400/P

PARAMETER		TEST CONDITIONS†		'416400-60 '416400P-60 MIN	'416400-60 '416400P-60 MAX	'416400-70 '416400P-70 MIN	'416400-70 '416400P-70 MAX	'416400-80 '416400P-80 MIN	'416400-80 '416400P-80 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	$\overline{V_{CC}}$ = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle			80		70		60	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high			2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'416400		1		1		1	mA
			'416400P		500		500		500	µA
I_{CC3}‡§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	$\overline{V_{CC}}$ = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			80		70		60	mA
I_{CC4}‡¶	Average page current	$\overline{V_{CC}}$ = 5.5 V, $\overline{t_{PC}}$ = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling			70		60		50	mA
I_{CC6}#	Self-refresh current	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			500		500		500	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms); CBR only	t_{RC} = 31.25 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			500		500		500	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}
# For TMS416400P only

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

TMS417400/P

PARAMETER		TEST CONDITIONS†		'417400-60 '417400P-60		'417400-70 '417400P-70		'417400-80 '417400P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	$\overline{V_{CC}}$ = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle			110		100		90	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), $\overline{After}$ 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high			2		2		2	mA
		$V_{IH} = V_{CC}$ – 0.2 V (CMOS), $\overline{After}$ 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'417400		1		1		1	mA
			'417400P		500		500		500	µA
I_{CC3}‡§	Average $\overline{refresh}$ current ($\overline{RAS}$-only refresh or CBR)	$\overline{V_{CC}}$ = 5.5 V, $\overline{RAS}$ cycling, $\overline{Minimum\ cycle}$, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			110		100		90	mA
I_{CC4}‡¶	Average page current	$\overline{V_{CC}}$ = 5.5 V, $\overline{RAS}$ low, $\overline{t_{PC}}$ = MIN, $\overline{CAS}$ cycling			70		60		50	mA
I_{CC6}#	Self-refresh current	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			500		500		500	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms); CBR only	t_{RC} = 62.5 µs, $t_{RAS} \le 1$ µs, $V_{CC} - 0.2\ V \le V_{IH} \le 6.5$ V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			500		500		500	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}
# For TMS417400P only

electrical characteristics over recommended ranges of supply voltage and operating free-air conditions (unless otherwise noted) (continued)

TMS426400/P

PARAMETER		TEST CONDITIONS†		'426400-60 '426400P-60		'426400-70 '426400P-70		'426400-80 '426400P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = – 100 µA	LVCMOS	V_{CC}–0.2		V_{CC}–0.2		V_{CC}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{CC} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 3.6 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 3.6 V, Minimum cycle			70		60		50	mA
I_{CC2}	Standby current	V_{IH} = 2 V (LVTTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high			1		1		1	mA
		V_{IH} = V_{CC} – 0.2 V (LVCMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'426400		500		500		500	µA
			'426400P		200		200		200	µA
I_{CC3}‡§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 3.6 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only refresh), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			70		60		50	mA
I_{CC4}‡¶	Average page current	V_{CC} = 3.6 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling			60		50		40	mA
I_{CC6}#	Self-refresh current	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			250		250		250	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms), CBR only	t_{RC} = 31.25 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			350		350		350	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}
# For TMS426400P only

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and operating free-air conditions (unless otherwise noted) (continued)

TMS427400/P

PARAMETER		TEST CONDITIONS†		'427400-60 '427400P-60		'427400-70 '427400P-70		'427400-80 '427400P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = – 100 µA	LVCMOS	V_{CC}–0.2		V_{CC}–0.2		V_{CC}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{CC} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 3.6 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 3.6 V, Minimum cycle			100		90		80	mA
I_{CC2}	Standby current	V_{IH} = 2 V (LVTTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high			1		1		1	mA
		V_{IH} = V_{CC} – 0.2 V (LVCMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'427400		500		500		500	µA
			'427400P		200		200		200	µA
I_{CC3}‡§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 3.6 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only refresh), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			100		90		80	mA
I_{CC4}‡¶	Average page current	V_{CC} = 3.6 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling			60		50		40	mA
I_{CC6}#	Self-refresh current	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			250		250		250	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms), CBR only	t_{RC} = 62.5 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			350		350		350	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}
# For TMS427400P only

PRODUCT PREVIEW

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A11		5	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_o	Output capacitance		7	pF

NOTE 3: V_{CC} = NOM supply voltage ±10%, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		’4xx400-60 ’4xx400P-60		’4xx400-70 ’4xx400P-70		’4xx400-80 ’4xx400P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address (see Note 4)		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low (see Note 4)		15		18		20	ns
t_{CPA}	Access time from column precharge (see Note 4)		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low (see Note 4)		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low (see Note 4)		15		18		20	ns
t_{CLZ}	Delay time, $\overline{CAS}$ low to output in low-impedance state	0		0		0		ns
t_{OH}	Output data hold time (from $\overline{CAS}$)	3		3		3		ns
t_{OHO}	Output data hold time (from $\overline{OE}$)	3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 5)	0	15	0	18	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 5)	0	15	0	18	0	20	ns

NOTES: 4. Access times for TMS42x400 measured with output reference levels of V_{OH} = 2 V and V_{OL} = 0.8 V.
5. t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'4xx400-60 '4xx400P-60		'4xx400-70 '4xx400P-70		'4xx400-80 '4xx400P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, read (see Note 6)	110		130		150		ns
t_{WC}	Cycle time, write (see Note 6)	110		130		150		ns
t_{RWC}	Cycle time, read-write (see Note 6)	155		181		205		ns
t_{PC}	Cycle time, page-mode read or write (see Notes 6 and 7)	40		45		50		ns
t_{PRWC}	Cycle time, page-mode read-write (see Note 6)	85		96		105		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ low, page mode (see Note 8)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low, nonpage mode (see Note 8)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 9)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data (see Note 10)	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low (early-write operation only)	0		0		0		ns
t_{WRP}	Setup time, $\overline{W}$ high before $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{WTS}	Setup time, $\overline{W}$ low before $\overline{RAS}$ low (test mode only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{DH}	Hold time, data (see Note 10)	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 11)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 11)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CAS}$ low (early-write operation only)	10		15		15		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high from $\overline{CAS}$ precharge	35		40		45		ns
t_{OEH}	Hold time, $\overline{OE}$ command	15		18		20		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$	10		10		10		ns
t_{CHS}	Hold time, $\overline{CAS}$ low after $\overline{RAS}$ high (self refresh)	– 50		– 50		– 50		ns
t_{WRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{WTH}	Hold time, $\overline{W}$ low after $\overline{RAS}$ low (test mode only)	10		10		10		ns

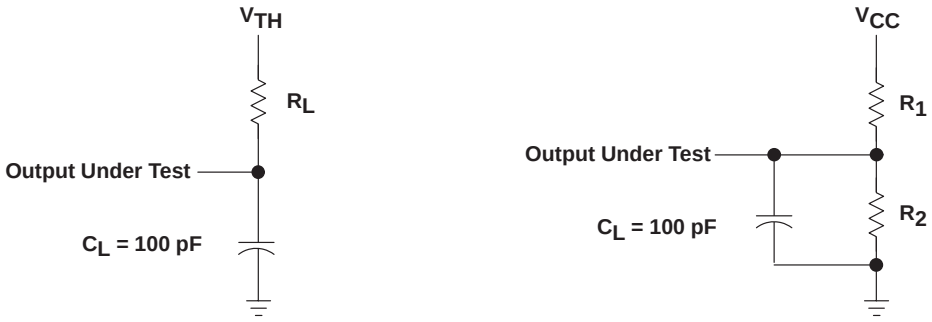
NOTES: 6. All cycle times assume t_T = 5 ns.
7. To assure t_{PC} min, t_{ASC} should be ≥ to t_{CP}.
8. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
9. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

			'4xx400-60 '4xx400P-60		'4xx400-70 '4xx400P-70		'4xx400-80 '4xx400P-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{AWD}	Delay time, column address to $\overline{W}$ low (read-write operation only)		55		63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)		10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high		60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)		5		5		5		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-write operation only)		40		46		50		ns
t_{OED}	Delay time, $\overline{OE}$ to data		15		18		20		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 12)		15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high		30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high		30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 12)		20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high		15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-write operation only)		85		98		110		ns
t_{CPW}	Delay time, $\overline{W}$ low after $\overline{CAS}$ precharge (read-write operation only)		60		68		75		ns
t_{RASS}	Pulse duration, self-refresh entry from $\overline{RAS}$ low		100		100		100		µs
t_{RPS}	Pulse duration, $\overline{RAS}$ precharge after self refresh		110		130		150		ns
t_{TAA}	Access time from address (test mode)		35		40		45		ns
t_{TCPA}	Access time from column precharge (test mode)		40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)		65		75		85		ns
t_{REF}	Refresh time interval	'4x6400		64		64		64	ms
		'4x6400P		128		128		128	
		'4x7400		32		32		32	
		'4x7400P		128		128		128	
t_T	Transition time		3	30	3	30	3	30	ns

NOTE 12: The maximum value is specified only to assure access time.

PARAMETER MEASUREMENT INFORMATION

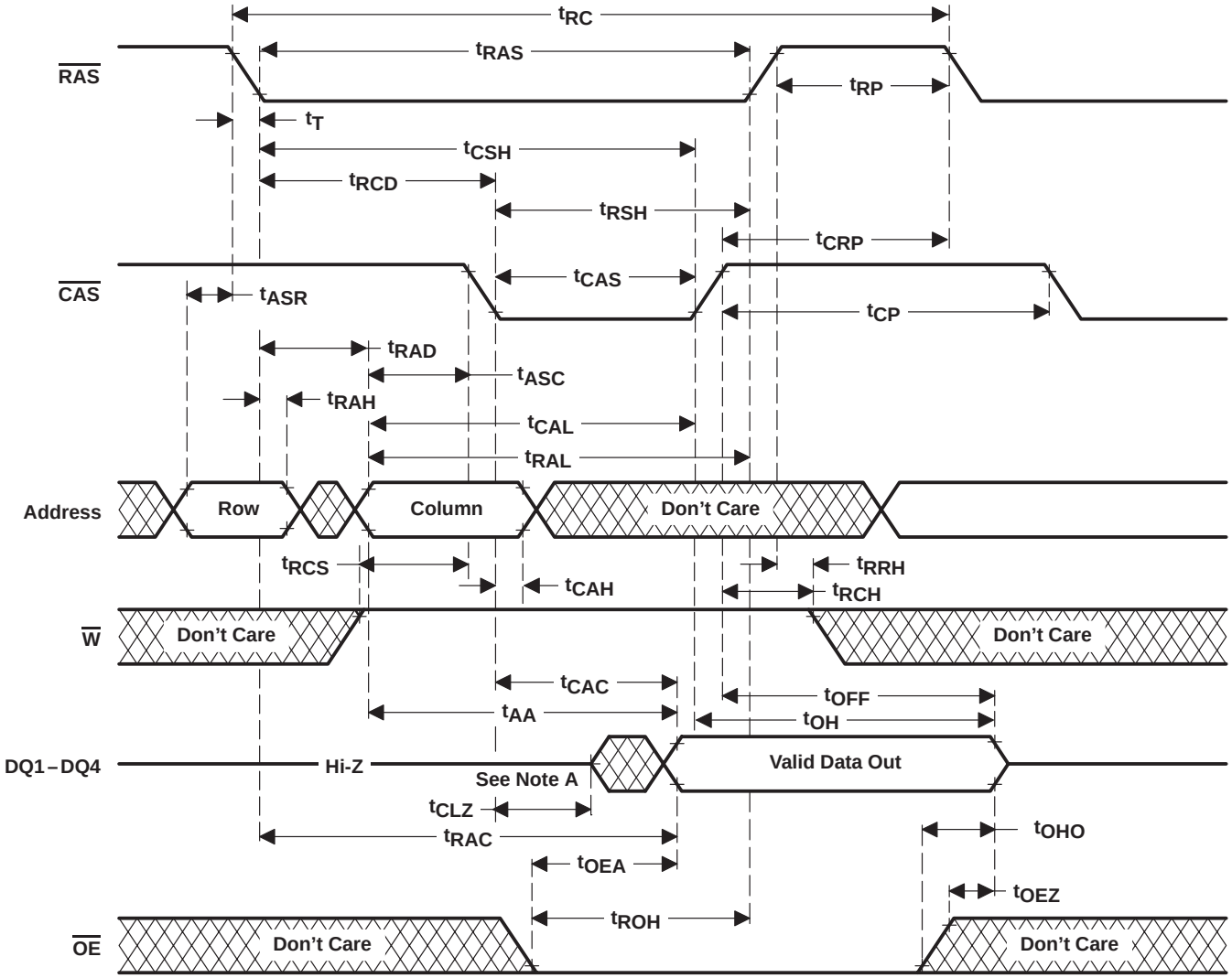


(a) LOAD CIRCUIT

(b) ALTERNATE LOAD CIRCUIT

DEVICE	V_{CC} (V)	R_1 (Ω)	R_2 (Ω)	V_{TH} (V)	R_L (Ω)
’41x400/P	5	828	295	1.31	218
’42x400/P	3.3	1178	868	1.4	500

Figure 2. Load Circuits for Timing Parameters



NOTE A: Output can go from high-impedance state to an invalid-data state prior to the specified access time.

Figure 3. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

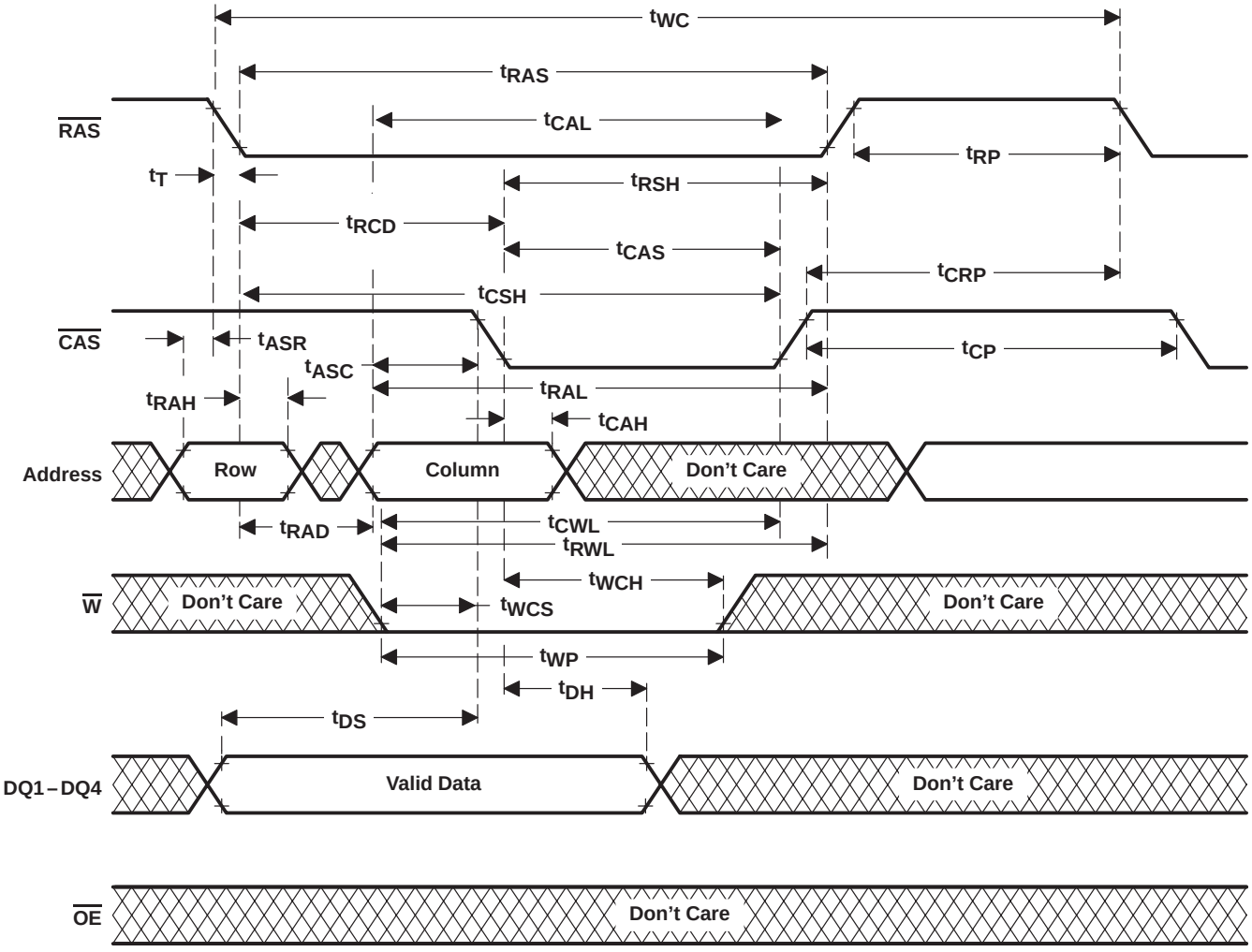


Figure 4. Early-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

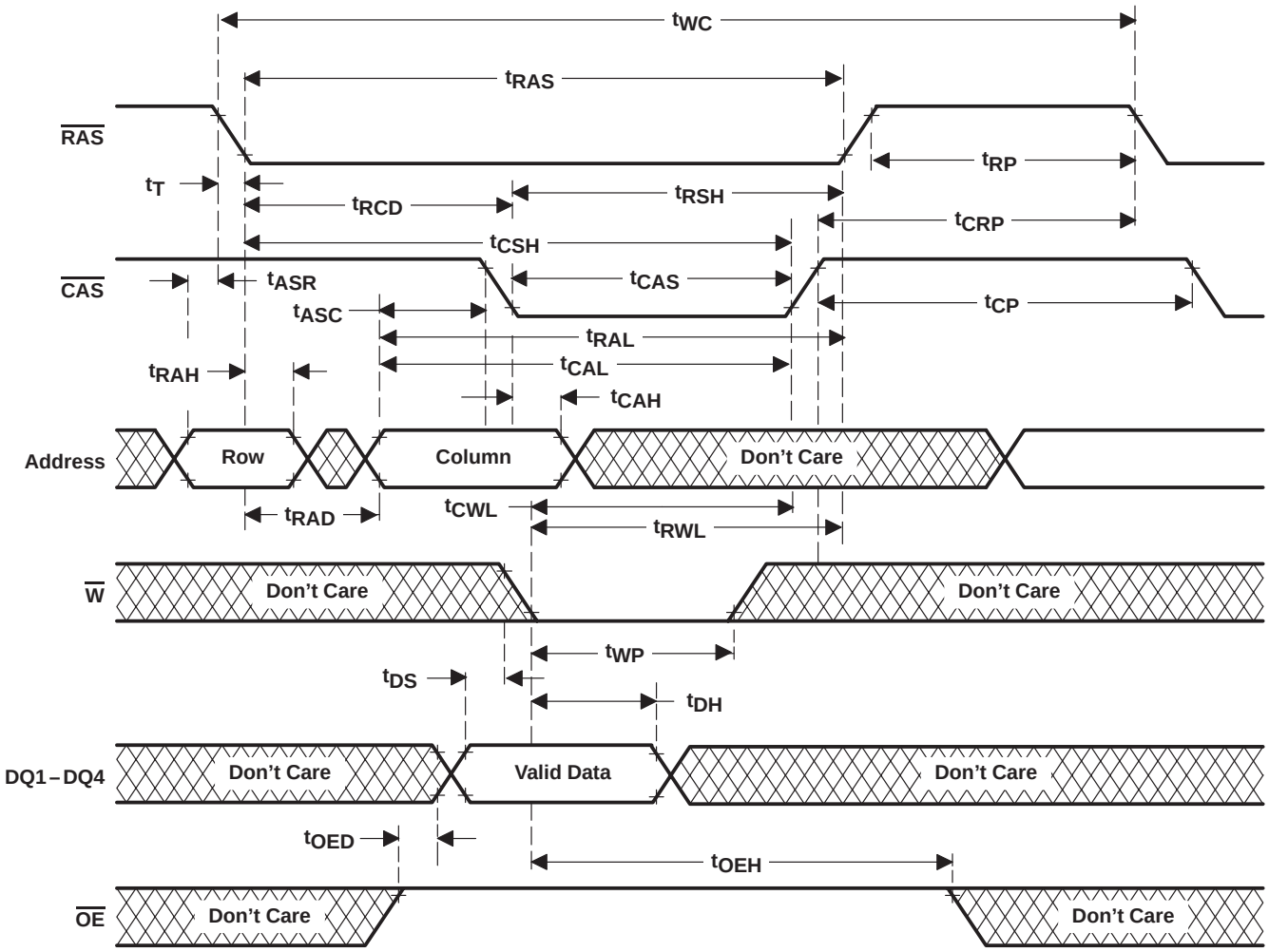
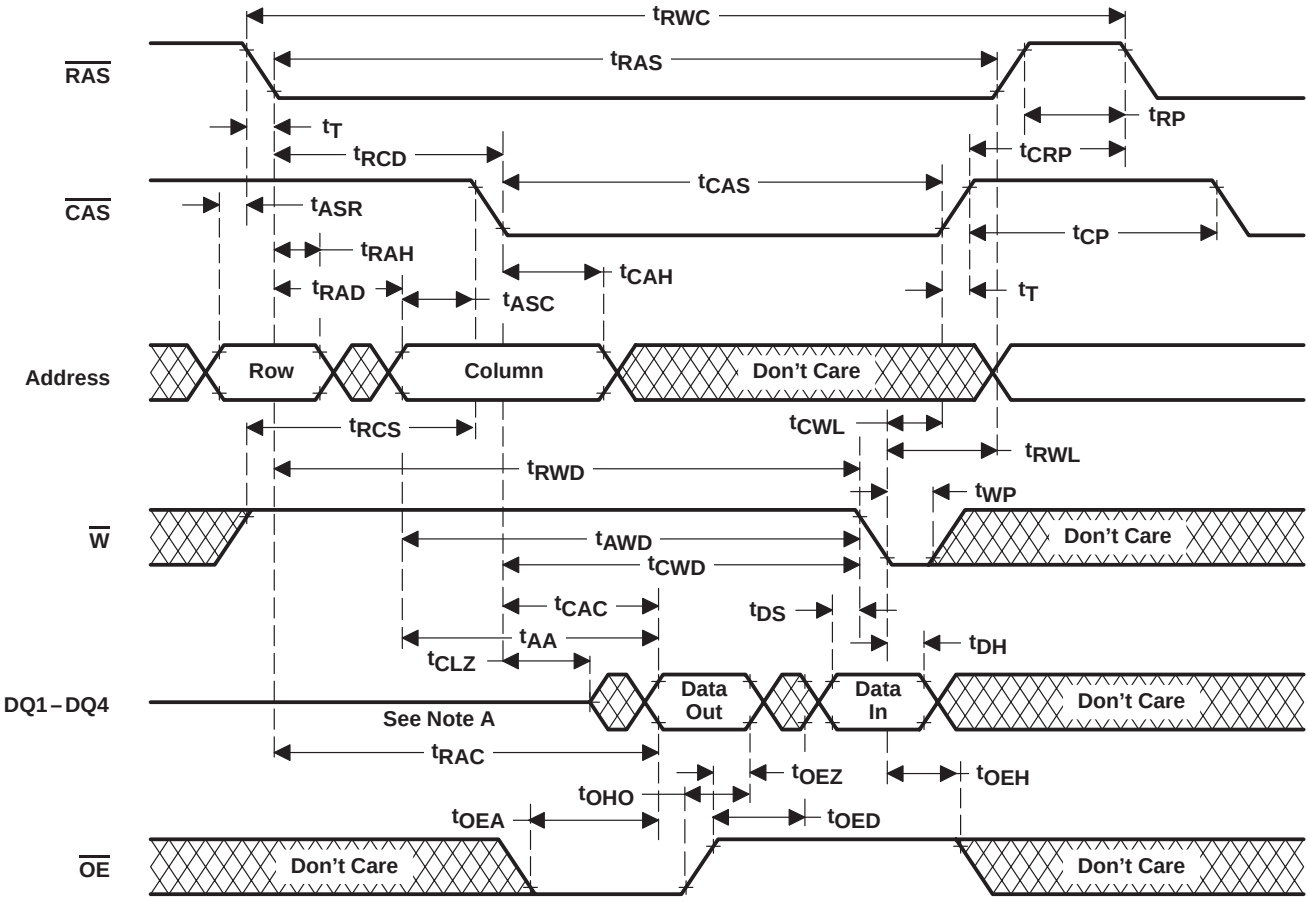


Figure 5. Write-Cycle Timing

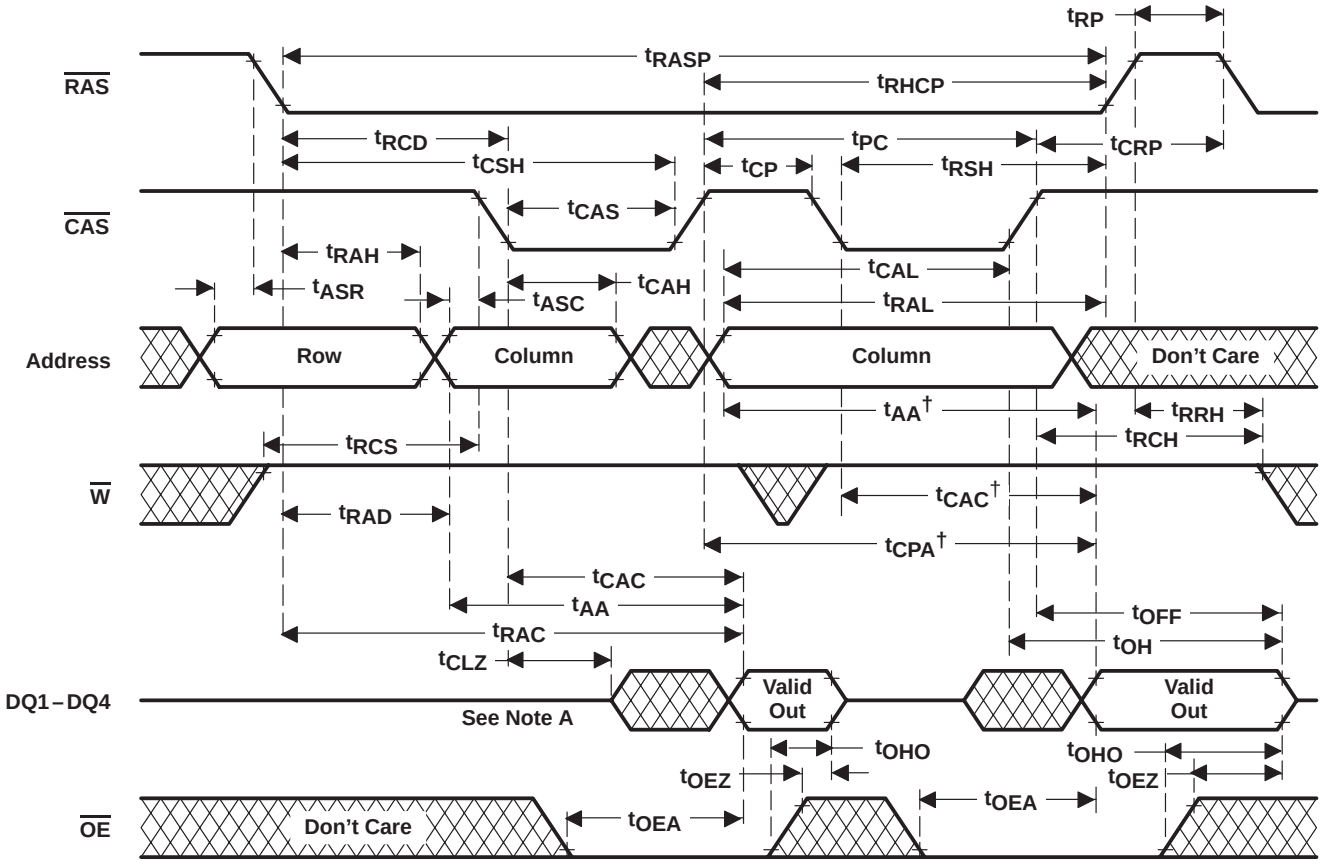
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from high-impedance state to an invalid-data state prior to the specified access time.

Figure 6. Read-Write-Cycle Timing

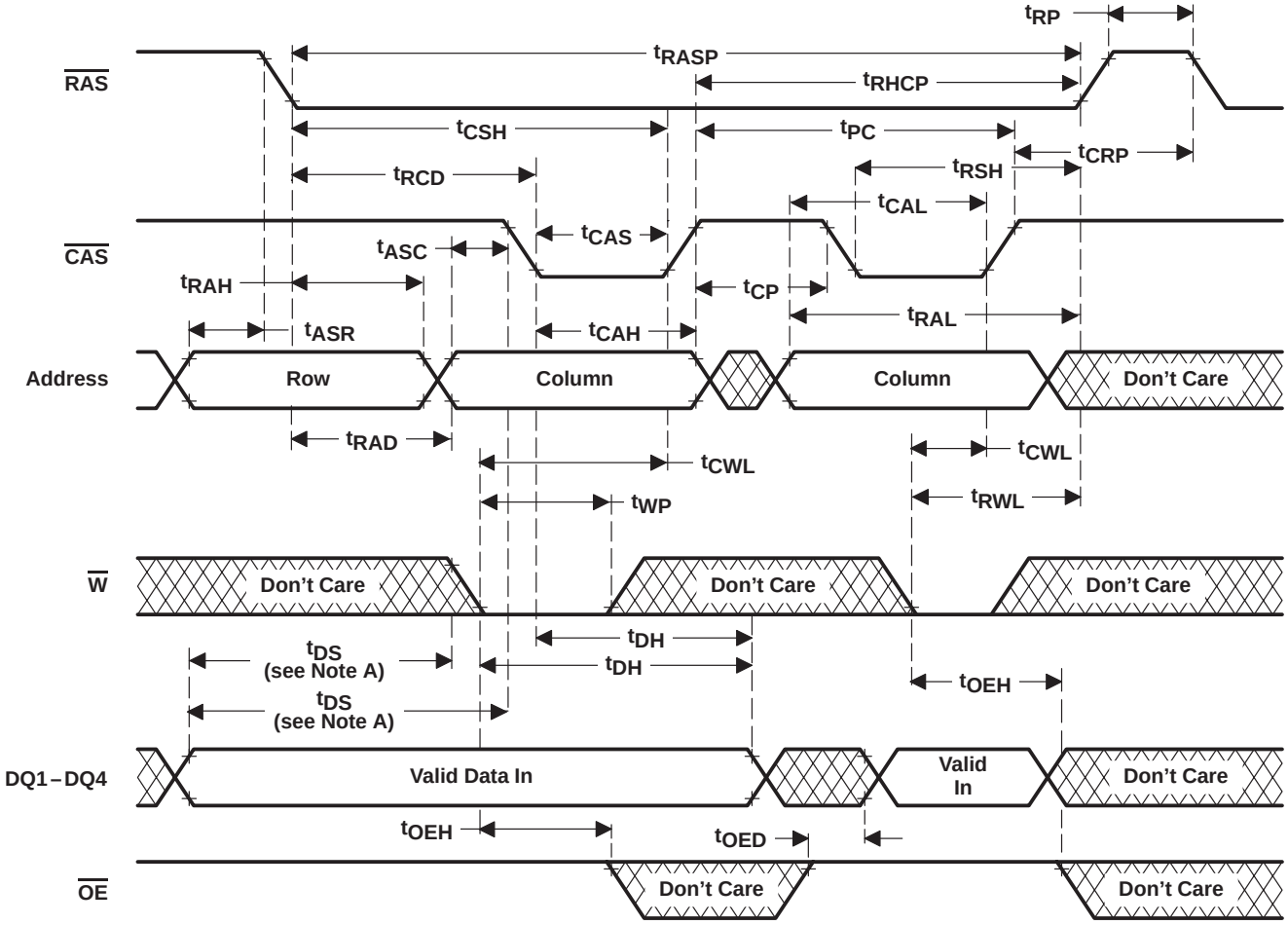
PARAMETER MEASUREMENT INFORMATION



† Access time is t_{CPA}, t_{CAC}, or t_{AA} dependent.
NOTE A: Output can go from high-impedance state to an invalid-data state prior to the specified access time.

Figure 7. Enhanced-Page-Mode Read-Cycle Timing

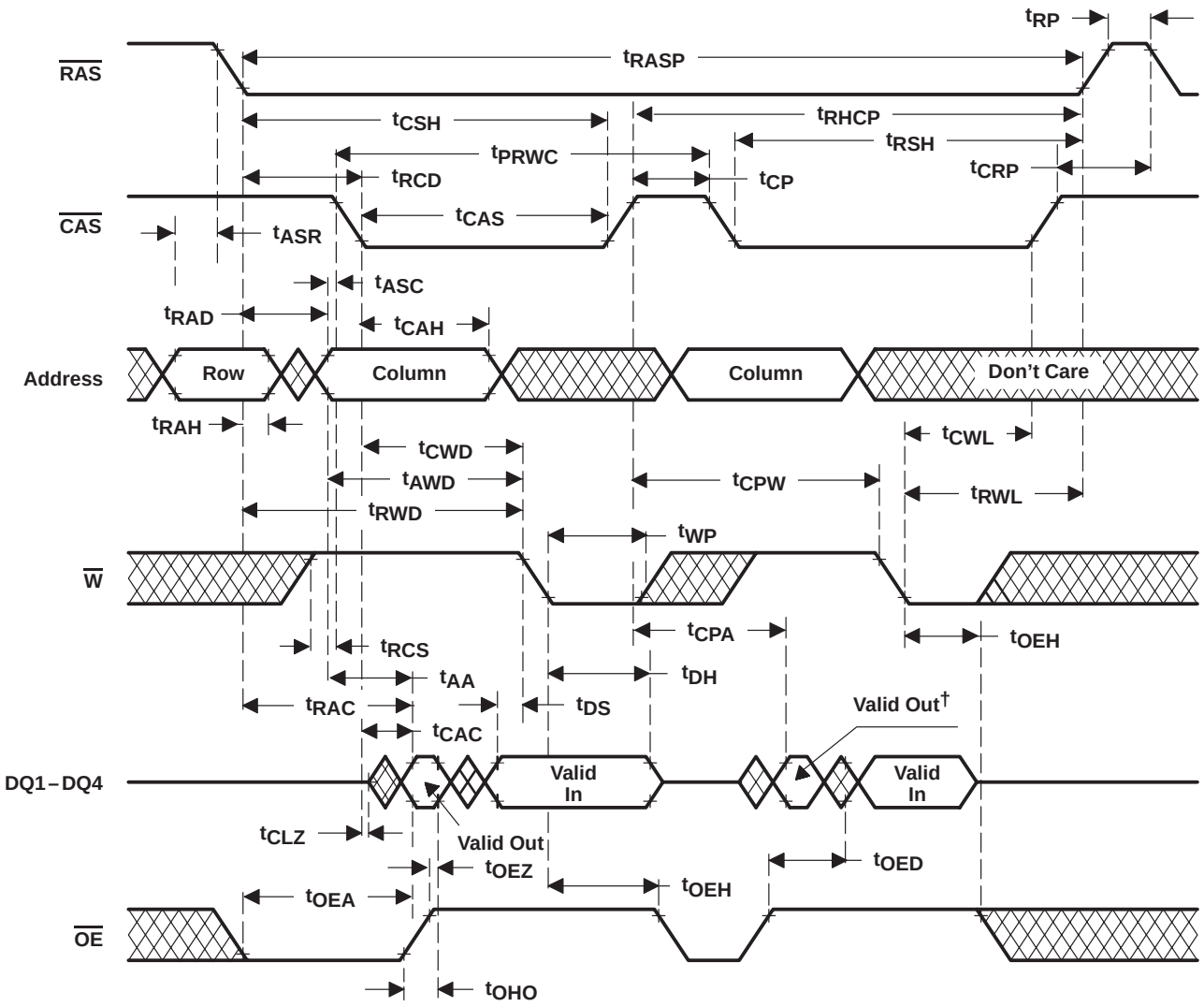
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last
B. A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† Output can go from high-impedance state to an invalid-data state prior to the specified access time.
NOTE A: A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 9. Enhanced-Page-Mode Read-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

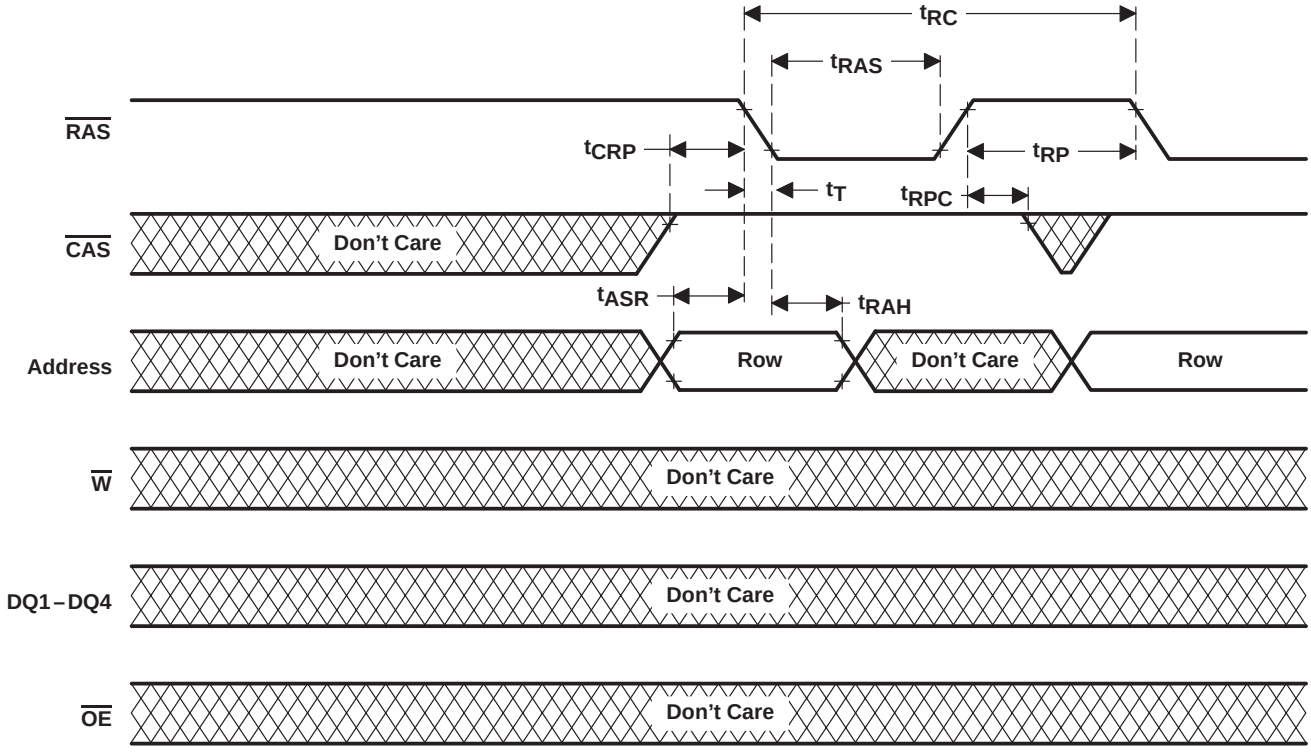


Figure 10. $\overline{\text{RAS}}$-Only Refresh Timing

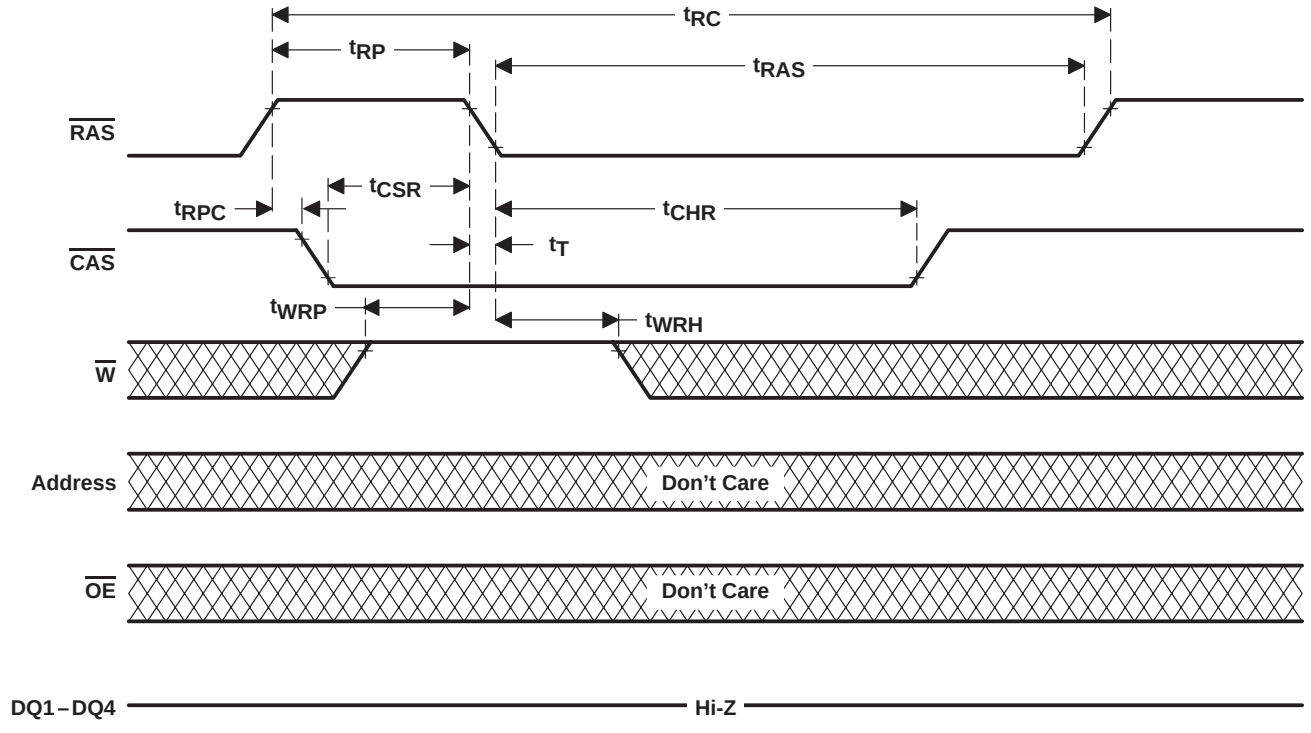


Figure 11. Automatic-CBR-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

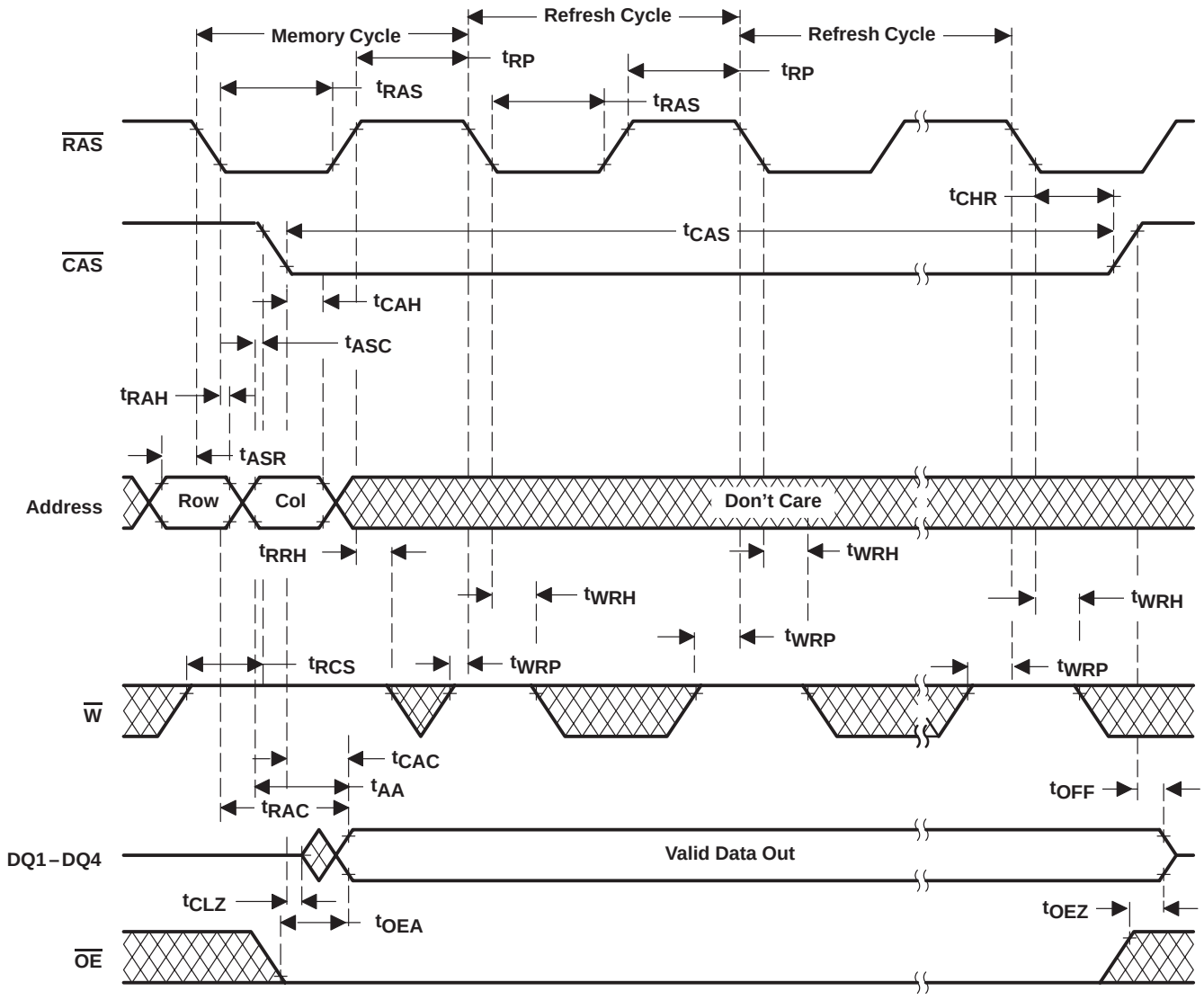


Figure 12. Hidden-Refresh-Cycle (Read) Timing

PARAMETER MEASUREMENT INFORMATION

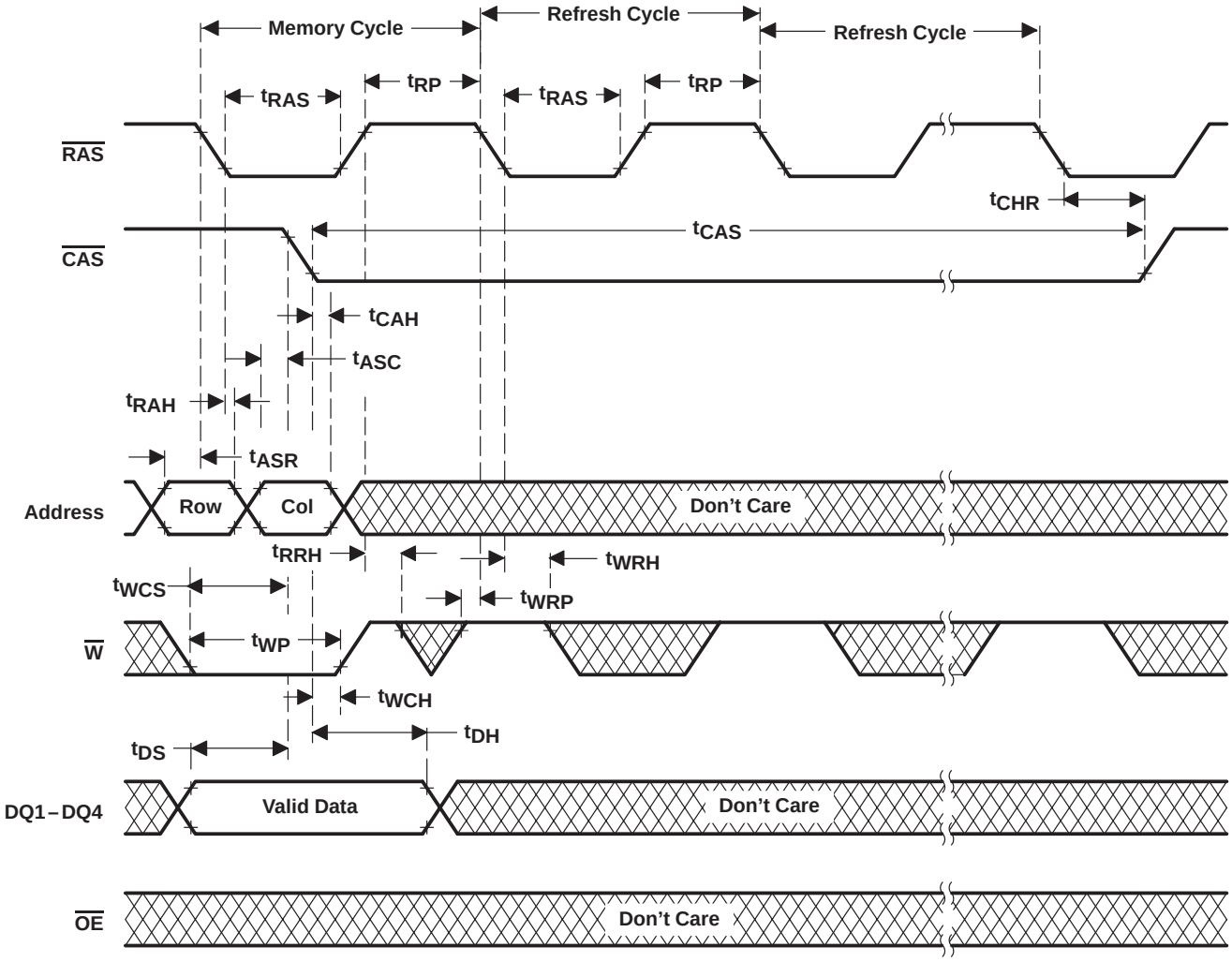


Figure 13. Hidden-Refresh-Cycle (Write) Timing

PARAMETER MEASUREMENT INFORMATION

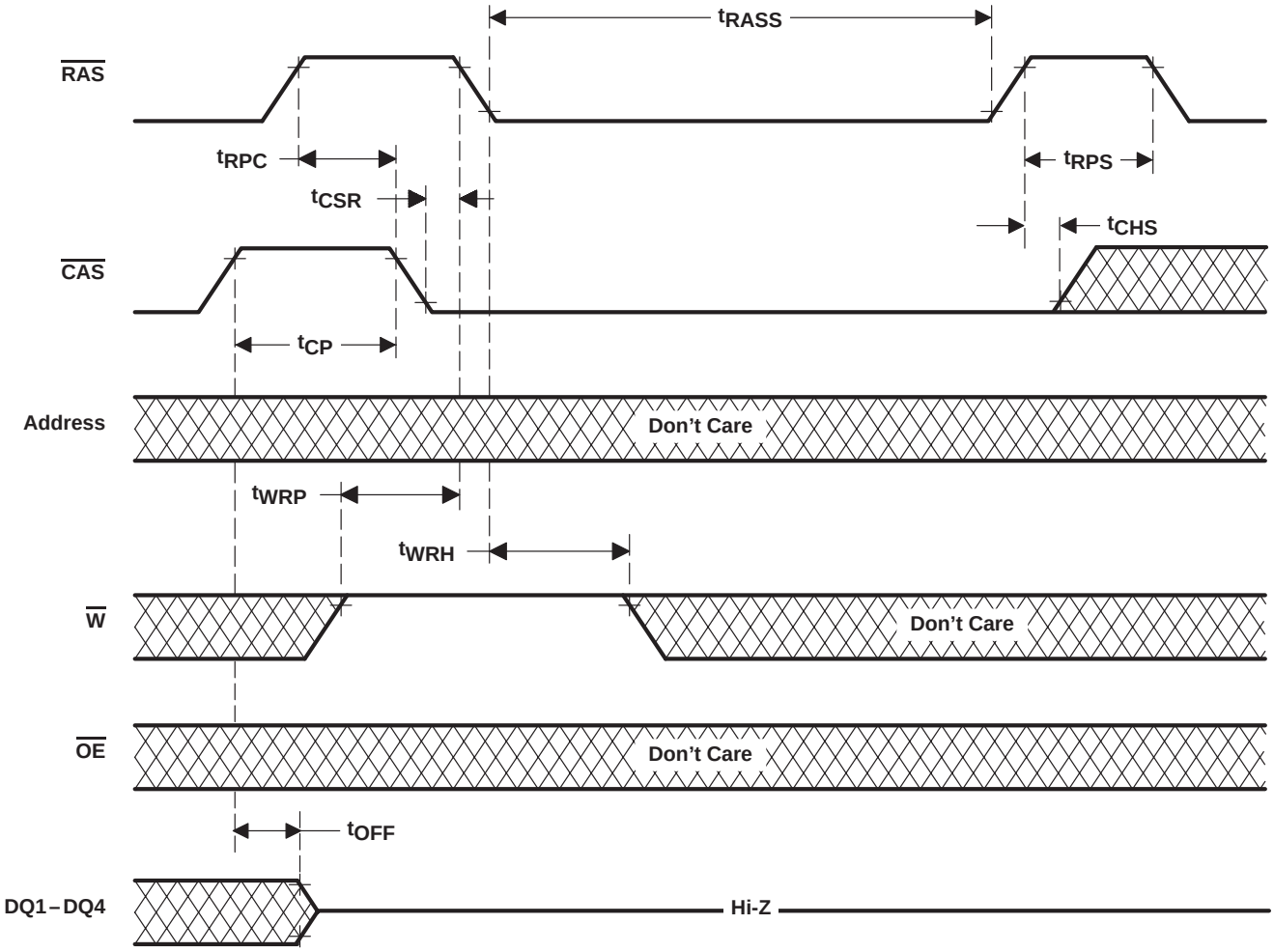


Figure 14. Self-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

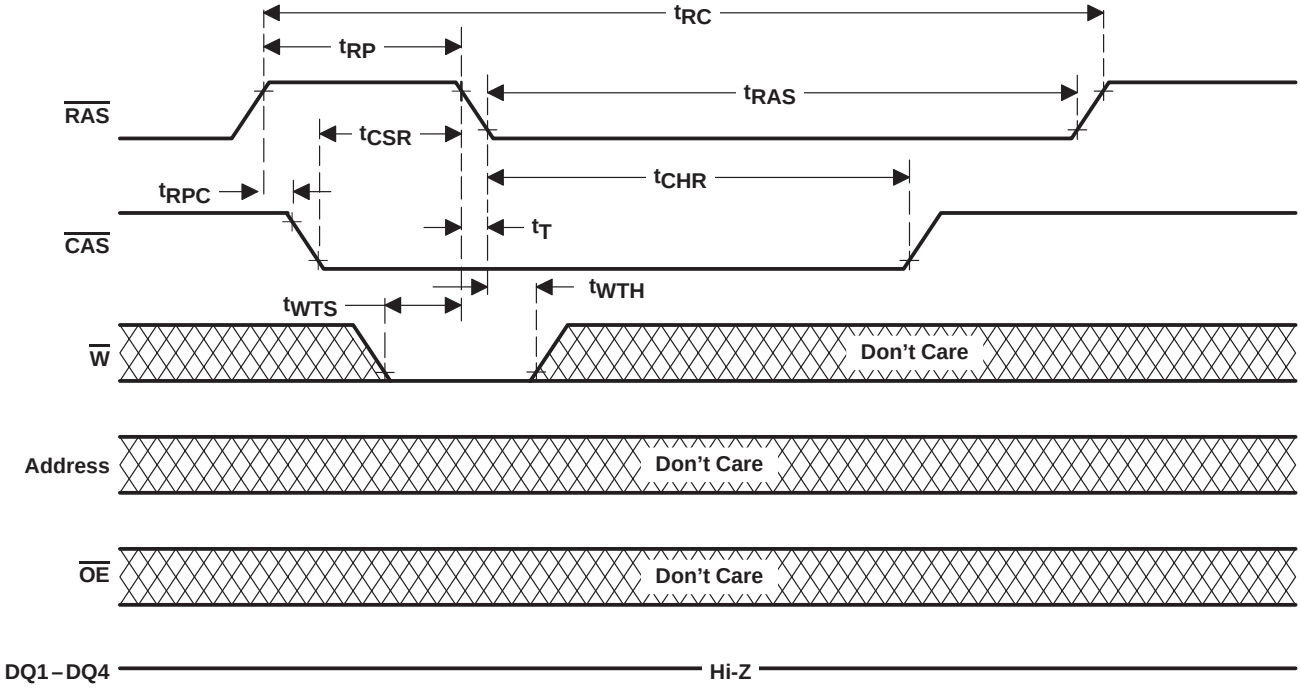


Figure 15. Test-Mode-Entry-Cycle Timing

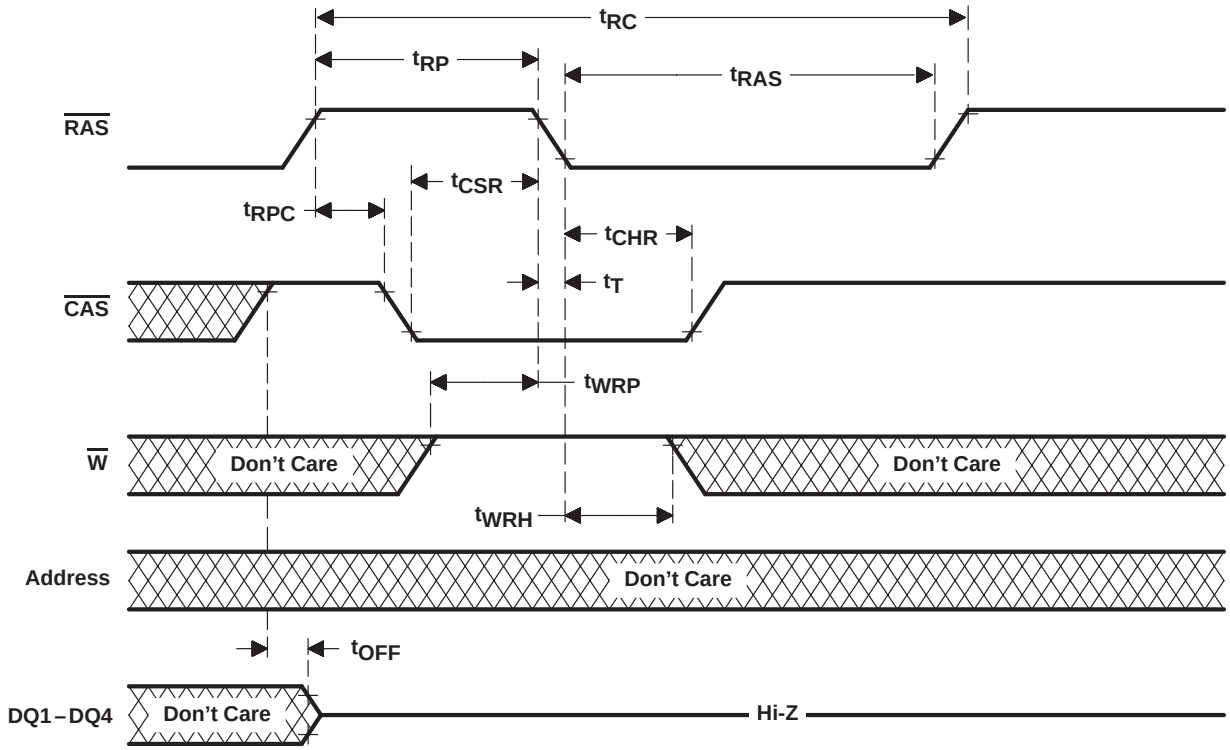
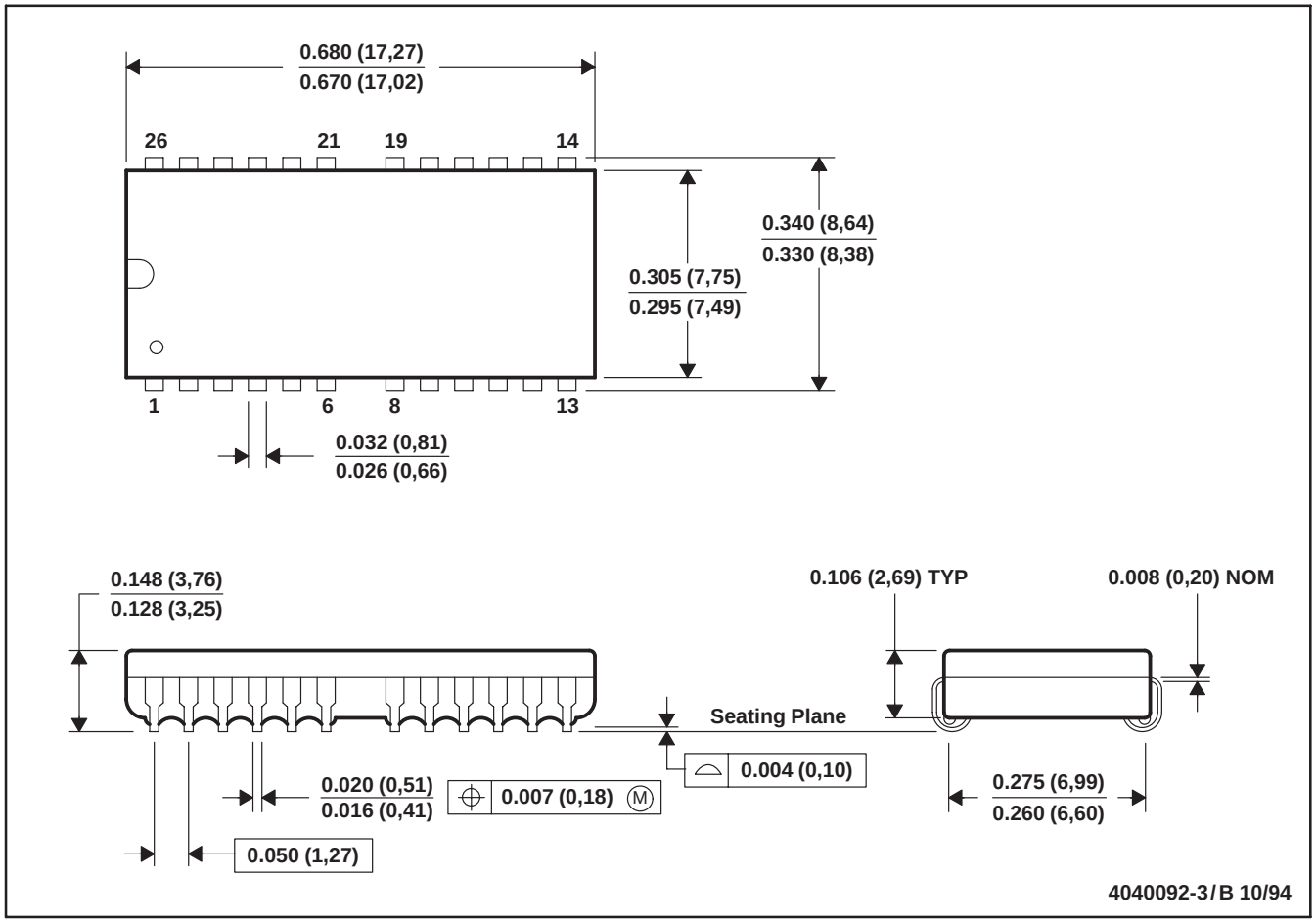


Figure 16. Test-Mode-Exit-Cycle CBR-Refresh-Cycle Timing

MECHANICAL DATA

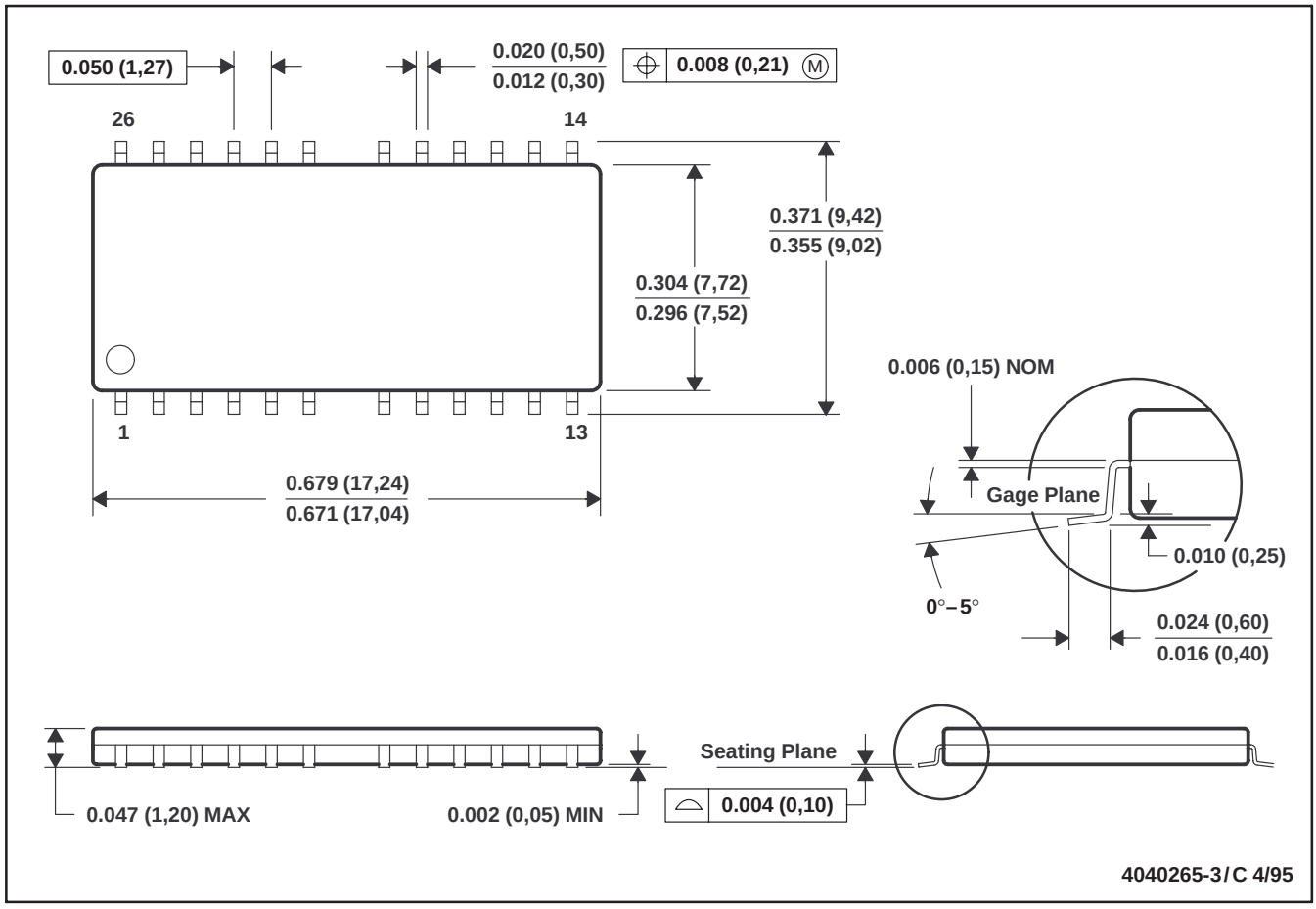
DJ (R-PDSO-J24/26) **PLASTIC SMALL-OUTLINE J-LEAD PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

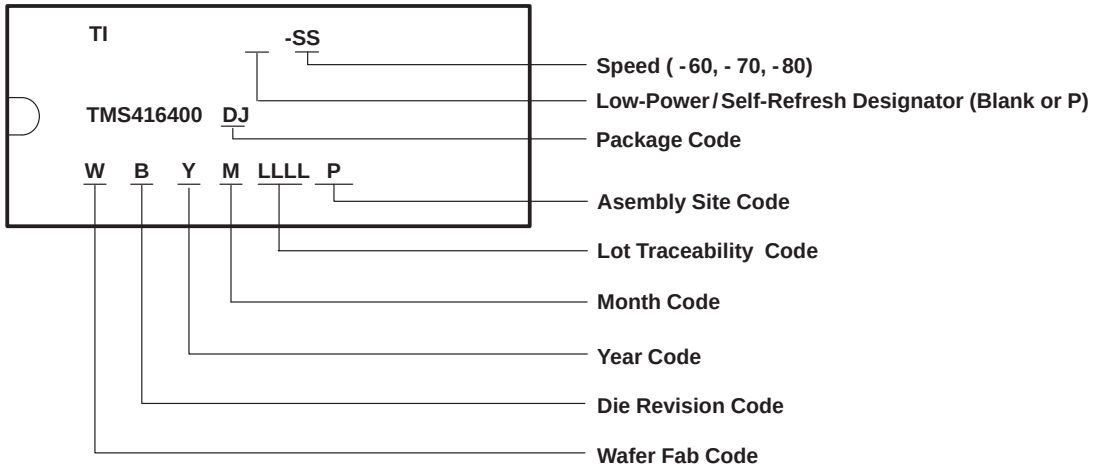
MECHANICAL DATA

DGA (R-PDSO-G24/26) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

device symbolization (TMS416400 illustrated)



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