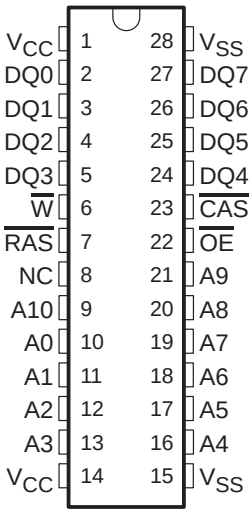
This data sheet is applicable to all TMS417809As and TMS427809A/Ps symbolized by Revision "E" and subsequent revisions as described in the device symbolization section.

- **Organization . . . 2097152 by 8 Bits**
- **Single Power Supply (5 V or 3.3 V)**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	EDO CYCLE t_{HPC} MIN
'417809A-50	50 ns	13 ns	25 ns	20 ns
'417809A-60	60 ns	15 ns	30 ns	25 ns
'417809A-70	70 ns	18 ns	35 ns	30 ns
'427809A/P-50	50 ns	13 ns	25 ns	20 ns
'427809A/P-60	60 ns	15 ns	30 ns	25 ns
'427809A/P-70	70 ns	18 ns	35 ns	30 ns

- **Extended-Data-Out (EDO) Operation**
- **$\overline{CAS}$-Before-$\overline{RAS}$ (CBR) Refresh**
- **Long Refresh Period and Self-Refresh Option (TMS427809AP)**
- **High-Impedance State Unlatched Output**
- **High-Reliability Plastic 28-Lead 400-Mil-Wide Surface-Mount Small-Outline J-Lead (SOJ) Package (DZ Suffix) and 28-Lead 400-Mil-Wide Surface-Mount Thin Small-Outline Package (TSOP) (DGC Suffix)**
- **Ambient Temperature Range 0°C to 70°C**

DZ/DGC PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A[0:10]	Address Inputs
DQ[0:7]	Data In/Data Out
$\overline{CAS}$	Column-Address Strobe
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
V_{CC}	3.3-V or 5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TMS417809A and TMS427809A series are 16777216-bit dynamic random access memory (DRAM) devices organized as 2097152 words of 8 bits each. The TMS427809AP series is a low-power, self-refresh, 16777216-bit DRAM organized as 4194304 words of four bits.They employ TI state-of-the-art technology for high performance, reliability, and low power.

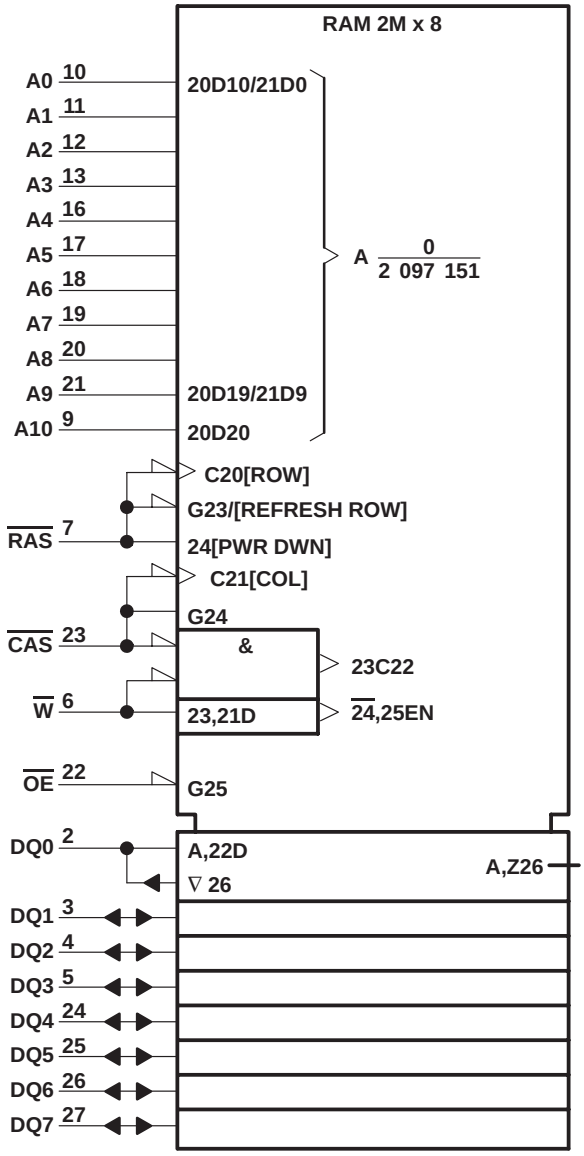
AVAILABLE OPTIONS

DEVICE	POWER SUPPLY	REFRESH CYCLES
TMS417809A	5 V	2048 in 32 ms
TMS427809A	3.3 V	2048 in 32 ms
TMS427809AP	3.3 V	2048 in 128 ms

These devices feature maximum $\overline{RAS}$ access times of 50-, 60-, and 70 ns. All address and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

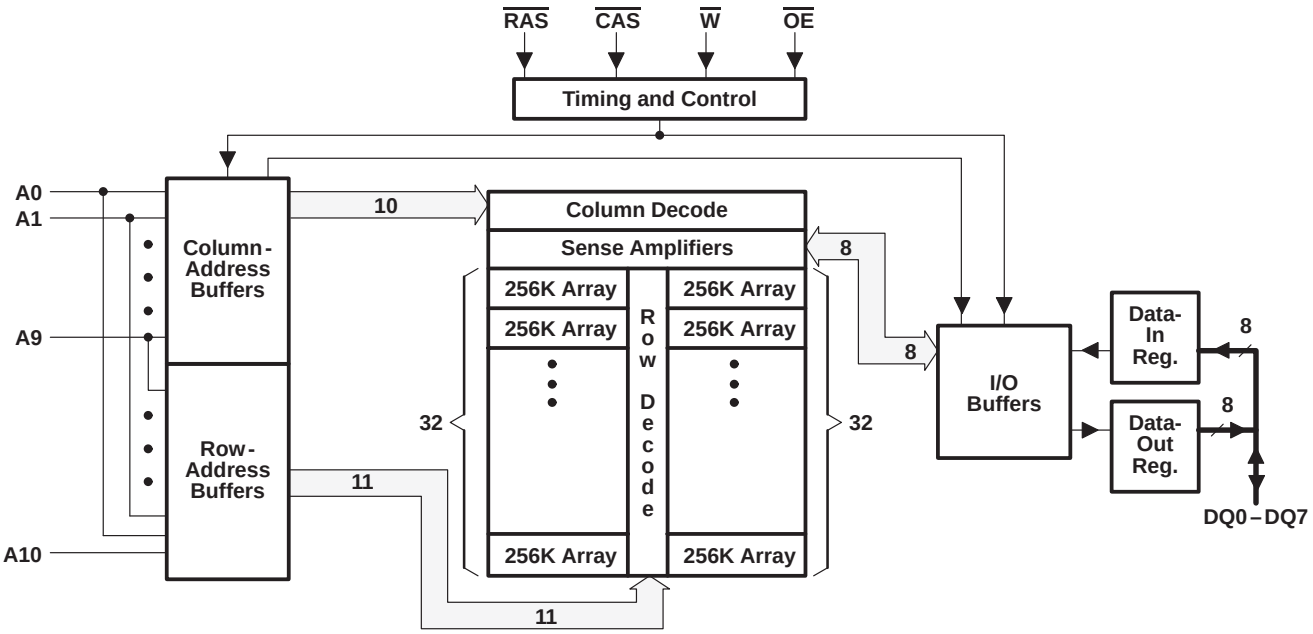
The TMS417809A is offered in a 28-lead plastic surface-mount SOJ package (DZ suffix). The TMS427809A/P is offered in a 28-lead plastic surface-mount TSOP package (DGC suffix). These packages are designed for operation from 0°C to 70°C.

logic symbol (TMS417809A and TMS427809A/P)†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 647-12.

functional block diagram (TMS417809A and TMS427809A/P)



operation

extended data out

Extended data out (EDO) allows data output rates up to 50 MHz for 50-ns devices. When keeping the same row address while selecting random column addresses, the time for row-address setup-and-hold and for address multiplexing is eliminated. The maximum number of columns that can be accessed is determined by t_{RASP}, the maximum $\overline{RAS}$ low time.

The EDO does not place the data-in/data-out pins (DQ pins) in the high-impedance state with the rising edge of $\overline{CAS}$. The output remains valid for the system to latch the data. After $\overline{CAS}$ goes high, the DRAM decodes the next address. $\overline{OE}$ and $\overline{W}$ can control the output impedance. Descriptions of $\overline{OE}$ and $\overline{W}$ further explain EDO operation benefits.

address: A0 – A10

Twenty-one address bits are required to decode each of the 2097152 storage-cell locations. Eleven row-address bits are set up on inputs A0 through A10 and latched onto the chip by $\overline{RAS}$. Ten column-address bits are set up on A0 through A9. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip-enable because it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip-select, activating the output buffers and latching the address bits into the column-address buffers.

output-enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. While $\overline{CAS}$ and $\overline{RAS}$ are low and $\overline{W}$ is high, $\overline{OE}$ can be brought low or high and the DQs transition between valid data and high impedance (see Figure 8). There are two methods of placing the DQs into the high-impedance state and maintaining that state during $\overline{CAS}$ high time. The first method is to transition $\overline{OE}$ high before $\overline{CAS}$ transitions high and keep $\overline{OE}$ high for t_{CHO} (hold time, $\overline{OE}$ from $\overline{CAS}$) past the $\overline{CAS}$ transition. This disables the DQs and they remain disabled, regardless of $\overline{OE}$, until $\overline{CAS}$ falls again. The second method is to have $\overline{OE}$ low as $\overline{CAS}$ transitions high. Then $\overline{OE}$ can pulse high for a minimum of t_{OEP} (precharge time, $\overline{OE}$) anytime during $\overline{CAS}$ high time, disabling the DQs regardless of further transitions on $\overline{OE}$ until $\overline{CAS}$ falls again (see Figure 8).

write-enable ($\overline{W}$)

The read- or write mode is selected through $\overline{W}$. A logic high on $\overline{W}$ selects the read mode, and a logic low selects the write mode. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation with $\overline{OE}$ grounded. If $\overline{W}$ goes low in an extended-data-out read cycle, the DQs are disabled as long as $\overline{CAS}$ is high (see Figure 8).

data in/data out (DQ0–DQ7)

Data is written during a write- or read-modify-write cycle. Depending on the mode of operation, the latter of the falling edges of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch with setup-and-hold times referenced to the latter edge. The DQs drive valid data after all access times are met and the data remains valid except in cases described in the $\overline{W}$ and $\overline{OE}$ descriptions.

$\overline{RAS}$-only refresh

A refresh operation must be performed once every 32 ms (128 ms for TMS427809AP) to retain data. This can be achieved by strobing each of the 2048 rows (A0–A10). A normal read- or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

A hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored and the refresh address is generated internally.

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

CBR refresh is performed by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive CBR-refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

battery-backup refresh

TMS427809AP

A low-power battery-backup refresh mode that requires less than 350 μA of refresh current is available on the TMS427809AP. Data integrity is maintained using CBR refresh with a period of 62.5 μs while holding $\overline{RAS}$ low for less than 300 ns. To minimize current consumption, all input levels must be at CMOS levels (V_{IL} < 0.2 V, V_{IH} > V_{CC} – 0.2 V).

self-refresh (TMS427809AP)

The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low, then $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 μs. The chip is refreshed internally by an on-board oscillator. No external address is required because the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}. Upon exiting self-refresh mode, a burst refresh (refreshes a full set of row addresses) must be executed before continuing with normal operation to ensure that the DRAM is fully refreshed.

power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after power up to the full V_{CC} level. These eight initialization cycles must include at least one refresh ($\overline{RAS}$-only or CBR) cycle.

absolute maximum ratings over ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (TMS417809A) . . . . . – 1 V to 7 V
Supply voltage range, V_{CC} (TMS427809A, TMS427809AP) . . . . . – 0.5 V to 4.6 V
Voltage range on any pin (TMS417809A) (see Note 1) . . . . . – 1 V to 7 V
Voltage range on any pin (TMS427809A, TMS427809AP) (see Note 1) . . . . . – 0.5 V to 4.6 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Ambient temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		TMS417809A			TMS427809A/P			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	3	3.3	3.6	V
V_{SS}	Supply voltage		0			0		V
V_{IH}	High-level input voltage	2.4		6.5	2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage‡	– 1		0.8	– 0.3		0.8	V
T_A	Ambient temperature	0		70	0		70	°C

‡ The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted)

TMS417809A

PARAMETER		TEST CONDITIONS†	'417809A-50		'417809A-60		'417809A-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}‡§	Average read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle		130		110		100	mA
I_{CC2}	Average standby current	V_{IH} = 2.4 V (TTL), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		1		1		1	
I_{CC3}‡§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		130		110		100	mA
I_{CC4}‡¶	Average EDO current	V_{CC} = 5.5 V, t_{HPC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling		110		90		80	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}

electrical characteristics over recommended ranges of supply voltage and ambient conditions (unless otherwise noted) (continued)

TMS427809A/P

PARAMETER		TEST CONDITIONS†		'427809A/P-50		'427809A/P-60		'427809A/P-70		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = – 100 µA	LVCMOS	V_{CC}–0.2		V_{CC}–0.2		V_{CC}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{CC} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	$\overline{V_{CC}}$ = 3.6 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Average read- or write-cycle current	V_{CC} = 3.6 V, Minimum cycle			120		100		90	mA
I_{CC2}	Average standby current	V_{IH} = 2 V (LVTTL) After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'427809A		2		2		2	mA
			'427809AP		1		1		1	
		V_{IH} = V_{CC} – 0.2 V (LVCMOS), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'427809A		1		1		1	mA
			'427809AP		150		150		150	µA
I_{CC3}‡§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	$\overline{V_{CC}}$ = 3.6 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only refresh), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			120		100		90	mA
I_{CC4}‡¶	Average EDO current	$\overline{V_{CC}}$ = 3.6 V, $t_{\overline{HPC}}$ = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling			110		90		80	mA
I_{CC6}#	Average self-refresh current	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			200		200		200	µA
I_{CC10}#	Battery back-up operating current (equivalent refresh time is 128 ms), CBR only	t_{RC} = 62.5 µs, t_{RAS} ≤ 300 ns V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			350		350		350	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}
# For TMS427809AP only

capacitance over recommended ranges of supply voltage and ambient temperature, f = 1 MHz (see Note 2)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A10		5	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_o	Output capacitance†		7	pF

† $\overline{CAS}$ and $\overline{OE}$ = V_{IH} to disable outputs

NOTE 2: V_{CC} = NOM supply voltage ±10%, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and ambient temperature (see Note 3)

PARAMETER		’417809A-50 ’427809A/P-50		’417809A-60 ’427809A/P-60		’417809A-70 ’427809A/P-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address (see Note 4)		25		30		35	ns
t_{CAC}	Access time from $\overline{CAS}$ (see Note 4)		13		15		18	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge (see Note 4)		28		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$ (see Note 4)		50		60		70	ns
t_{OEA}	Access time from $\overline{OE}$ (see Note 4)		13		15		18	ns
t_{CLZ}	Delay time, $\overline{CAS}$ to output in low impedance	0		0		0		ns
t_{REZ}	Output buffer turn-off delay from $\overline{RAS}$ (see Note 5)	3	13	3	15	3	18	ns
t_{CEZ}	Output buffer turn-off delay from $\overline{CAS}$ (see Note 5)	3	13	3	15	3	18	ns
t_{OEZ}	Output buffer turn-off delay from $\overline{OE}$ (see Note 5)	3	13	3	15	3	18	ns
t_{WEZ}	Output buffer turn-off delay from $\overline{W}$ (see Note 5)	3	13	3	15	3	18	ns

NOTES: 3. With ac parameters, it is assumed that t_T = 2 ns.
4. For TMS427809A/P, access times are measured with output reference levels of V_{OH} = 2 V and V_{OL} = 0.8 V.
5. The maximum values of t_{REZ}, t_{CEZ}, t_{OEZ}, and t_{WEZ} are specified when the output is no longer driven. Data-in should not be enabled until one of the applicable maximum values is satisfied.

EDO timing requirements (see Note 3)

		’417809A-50 ’427809A/P-50		’417809A-60 ’427809A/P-60		’417809A-70 ’427809A/P-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{HPC}	Cycle time, EDO page mode, read-write	20		25		30		ns
t_{PRWC}	Cycle time, EDO read-write	57		68		78		ns
t_{CSH}	Delay time, $\overline{RAS}$ active to $\overline{CAS}$ precharge	40		48		58		ns
t_{CHO}	Hold time, $\overline{OE}$ from $\overline{CAS}$	7		10		10		ns
t_{DOH}	Hold time, output from $\overline{CAS}$	5		5		5		ns
t_{CAS}	Pulse duration, $\overline{CAS}$ active (see Note 6)	8	10000	10	10000	12	10000	ns
t_{WPE}	Pulse duration, $\overline{W}$ active (output disable only)	7		7		7		ns
t_{CP}	Pulse duration, $\overline{CAS}$ precharge	8		10		10		ns
t_{OCH}	Setup time, $\overline{OE}$ before $\overline{CAS}$	8		10		10		ns
t_{OEP}	Precharge time, $\overline{OE}$	5		5		5		ns

NOTES: 3. With ac parameters, it is assumed that t_T = 2 ns.
6. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.

ac timing requirements (see Note 3)

		’417809A-50 ’427809A/P-50		’417809A-60 ’427809A/P-60		’417809A-70 ’427809A/P-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write	84		104		124		ns
t_{RWC}	Cycle time, read-write	111		135		160		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ active, fast page mode (see Note 7)	50	100 000	60	100 000	70	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ active, non-page mode (see Note 7)	50	10 000	60	10 000	70	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ precharge	30		40		50		ns
t_{WP}	Pulse duration, write command	8		10		10		ns
t_{RASS}	Pulse duration, $\overline{RAS}$ active, self refresh (see Note 8)	100		100		100		µs
t_{RPS}	Pulse duration, $\overline{RAS}$ precharge after self refresh	90		110		130		ns
t_{ASC}	Setup time, column address	0		0		0		ns
t_{ASR}	Setup time, row address	0		0		0		ns
t_{DS}	Setup time, data in (see Note 9)	0		0		0		ns
t_{RCS}	Setup time, read command	0		0		0		ns
t_{CWL}	Setup time, write command before $\overline{CAS}$ precharge	8		10		12		ns
t_{RWL}	Setup time, write command before $\overline{RAS}$ precharge	8		10		12		ns
t_{WCS}	Setup time, write command before $\overline{CAS}$ active (early-write only)	0		0		0		ns
t_{WRP}	Setup time, $\overline{W}$ high before $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{CSR}	Setup time, $\overline{CAS}$ referenced to $\overline{RAS}$ (CBR refresh only)	5		5		5		ns
t_{CAH}	Hold time, column address	8		10		12		ns
t_{DH}	Hold time, data in (see Note 9)	8		10		12		ns
t_{RAH}	Hold time, row address	8		10		10		ns
t_{RCH}	Hold time, read command referenced to $\overline{CAS}$ (see Note 10)	0		0		0		ns
t_{RRH}	Hold time, read command referenced to $\overline{RAS}$ (see Note 10)	0		0		0		ns
t_{WCH}	Hold time, write command during $\overline{CAS}$ active (early-write only)	8		10		12		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$	8		10		10		ns
t_{WRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{CHR}	Hold time, $\overline{CAS}$ referenced to $\overline{RAS}$ (CBR refresh only)	10		10		10		ns
t_{OEH}	Hold time, $\overline{OE}$ command	13		15		18		ns
t_{RHCP}	Hold time, $\overline{RAS}$ active from $\overline{CAS}$ precharge	28		35		40		ns
t_{CHS}	Hold time, $\overline{CAS}$ referenced to $\overline{RAS}$ (self refresh only)	– 50		– 50		– 50		ns
t_{AWD}	Delay time, column address to write command (read-write only)	42		49		57		ns
t_{CRP}	Delay time, $\overline{CAS}$ precharge to $\overline{RAS}$	5		5		5		ns

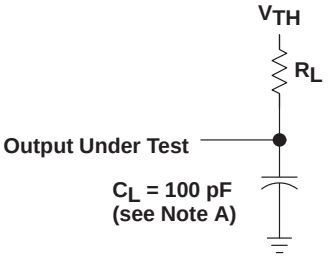
NOTES: 3. With ac parameters, it is assumed that t_T = 2 ns.
7. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
8. During the period of 10 µs ≤ t_{RASS} ≤100 µs, the device is in a transition state from normal-operation mode to self-refresh mode.
9. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

ac timing requirements (see Note 3) (continued)

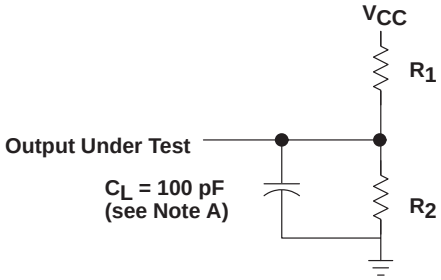
			’417809A-50 ’427809A/P-50		’417809A-60 ’427809A/P-60		’417809A-70 ’427809A/P-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CWD}	Delay time, $\overline{CAS}$ to write command (read-write only)		30		34		40		ns
t_{OED}	Delay time, $\overline{OE}$ to data in		13		15		18		ns
t_{RAD}	Delay time, $\overline{RAS}$ to column address (see Note 11)		10	25	12	30	12	35	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ precharge		25		30		35		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ precharge		18		20		25		ns
t_{RCD}	Delay time, $\overline{RAS}$ to $\overline{CAS}$ (see Note 11)		12	37	14	45	14	52	ns
t_{RPC}	Delay time, $\overline{RAS}$ precharge to $\overline{CAS}$		5		5		5		ns
t_{RSH}	Delay time, $\overline{CAS}$ active to $\overline{RAS}$ precharge		8		10		12		ns
t_{RWD}	Delay time, $\overline{RAS}$ to write command (read-write only)		67		79		92		ns
t_{CPW}	Delay time, $\overline{CAS}$ precharge to write command (read-write only)		45		54		62		ns
t_{REF}	Refresh time interval	’417809A		32		32		32	ms
		’427809A		32		32		32	
		’427809AP		128		128		128	
t_T	Transition time		2	30	2	30	2	30	ns

NOTES: 3. With ac parameters, it is assumed that t_T = 2 ns.
11. The maximum value is specified only to ensure access time.

PARAMETER MEASUREMENT INFORMATION



(a) LOAD CIRCUIT



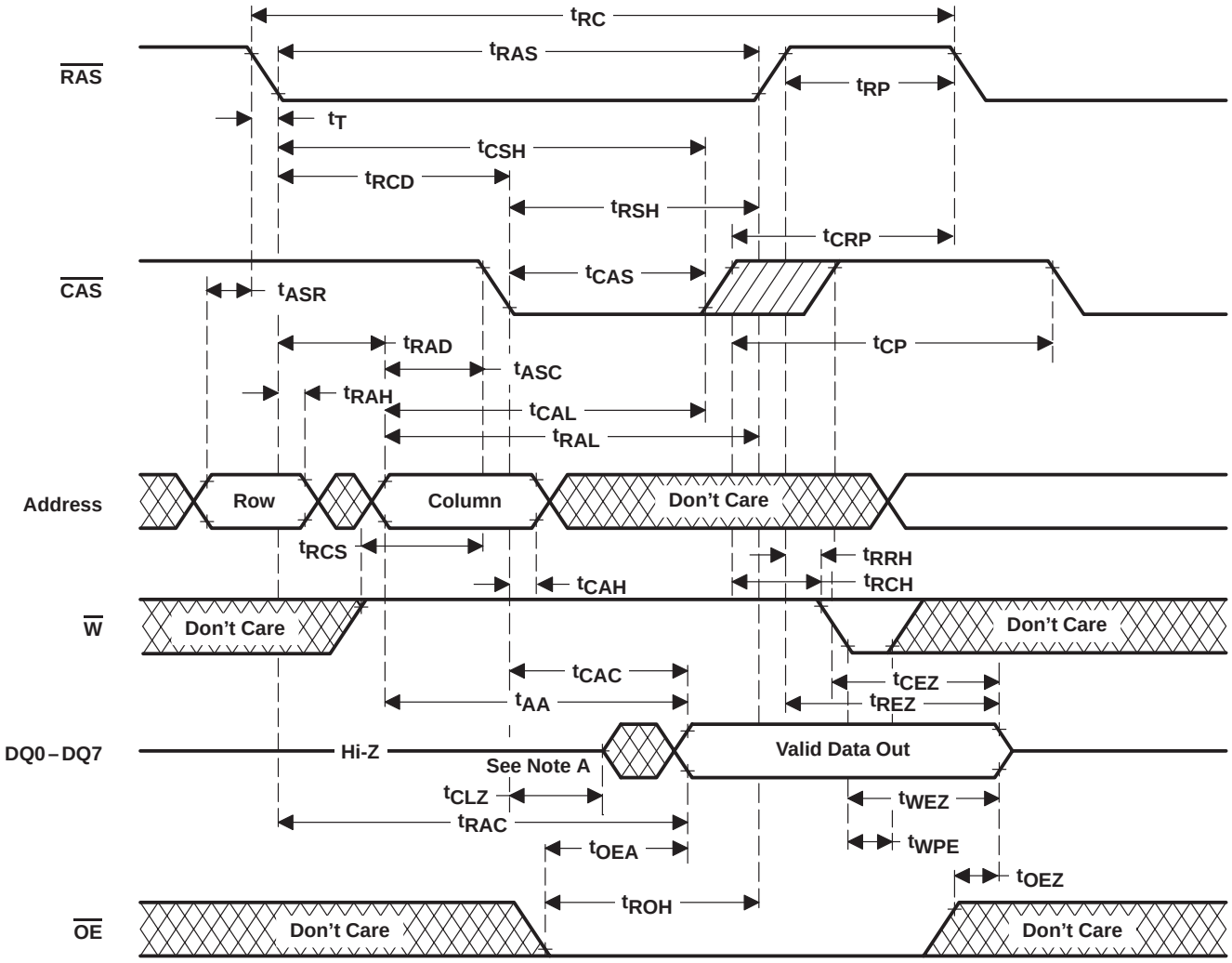
(b) ALTERNATE LOAD CIRCUIT

NOTE A: C_L includes probe and fixture capacitance.

DEVICE	V_{CC} (V)	R_1 (Ω)	R_2 (Ω)	V_{TH} (V)	R_L (Ω)
’417809A	5	828	295	1.31	218
’427809A/P	3.3	1178	868	1.4	500

Figure 1. Load Circuits for Timing Parameters

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 2. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

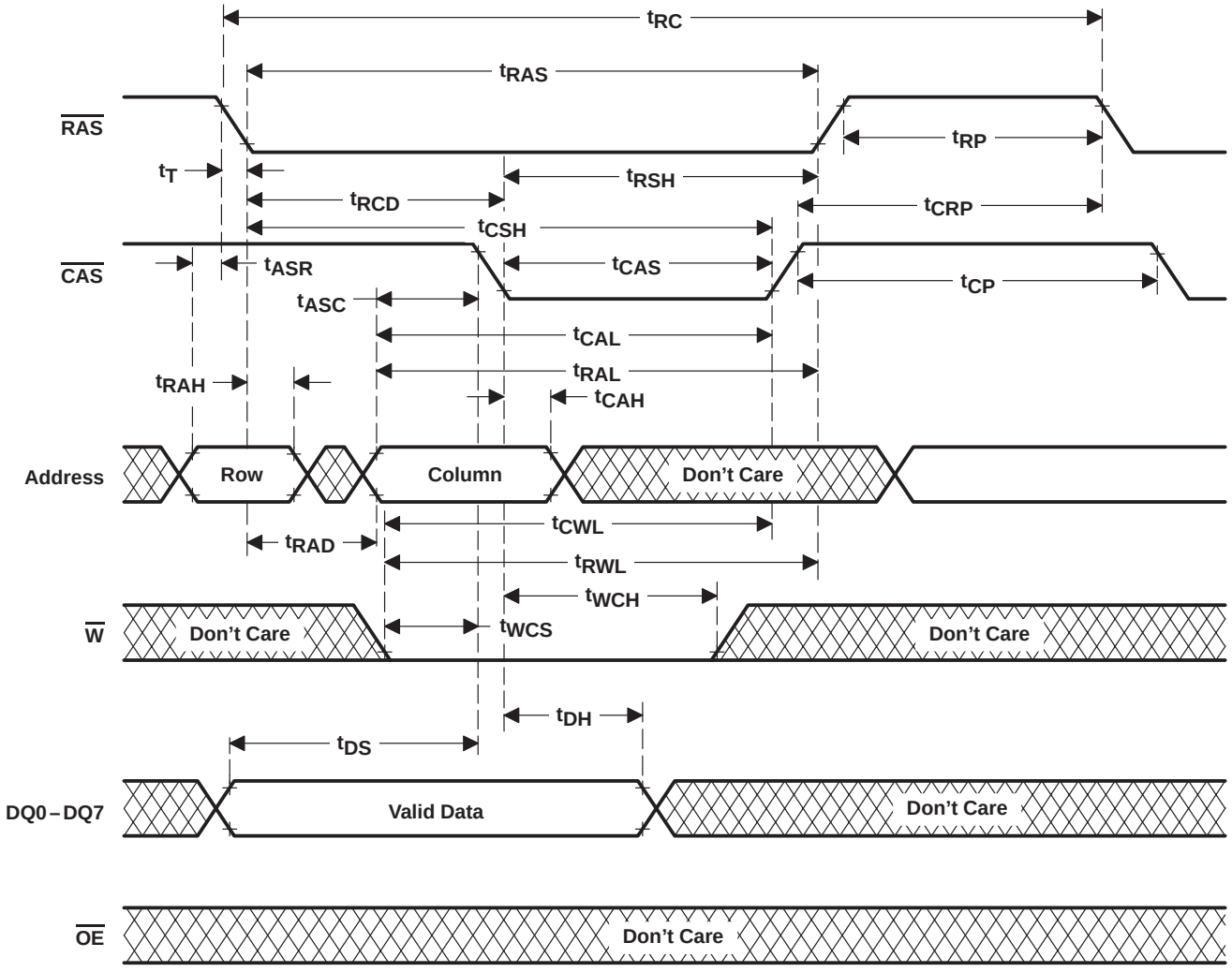


Figure 3. Early-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

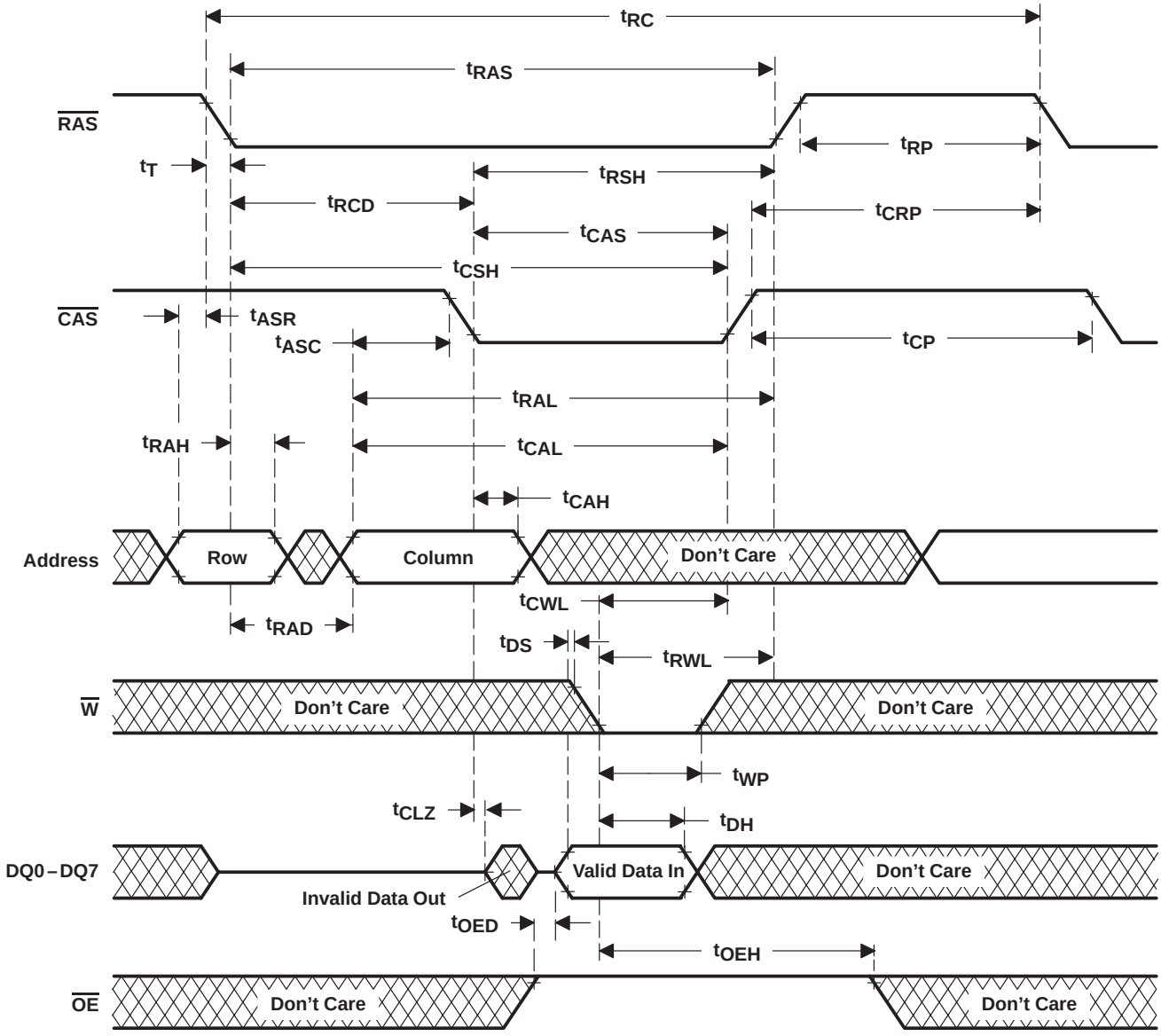
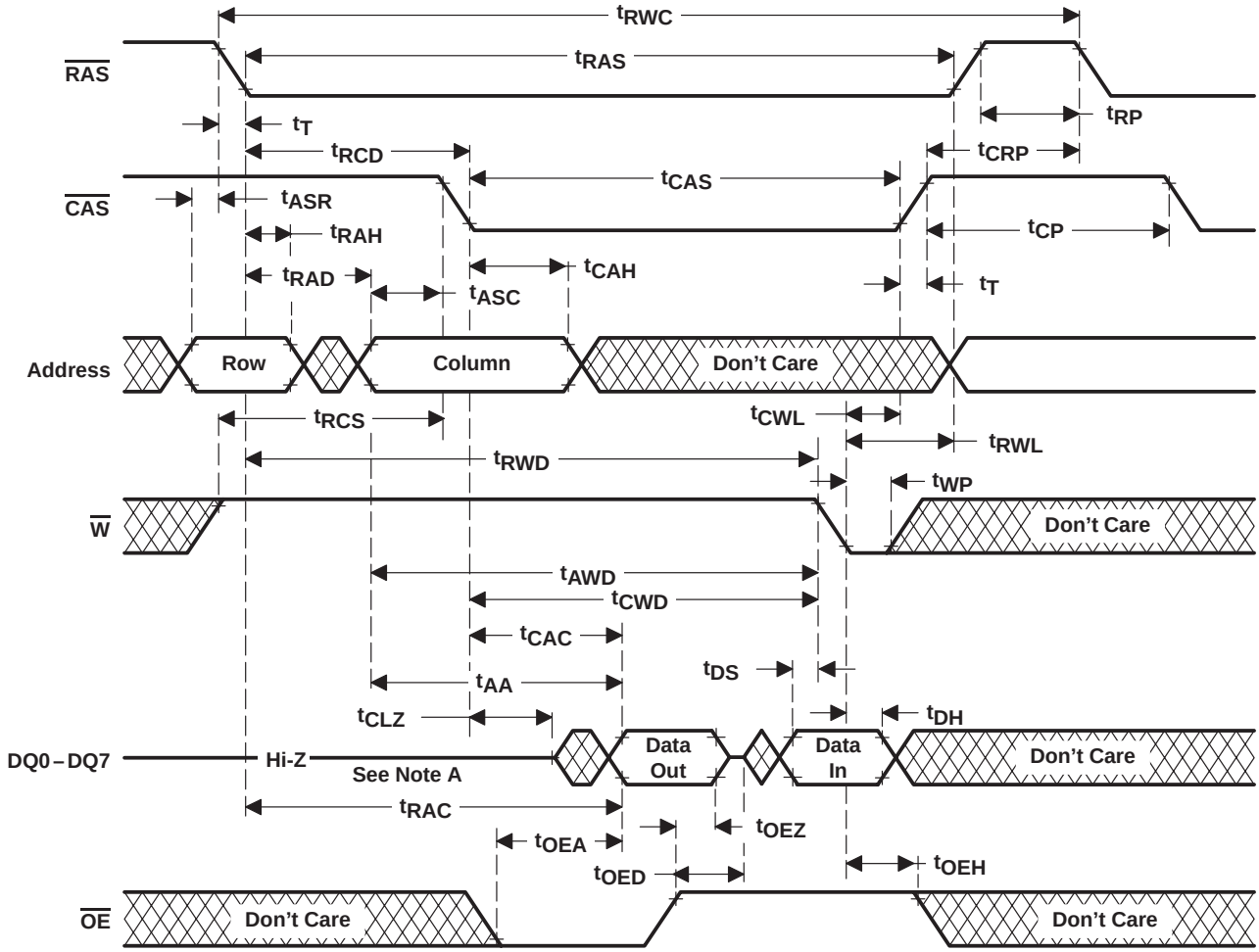


Figure 4. Write-Cycle Timing

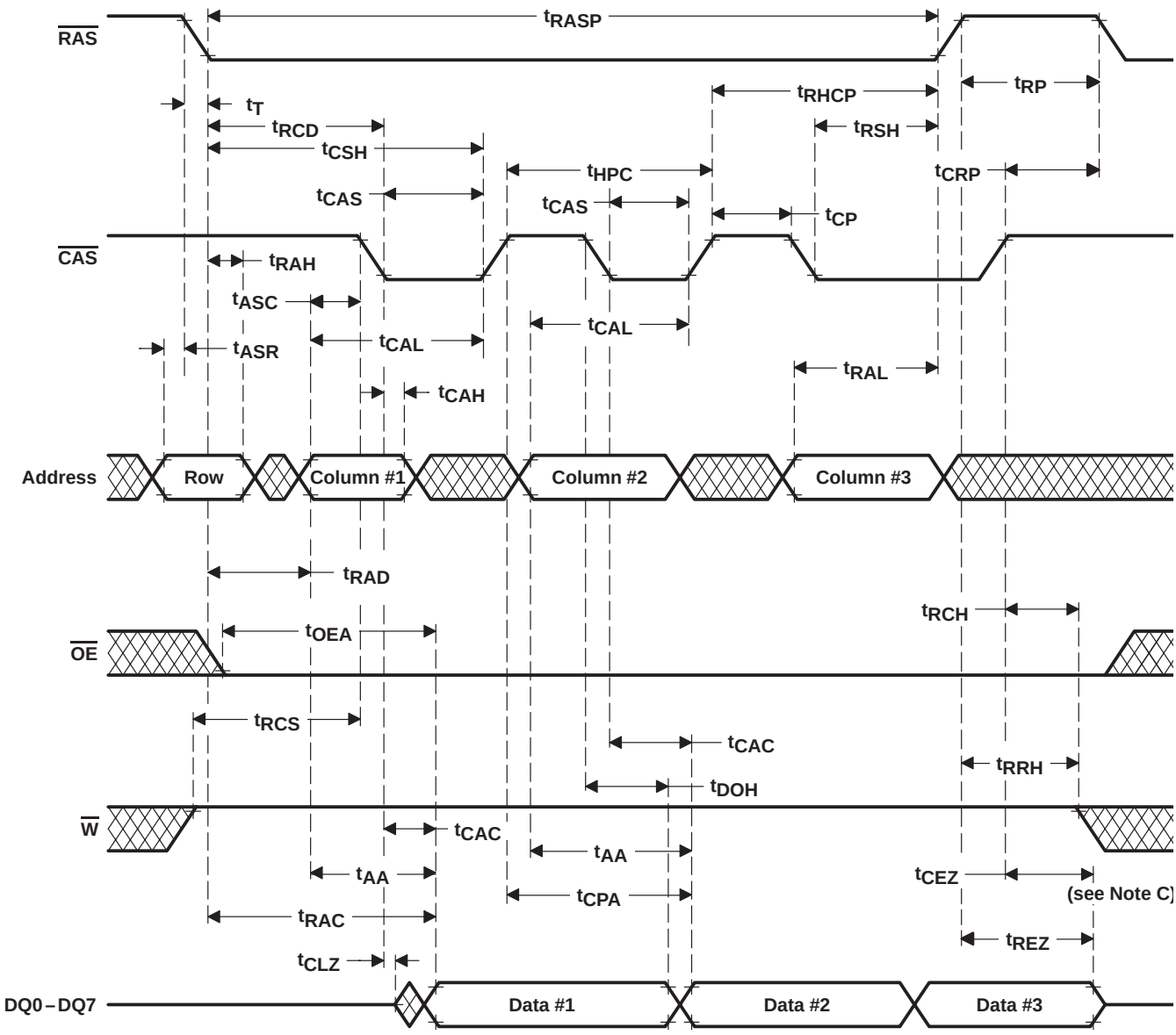
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 5. Read-Write-Cycle Timing

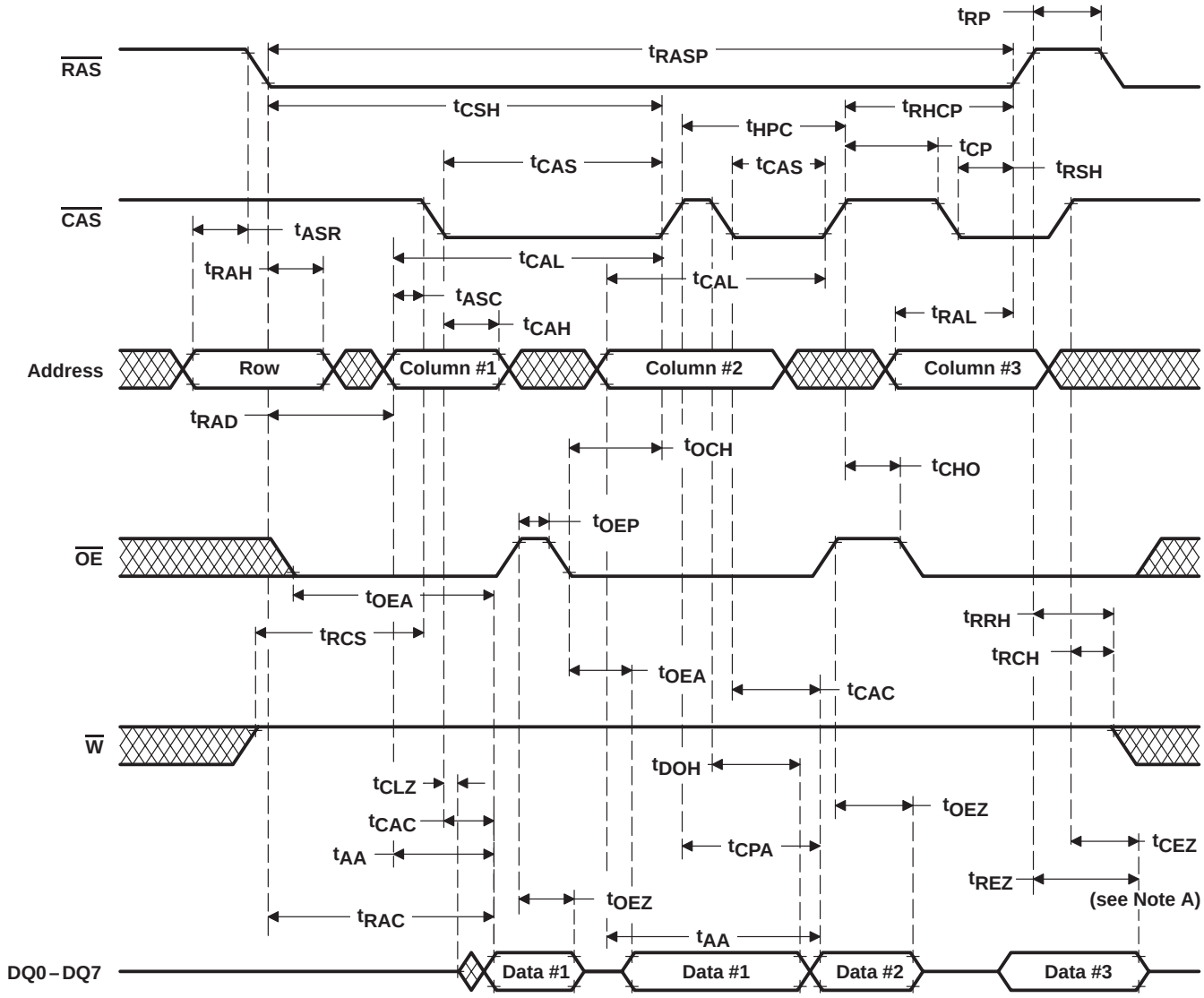
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. Access time is t_{CPA}-, t_{AA}-, or t_{CAC}-dependent.
C. Output is turned off by t_{CEZ} if $\overline{RAS}$ goes high during $\overline{CAS}$ low.

Figure 6. EDO Read Cycle

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output is turned off by t_{CEZ} if $\overline{RAS}$ goes high during $\overline{CAS}$ low.

Figure 7. EDO Read-Cycle With $\overline{OE}$ Control

PARAMETER MEASUREMENT INFORMATION

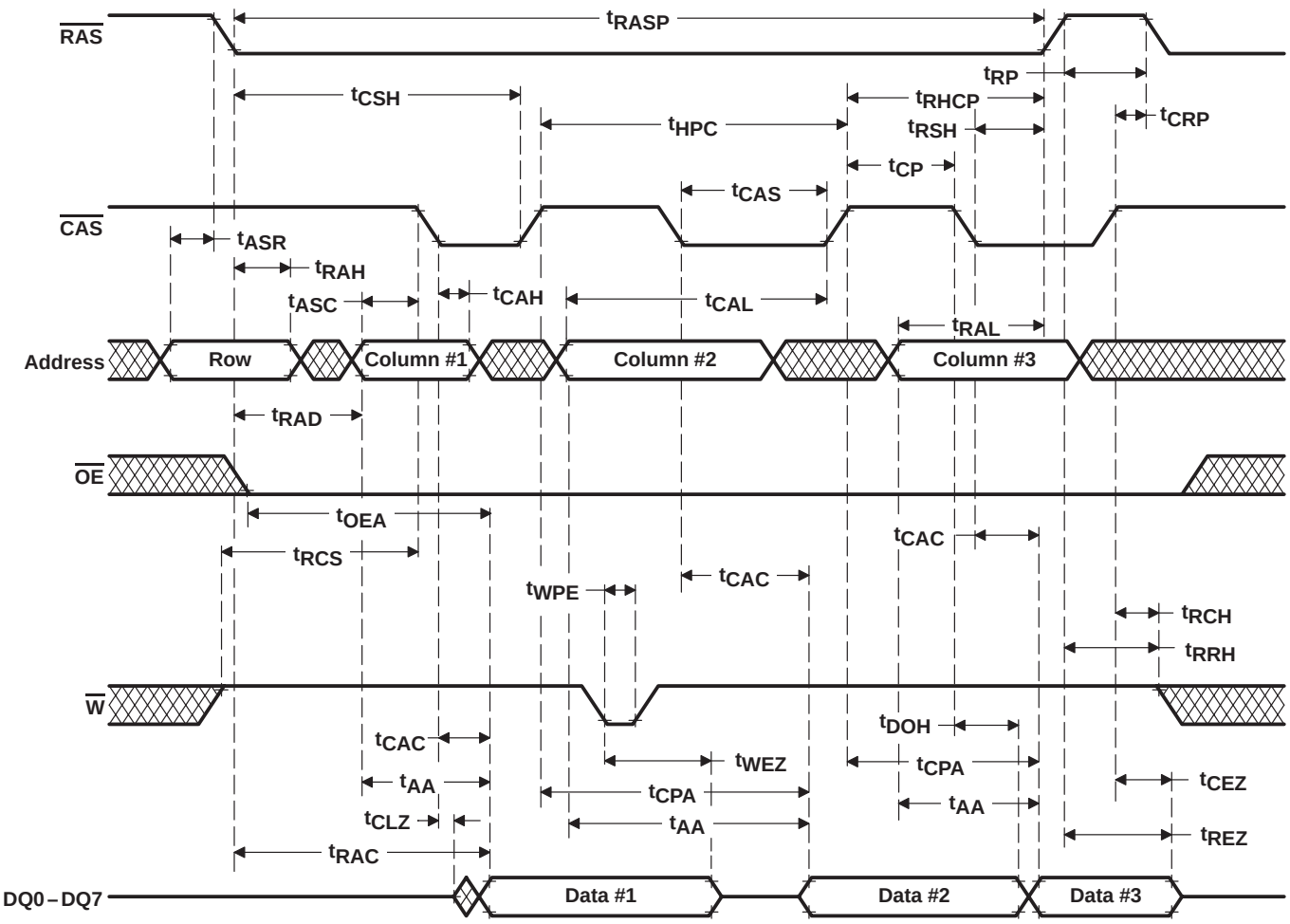
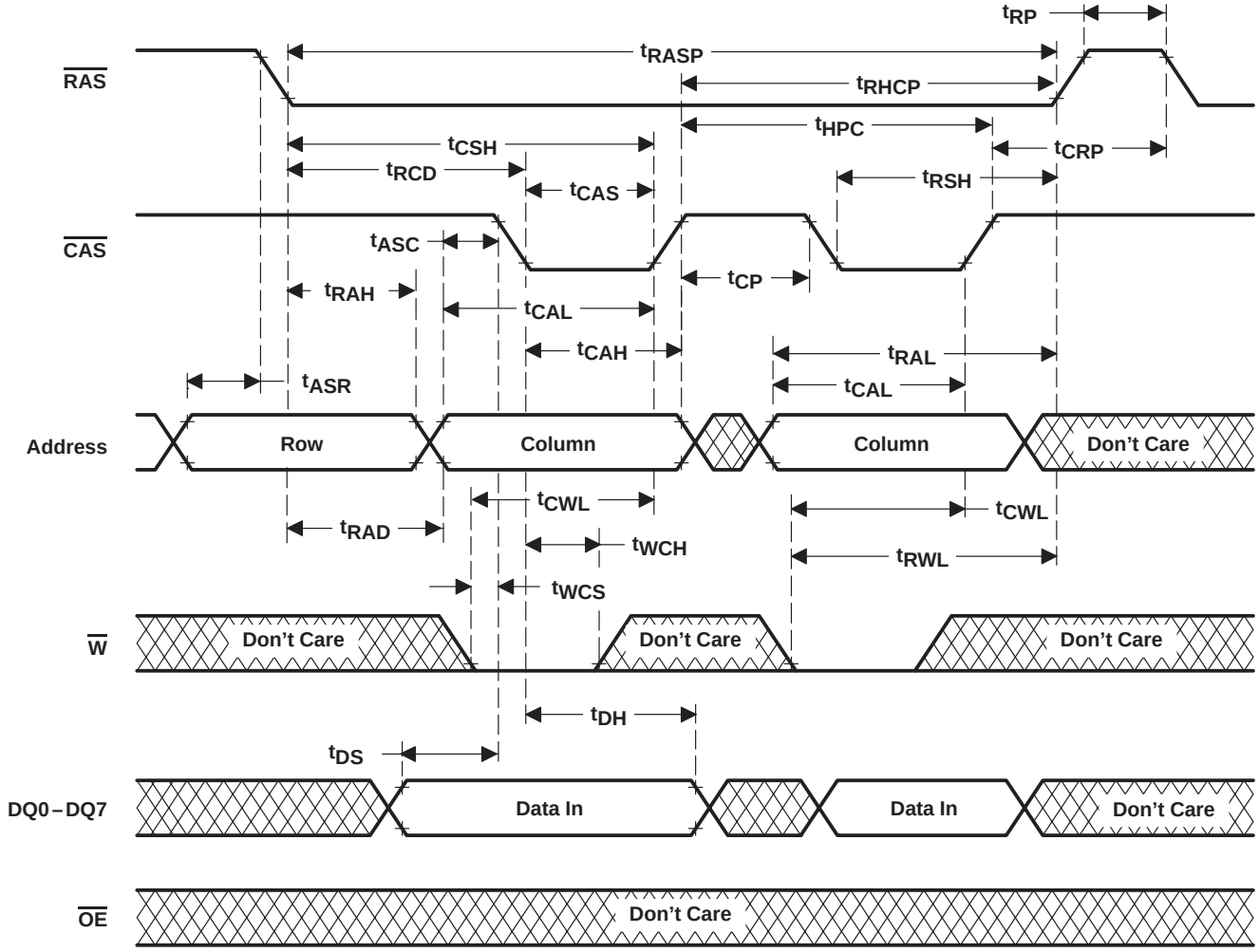


Figure 8. EDO Read-Cycle With $\overline{W}$ Control

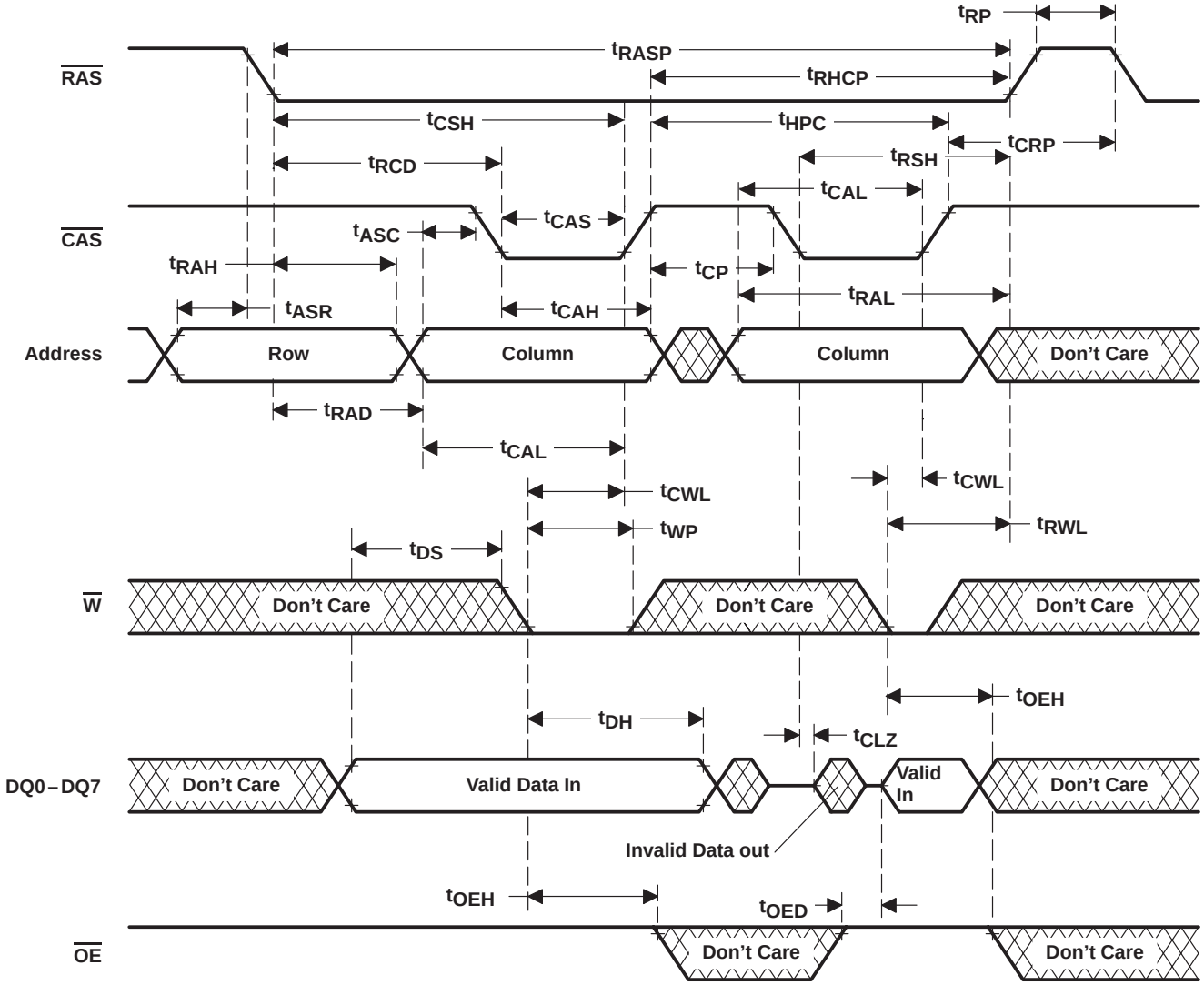
PARAMETER MEASUREMENT INFORMATION



NOTE A: A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 9. EDO-Early-Write-Cycle Timing

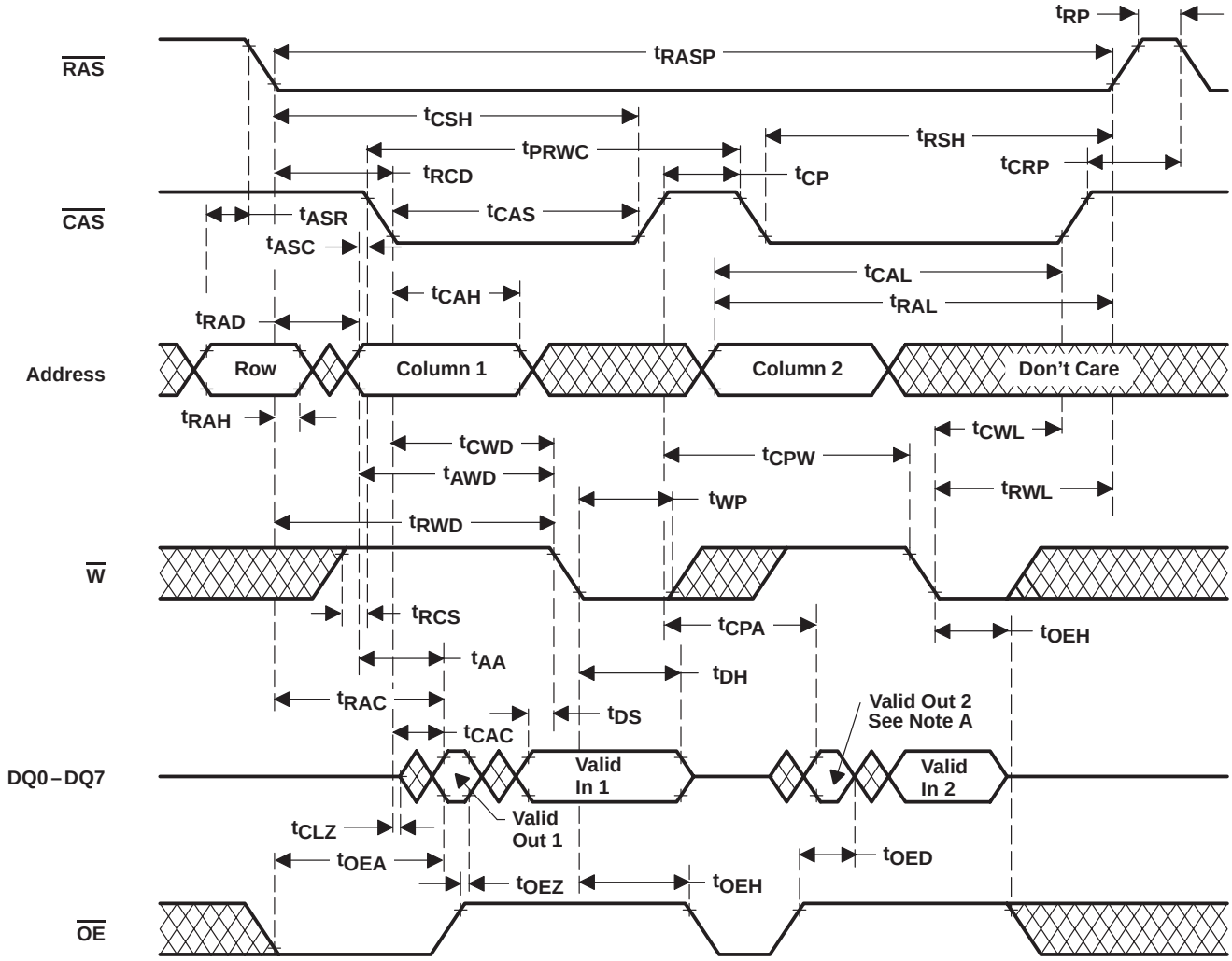
PARAMETER MEASUREMENT INFORMATION



NOTE A: A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 10. EDO Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read- and write-timing specifications are not violated.

Figure 11. EDO Read-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

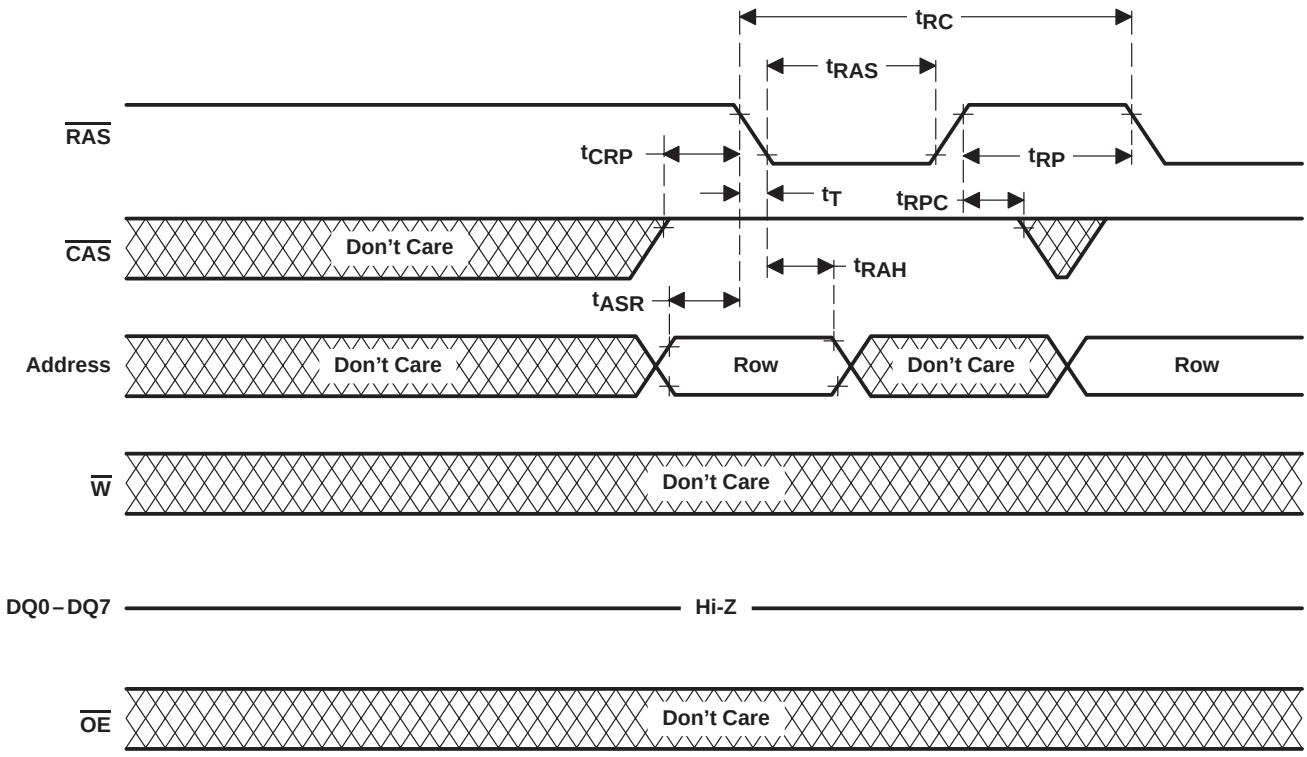


Figure 12. $\overline{\text{RAS}}$-Only Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

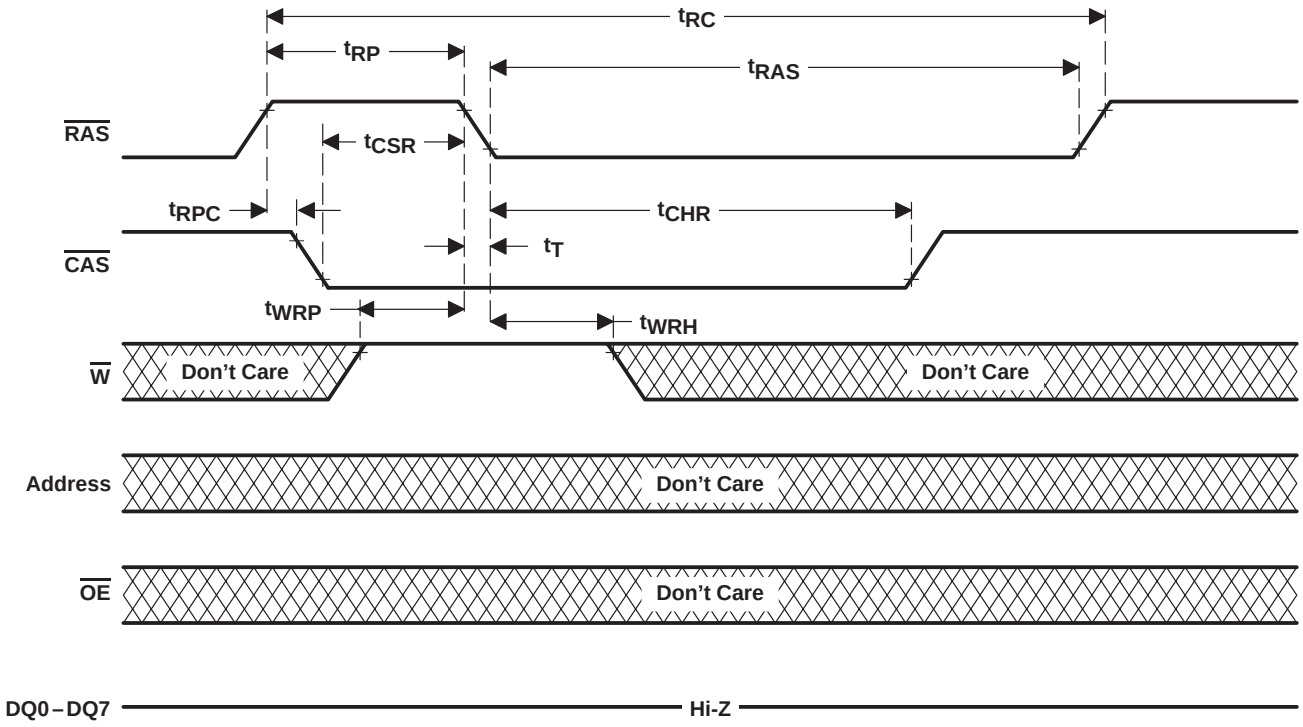


Figure 13. Automatic-CBR-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

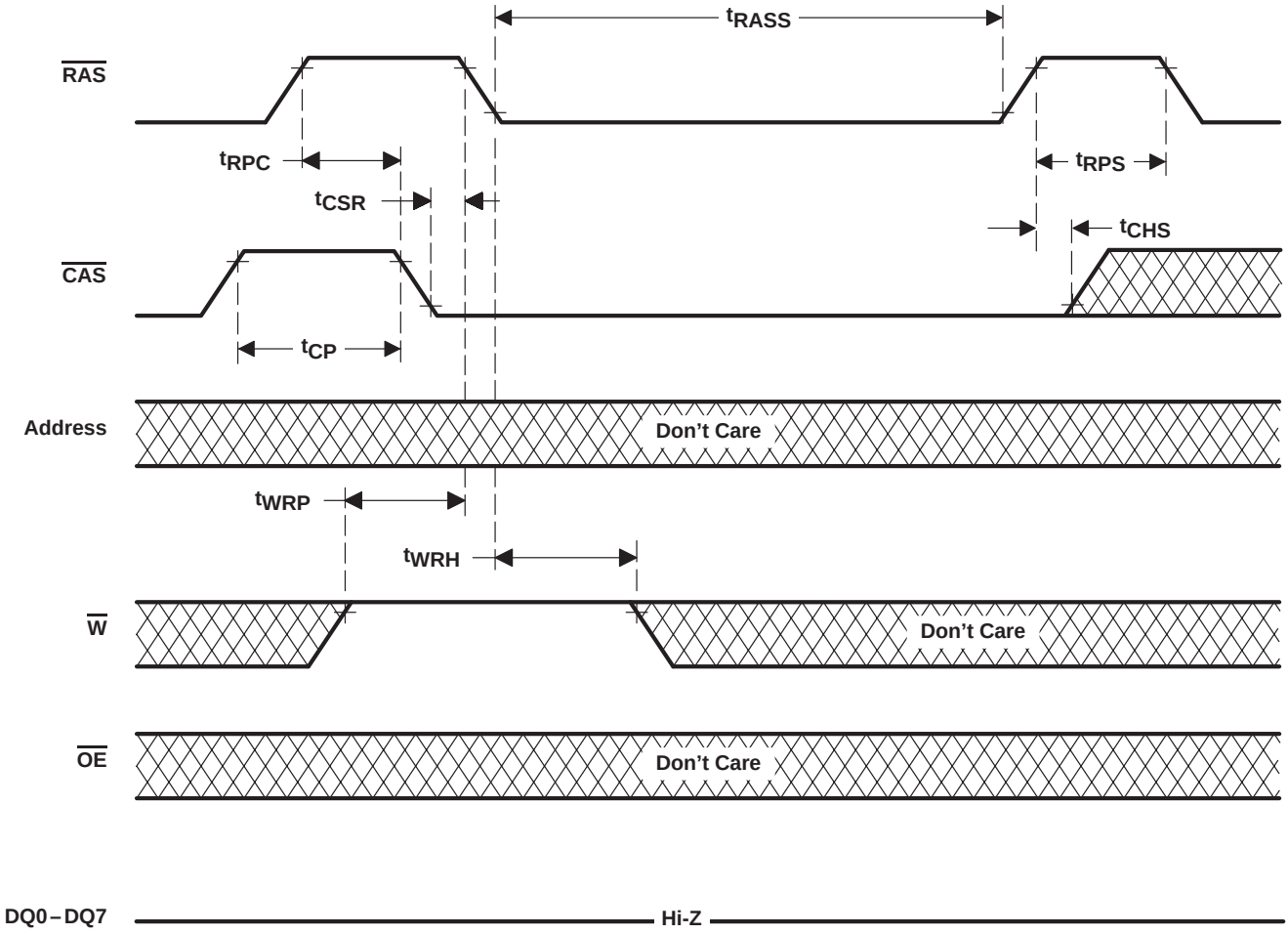


Figure 14. Self-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

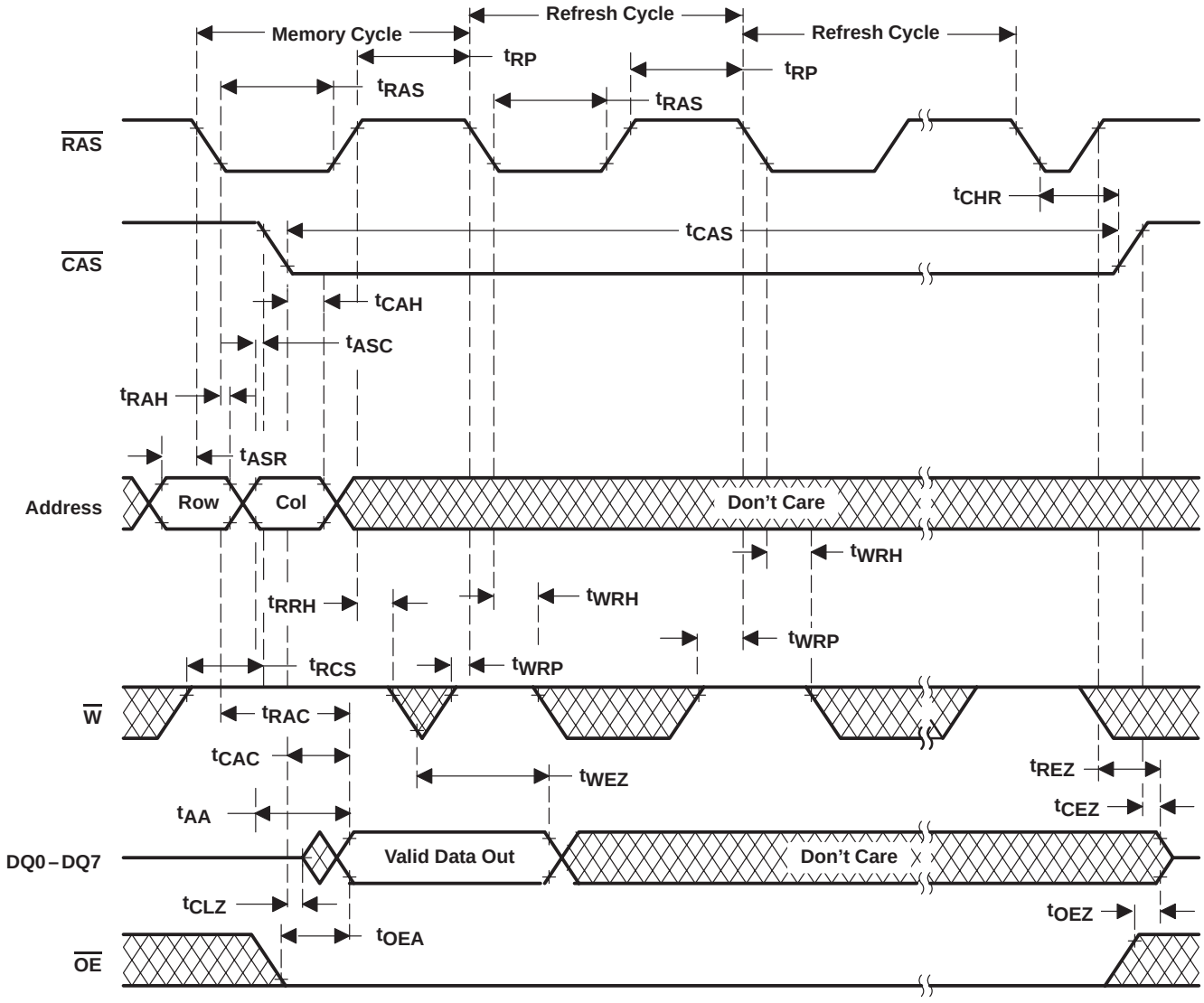


Figure 15. Hidden-Refresh-Cycle (Read) Timing

PARAMETER MEASUREMENT INFORMATION

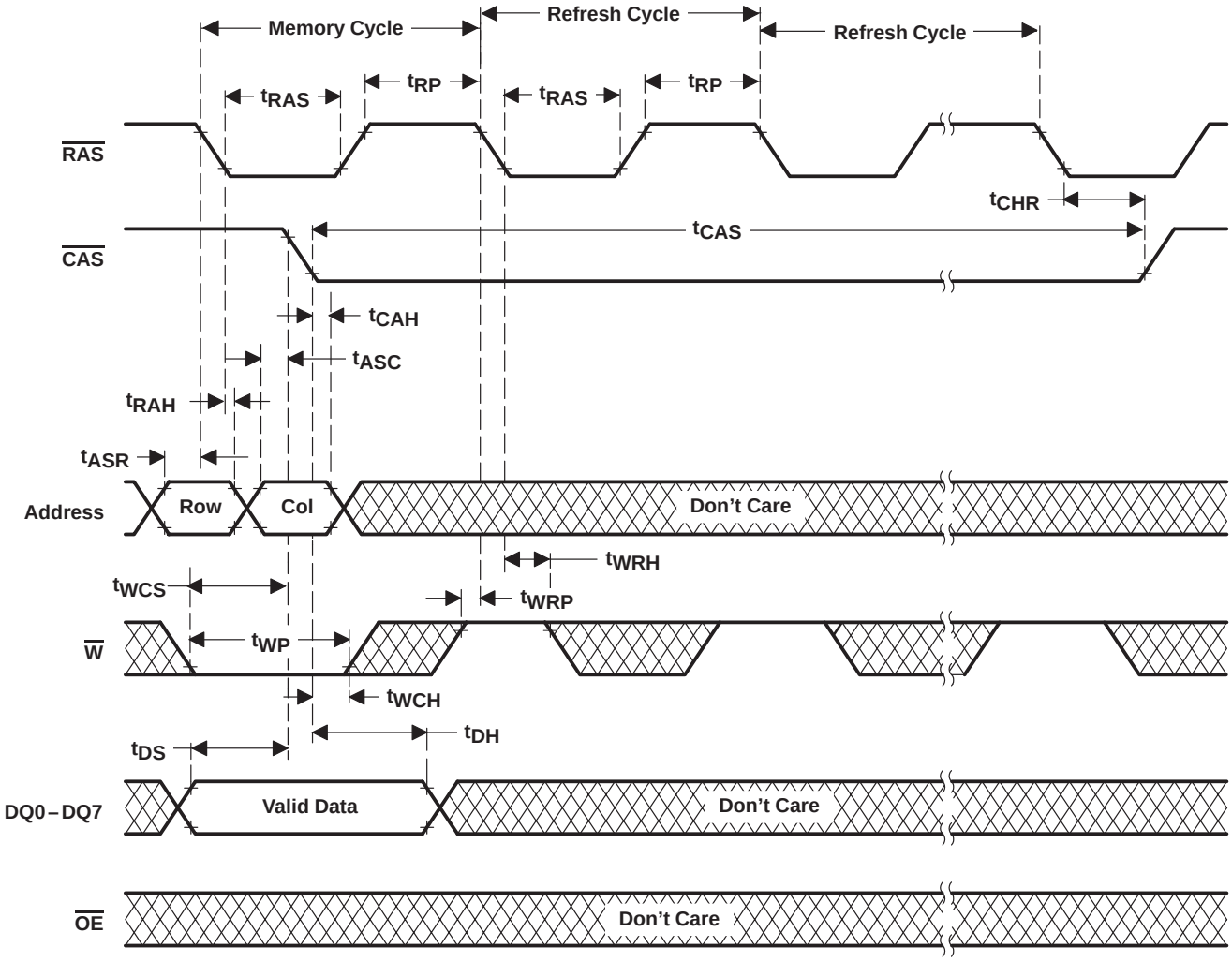
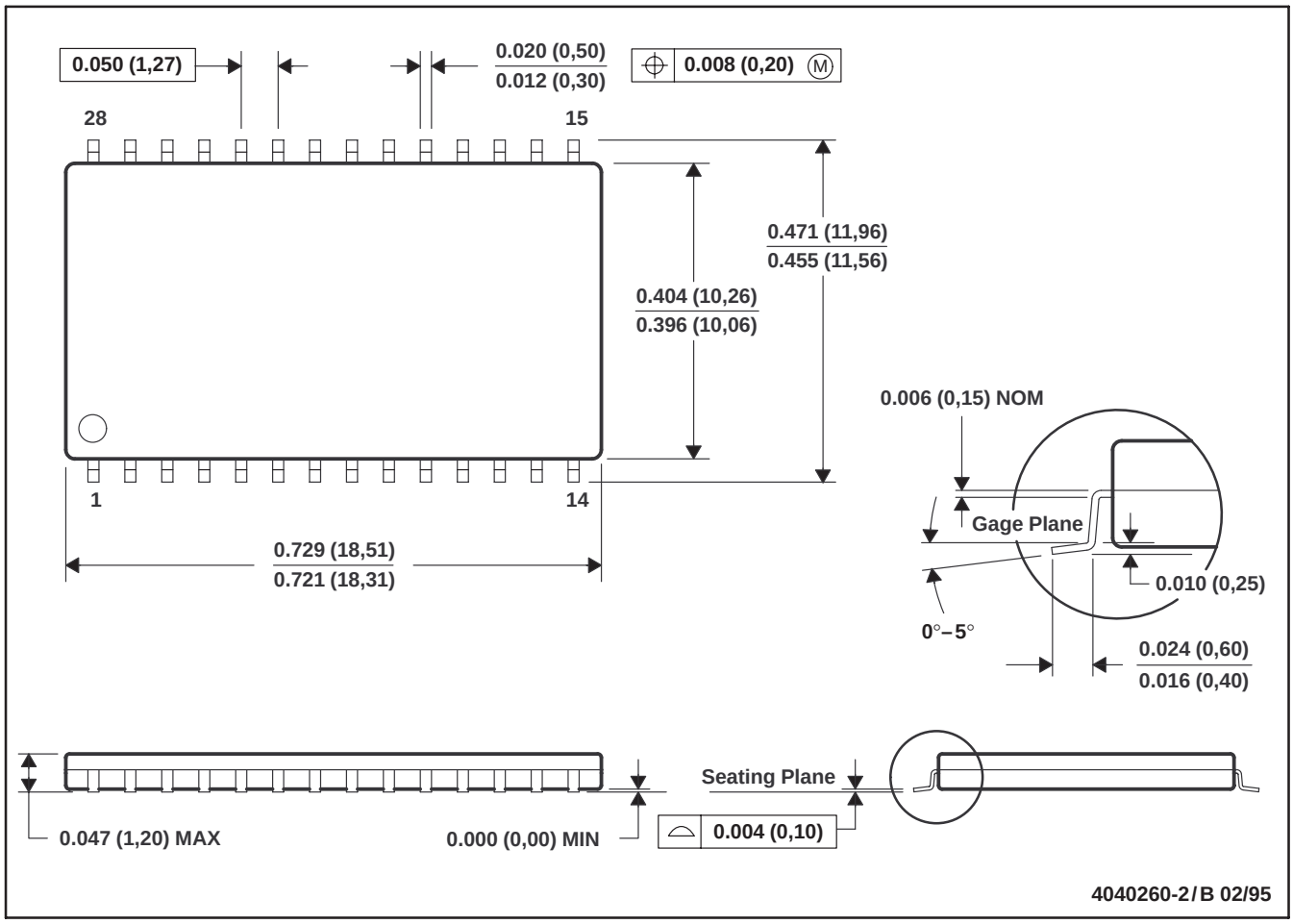


Figure 16. Hidden-Refresh-Cycle (Write) Timing

MECHANICAL DATA

DGC (R-PDSO-G28) **PLASTIC SMALL-OUTLINE PACKAGE**

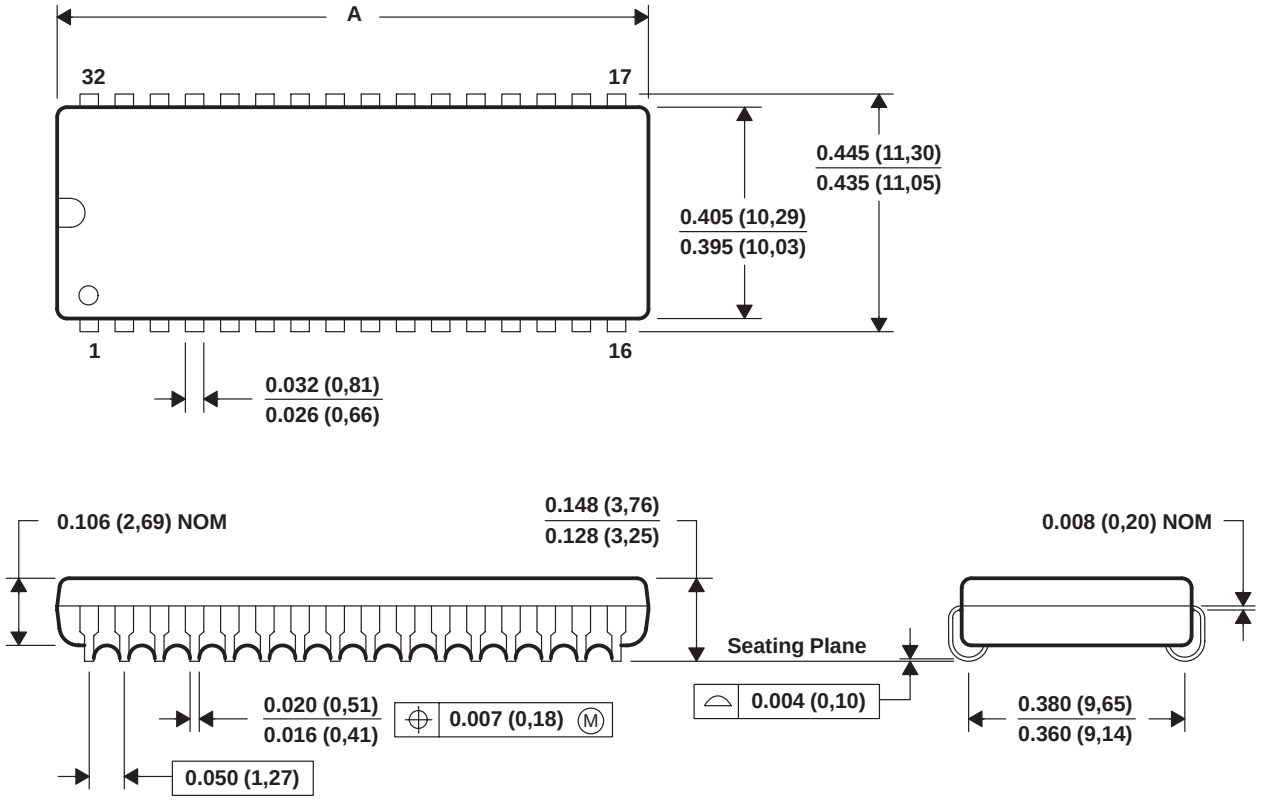


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

MECHANICAL DATA

DZ (R-PDSO-J)** **PLASTIC SMALL-OUTLINE J-LEAD PACKAGE**

32 PIN SHOWN

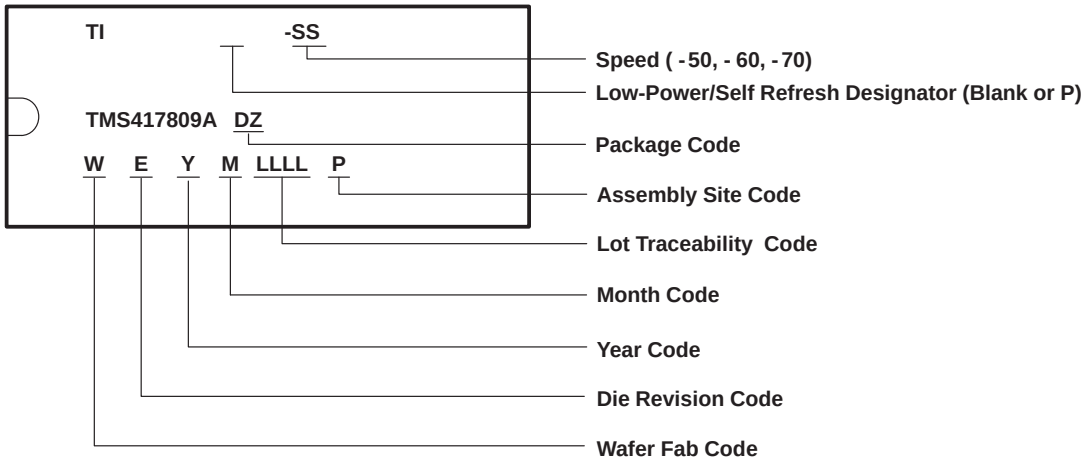


DIM \ PINS **	24	28	32	40	42
A MAX	0.730 (18,54)	0.730 (18,54)	0.830 (21,08)	1.030 (26,16)	1.080 (27,43)
A MIN	0.720 (18,29)	0.720 (18,29)	0.820 (20,83)	1.020 (25,91)	1.070 (27,18)

4040094/C 11/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,13).
D. The 24 pin package has the center two pins removed on both sides.

device symbolization (TMS417809A illustrated)



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