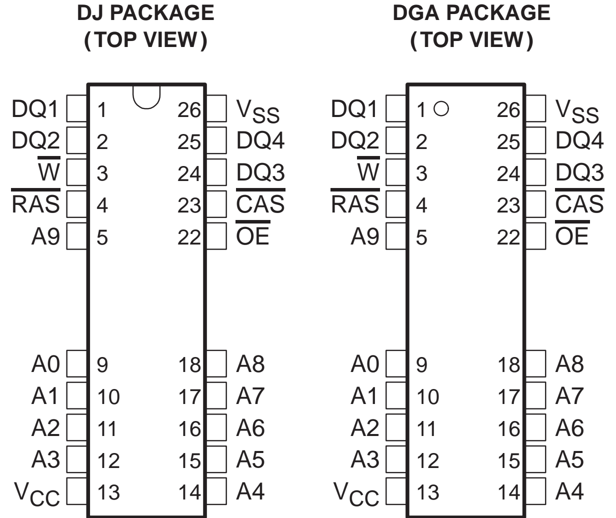
- **Organization . . . 1048576 × 4**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	EDO CYCLE (t_{HPC}) (MIN)
’44409/P-60	60 ns	15 ns	30 ns	25 ns
’44409/P-70	70 ns	18 ns	35 ns	30 ns
’44409/P-80	80 ns	20 ns	40 ns	35 ns

- **Extended Data Out (EDO) Operation**
- **CAS-Before-RAS (CBR) Refresh**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **All Inputs/Outputs and Clocks are TTL-Compatible**
- **Long Refresh Period**
  - **1 024 Cycle Refresh in 16 ns (max)**
  - **128 ms on Low Power, Self-Refresh Version (TMS44409P Only)**
- **Operating Free-Air Temperature Range 0°C to 70°C**



PIN NOMENCLATURE	
A0–A9	Address Inputs
CAS	Column-Address Strobe
DQ1 – DQ4	Data In/Data Out
OE	Output Enable
RAS	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
W	Write Enable

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description

The TMS44409 is a high-speed 4194304-bit dynamic random-access memory (DRAM) organized as 1048576 words of four bits each. This device features maximum RAS access times of 60 ns, 70 ns and 80 ns. Maximum power consumption is as low as 385 mW operating and 6 mW standby. All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS44409P is a high-speed, low-power, self-refresh version of the TMS44409 DRAM.

All versions of the TMS44409/P are offered in a 300-mil 20/26 J-lead plastic surface-mount SOJ package (DJ suffix) and a 20/26-lead plastic small outline package (DGA suffix). These devices are characterized for operation from 0°C to 70°C.

ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

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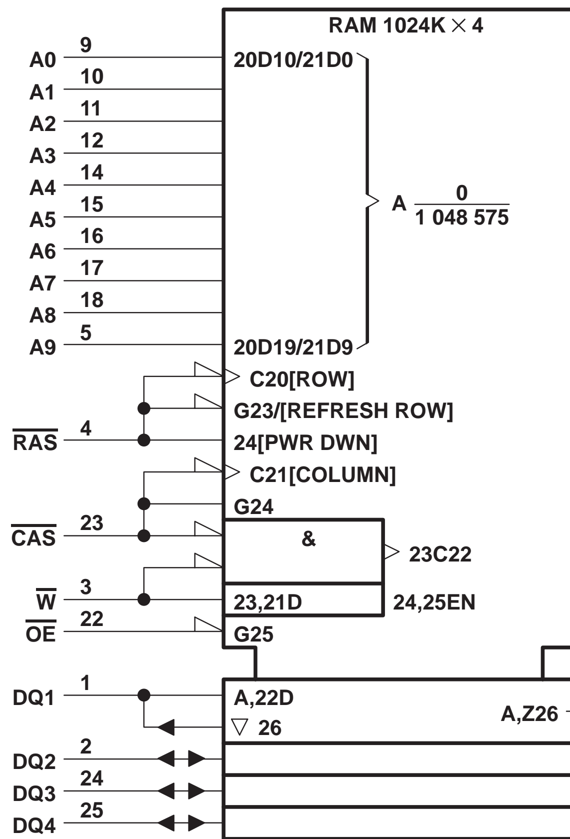
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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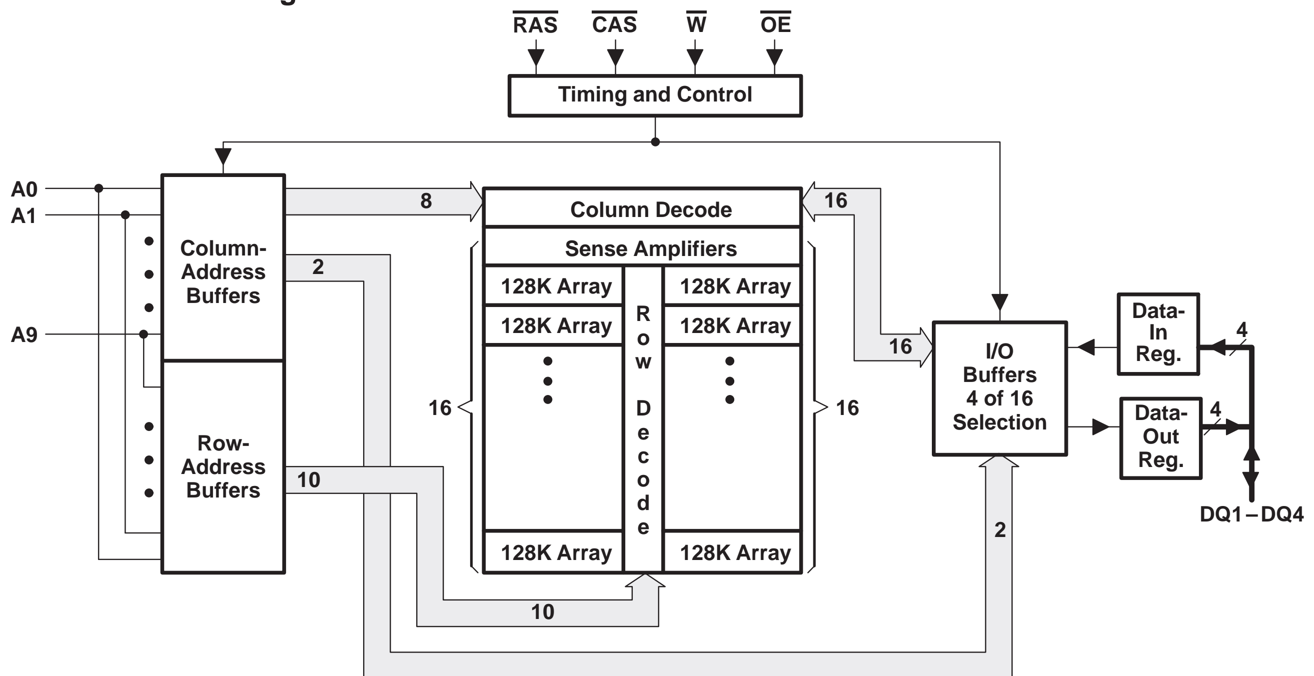
functional block diagram



operation

extended data out

Extended data out allows for data output rates of up to 40 MHz for 60-ns devices. When keeping the same row address while selecting random column addresses, the time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by t_{RASP}, the maximum $\overline{RAS}$ low time.

Extended data out does not place the DQs into the high-impedance state with the rising edge of $\overline{CAS}$. The output remains valid for the system to latch the data. After $\overline{CAS}$ goes high, the DRAM decodes the next address. $\overline{OE}$ and $\overline{W}$ can be used to control the output impedance. Descriptions of $\overline{OE}$ and $\overline{W}$ further explain EDO operation benefit.

address (A0 – A9)

Twenty address bits are required to decode one of 1048576 storage cell locations. Ten row-address bits are set up on A0 through A9 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The ten column-address bits are set up on pins A0 through A9 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip-enable in that it activates the sense amplifiers as well as the row decoder.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. While $\overline{CAS}$ and $\overline{RAS}$ are low and $\overline{W}$ is high, $\overline{OE}$ can be brought low or high and the DQs transition between valid data and high impedance (see Figure 7). There are two methods for placing the DQs into the high-impedance state and keeping them that way during $\overline{CAS}$ high time. The first method is to transition $\overline{OE}$ high before $\overline{CAS}$ transitions high and keep $\overline{OE}$ high for t_{CHO} past the $\overline{CAS}$ transition. This disables the DQs and they remain disabled, regardless of $\overline{OE}$, until $\overline{CAS}$ falls again. The second method is to have $\overline{OE}$ low as $\overline{CAS}$ transitions high. Then $\overline{OE}$ can pulse high for a minimum of t_{OEP} anytime during $\overline{CAS}$ high time, thus, disabling the DQs regardless of further transitions on $\overline{OE}$ until $\overline{CAS}$ falls again (see Figure 7).

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write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation independent of the state of $\overline{OE}$. This permits early-write operation to be completed with $\overline{OE}$ grounded. If $\overline{W}$ goes low in an extended-data-out read cycle, the DQs are disabled so long as $\overline{CAS}$ is high (see Figure 8).

data in/data out (DQ1–DQ4)

Data is written during a write or a read-modify-write cycle. Depending on the mode of operation, data is strobed in by the later falling edge of $\overline{CAS}$ or $\overline{W}$ with setup and hold times referenced to the latter edge. The DQs drive valid data after all access times are met and remain valid except in the cases described in the $\overline{W}$ and $\overline{OE}$ descriptions (above).

refresh

A refresh operation must be performed at least once every 16 ms to retain data. This is achieved by strobing each of the 1 024 rows (A0–A9). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored during the hidden-refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

CBR refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive CBR-refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

self-refresh (TMS44409P)

The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 µs. The chip is then refreshed by an on-board oscillator. No external address is required because the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}. Upon exiting the self-refresh mode, a burst refresh (refresh of a full set of row addresses) must be executed before continuing with normal operation. This ensures the DRAM is fully refreshed.

power up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after power up to the full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$ only or CBR) cycle.

test mode

A design for test (DFT) mode is incorporated in the TMS44409. A CBR with $\overline{W}$ low (WCBR) cycle is used to enter the test mode. In the test mode, data is written into and read from eight sections of the array in parallel. All data is written into the array through DQ1. Data is compared upon reading and if all bits are equal, all DQ pins go high. If any one bit is different, a DQ pin goes low. Any combination of read, write, read-write, or page-mode can be used in the test mode. The test-mode function reduces test times by enabling the 1-megabit × 4 DRAM to be tested as if it were a 512K DRAM where column address 0 is not used. A $\overline{RAS}$-only or CBR-refresh cycle is used to exit the DFT mode.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) . . . . – 1 V to 7 V
Voltage range on V_{CC} . . . . – 1 V to 7 V
Short-circuit output current . . . . 50 mA
Power dissipation . . . . 1 W
Operating free-air temperature range, T_A . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . – 55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			’44409-60 ’44409P-60 MIN	’44409-60 ’44409P-60 MAX	’44409-70 ’44409P-70 MIN	’44409-70 ’44409P-70 MAX	’44409-80 ’44409P-80 MIN	’44409-80 ’44409P-80 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 5 mA			2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA				0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}				± 10		± 10		± 10	mA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to 6.5 V, $\overline{CAS}$ high				± 10		± 10		± 10	µA
I_{CC1} †	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, t_{RWC} = MIN				105		90		80	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V	TTL			2		2		2	mA
			CMOS	’44409		1		1		1	mA
				’44409P		500		500		500	µA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, t_{RWC} = MIN, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)				105		90		80	mA
I_{CC4} †	Average EDO page current (see Note 4)	V_{CC} = 5.5 V, t_{HPC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling				90		80		70	mA
I_{CC6} ‡	Self-refresh current	$\overline{CAS}$, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min				500		500		500	µA
I_{CC7} †	Standby current	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled				5		5		5	mA
I_{CC10} ‡	Battery-backup current	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Addresses and data stable				500		500		500	µA

† Measured with outputs open
‡ TMS44409P only
NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)§

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0 – A9		5	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_o	Output capacitance		7	pF

§ Capacitance measurements are made on a sample basis only.
NOTE 5: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER		’44409-60 ’44409P-60		’44409-70 ’44409P-70		’44409-80 ’44409P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20	ns
t_{CLZ}	$\overline{CAS}$ to output in low-impedance state	0		0		0		ns
t_{REZ}	Output disable time, start of $\overline{RAS}$ high (see Note 6)	3	15	3	18	3	20	ns
t_{CEZ}	Output disable time, start of $\overline{CAS}$ high (see Note 6)	3	15	3	18	3	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 6)	3	15	3	18	3	20	ns
t_{WEZ}	Output disable time after $\overline{W}$ high (see Note 6)	3	15	3	18	3	20	ns

NOTE 6: Maximum t_{REZ}, t_{CEZ}, t_{WEZ} and t_{OEZ} are specified when the output is no longer driven.

EDO timing requirements over recommended ranges of supply voltage and operating free-air temperature

		’44409-60 ’44409P-60		’44409-70 ’44409P-70		’44409-80 ’44409P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{HPC}	Cycle time, EDO page-mode read or write	25		30		35		ns
t_{CSH}	Hold time, $\overline{CAS}$ from $\overline{RAS}$	50		55		60		ns
t_{CHO}	Hold time, $\overline{OE}$ from $\overline{CAS}$	10		10		10		ns
t_{DOH}	Hold time, output from $\overline{CAS}$	3		3		3		ns
t_{CAS}	Pulse duration, $\overline{CAS}$	10	10 000	12	10 000	15	10 000	ns
t_{WPE}	Pulse duration, $\overline{W}$ (output disable only)	5		5		5		ns
t_{OCH}	Setup time, $\overline{OE}$ before $\overline{CAS}$	10		10		10		ns
t_{CP}	Precharge time, $\overline{CAS}$	5		5		5		ns
t_{OEP}	Precharge time, $\overline{OE}$	5		5		5		ns

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timing requirements over recommended ranges of supply voltage and operating free-air temperature

		’44409-60 ’44409P-60		’44409-70 ’44409P-70		’44409-80 ’44409P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t_{RWC}	Cycle time, read-write (see Note 7)	150		175		200		ns
t_{PRWC}	Cycle time, EDO page-mode read-write	80		90		100		ns
t_{RASP}	Pulse duration, page mode, $\overline{RAS}$ low, (see Note 8)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low, (see Note 8)	60	10 000	70	10 000	80	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, $\overline{W}$	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{W}$ low (see Note 9)	0		0		0		ns
t_{RCS}	Setup time, read before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	10		12		15		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	10		12		15		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low (early-write operation only)	0		0		0		ns
t_{WSR}	Setup time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{DH}	Hold time, data after $\overline{CAS}$ low (see Note 9)	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, read after $\overline{CAS}$ high (see Note 10)	0		0		0		ns
t_{RRH}	Hold time, read after $\overline{RAS}$ high (see Note 10)	0		0		0		ns
t_{WCH}	Hold time, write after $\overline{CAS}$ low (early-write operation only)	10		15		15		ns
t_{WHR}	Hold time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$	10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (read-write operation only)	55		63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	15		15		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	5		5		5		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-write operation only)	40		46		50		ns
t_{OEH}	Hold time, $\overline{OE}$ command	15		18		20		ns
t_{OED}	Delay time, valid data in after $\overline{OE}$ high	15		18		20		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	20		25		30		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 11)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (CBR refresh only)	0		0		0		ns

NOTES: 7. All timing requirements assume t_T = 5 ns.
8. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
9. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
10. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
11. The minimum value is specified only to assure access time.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

			'44409-60 '44409P-60		'44409-70 '44409P-70		'44409-80 '44409P-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high		10		12		15		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low		85		98		110		ns
t_{REF}	Refresh time interval	'44409		16		16		16	ms
		'44409P		128		128		128	ms
t_T	Transition time		2	50	2	50	2	50	ms
t_{WTH}	Hold time, write low (test mode)		10		10		10		ns
t_{CHS}	Hold time, $\overline{CAS}$ low after $\overline{RAS}$ high (self refresh) (TMS44409P only)		– 50		– 50		– 50		ns
t_{WTS}	Setup time, write low (test mode)		10		10		10		ns
t_{CPS}	$\overline{CAS}$ precharge before self refresh		0		0		0		ns
t_{RPS}	$\overline{RAS}$ precharge after self refresh		110		130		150		ns
t_{RASS}	Self-refresh entry from $\overline{RAS}$ low (TMS44409P only)		100		100		100		µs

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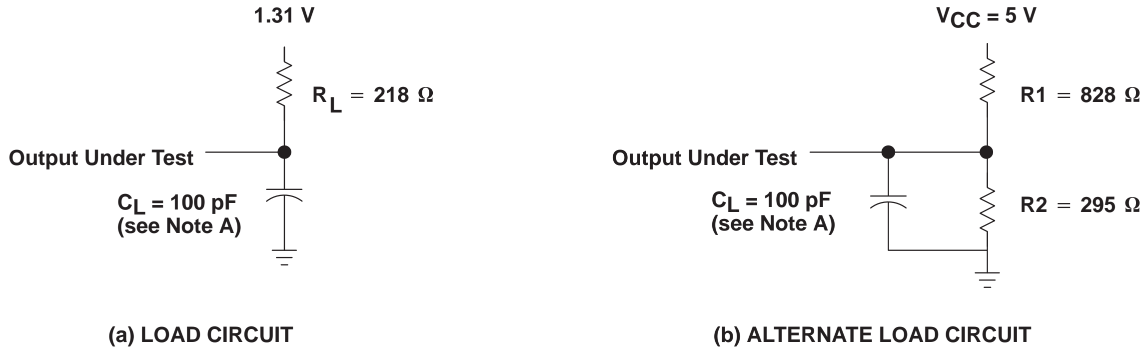

NOTE A: C_L includes probe and fixture capacitance.

Figure 1. Load Circuits for Timing Parameters

NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 2. Read-Cycle Timing

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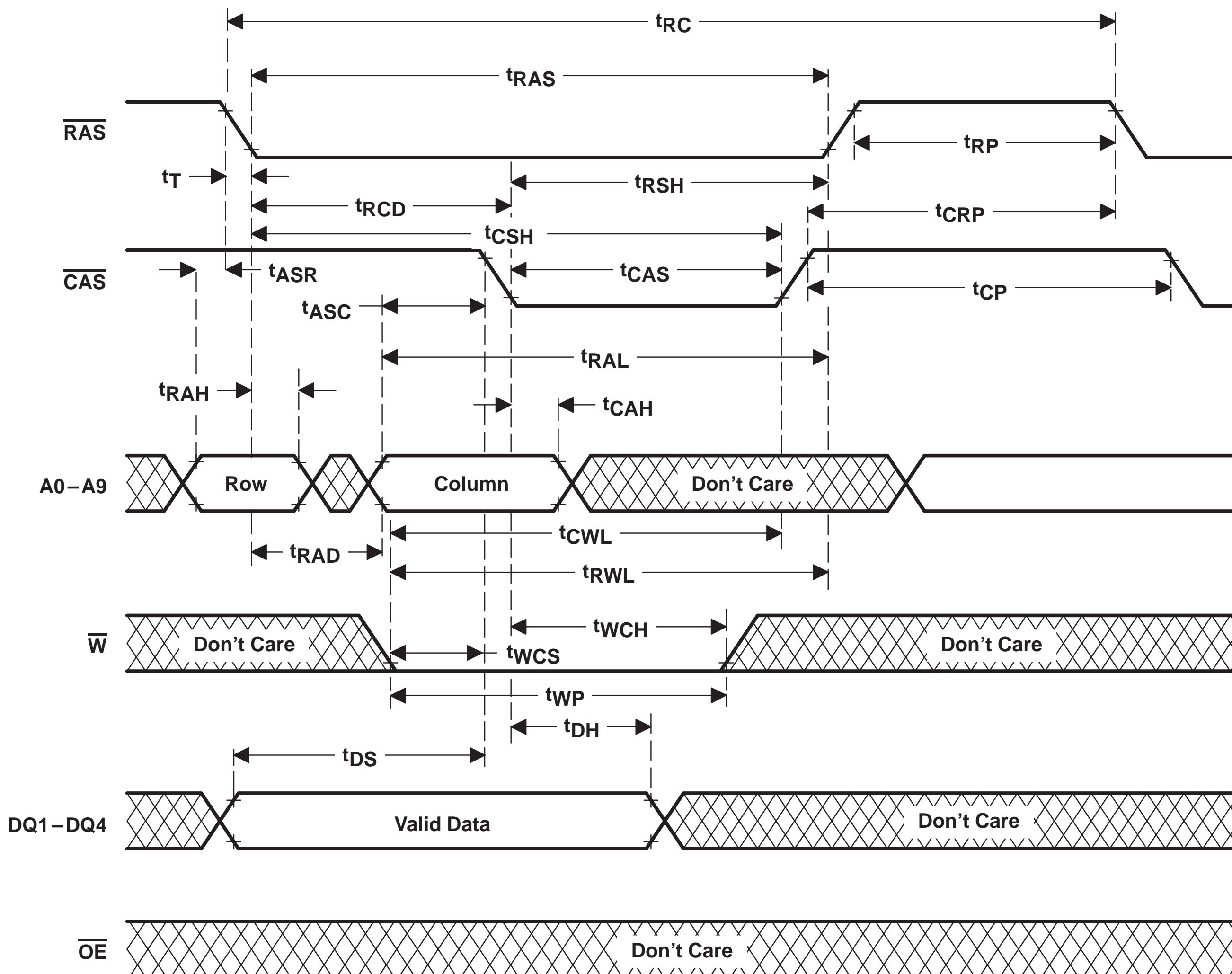

Figure 3. Early-Write-Cycle Timing

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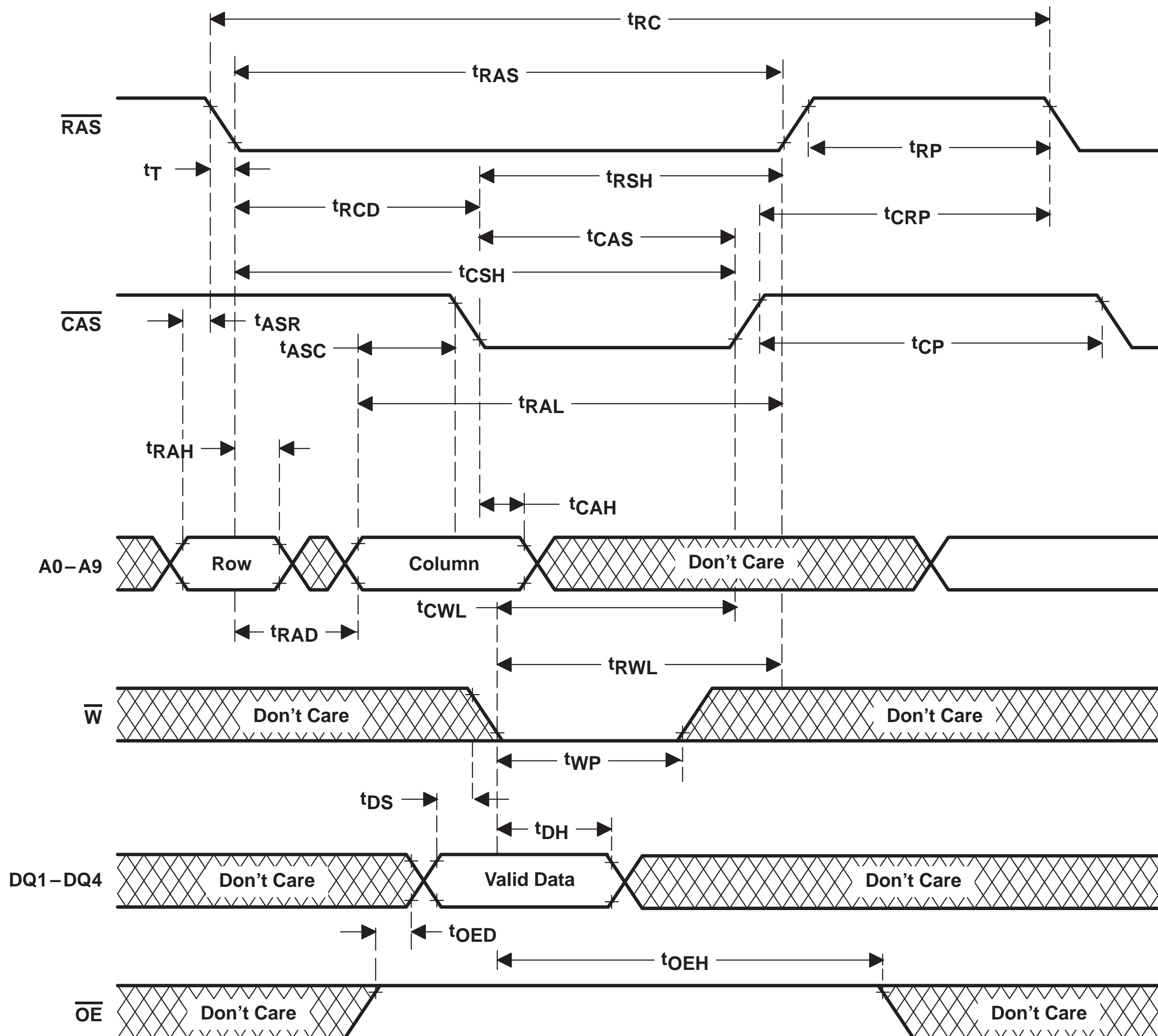
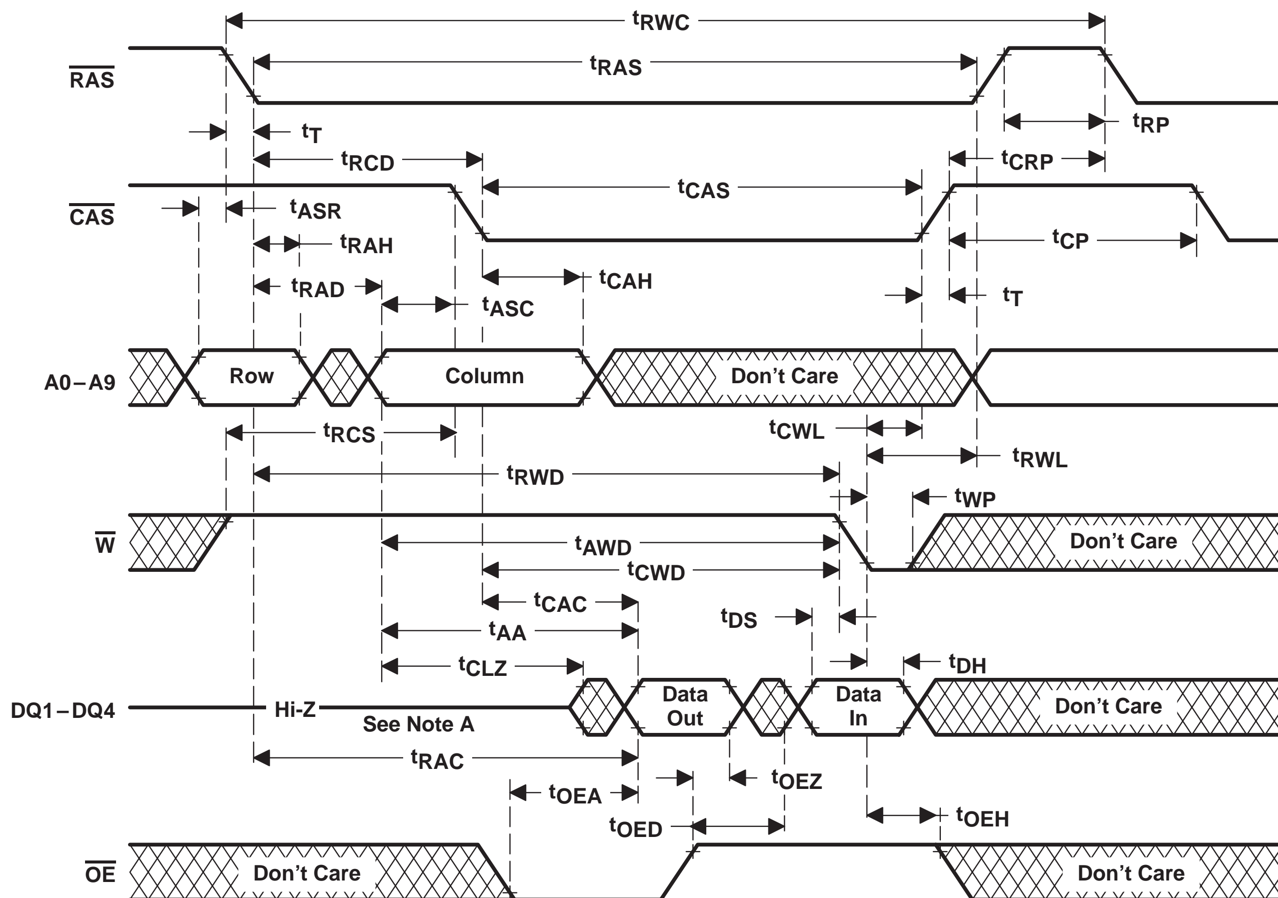


Figure 4. Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 5. Read-Write-Cycle Timing

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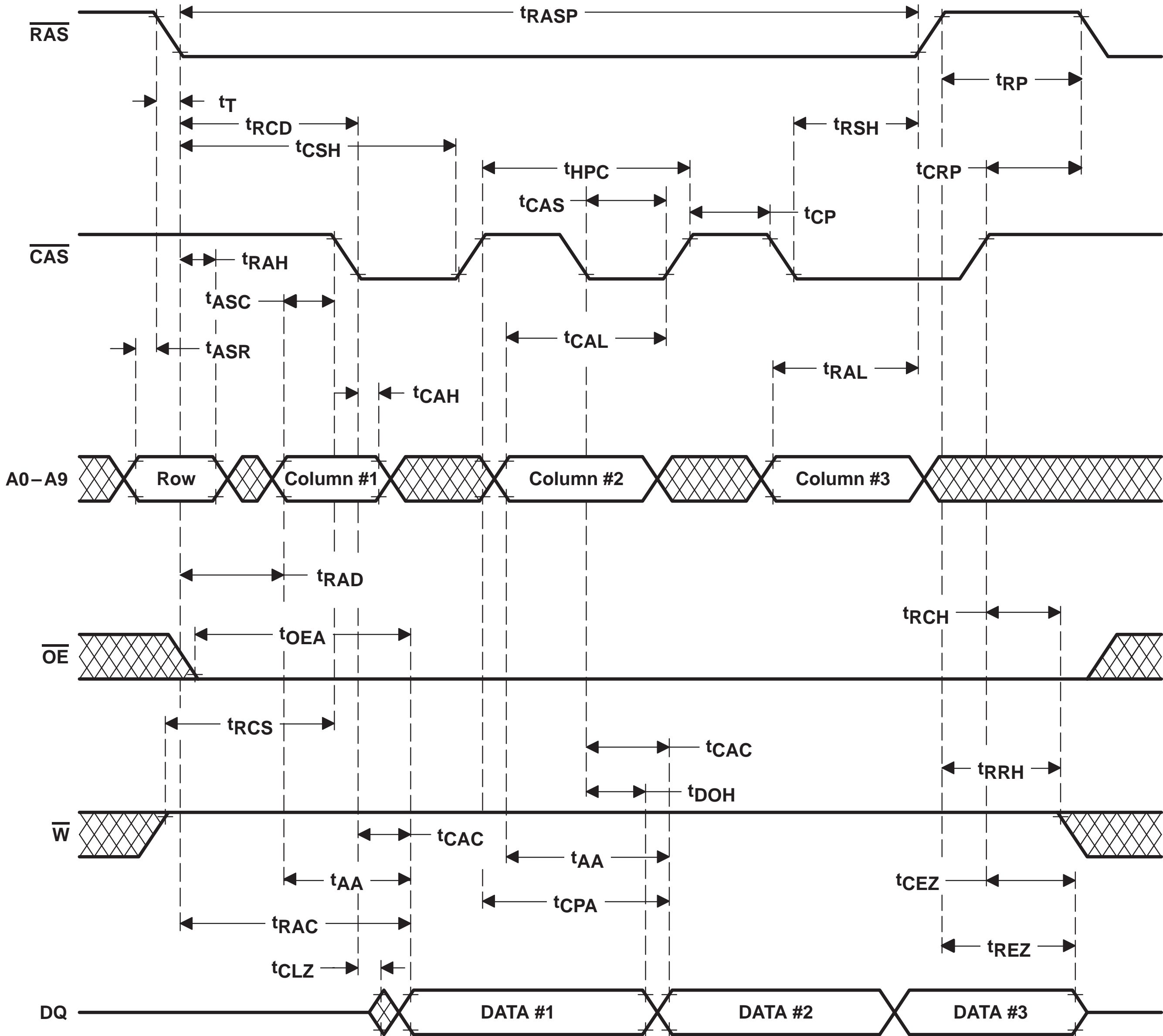
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. Access time is t_{CPA}- or t_{AA}- dependent.

Figure 6. Extended-Data-Out Read Cycle

PARAMETER MEASUREMENT INFORMATION

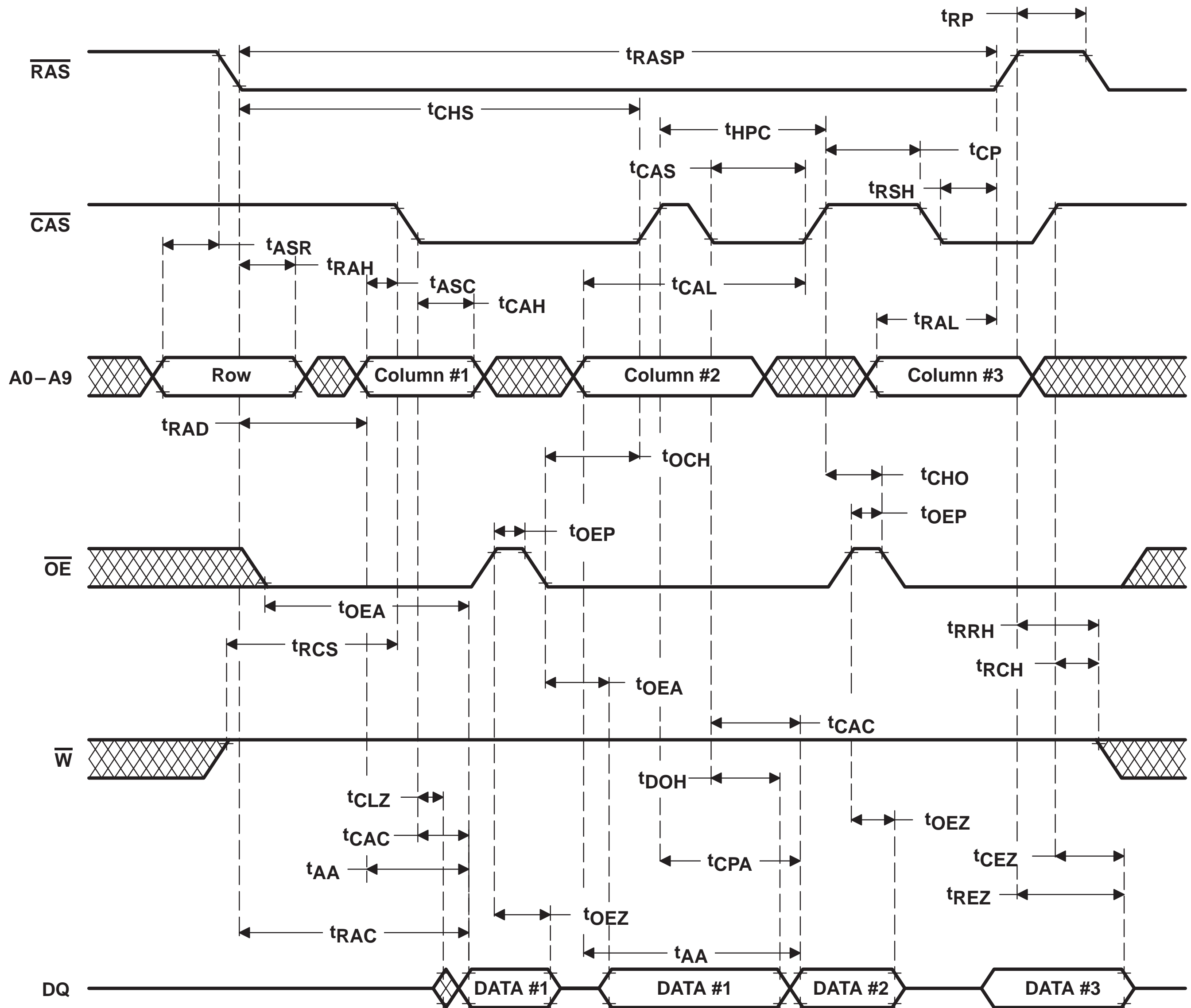


Figure 7. Extended-Data-Out Read-Cycle With $\overline{OE}$ Control

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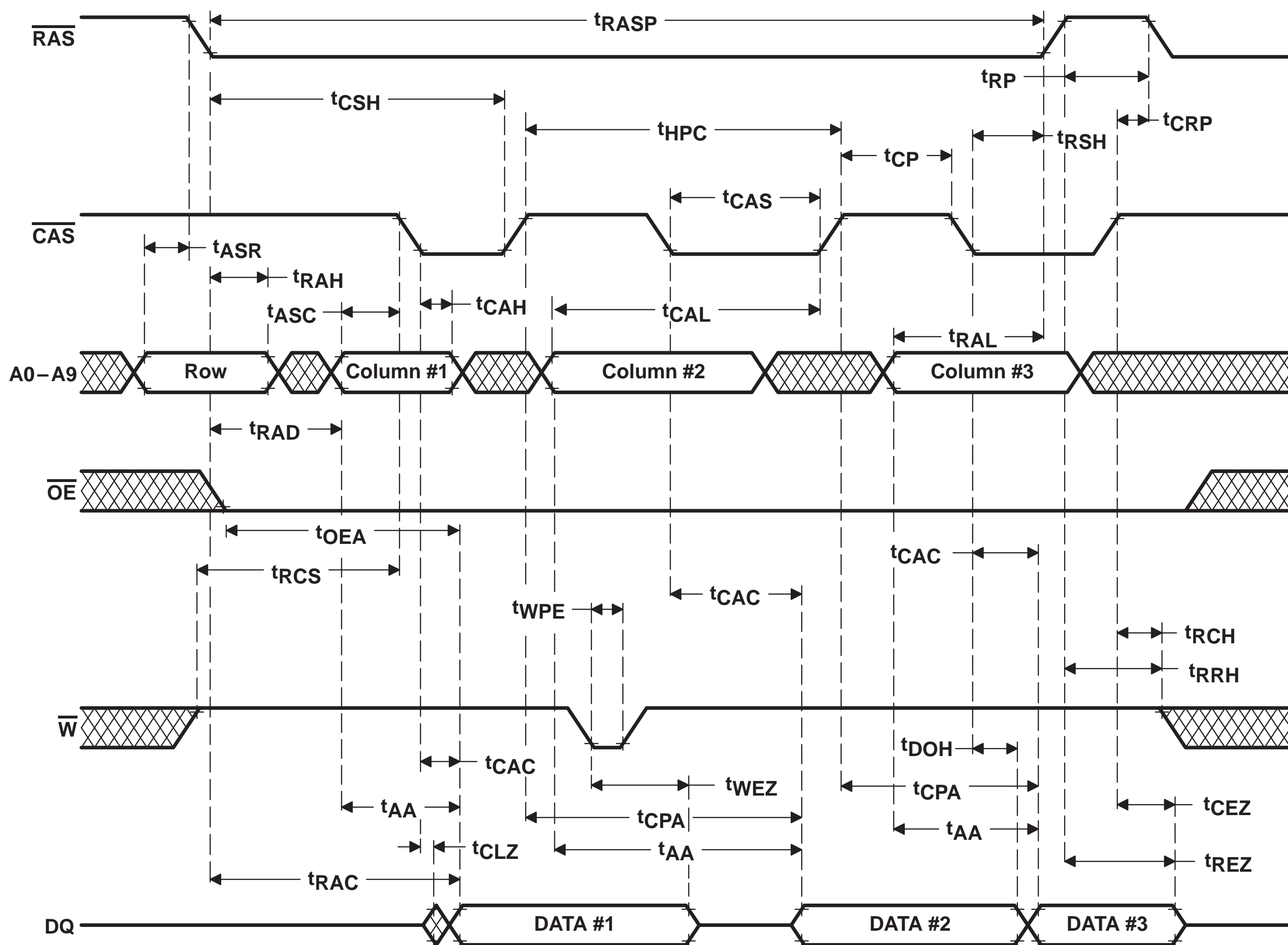

Figure 8. Extended-Data-Out Read-Cycle With $\overline{W}$ Control

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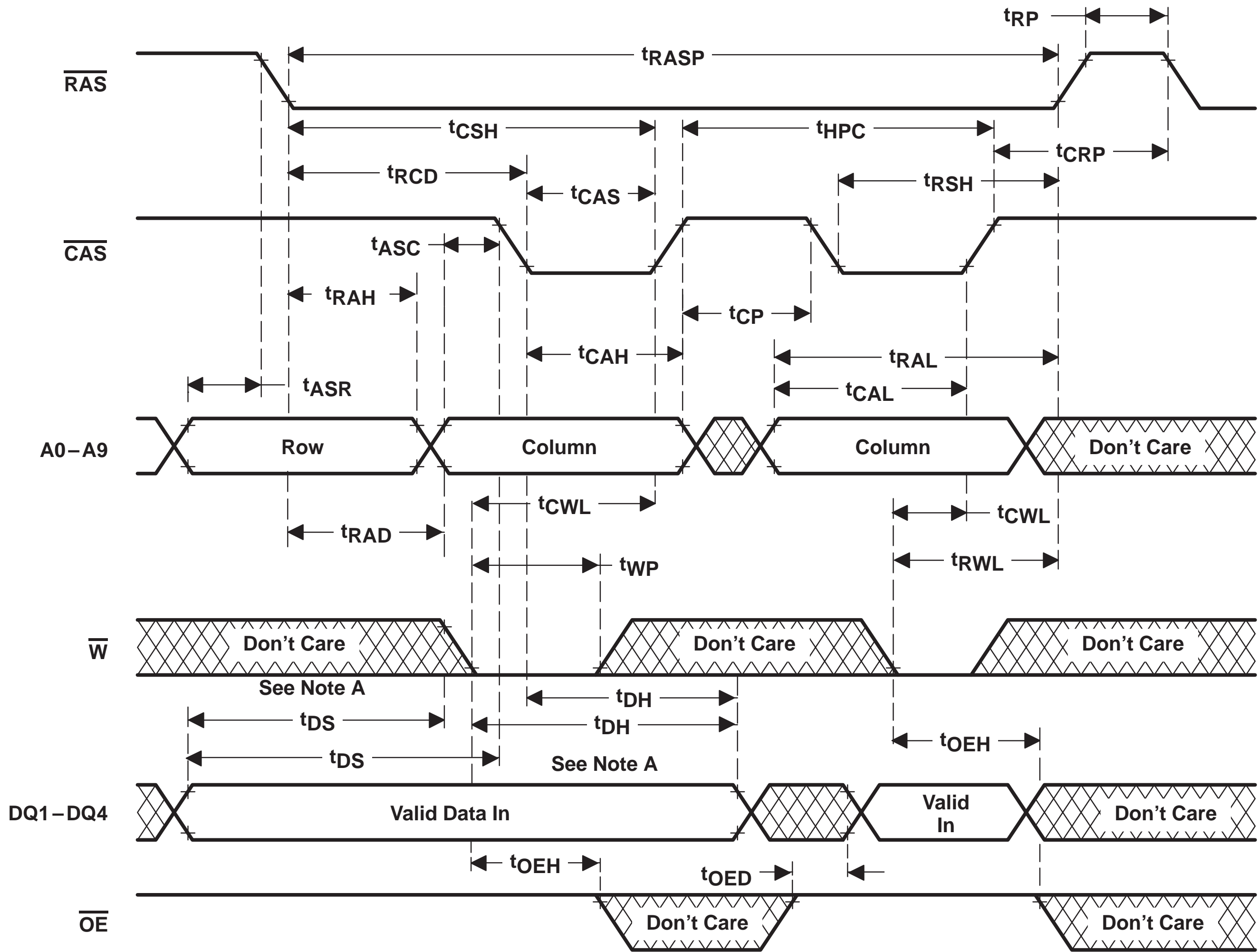

NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 9. EDO-Write-Cycle Timing

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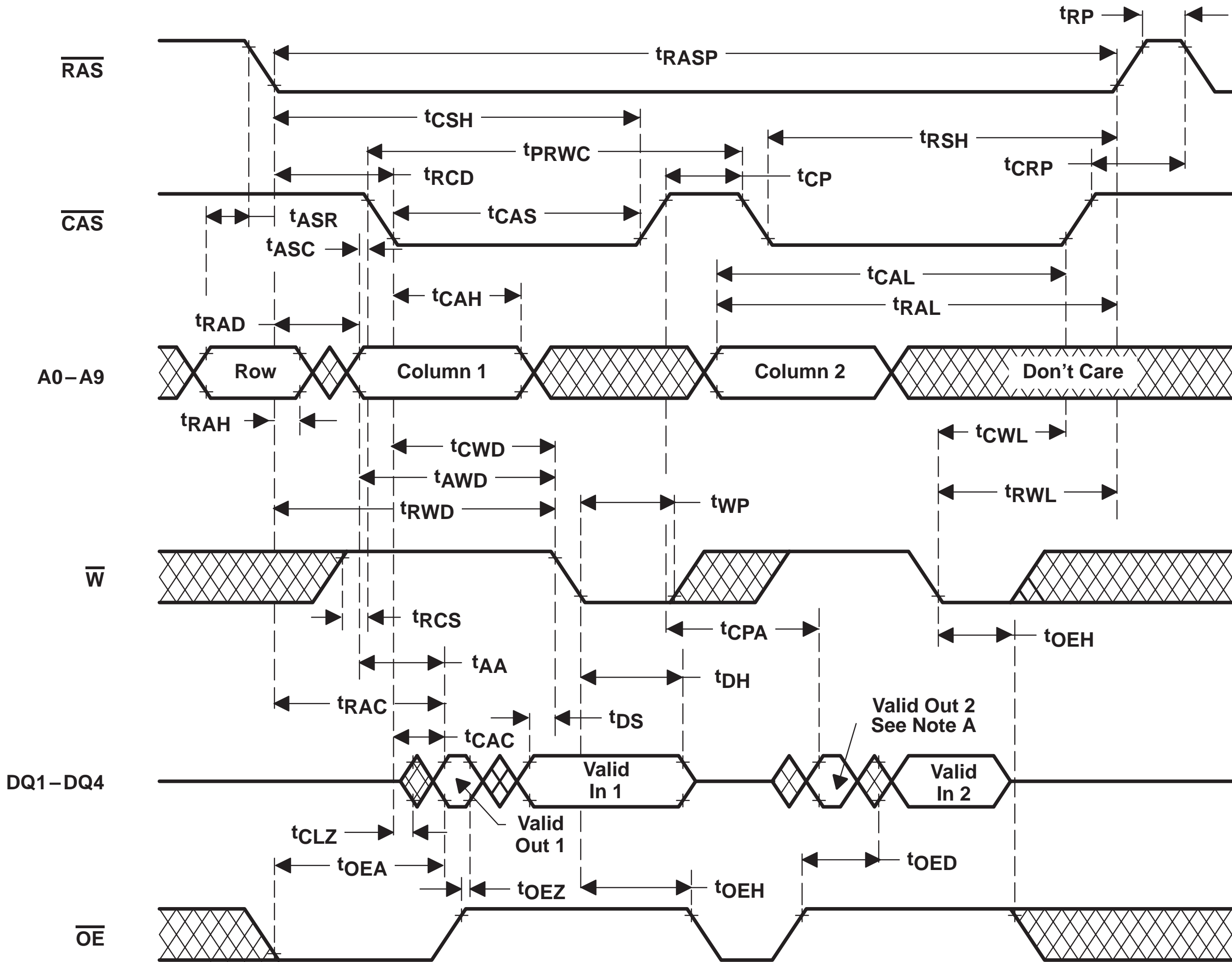
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read- and write-timing specifications are not violated.

Figure 10. EDO Read-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

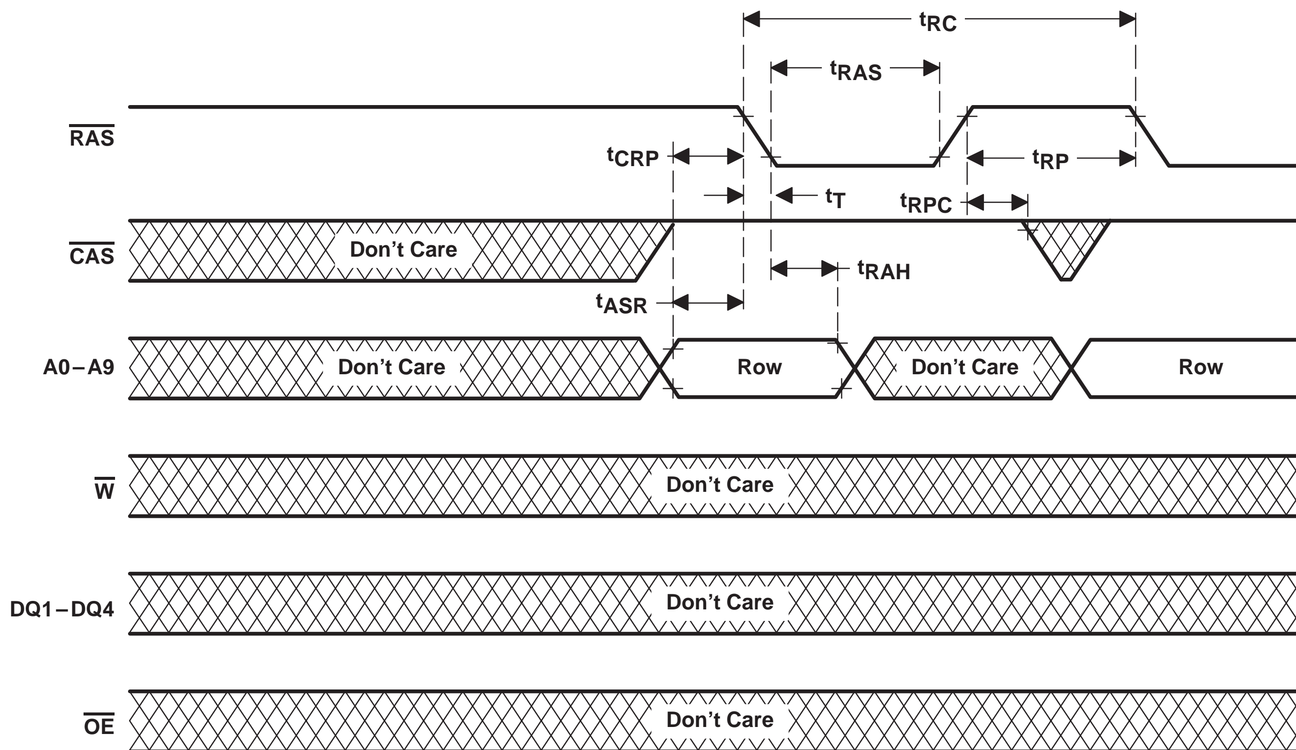


Figure 11. RAS-Only Refresh-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

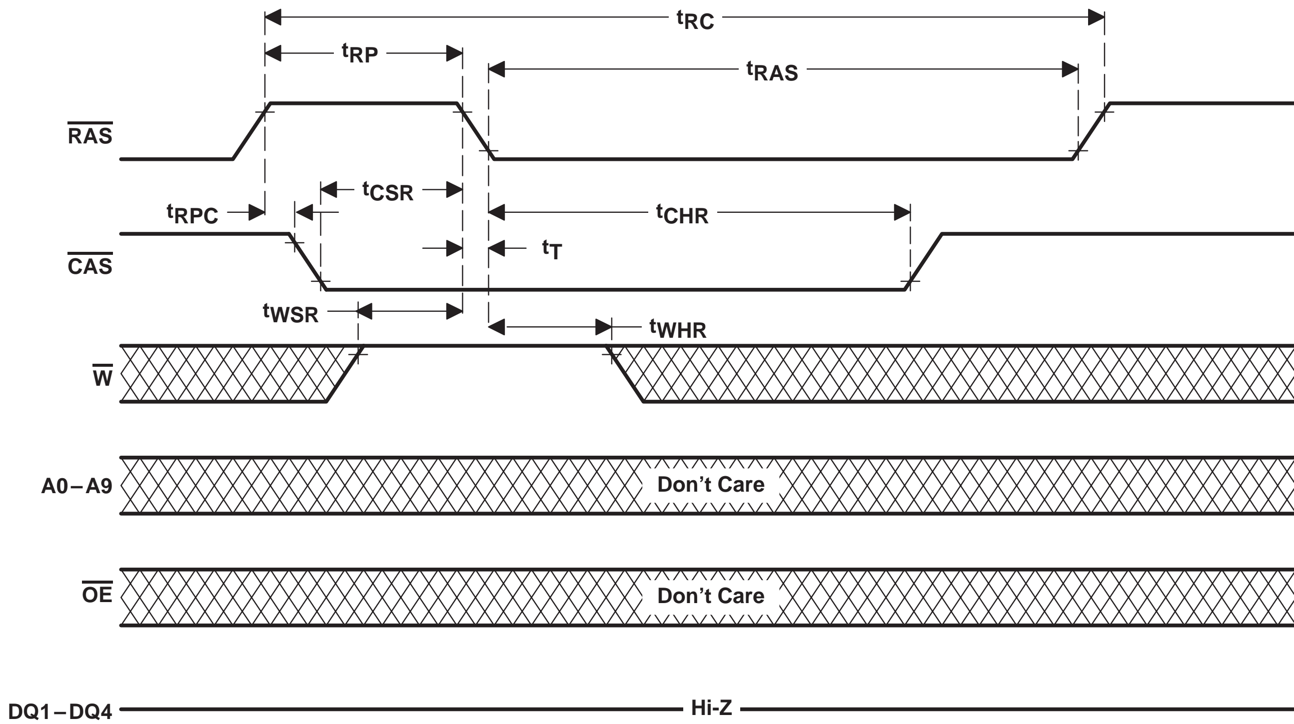


Figure 12. Automatic-CBR-Refresh-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

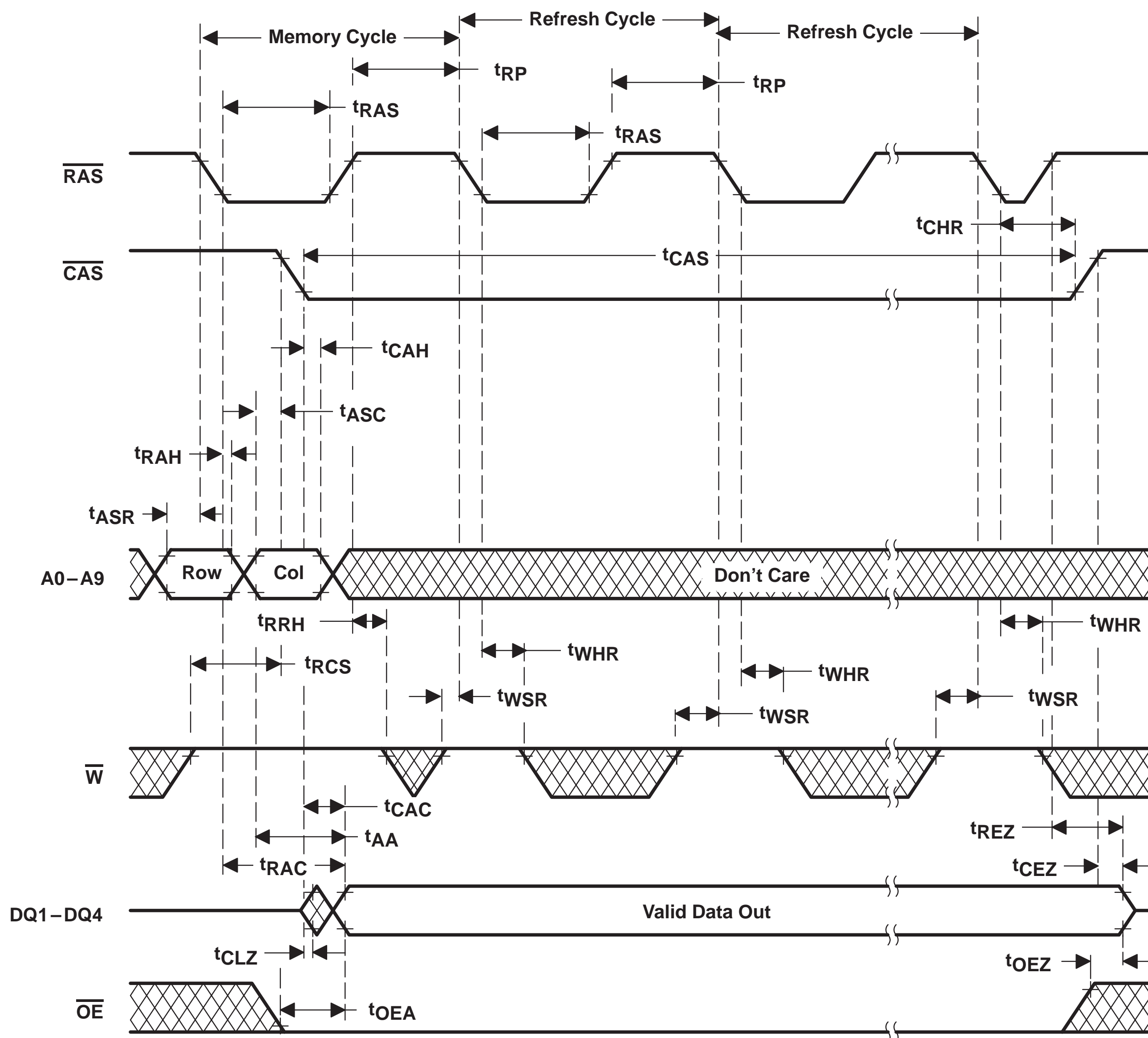


Figure 13. Hidden-Refresh Cycle (Read)

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

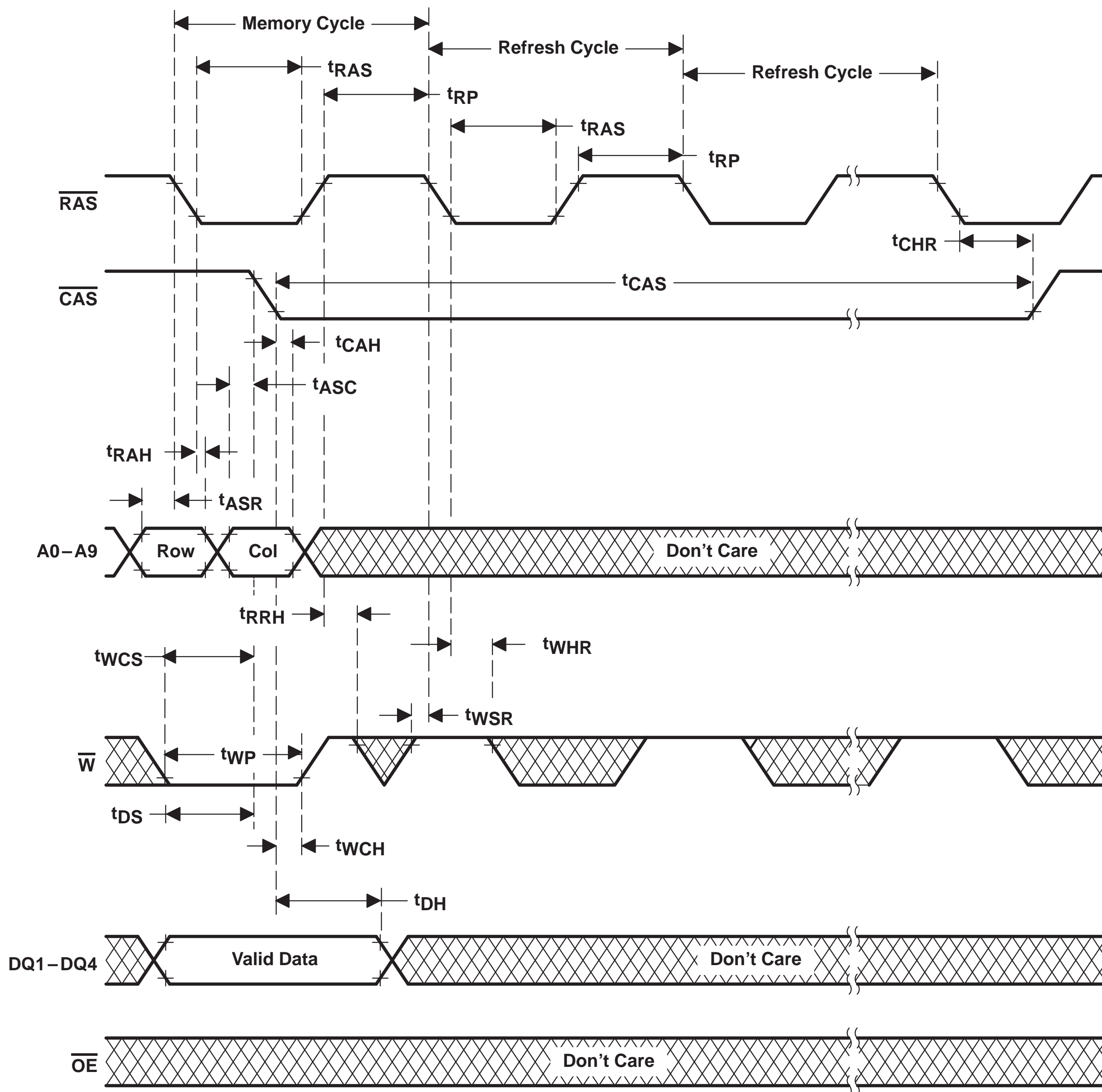


Figure 14. Hidden-Refresh Cycle (Write)

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

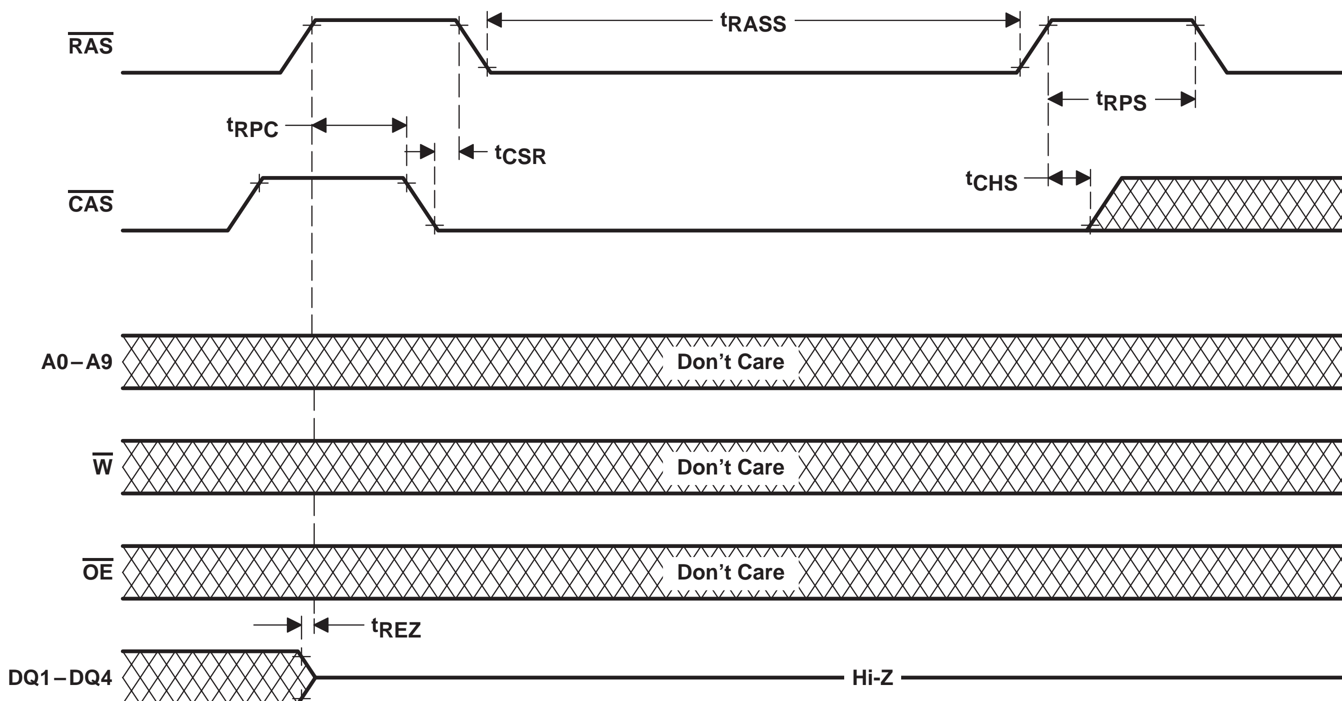


Figure 15. Self Refresh Timing

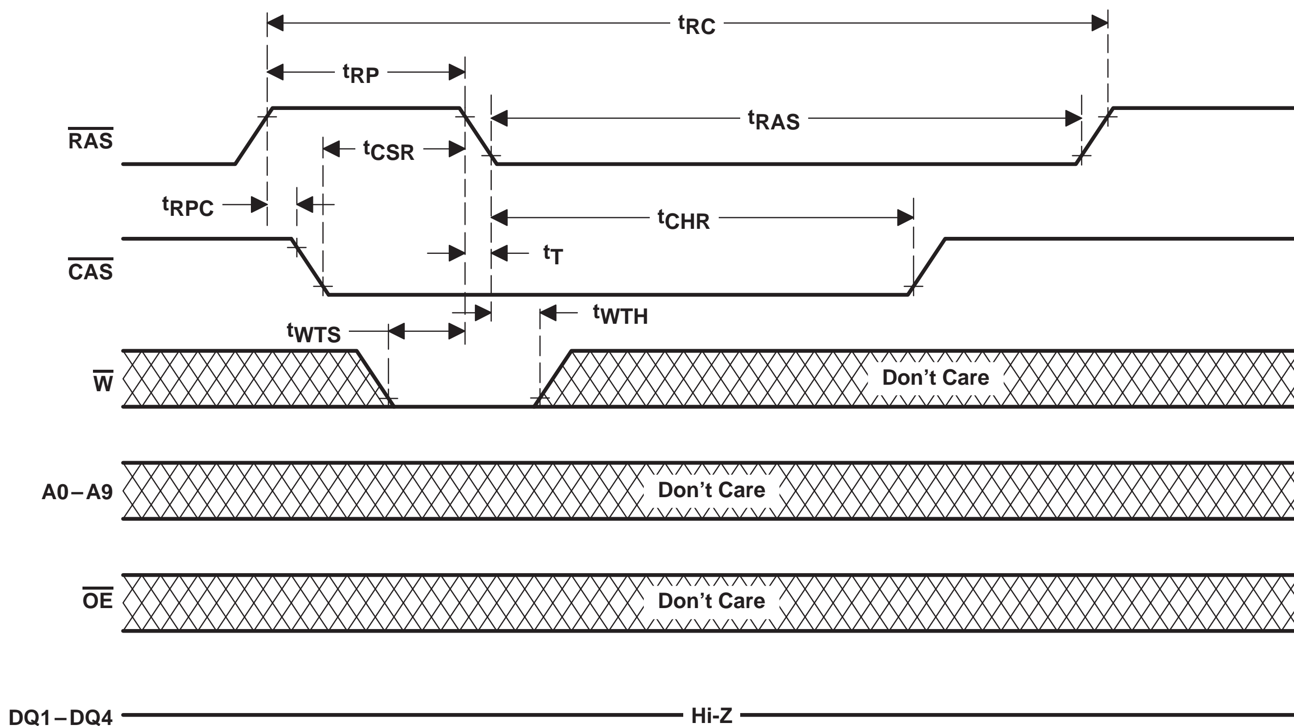
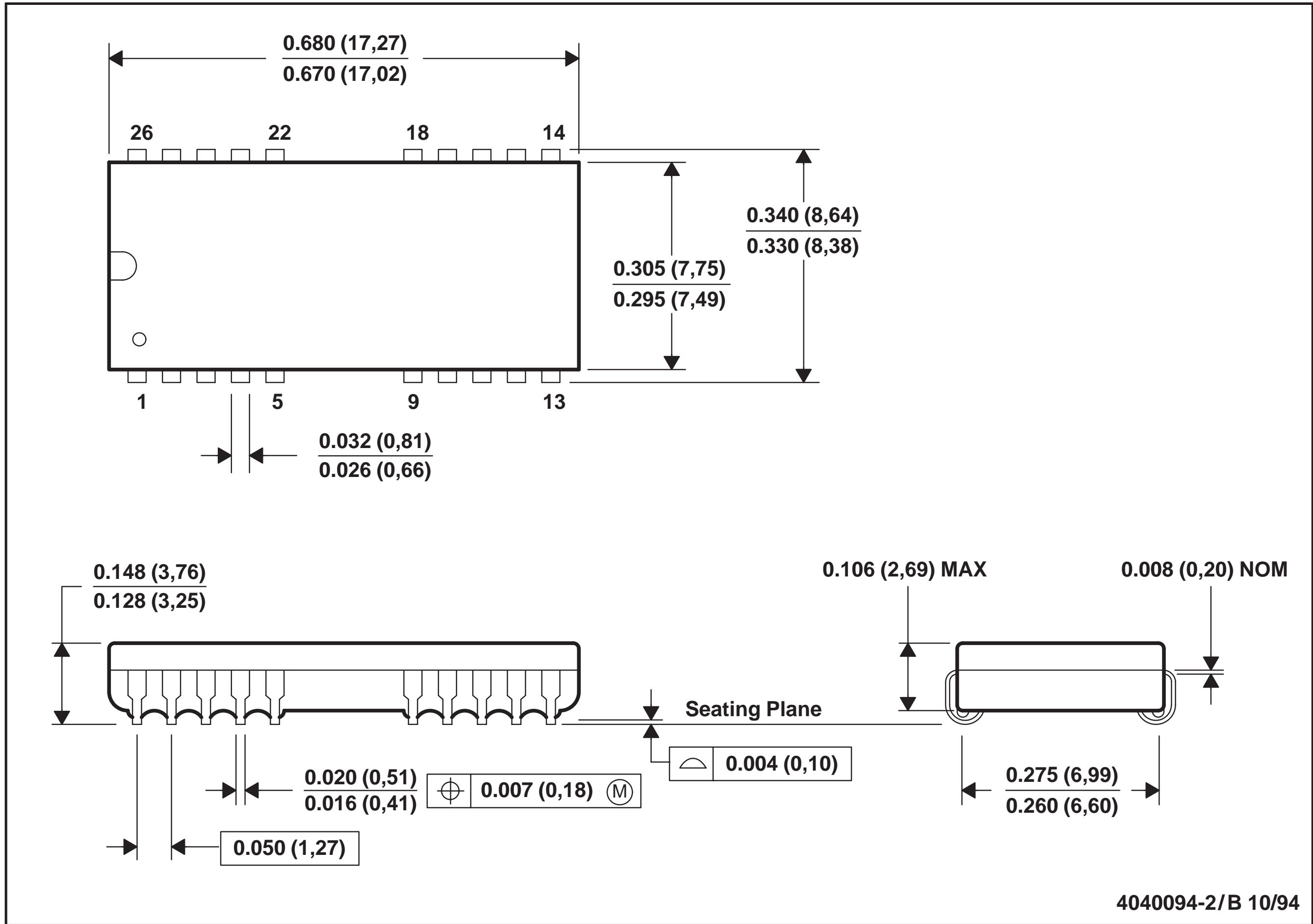


Figure 16. Test-Mode Entry Cycle

ADVANCE INFORMATION

MECHANICAL DATA

DJ (R-PDSO-J20/26) **PLASTIC SMALL-OUTLINE J-LEAD PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

ADVANCE INFORMATION

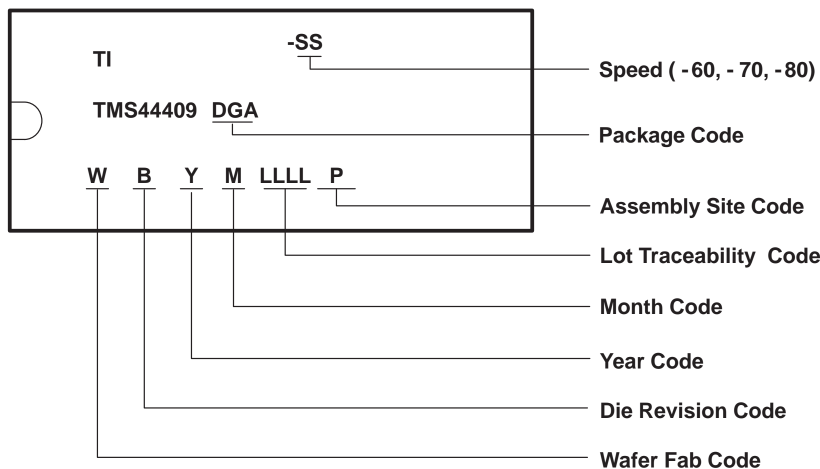
MECHANICAL DATA

DGA (R-PDSO-G20/26) **PLASTIC SMALL-OUTLINE PACKAGE**

0.050 (1,27)
0.020 (0,50)
0.012 (0,30)
0.008 (0,21) M
26
14
0.371 (9,42)
0.355 (9,02)
0.304 (7,72)
0.296 (7,52)
0.006 (0,15) NOM
1
13
Gage Plane
0.679 (17,24)
0.671 (17,04)
0.010 (0,25)
0°–5°
0.024 (0,60)
0.016 (0,40)
Seating Plane
0.047 (1,20) MAX
0.000 (0,00) MIN
0.004 (0,10)
4040265-2/C 4/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

device symbolization (TMS44409 illustrated)



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