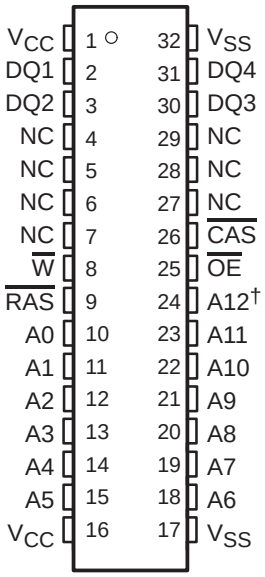
- **Organization . . . 16 777 216 by 4 Bits**
- **Single 3.3-V Power Supply (±0.3-V Tolerance)**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	EDO CYCLE t_{HPC} (MIN)
'46x409/P-40	40 ns	11 ns	20 ns	16 ns
'46x409/P-50	50 ns	13 ns	25 ns	20 ns
'46x409/P-60	60 ns	15 ns	30 ns	25 ns

- **Extended-Data-Out (EDO) Operation**
- **$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ (CBR) Refresh**
- **Long Refresh Period (See Available Options Table)**
- **Low-Power, Self-Refresh Version (TMS46x409P)**
- **3-State Unlatched Output**
- **All Inputs/Outputs and Clocks Are Low-Voltage TTL (LVTTL) Compatible**
- **High-Reliability Plastic 32-Lead 400-Mil-Wide Thin Small-Outline (TSOP) Package (DGC Suffix)**
- **Operating Free-Air Temperature Range 0°C to 70°C**

DGC PACKAGE
(TOP VIEW)



† A12 is NC for TMS465409 and TMS465409P.

PIN NOMENCLATURE	
A0–A12	Address Inputs
$\overline{\text{CAS}}$	Column-Address Strobe
DQ1–DQ4	Data In/Data Out
NC	No Internal Connection
$\overline{\text{OE}}$	Output Enable
$\overline{\text{RAS}}$	Row-Address Strobe
$\overline{\text{W}}$	Write Enable
V_{CC}	3.3-V Supply
V_{SS}	Ground

AVAILABLE OPTIONS

DEVICE	SELF-REFRESH BATTERY BACKUP	$\overline{\text{RAS}}$-ONLY REFRESH CYCLES	CBR REFRESH CYCLES
TMS464409	—	8192 in 64 ms	4096 in 64 ms
TMS464409P	YES	8192 in 128 ms	4096 in 128 ms
TMS465409	—	4096 in 64 ms	4096 in 64 ms
TMS465409P	YES	4096 in 128 ms	4096 in 128 ms

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description

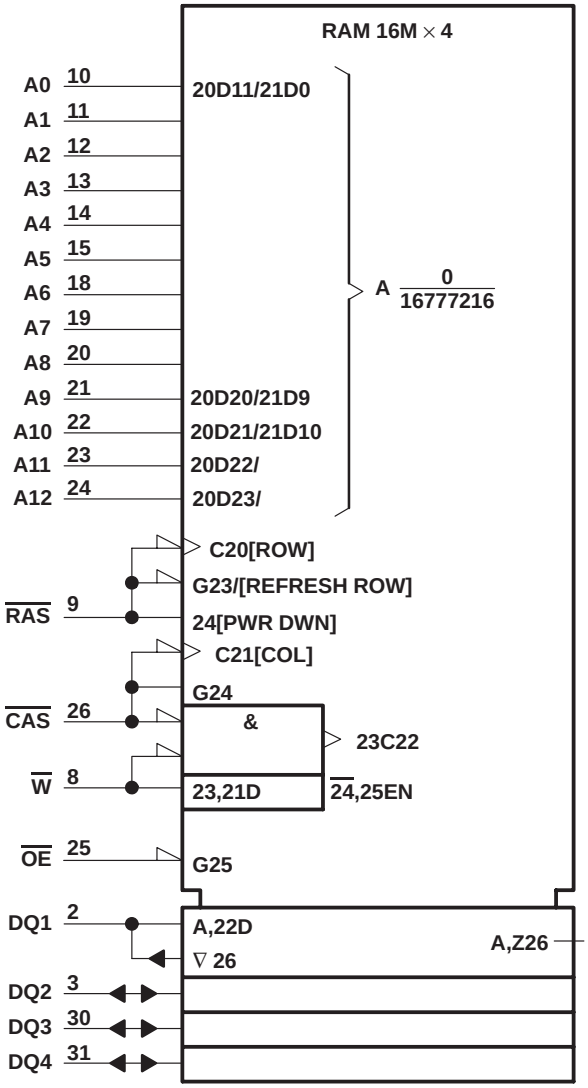
The TMS464409 and TMS465409 series are low-voltage, 67 108 864-bit dynamic random-access memories (DRAMs), organized as 16 777 216 words of 4 bits each. The TMS464409P and TMS465409P series are high-speed, low-voltage, low-power, self-refresh, 67 108 864-bit DRAMs, organized as 16 777 216 words of 4 bits each. Both sets of devices employ state-of-the-art technology for high performance, reliability, and low power.

These devices feature maximum $\overline{\text{RAS}}$ access times of 40, 50, and 60 ns. All inputs and outputs, including clocks, are compatible with LVTTL. All addresses and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

description (continued)

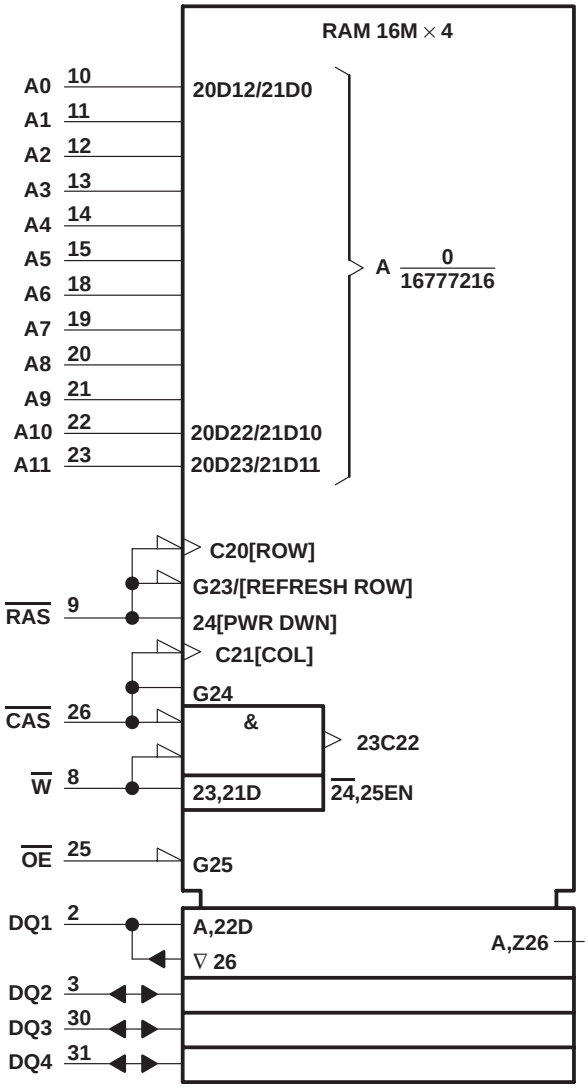
The TMS46x409 and TMS46x409P series are offered in a 400-mil, 32-lead plastic surface mount TSOP package (DGC suffix). This package is designed for operation from 0°C to 70°C.

logic symbol (TMS464409 and TMS464409P)†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic symbol (TMS465409 and TMS465409P)†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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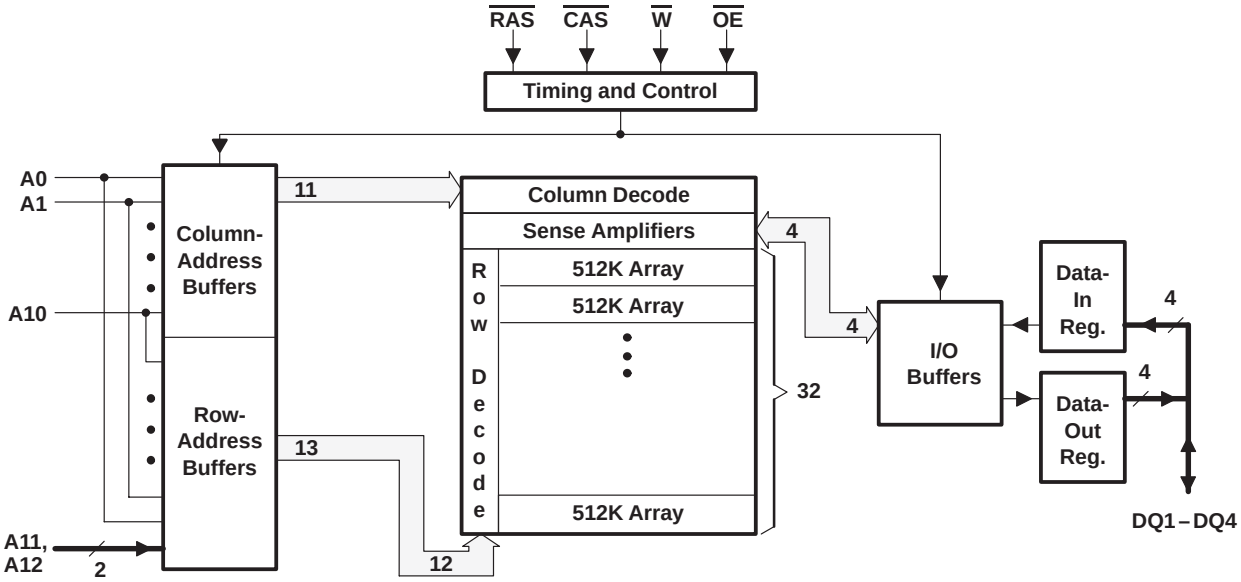
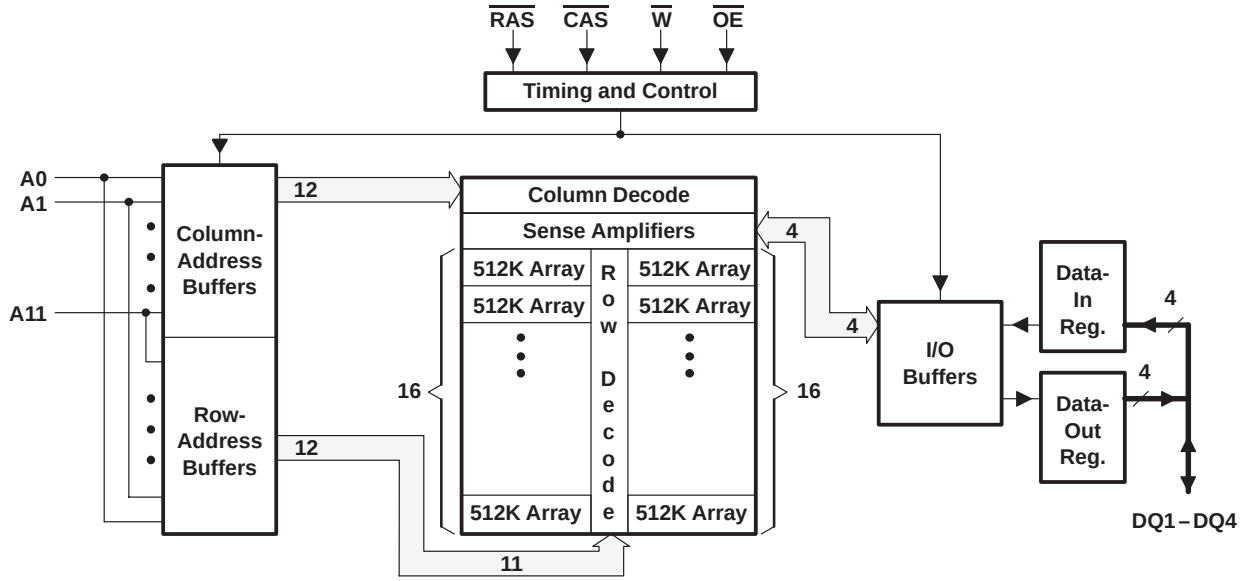
functional block diagram

TMS464409, TMS464409P



TMS465409, TMS465409P



operation

extended data out

Extended data out (EDO) allows data output rates up to 66 MHz for 40-ns devices. When keeping the same row address while selecting random column addresses, the time for row-address setup and hold and for address multiplex is eliminated. The maximum number of columns that can be accessed is determined by t_{RASP}, the maximum $\overline{RAS}$ low time.

Extended data out does not place the data in/data out pins (DQ pins) into the high-impedance state with the rising edge of $\overline{CAS}$ during $\overline{RAS}$ low. The output remains valid for the system to latch the data. After $\overline{CAS}$ goes high, the DRAM decodes the next address. $\overline{OE}$ and $\overline{W}$ can control the output impedance. Descriptions of $\overline{OE}$ and $\overline{W}$ further explain EDO operation benefit.

address: A0 – A11 (TMS465409/P) and A0 – A12 (TMS464409/P)

Twenty-four address bits are required to decode each one of 16777216 storage cell locations. For the TMS465409 and TMS465409P,12 row-address bits are set up on A0 through A11 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Twelve column-address bits are set up on A0 through A11. For the TMS464409 and TMS464409P, 13 row-address bits are set up on inputs A0 through A12 and latched onto the chip by $\overline{RAS}$. Eleven column-address bits are set up on A0 through A10. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable because it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffers and latching the address bits into the column-address buffers.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. While $\overline{CAS}$ and $\overline{RAS}$ are low and $\overline{W}$ is high, $\overline{OE}$ can be brought low or high and the DQs transition between valid data and high impedance (see Figure 8). There are two methods for placing the DQs into the high-impedance state and maintaining that state during $\overline{CAS}$ high time. The first method is to transition $\overline{OE}$ high before $\overline{CAS}$ transitions high and keep $\overline{OE}$ high for t_{CHO} (hold time, $\overline{OE}$ from $\overline{CAS}$) past the $\overline{CAS}$ transition. This disables the DQs and they remain disabled, regardless of $\overline{OE}$, until $\overline{CAS}$ falls again. The second method is to have $\overline{OE}$ low as $\overline{CAS}$ transitions high. Then $\overline{OE}$ can pulse high for a minimum of t_{OEP} (precharge time, $\overline{OE}$) anytime during $\overline{CAS}$ high time, disabling the DQs regardless of further transitions on $\overline{OE}$ until $\overline{CAS}$ falls again (see Figure 8).

write enable ($\overline{W}$)

The read or write mode is selected through $\overline{W}$. A logic high on $\overline{W}$ selects the read mode, and a logic low selects the write mode. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation with $\overline{OE}$ grounded. If $\overline{W}$ goes low in an extended-data-out read cycle, the DQs are disabled so long as $\overline{CAS}$ is high (see Figure 9).

data in/data out (DQ1 – DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the later falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch with setup and hold times referenced to the later edge. The DQs drive valid data after all access times are met and remain valid except in cases described in the $\overline{W}$ and $\overline{OE}$ descriptions.

$\overline{RAS}$-only refresh

A refresh operation must be performed at least once every 64 ms (128 ms for TMS46x409P) to retain data by strobing each of the 4096 rows for TMS465409/P or 8192 rows for TMS464409/P. A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

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hidden refresh

A hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored, and the refresh address is generated internally.

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

CBR refresh is performed by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive CBR refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored, and the refresh address is generated internally.

battery-backup refresh

A low-power battery-backup refresh mode that requires less than 250 μA of refresh current is available on the TMS464409P and TMS465409P. Data integrity is maintained using CBR refresh with a period of 31.25 μs while holding $\overline{RAS}$ low for less than 300 ns. To minimize current consumption, all input levels must be at LVCMOS levels (V_{IL} < 0.2 V, V_{IH} > V_{CC} – 0.2 V).

self-refresh (TMS46x409P)

The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 μs. The chip is then refreshed internally by an on-board oscillator. No external address is required because the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}. Upon exiting self-refresh mode, a burst refresh (refreshes a full set of row addresses) must be executed before continuing with normal operation. The burst refresh ensures the DRAM is fully refreshed.

power up

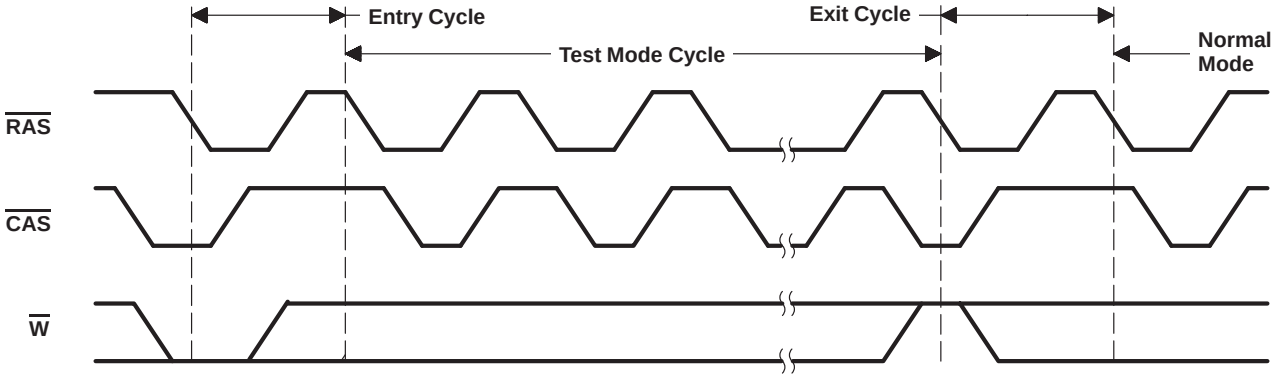
To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after power up to the full V_{CC} level. These eight initialization cycles must include at least one refresh ($\overline{RAS}$-only or CBR) cycle.

test mode

The test mode (see Figure 1) is initiated with a CBR-refresh cycle while simultaneously holding the $\overline{W}$ input low. The entry cycle performs an internal refresh cycle while internally setting the device to perform parallel read or write on subsequent cycles. While in the test mode, any data sequence can be performed. The device exits test mode if a CBR refresh cycle with $\overline{W}$ held high or a $\overline{RAS}$-only refresh cycle is performed.

In the test mode, the device is configured as 1024K bits × 4 bits for each DQ. Each DQ pin has a separate 4-bit parallel read and write data bus that ignores column addresses A0 and A1. During a read cycle, the four internal bits are compared for each DQ pin. If the four bits agree, DQ goes high; if not, DQ goes low. During a write cycle, the data states of all four DQs must be the same to ensure proper function of the test mode. Test time is reduced by a factor of four for this series.

test mode (continued)



NOTE A: The states of $\overline{W}$, data in, and address are defined by the type of cycle used during test mode.

Figure 1. Test-Mode Cycle

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on V_{CC} . . . . . – 0.5 V to 4.6 V
Voltage range on any pin (see Note 1) . . . . . – 0.5 V to 4.6 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2		V_{CC} +0.3	V
V_{IL}	Low-level input voltage (see Note 2)	– 0.3		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic voltage levels only.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TMS464409/P

PARAMETER		TEST CONDITIONS†		'464409-40 '464409P-40		'464409-50 '464409P-50		'464409-60 '464409P-60		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = – 100 µA	LVCMOS	V_{CC}–0.2		V_{CC}–0.2		V_{CC}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{CC} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 3.6 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Average read- or write-cycle current	V_{CC} = 3.6 V, Minimum cycle			125		100		90	mA
I_{CC2}	Average standby current	After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2 V (LVTTL)			1		1		1	mA
		After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (LVCMOS)	'464409		500		500		500	µA
			'464409P		150		150		150	µA
I_{CC3}§	Average $\overline{RAS}$-only refresh current	V_{CC} = 3.6 V, $\overline{RAS}$ cycling, Minimum cycle, $\overline{CAS}$ high ($\overline{RAS}$ only)			125		100		90	mA
I_{CC4}‡¶	Average EDO current	V_{CC} = 3.6 V, $\overline{RAS}$ low, t_{PC} = minimum, $\overline{CAS}$ cycling			140		110		90	mA
I_{CC5}	Average CBR refresh current	V_{CC} = 3.6 V, Minimum cycle, $\overline{RAS}$ low after $\overline{CAS}$ low			160		130		110	mA
I_{CC6}#	Average self-refresh current	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} minimum			300		300		300	µA
I_{CC10}#	Average battery-backup operating current, CBR only	t_{RAS} ≤ 300 ns, t_{RC} = 31.25 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			400		400		400	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change per EDO cycle, t_{HPC}
# For TMS464409P only

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

TMS465409/P

PARAMETER		TEST CONDITIONS†		’465409-40 ’465409P-40		’465409-50 ’465409P-50		’465409-60 ’465409P-60		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = – 100 µA	LVCMOS	V_{CC}–0.2		V_{CC}–0.2		V_{CC}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{CC} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 3.6 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Average read- or write-cycle current	V_{CC} = 3.6 V, Minimum cycle			160		130		110	mA
I_{CC2}	Average standby current	After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2 V (LVTTL)			1		1		1	mA
		After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (LVCMOS)	’465409		500		500		500	µA
			’465409P		150		150		150	µA
I_{CC3}§	Average $\overline{RAS}$-only refresh current	V_{CC} = 3.6 V, $\overline{RAS}$ cycling, Minimum cycle, $\overline{CAS}$ high ($\overline{RAS}$ only)			160		130		110	mA
I_{CC4}‡¶	Average EDO current	V_{CC} = 3.6 V, $\overline{RAS}$ low, t_{PC} = minimum, $\overline{CAS}$ cycling			150		120		100	mA
I_{CC5}	Average CBR refresh current	V_{CC} = 3.6 V, Minimum cycle, $\overline{RAS}$ low after $\overline{CAS}$ low			160		130		110	mA
I_{CC6}#	Average self-refresh current	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} minimum			300		300		300	µA
I_{CC10}#	Average battery-backup operating current, CBR only	t_{RAS} ≤ 300 ns, t_{RC} = 31.25 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			400		400		400	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change per EDO cycle, t_{HPC}
# For TMS465409P only

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capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A12†		5	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_o	Output capacitance‡		7	pF

† $\overline{A12}$ is NC (no internal connection) for TMS465409 and TMS465409P.
‡ $\overline{CAS}$ and $\overline{OE}$ = V_{IH} to disable outputs
NOTE 3: V_{CC} = 3.3 V ±10%, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 4)

PARAMETER		’46x409-40 ’46x409P-40		’46x409-50 ’46x409P-50		’46x409-60 ’46x409P-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address (see Note 5)		20		25		30	ns
t_{CAC}	Access time from $\overline{CAS}$ (see Note 5)		11		13		15	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge (see Note 5)		22		28		35	ns
t_{RAC}	Access time from $\overline{RAS}$ (see Note 5)		40		50		60	ns
t_{OEA}	Access time from $\overline{OE}$ (see Note 5)		11		13		15	ns
t_{CLZ}	Delay time, $\overline{CAS}$ to output in low impedance	0		0		0		ns
t_{REZ}	Output buffer turn off delay from $\overline{RAS}$ (see Note 6)	3	11	3	13	3	15	ns
t_{CEZ}	Output buffer turn off delay from $\overline{CAS}$ (see Note 6)	3	11	3	13	3	15	ns
t_{OEZ}	Output buffer turn off delay from $\overline{OE}$ (see Note 6)	3	11	3	13	3	15	ns
t_{WEZ}	Output buffer turn off delay from $\overline{W}$ (see Note 6)	3	11	3	13	3	15	ns

NOTES: 4. With ac parameters, it is assumed that t_T = 2 ns.
5. Access times are measured with output reference levels of V_{OH} = 2 V and V_{OL} = 0.8 V.
6. The maximum values of t_{REZ}, t_{CEZ}, t_{OEZ}, and t_{WEZ} are specified when the output is no longer driven. Data in should not be driven until one of the applicable maximum specs is satisfied.

EDO timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 4)

		’46x409-40 ’46x409P-40		’46x409-50 ’46x409P-50		’46x409-60 ’46x409P-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{HPC}	Cycle time, EDO page mode, read-write	16		20		25		ns
t_{PRWC}	Cycle time, EDO read-write	47		57		68		ns
t_{CSH}	Delay time, $\overline{RAS}$ active to $\overline{CAS}$ precharge	32		40		48		ns
t_{CHO}	Hold time, $\overline{OE}$ from $\overline{CAS}$	5		5		5		ns
t_{DOH}	Hold time, output from $\overline{CAS}$	5		5		5		ns
t_{CAS}	Pulse duration, $\overline{CAS}$ active (see Note 7)	6	10000	8	10000	10	10000	ns
t_{WPE}	Pulse duration, $\overline{W}$ active (output disable only)	5		5		5		ns
t_{OCH}	Setup time, $\overline{OE}$ before $\overline{CAS}$	5		5		5		ns
t_{CP}	Pulse duration, $\overline{CAS}$ precharge	6		8		10		ns
t_{OEP}	Precharge time, $\overline{OE}$	5		5		5		ns

NOTES: 4. With ac parameters, it is assumed that t_T = 2 ns.
7. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.

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timing requirements (see Note 4)

		’46x409-40 ’46x409P-40		’46x409-50 ’46x409P-50		’46x409-60 ’46x409P-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write	69		84		104		ns
t_{RWC}	Cycle time, read-write	92		111		135		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ active, fast page mode (see Note 8)	40	100 000	50	100 000	60	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ active, non-page mode (see Note 8)	40	10 000	50	10 000	60	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ precharge	25		30		40		ns
t_{WP}	Pulse duration, write command	6		8		10		ns
t_{RASS}	Pulse duration, $\overline{RAS}$ active, self refresh (see Note 9)	100		100		100		µs
t_{RPS}	Pulse duration, $\overline{RAS}$ precharge after self refresh	70		90		110		ns
t_{ASC}	Setup time, column address	0		0		0		ns
t_{ASR}	Setup time, row address	0		0		0		ns
t_{DS}	Setup time, data in (see Note 9)	0		0		0		ns
t_{RCS}	Setup time, read command	0		0		0		ns
t_{CWL}	Setup time, write command before $\overline{CAS}$ precharge	6		8		10		ns
t_{RWL}	Setup time, write command before $\overline{RAS}$ precharge	6		8		10		ns
t_{WCS}	Setup time, write command before $\overline{CAS}$ active (early-write only)	0		0		0		ns
t_{WRP}	Setup time, $\overline{W}$ high before $\overline{RAS}$ low (CBR refresh only)	5		5		5		ns
t_{WTS}	Setup time, $\overline{W}$ low before $\overline{RAS}$ low (test mode only)	5		5		5		ns
t_{CSR}	Setup time, $\overline{CAS}$ referenced to $\overline{RAS}$ (CBR refresh only)	5		5		5		ns
t_{CAH}	Hold time, column address	6		8		10		ns
t_{DH}	Hold time, data in (see Note 10)	6		8		10		ns
t_{RAH}	Hold time, row address	6		8		10		ns
t_{RCH}	Hold time, read command referenced to $\overline{CAS}$ (see Note 11)	0		0		0		ns
t_{RRH}	Hold time, read command referenced to $\overline{RAS}$ (see Note 11)	0		0		0		ns
t_{WCH}	Hold time, write command during $\overline{CAS}$ active (early-write only)	6		8		10		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$	6		8		10		ns
t_{WRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ low (CBR refresh)	6		8		10		ns
t_{WTH}	Hold time, $\overline{W}$ low after $\overline{RAS}$ low (test mode only)	6		8		10		ns
t_{CHR}	Hold time, $\overline{CAS}$ referenced to $\overline{RAS}$ (CBR refresh only)	6		8		10		ns
t_{OEH}	Hold time, $\overline{OE}$ command	11		13		15		ns
t_{CHS}	Hold time, $\overline{CAS}$ active after $\overline{RAS}$ precharge (self-refresh)	–50		–50		–50		ns
t_{RHCP}	Hold time, $\overline{RAS}$ active from $\overline{CAS}$ precharge	22		28		35		ns

NOTES: 4. With ac parameters, it is assumed that t_T = 2 ns.
8. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
9. During the period of 10 µs $\leq t_{RASS} \leq$ 100 µs, the device is in transition state from normal operation mode to self-refresh mode.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

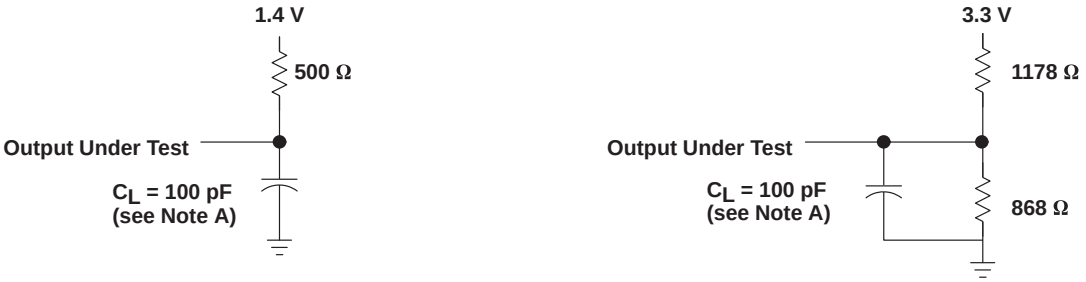
timing requirements (see Note 4) (continued)

			’46x409-40 ’46x409P-40		’46x409-50 ’46x409P-50		’46x409-60 ’46x409P-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{AWD}	Delay time, column address to write command (read-write only)		35		42		49		ns
t_{CPW}	Delay time, $\overline{W}$ low after x$\overline{CAS}$ precharge (read-write only)		37		45		54		ns
t_{CRP}	Delay time, $\overline{CAS}$ precharge to $\overline{RAS}$		5		5		5		ns
t_{CWD}	Delay time, $\overline{CAS}$ to write command (read-write only)		26		30		34		ns
t_{OED}	Delay time, $\overline{OE}$ to data in		11		13		15		ns
t_{RAD}	Delay time, $\overline{RAS}$ to column address (see Note 12)		8	20	10	25	12	30	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ precharge		20		25		30		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ precharge		12		15		18		ns
t_{RCD}	Delay time, $\overline{RAS}$ to $\overline{CAS}$ (see Note 12)		10	29	12	37	14	45	ns
t_{RPC}	Delay time, $\overline{RAS}$ precharge to $\overline{CAS}$		5		5		5		ns
t_{RSH}	Delay time, $\overline{CAS}$ active to $\overline{RAS}$ precharge		6		8		10		ns
t_{RWD}	Delay time, $\overline{RAS}$ to write command (read-write only)		55		67		79		ns
t_{TAA}	Access time from address (test mode)		25		30		35		ns
t_{TCPA}	Access time, from column precharge (test mode)		30		35		40		ns
t_{TRAC}	Access time, from $\overline{RAS}$ (test mode)		45		55		65		ns
t_T	Transition time		1	50	1	50	1	50	ns
t_{REF}	Refresh time interval	’46x409		64		64		64	ms
		’46x409P		128		128		128	ms

NOTES: 4. With ac parameters, it is assumed that t_T = 2 ns.
12. The maximum value is specified only to ensure access time.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



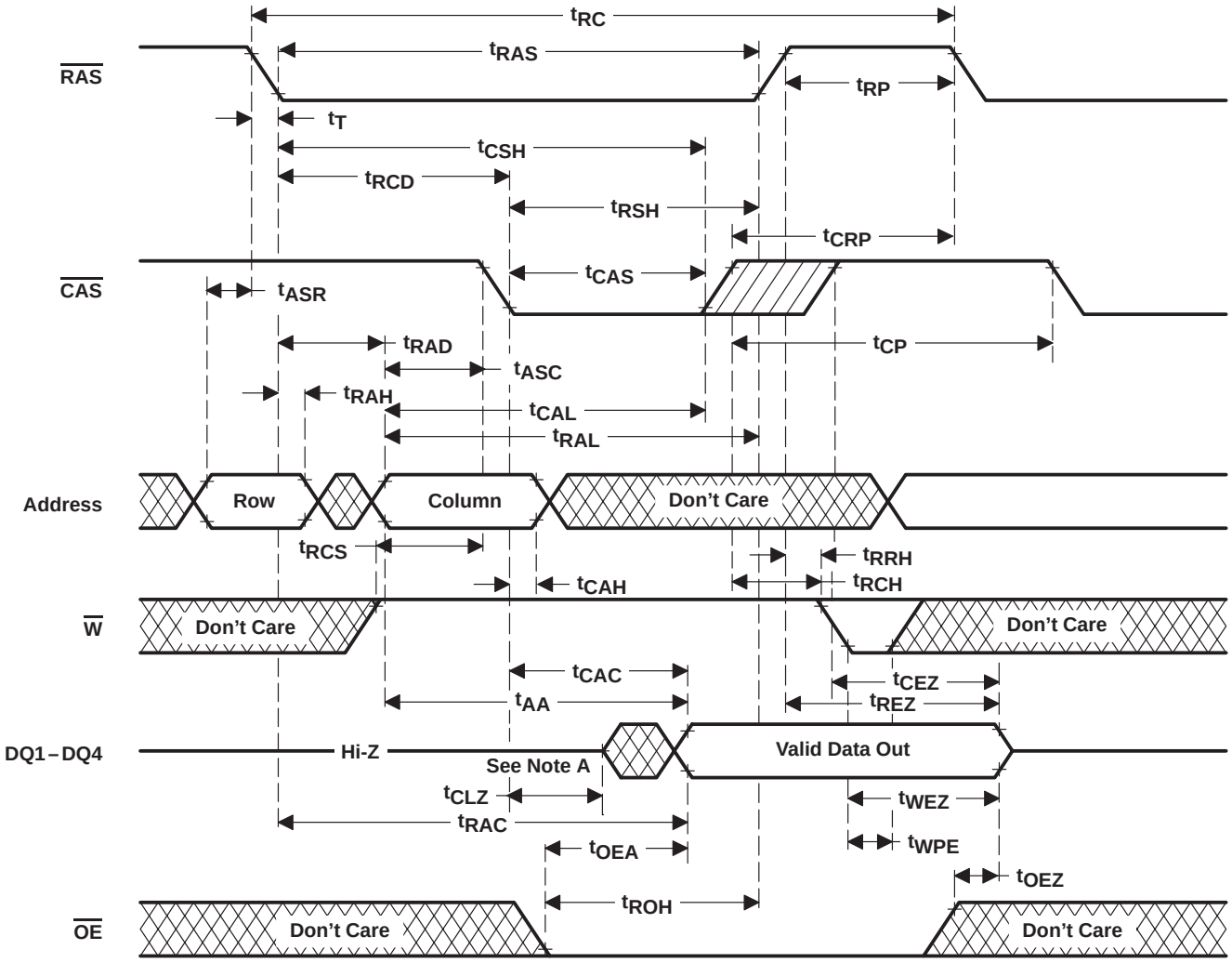
(a) LOAD CIRCUIT **(b) ALTERNATE LOAD CIRCUIT**

NOTE A: C_L includes probe and fixture capacitance.

Figure 2. Load Circuits for Timing Parameters

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 3. Read-Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

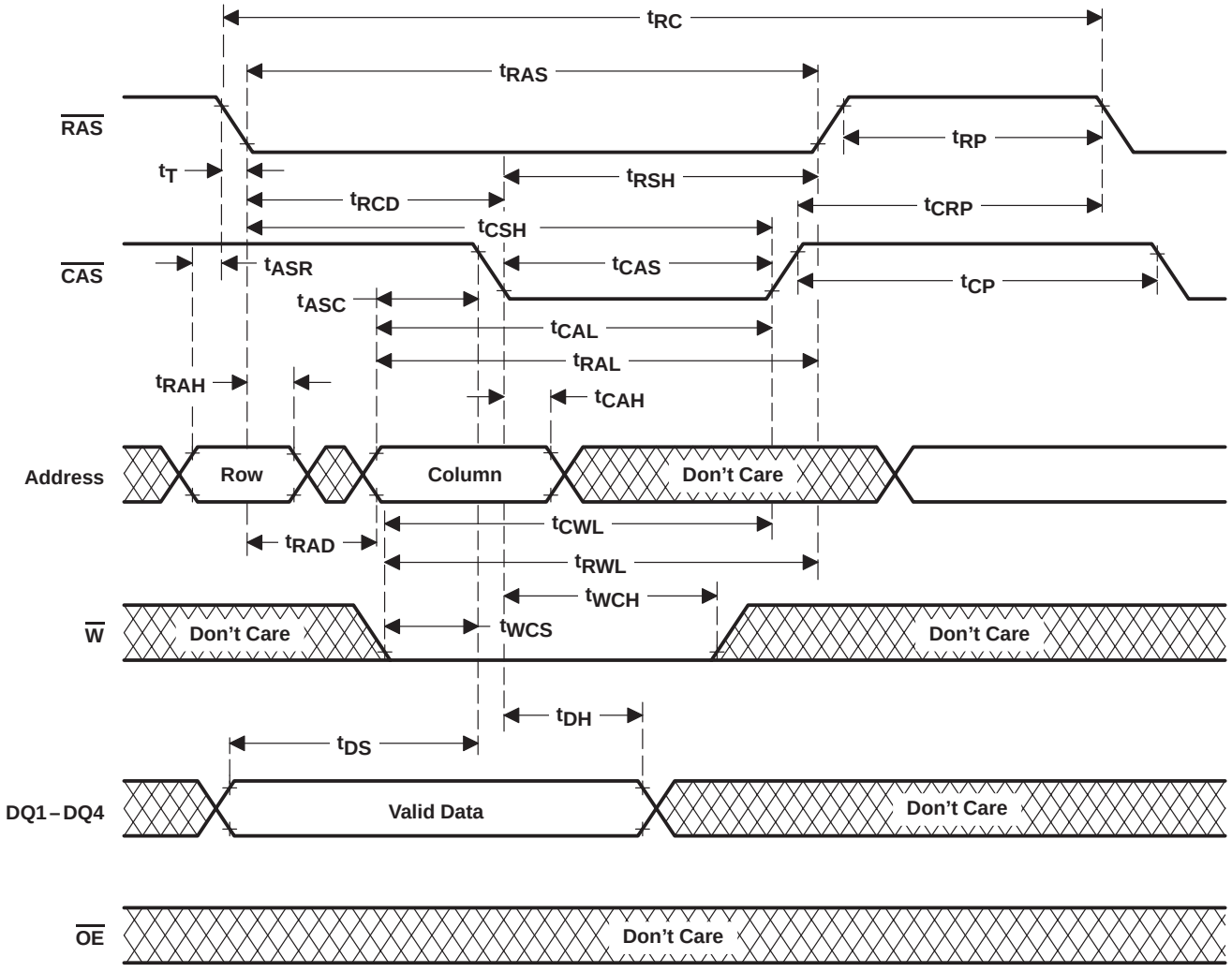


Figure 4. Early-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

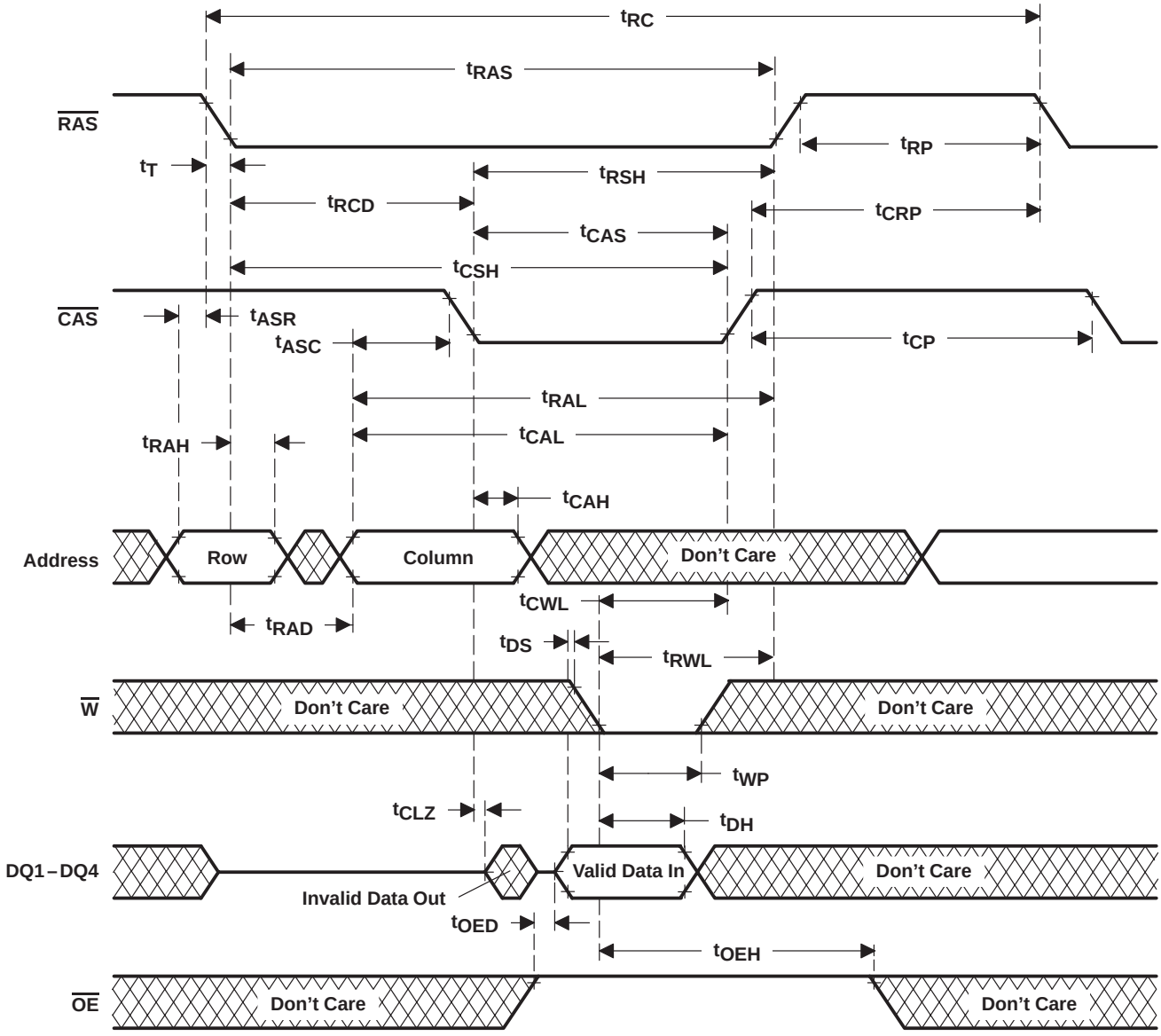
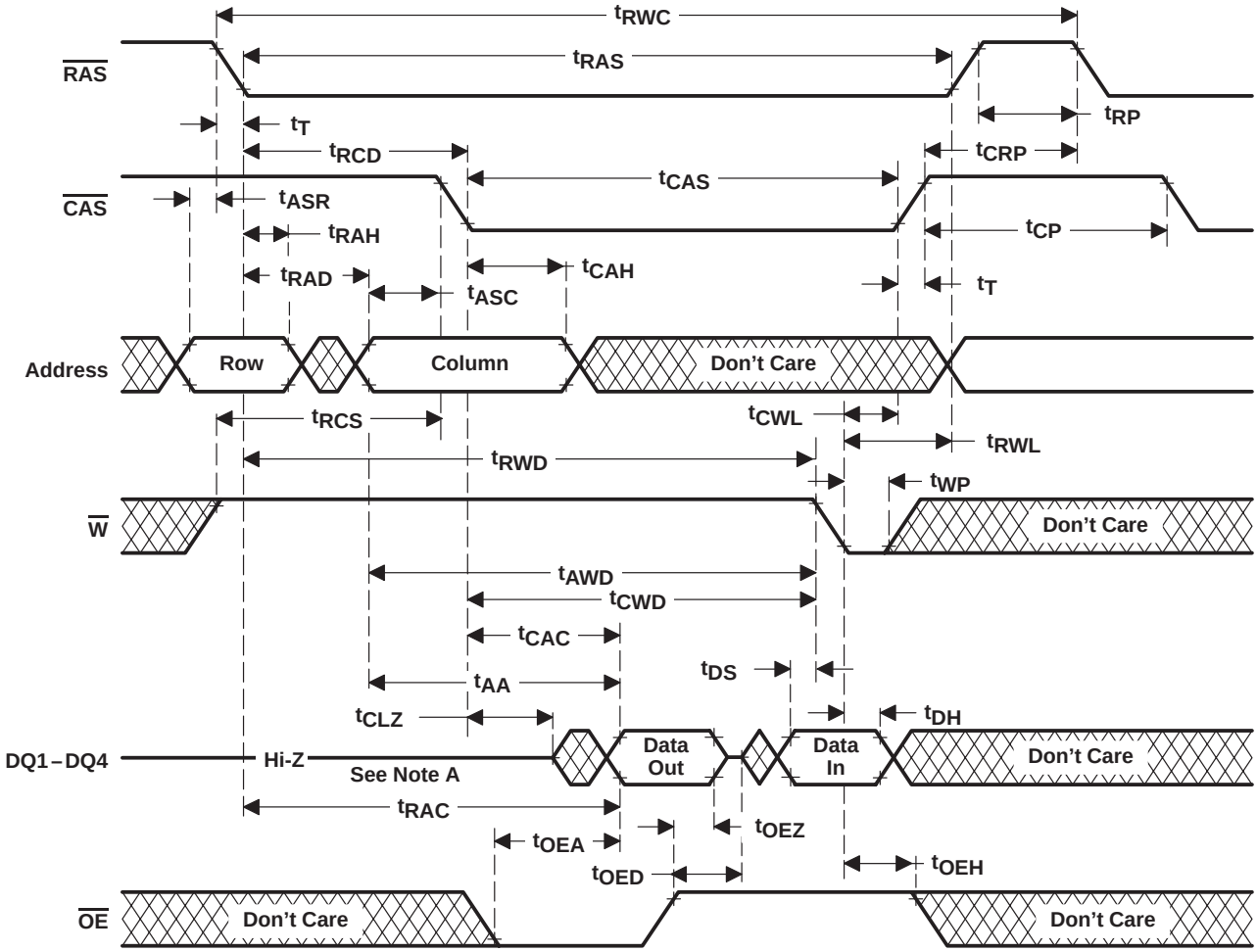


Figure 5. Write-Cycle Timing

PRODUCT PREVIEW

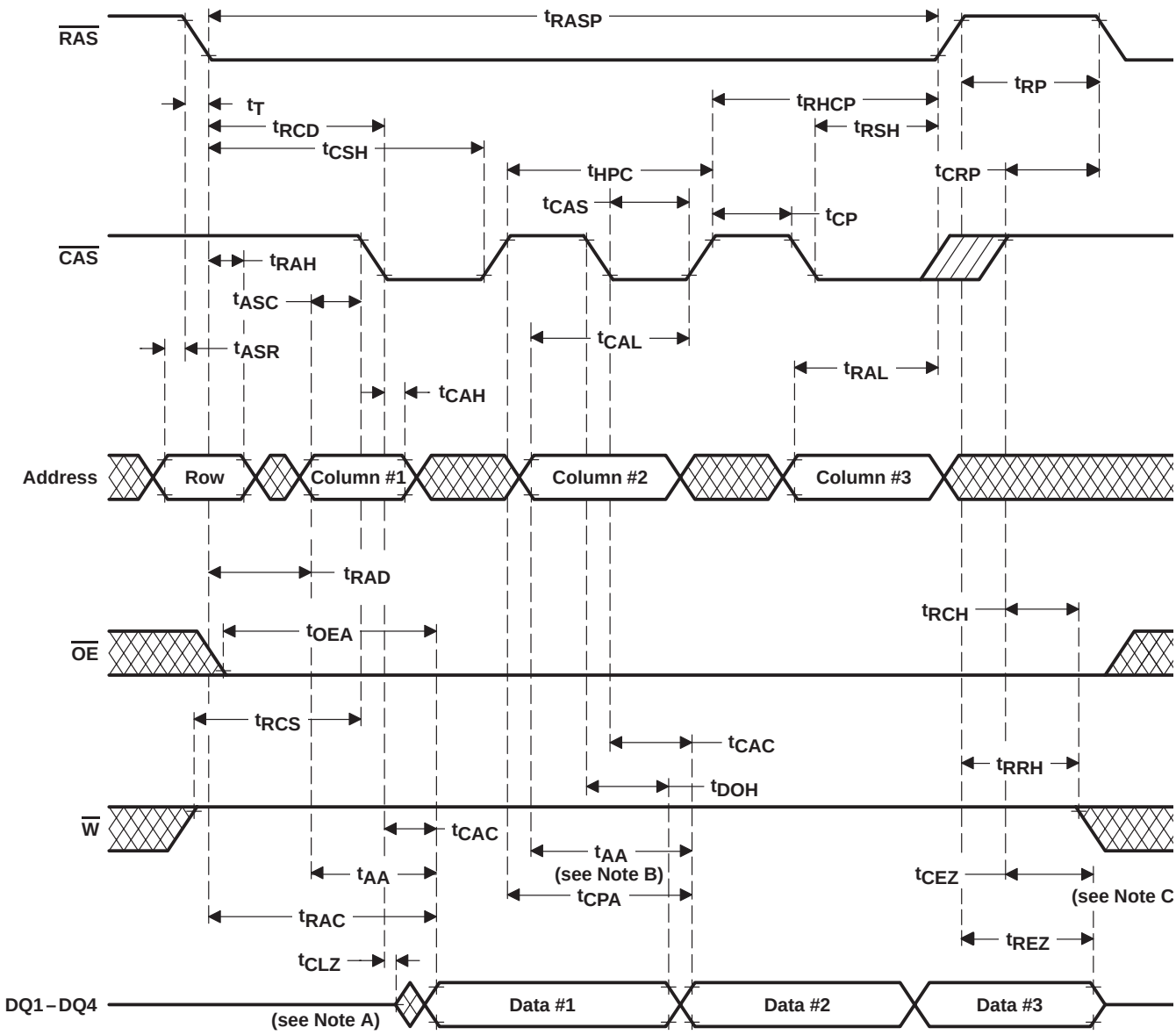
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 6. Read-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

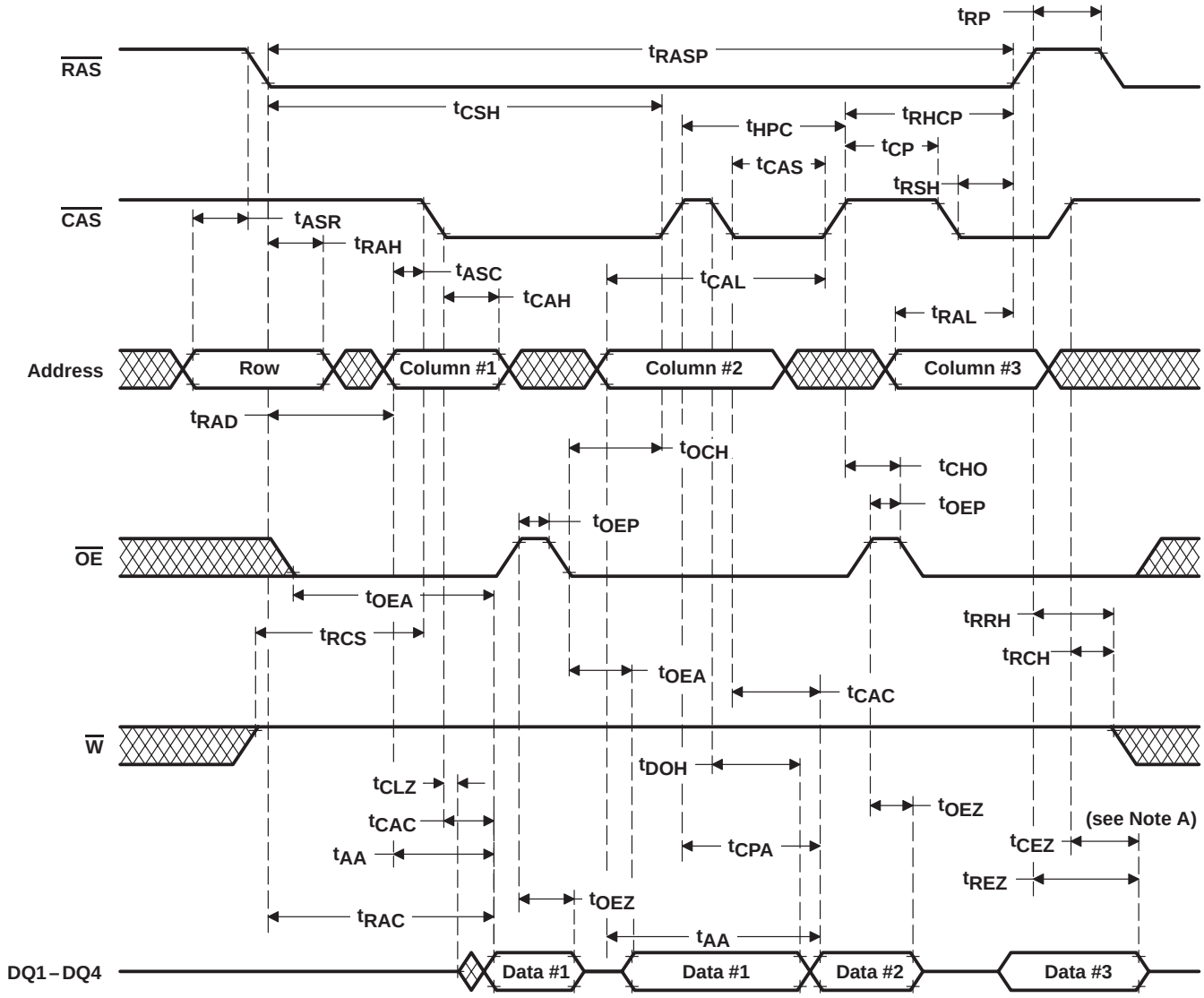


NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. Access time is t_{CPA}-, t_{AA}-, or t_{CAC}-dependent.
C. Output is turned off by t_{CEZ} if $\overline{RAS}$ goes high during $\overline{CAS}$ low.

Figure 7. EDO Read Cycle

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output is turned off by t_{CEZ} if $\overline{RAS}$ goes high during $\overline{CAS}$ low.

Figure 8. EDO Read-Cycle With $\overline{OE}$ Control

PARAMETER MEASUREMENT INFORMATION

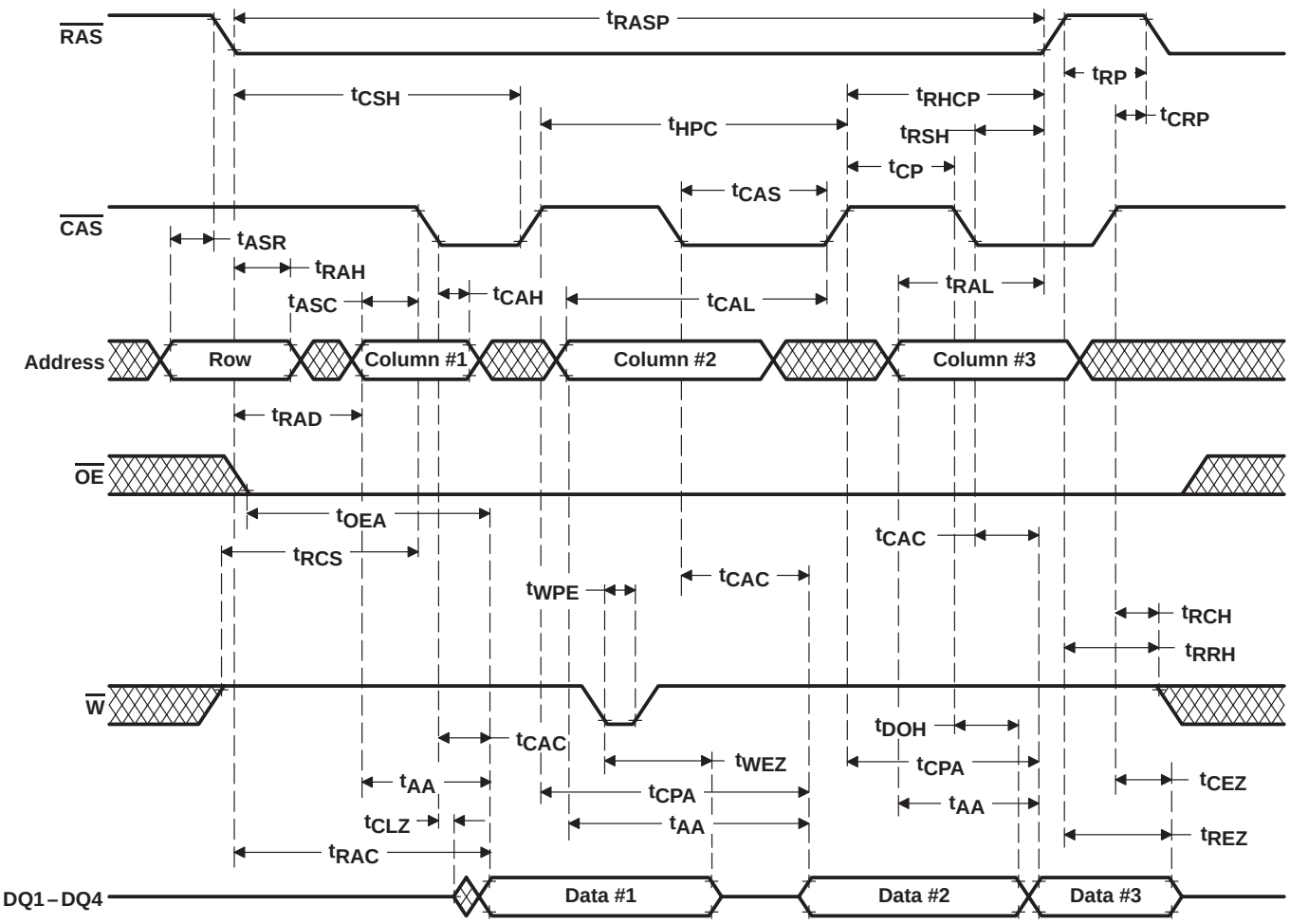
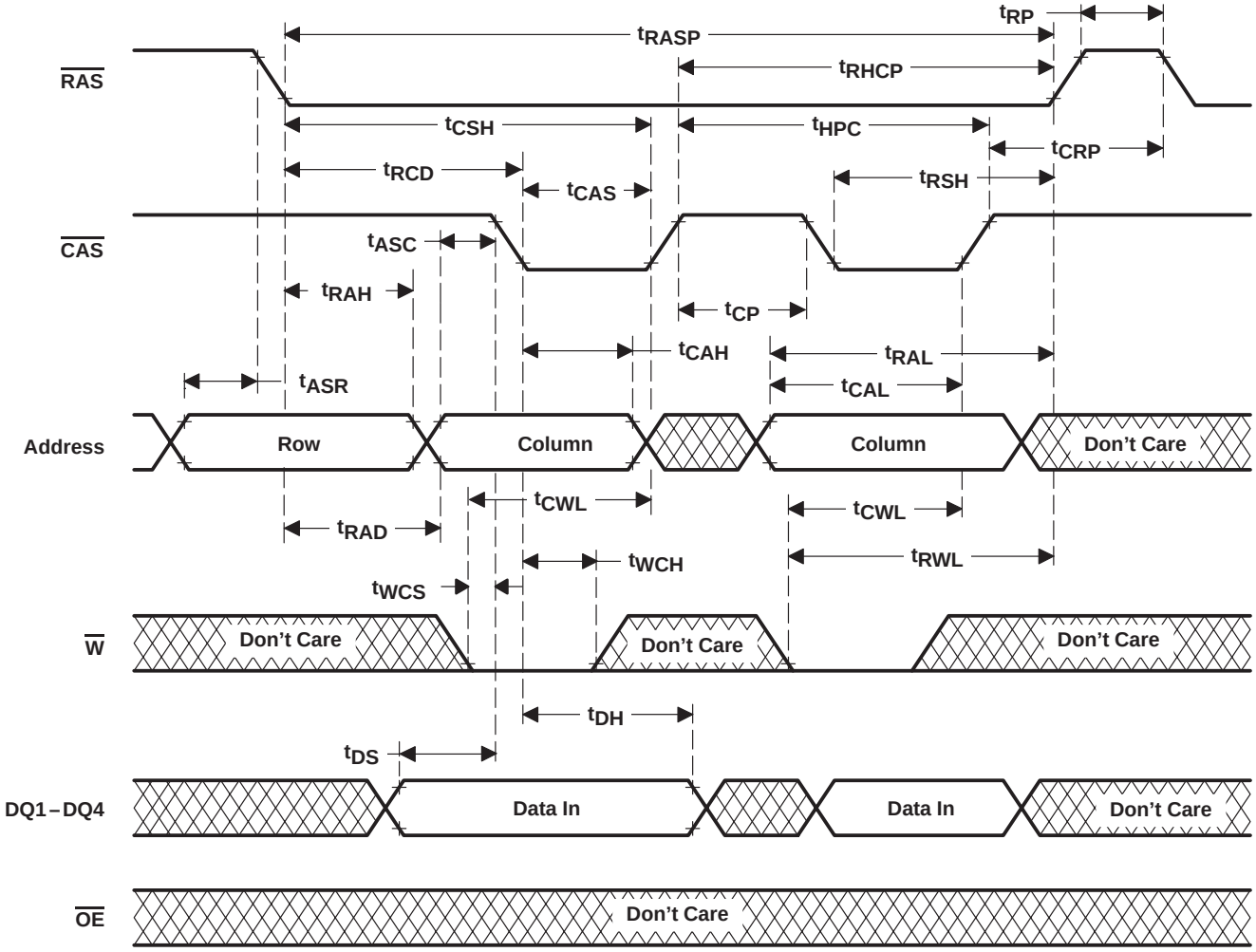


Figure 9. EDO Read-Cycle With $\overline{W}$ Control

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

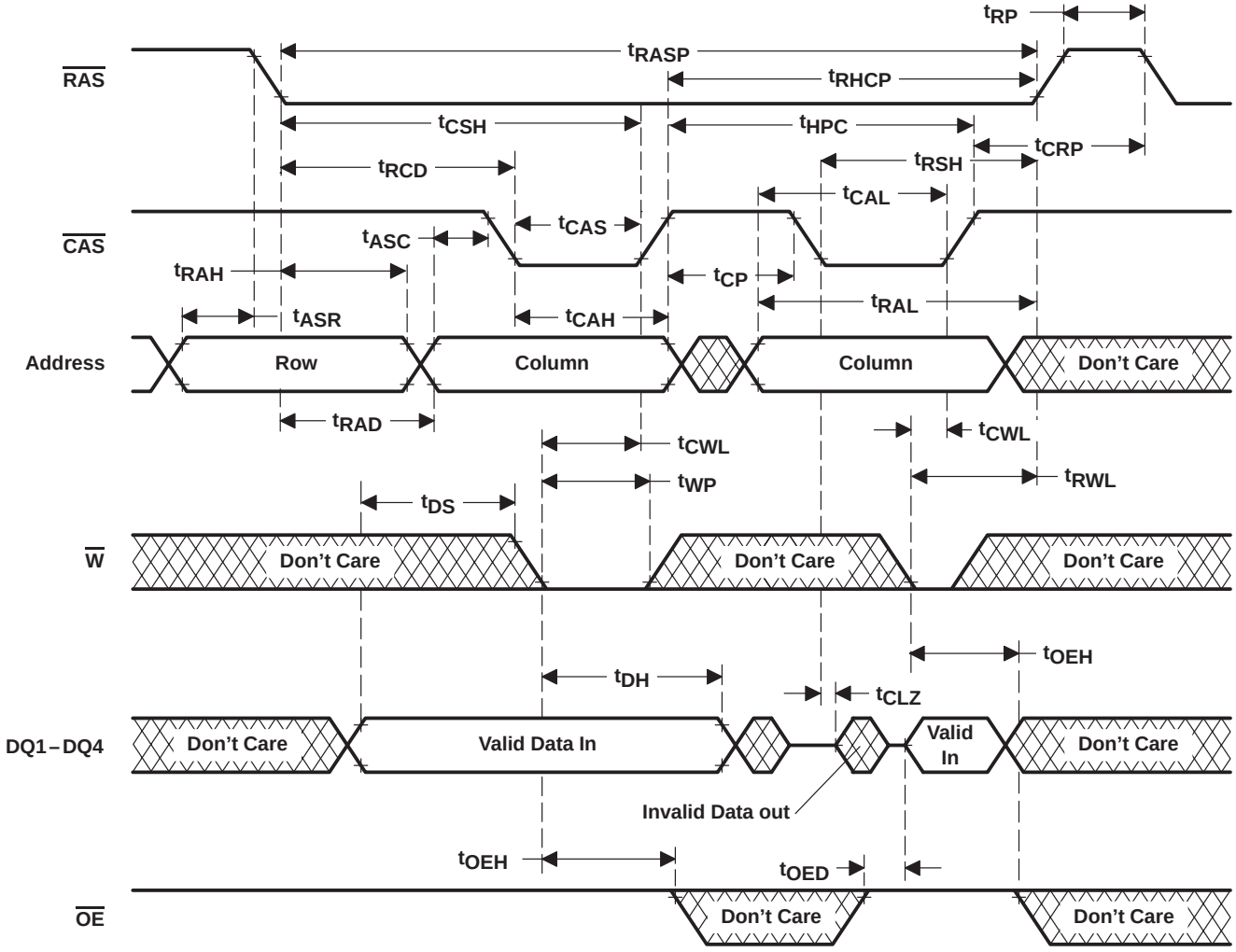


NOTE A: A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 10. EDO Early-Write-Cycle Timing (see Note A)

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTE A: A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 11. EDO Write-Cycle Timing (see Note A)

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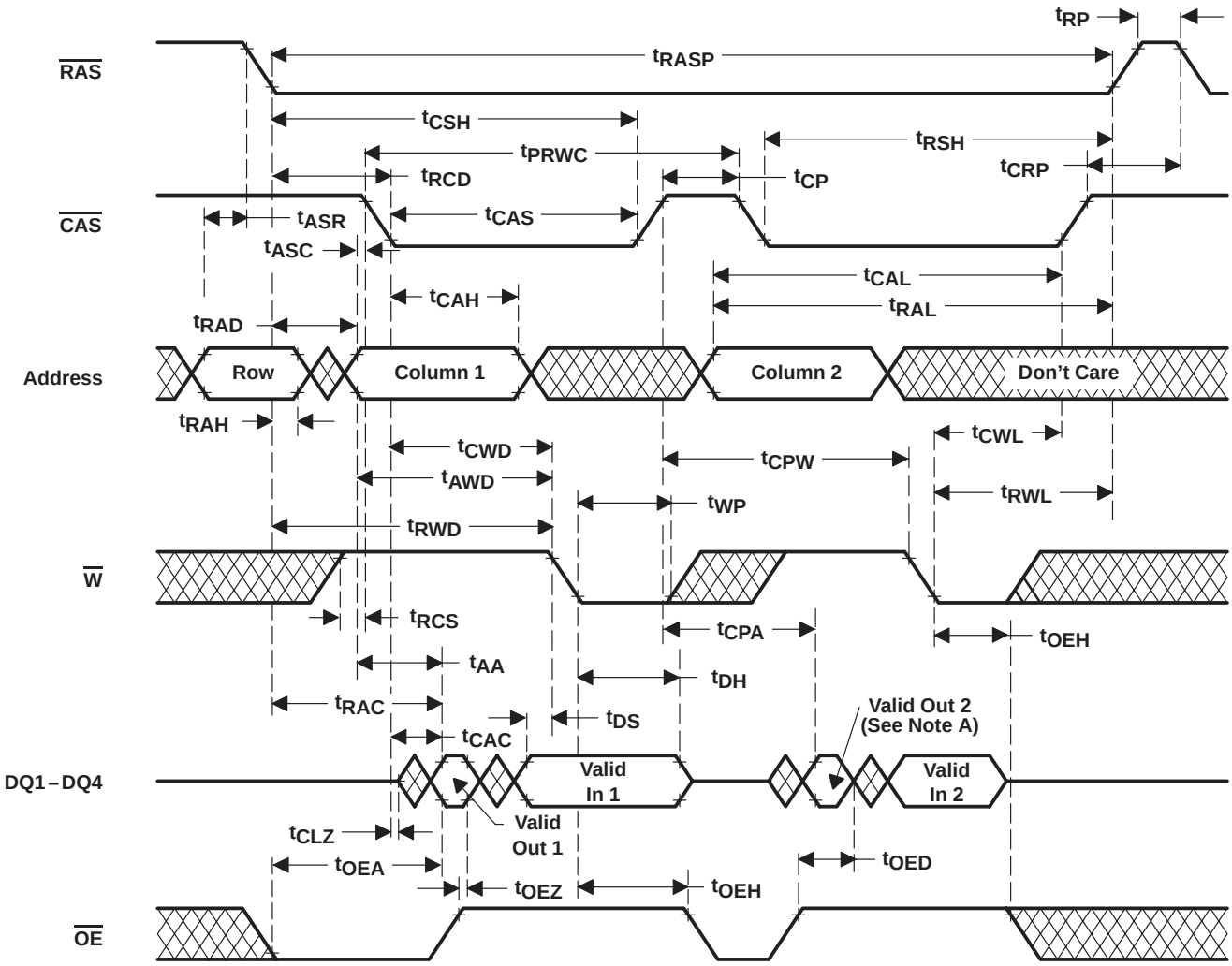
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read- and write-timing specifications are not violated.

Figure 12. EDO Read-Write-Cycle Timing (see Note B)

PARAMETER MEASUREMENT INFORMATION

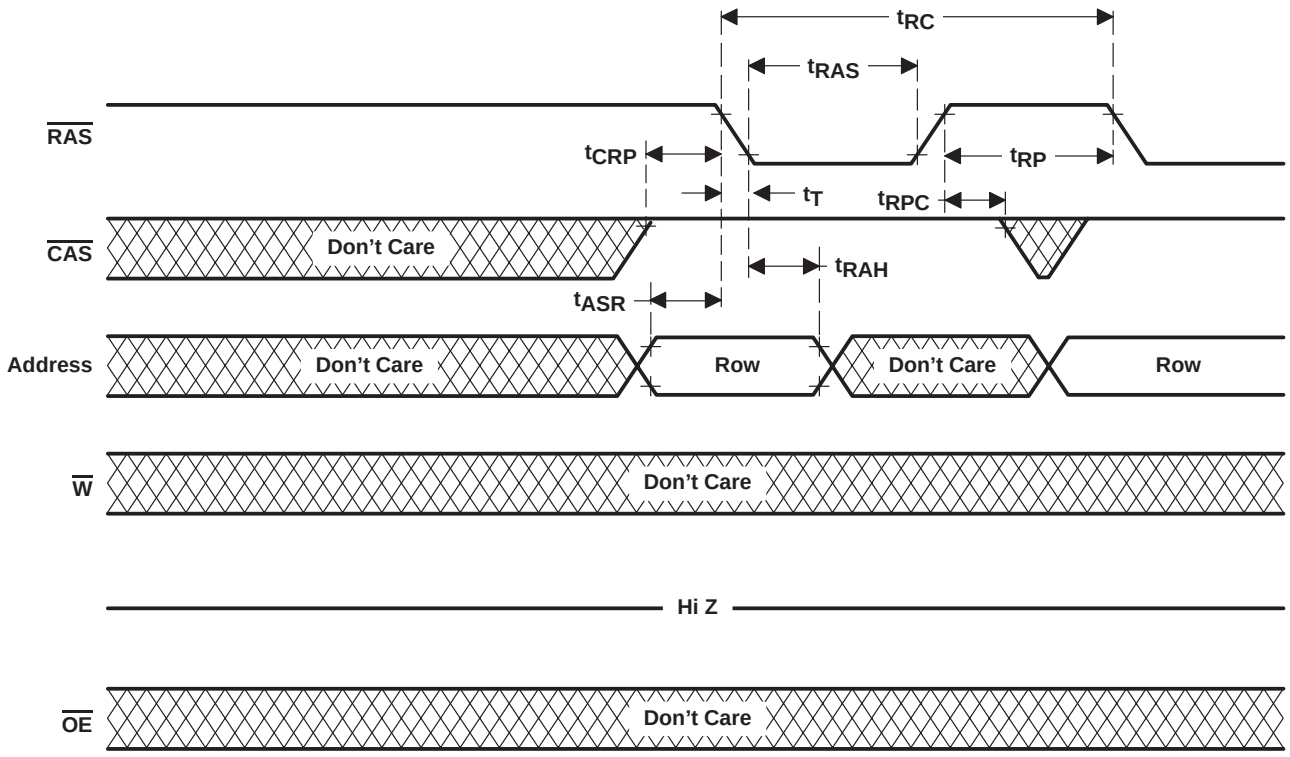


Figure 13. $\overline{\text{RAS}}$-Only Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

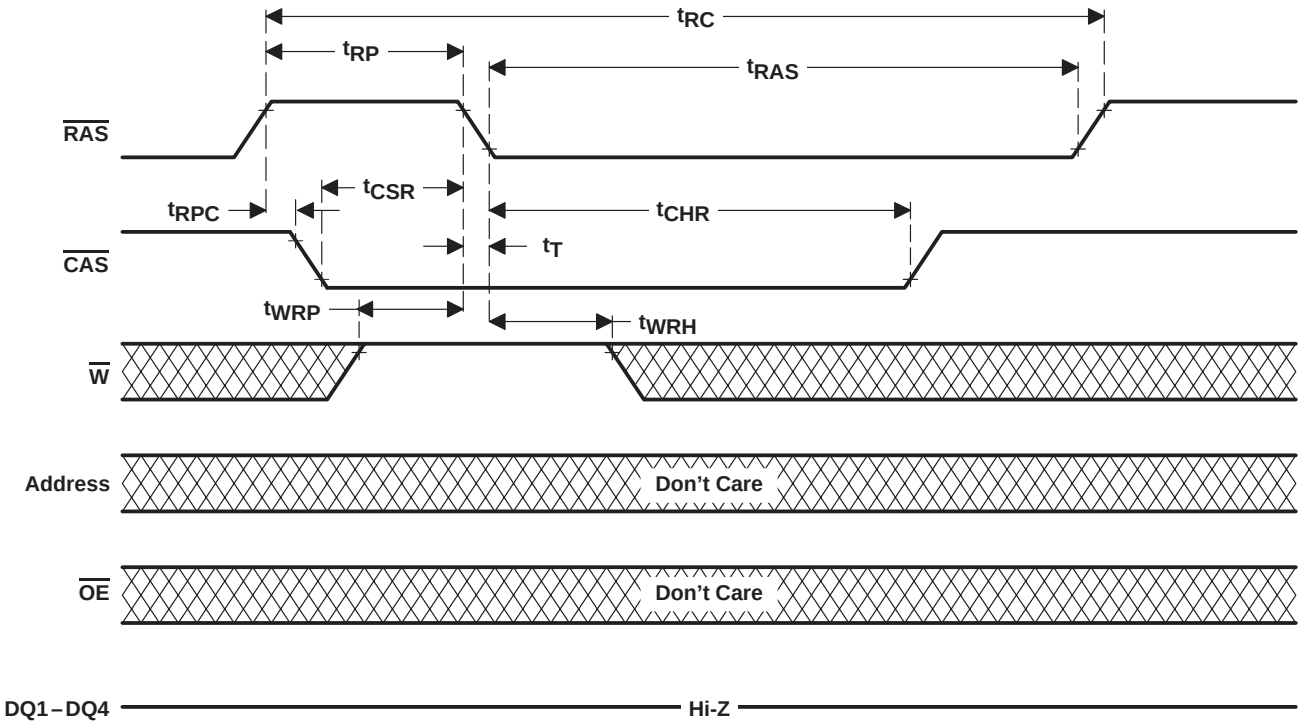


Figure 14. Automatic-CBR-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

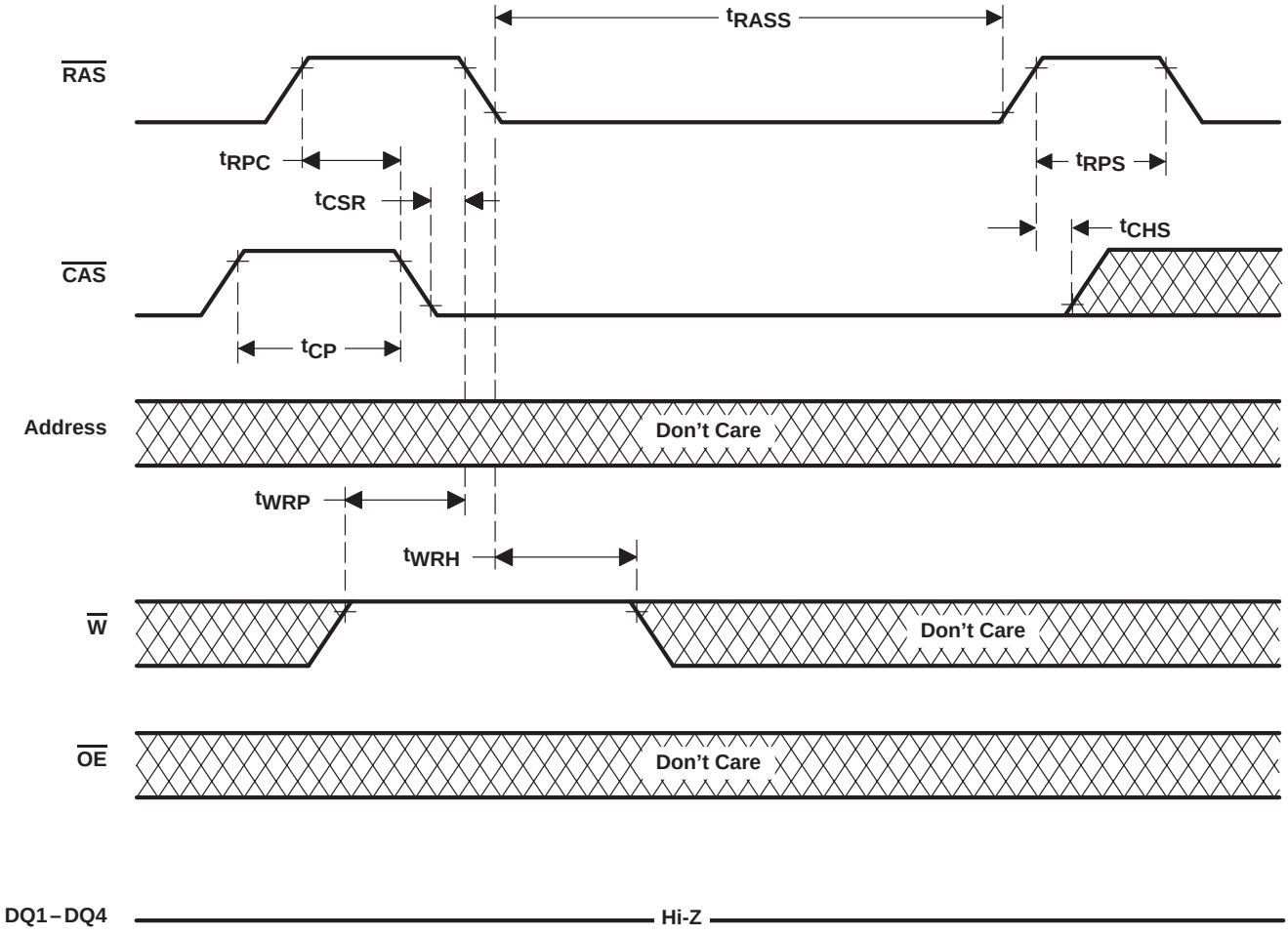


Figure 15. Self-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

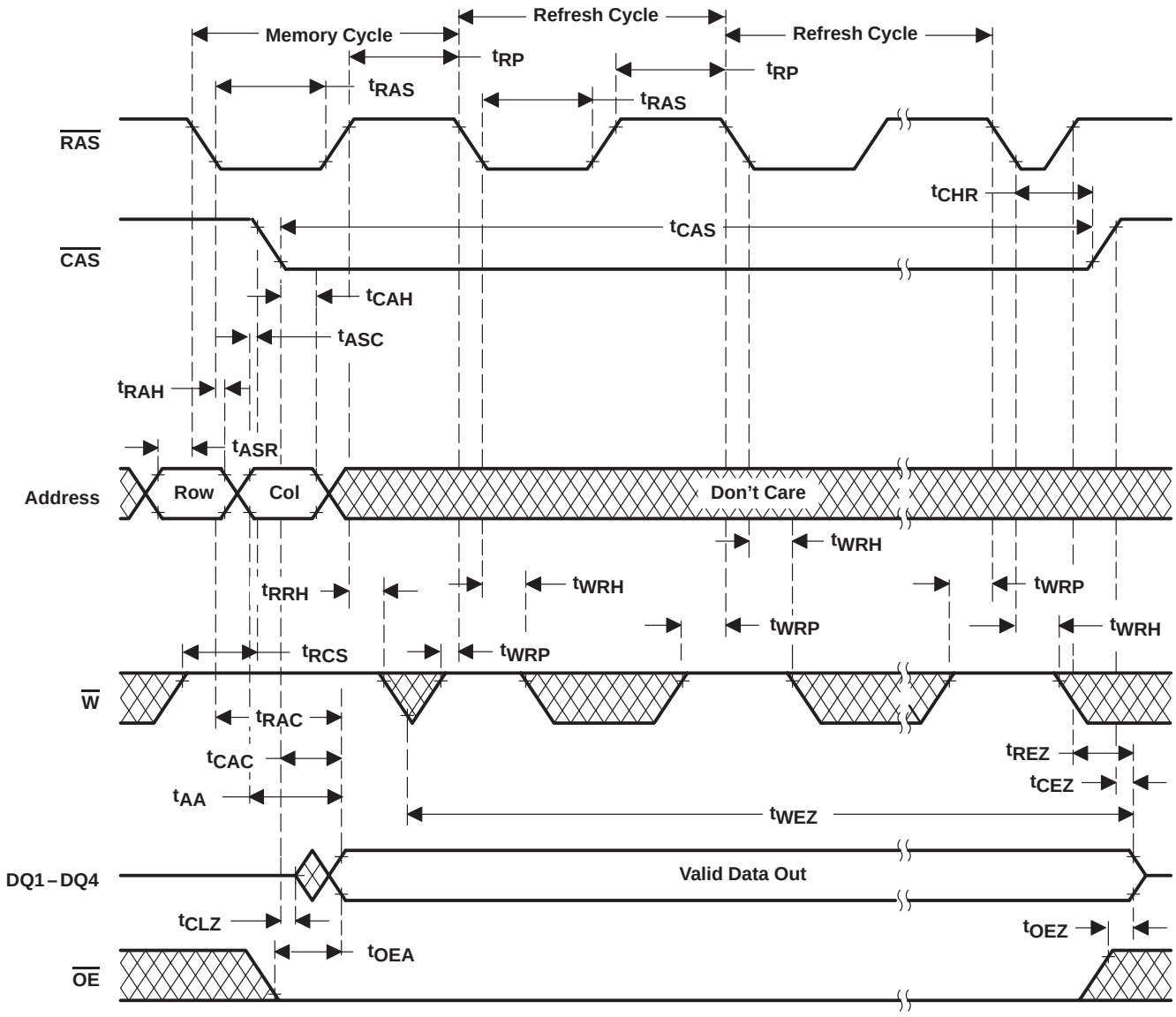


Figure 16. Hidden-Refresh-Cycle (Read) Timing

PARAMETER MEASUREMENT INFORMATION

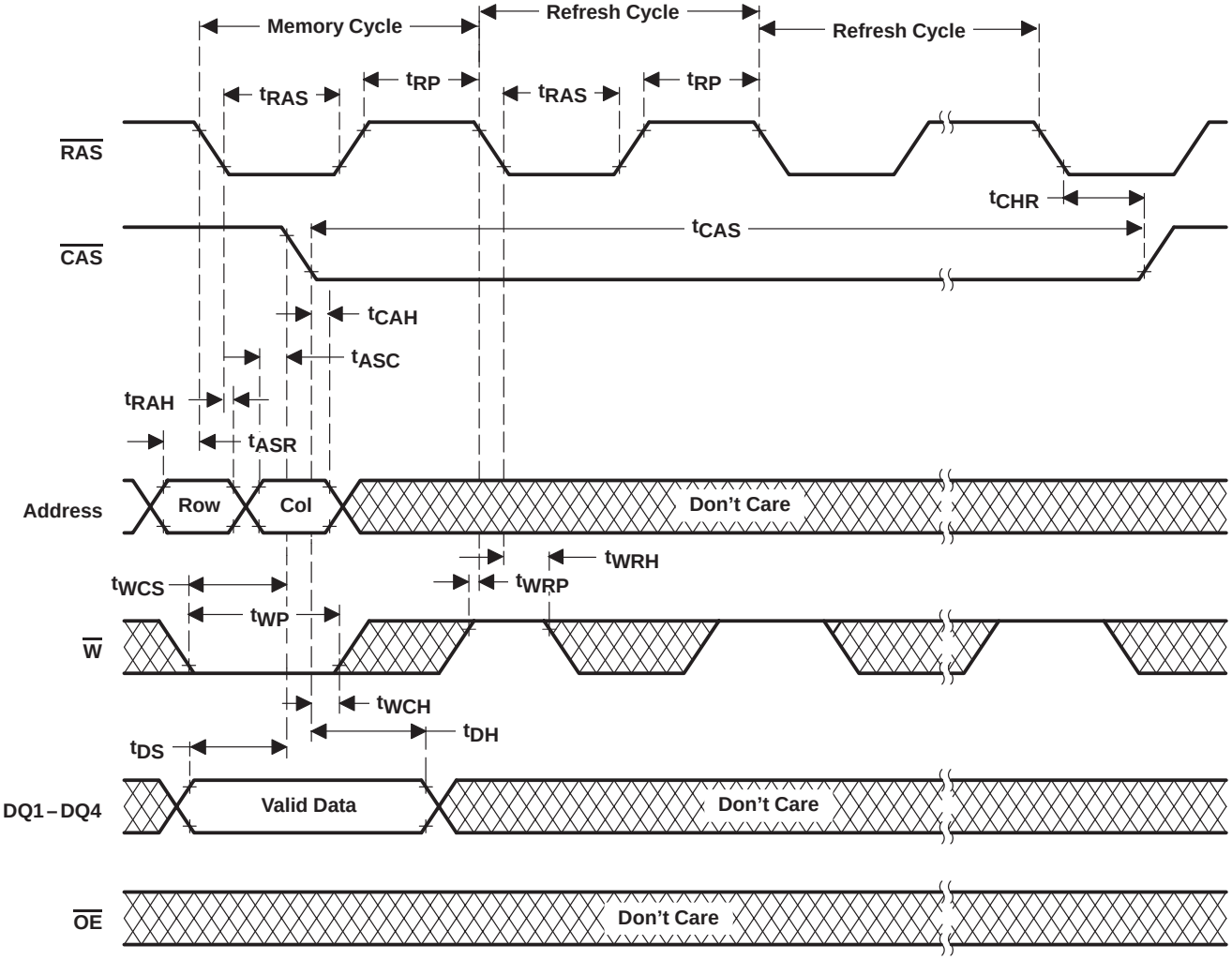


Figure 17. Hidden-Refresh-Cycle (Write) Timing

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PARAMETER MEASUREMENT INFORMATION

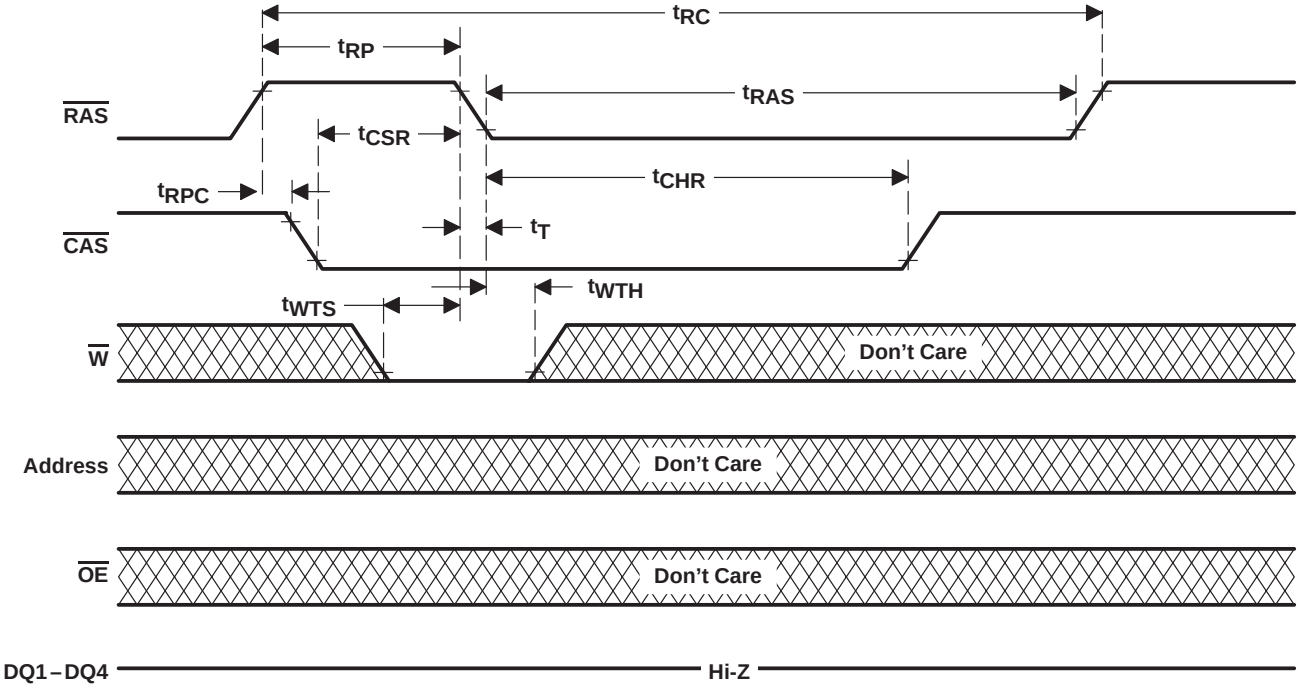


Figure 18. Test-Mode-Entry-Cycle Timing

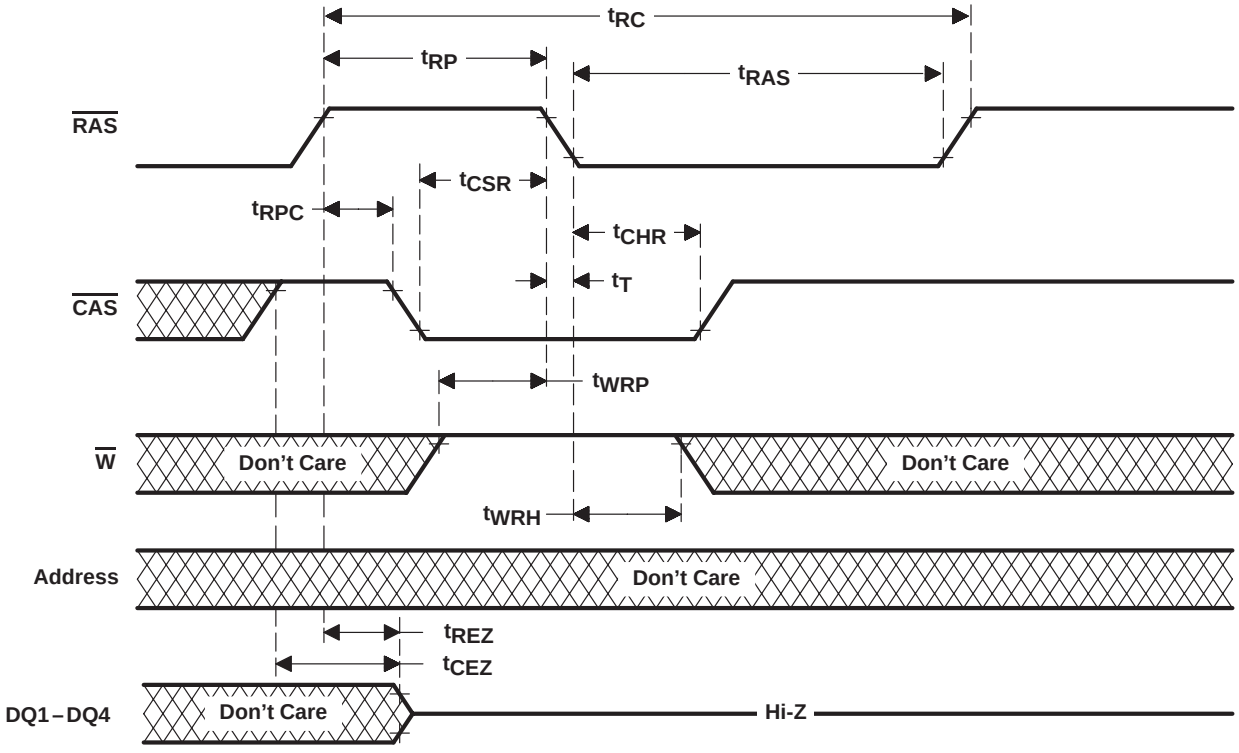
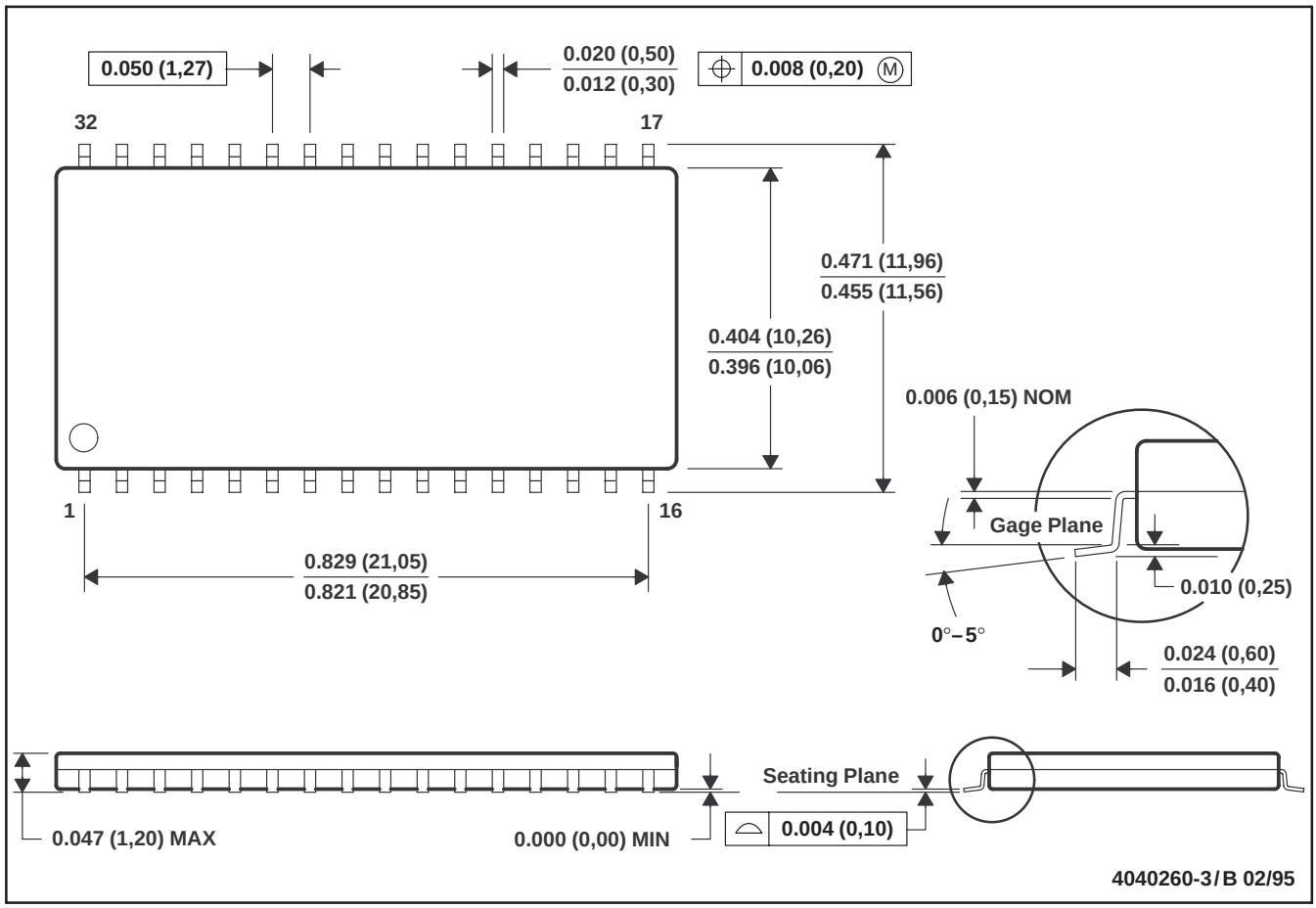


Figure 19. Test-Mode-Exit-Cycle CBR-Refresh-Cycle Timing

MECHANICAL DATA

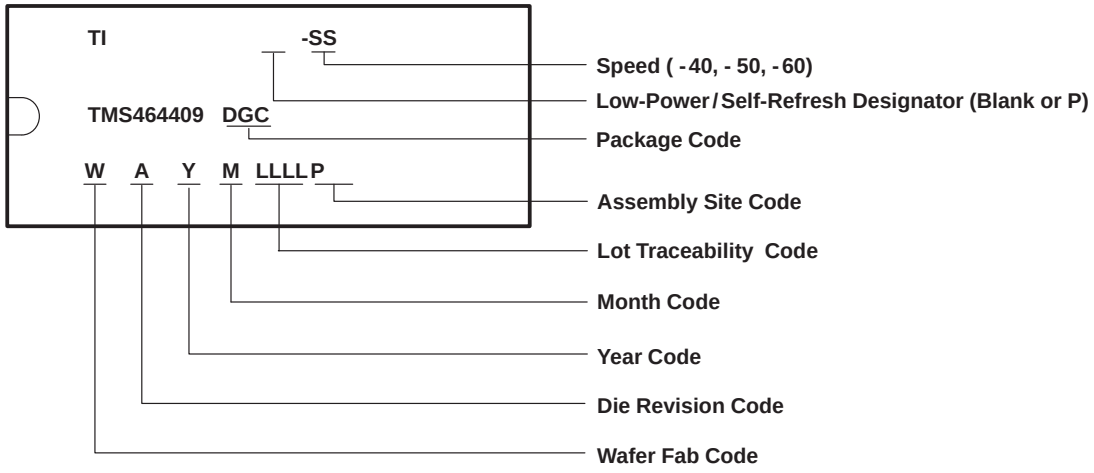
DGC (R-PDSO-G32) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

PRODUCT PREVIEW

device symbolization (TMS464409 illustrated)



PRODUCT PREVIEW

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