TMS470R1VF288
16/32-BIT RISC FLASH MICROCONTROLLER

SPNS095E – JULY 2004 – REVISED DECEMBER 2005

- **High-Performance Static CMOS Technology**
- **TMS470R1x 16/32-Bit RISC Core (ARM7TDMI™)**
  - **24-MHz System Clock (48-MHz Pipeline)**
  - **Independent 16/32-Bit Instruction Set**
  - **Open Architecture With Third-Party Support**
  - **Built-In Debug Module**
- **Integrated Memory**
  - **288K-Byte Program Flash**
    - **Two Banks With 8 Contiguous Sectors**
  - **16K-Byte Static RAM (SRAM)**
  - **Memory Security Module (MSM)**
  - **JTAG Security Module**
- **Operating Features**
  - **Low-Power Modes: STANDBY and HALT**
  - **Industrial/Automotive Temperature Ranges**
- **470+ System Module**
  - **32-Bit Address Space Decoding**
  - **Bus Supervision for Memory/Peripherals**
  - **Digital Watchdog (DWD) Timer**
  - **Analog Watchdog (AWD) Timer**
  - **Enhanced Real-Time Interrupt (RTI)**
  - **Interrupt Expansion Module (IEM)**
  - **System Integrity and Failure Detection**
  - **ICE Breaker**
- **Direct Memory Access (DMA) Controller**
  - **32 Control Packets and 16 Channels**
- **Frequency-Modulated Zero-Pin Phase-Locked Loop (FM_ZPLL)-Based Clock Module With Prescaler**
  - **Multiply-by-8 Internal FM_ZPLL Option**
  - **ZPLL Bypass Mode**
- **Ten Communication Interfaces:**
  - **Two Serial Peripheral Interfaces (SPIs)**
    - **255 Programmable Baud Rates**
  - **Two Serial Communication Interfaces (SCIs)**
    - **2^{24} Selectable Baud Rates**
    - **Asynchronous/Isosynchronous Modes**
  - **Two Standard CAN Controllers (SCC)**
    - **16-Mailbox Capacity**
    - **Fully Compliant With CAN Protocol, Version 2.0B**
  - **Class II Serial Interface B (C2SIb)**
    - **Normal 10.4 Kbps and 4X Mode 41.6 Kbps**
  - **Three Inter-Integrated Circuit (I2C) Modules**
    - **Multi-Master and Slave Interfaces**
    - **Up to 400 Kbps (Fast Mode)**
    - **7- and 10-Bit Address Capability**
- **High-End Timer Lite (HET)**
  - **12 Programmable I/O Channels:**
    - **12 High-Resolution Pins**
  - **High-Resolution Share Feature (XOR)**
  - **High-End Timer RAM**
    - **64-Instruction Capacity**
- **External Clock Prescale (ECP) Module**
  - **Programmable Low-Frequency External Clock (CLK)**
- **12-Channel 10-Bit Multi-Buffered ADC (MibADC)**
  - **64-Word FIFO Buffer**
  - **Single- or Continuous-Conversion Modes**
  - **1.55 μs Minimum Sample/Conversion Time**
  - **Calibration Mode and Self-Test Features**
- **Flexible Interrupt Handling**
- **Expansion Bus Module (EBM) (PGE only)**
  - **Supports 8- and 16-Bit Expansion Bus Memory Interface Mappings**
  - **42 I/O Expansion Bus Pins**
- **50 Dedicated General-Purpose I/O (GIO) Pins and 43 Additional Peripheral I/Os (PGE)**
- **14 Dedicated General-Purpose I/O (GIO) Pins and 43 Additional Peripheral I/Os (PZ)**
- **Sixteen External Interrupts**
- **Compatible ROM Device (Planned)**
- **On-Chip Scan-Base Emulation Logic, IEEE Standard 1149.1(1) (JTAG) Test-Access Port**
- **144-Pin Plastic Low-Profile Quad Flatpack (PGE Suffix)**
- **100-Pin Plastic Low-Profile Quad Flatpack (PZ Suffix)**
- **Development System Support Tools Available**
  - **Code Composer Studio™ Integrated Development Environment (IDE)**
  - **HET Assembler and Simulator**
  - **Real-Time In-Circuit Emulation**
  - **Flash Programming**

PRODUCT PREVIEW

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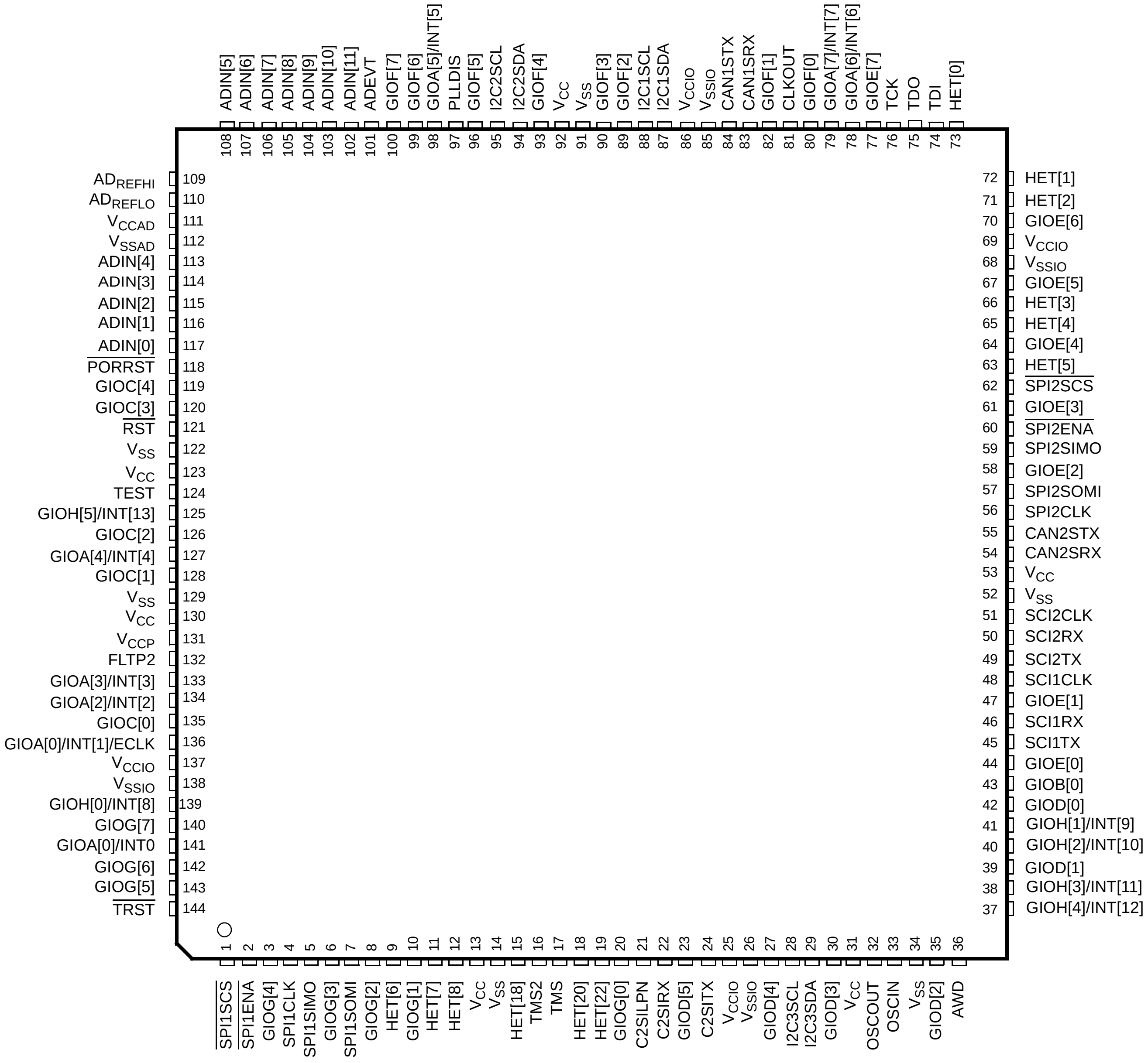
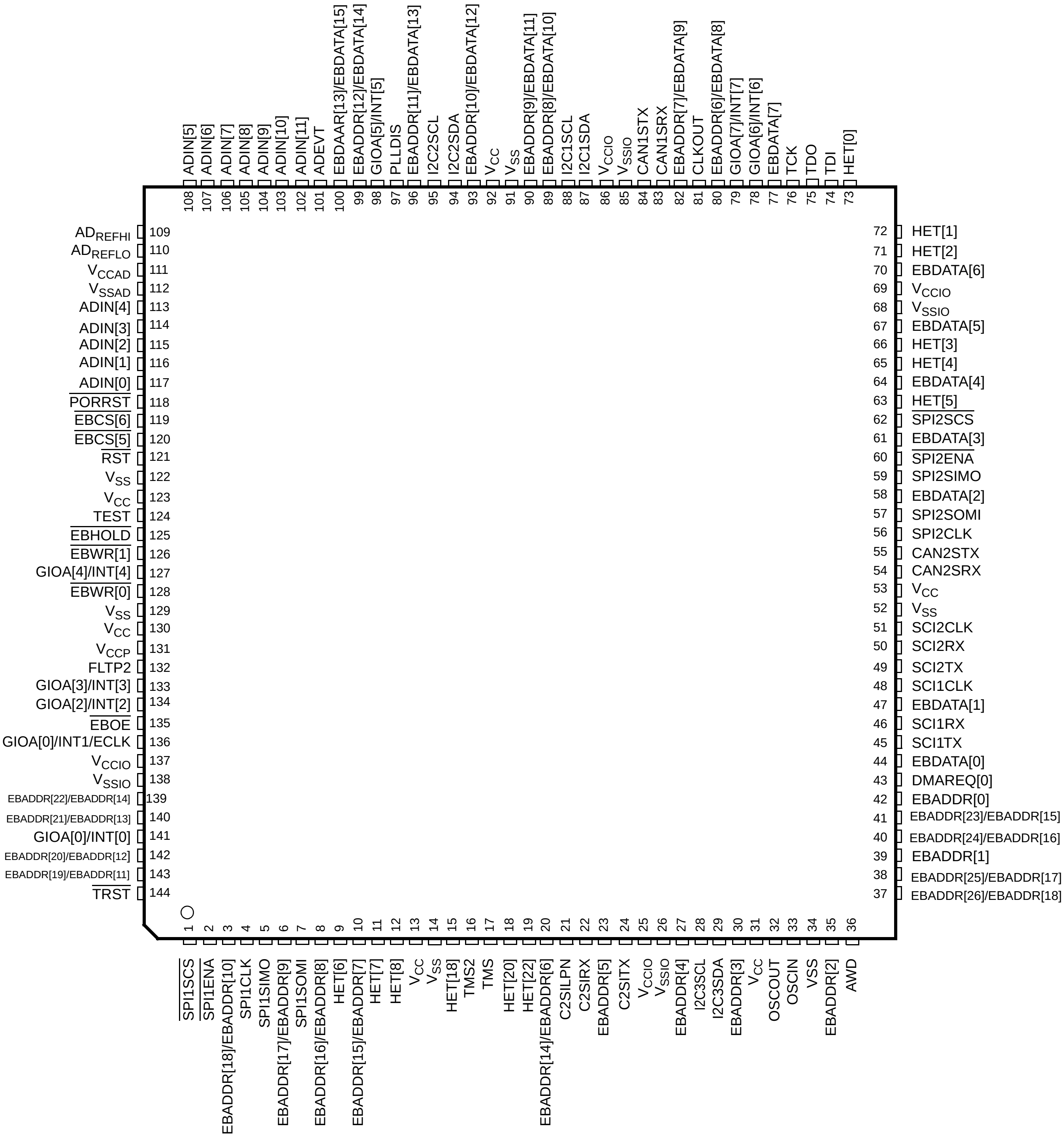
1 The test-access port is compatible with the IEEE Standard 1149.1-1990, *IEEE Standard Test-Access Port and Boundary Scan Architecture* specification. Boundary scan is not supported on this device.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

TMS470R1VF288 144-PIN PGE PACKAGE (TOP VIEW) (without Expansion Bus)

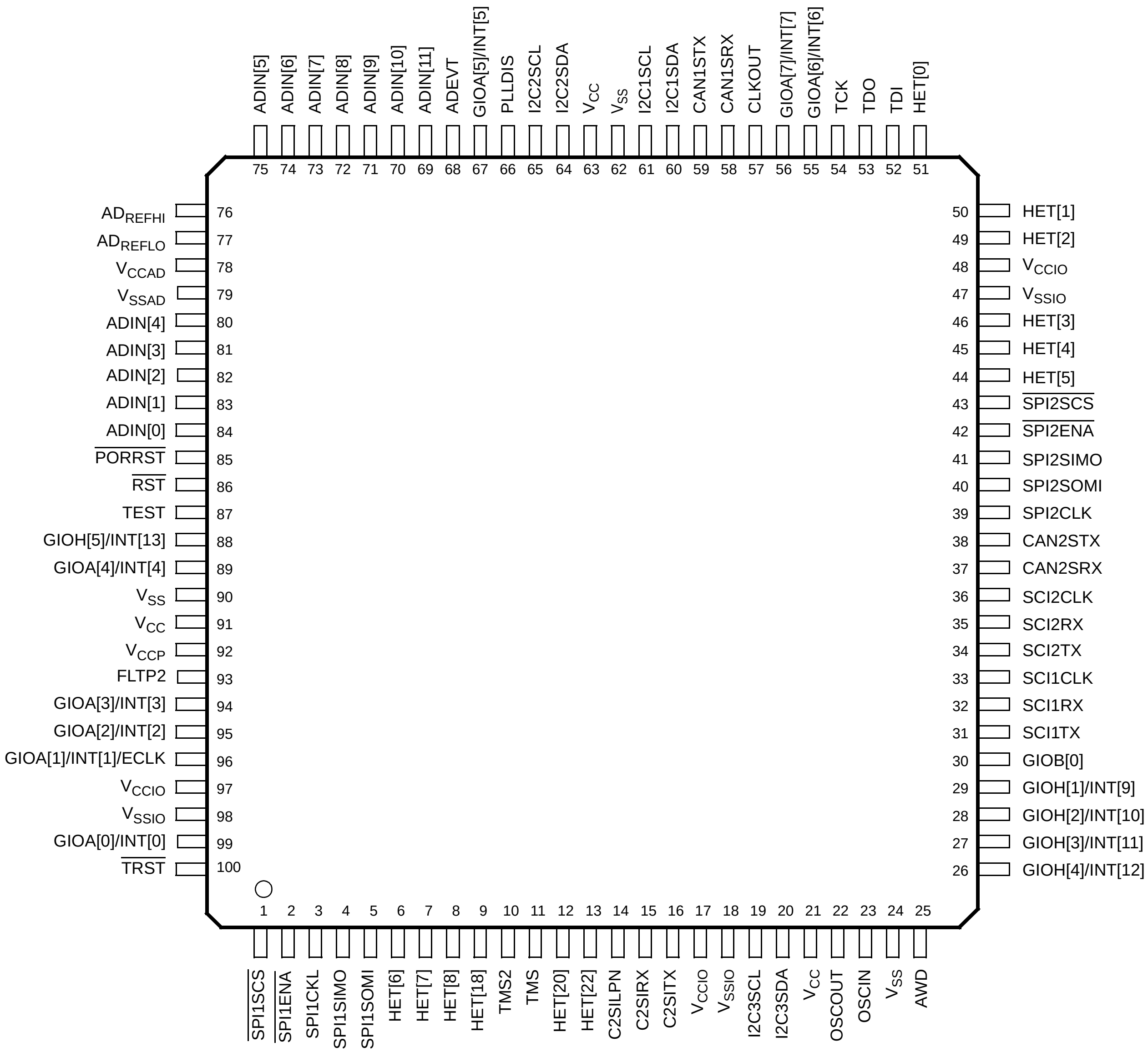


TMS470R1VF288 144-PIN PGE PACKAGE (TOP VIEW) (with Expansion Bus)



PRODUCT PREVIEW

TMS470R1VF288 100-PIN PZ PACKAGE (TOP VIEW)



description

The TMS470R1VF288(1) devices are members of the Texas Instruments TMS470R1x family of general-purpose16/32-bit reduced instruction set computer (RISC) microcontrollers. The VF288 microcontroller offers high performance utilizing the high-speed ARM7TDMI 16/32-bit RISC central processing unit (CPU), resulting in a high instruction throughput while maintaining greater code efficiency. The ARM7TDMI 16/32-bit RISC CPU views memory as a linear collection of bytes numbered upwards from zero. The TMS470R1VF288 utilizes the big-endian format where the most significant byte of a word is stored at the lowest numbered byte and the least significant byte at the highest numbered byte.

High-end embedded control applications demand more performance from their controllers while maintaining low costs. The VF288 RISC core architecture offers solutions to these performance and cost demands while maintaining low power consumption.

The VF288 devices contain the following:

- ARM7TDMI 16/32-Bit RISC CPU
- TMS470R1x system module (SYS) with 470+ enhancements
- 288K-byte flash
- 16K-byte SRAM
- Frequency-modulated zero-pin phase-locked loop (FM_ZPLL) clock module
- Digital watchdog (DWD) timer
- Analog watchdog (AWD) timer
- Enhanced real-time interrupt (RTI) module
- Interrupt expansion module (IEM)
- Memory security module (MSM)
- JTAG security module
- Two serial peripheral interface (SPI) modules
- Two serial communications interface (SCI) modules
- Two standard CAN controllers (SCC)
- Three inter-integrated circuit (I2C) modules
- Class II Serial Interface B (C2SIb) module
- 10-bit multi-buffered analog-to-digital converter (MibADC), with 12 input channels
- High-end timer lite (HET) controlling 12 I/Os
- External Clock Prescale (ECP)
- Expansion Bus Module (EBM)
- Up to 93 I/O pins (PGE only), up to 57 I/O (PZ only)

The functions performed by the 470+ system module (SYS) include:

- Address decoding
- Memory protection
- Memory and peripherals bus supervision
- Reset and abort exception management
- Prioritization for all internal interrupt sources
- Device clock control
- Parallel signature analysis (PSA)

The enhanced real-time interrupt (RTI) module on the VF288 has the option to be driven by the oscillator clock. The digital watchdog (DWD) is a 25-bit resettable decrementing counter that provides a system reset when the watchdog counter expires. This data sheet includes device-specific information such as memory and peripheral select assignment, interrupt priority, and a device memory map. For a more detailed functional description of the SYS module, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

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1 Throughout the remainder of this document, the TMS470R1VF288 shall be referred to as either the full device name or VF288.

description (continued)

The VF288 memory includes general-purpose SRAM supporting single-cycle read/write accesses in byte, half-word, and word modes.

The flash memory on this device is a nonvolatile, electrically erasable and programmable memory implemented with a 32-bit-wide data bus interface.The flash operates with a system clock frequency of up to 24 MHz. When in pipeline mode, the flash operates with a system clock frequency of up to 48 MHz. For more detailed information on the flash, see the flash section of this data sheet and the *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213).

The memory security module (MSM) and JTAG security module prevent unauthorized access and visibility to on-chip memory, thereby preventing reverse engineering or manipulation of proprietary code. For more information, see the *TMS470R1x Memory Security Module Reference Guide* (literature number SPNU246) and the *TMS470R1x JTAG Security Module Reference Guide* (literature number SPNU245).

The VF288 device has ten communication interfaces: two SPIs, two SCIs, two SCCs, a C2SI, and three I2Cs. The SPI provides a convenient method of serial interaction for high-speed communications between similar shift-register type devices. The SCI is a full-duplex, serial I/O interface intended for asynchronous communication between the CPU and other peripherals using the standard non-return-to-zero (NRZ) format. The SCC uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 megabit per second (Mbps). The SCC is ideal for applications operating in noisy and harsh environments (e.g., automotive and industrial fields) that require reliable serial communication or multiplexed wiring. The C2SIb allows the VF68x to transmit and receive messages on a class II network following an SAE Standard J1850 Class B Data Communication Network Interface standard. The I2C module is a multi-master communication module providing an interface between the VF288 microcontroller and an I2C-compatible device via the I2C serial bus. The I2C supports both 100 Kbps and 400 Kbps speeds. For more detailed functional information on the SPI, SCI, and CAN peripherals, see the specific reference guides (literature numbers SPNU195, SPNU196, and SPNU197). For more detailed functional information on the I2C, see the *TMS470R1x Inter-Integrated Circuit (I2C) Reference Guide* (literature number SPNU223*).* For more detailed functional information on the C2SI, see the *TMS470R1x Class II Serial Interface B (C2SIb) Reference Guide* (literature number SPNU214*).*

The HET is an advanced intelligent timer that provides sophisticated timing functions for real-time applications. The timer is software-controlled, using a reduced instruction set, with a specialized timer micromachine and an attached I/O port. The HET can be used for compare, capture, or general-purpose I/O. It is especially well suited for applications requiring multiple sensor information and drive actuators with complex and accurate time pulses. The HET used in this device is the high-end timer lite. It has fewer I/Os than the usual 32 in a standard HET. For more detailed functional information on the HET, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199). The VF288 HET peripheral contains the XOR-share feature. This feature allows two adjacent HET high- resolution channels to be XORed together, making it possible to output smaller pulses than a standard HET. For more detailed information on the HET XOR-share feature, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).

The VF288 device has one 10-bit-resolution, sample-and-hold MibADC. Each of the MibADC channels can be converted individually or can be grouped by software for sequential conversion sequences. There are three separate groupings, two of which can be triggered by an external event. Each sequence can be converted once when triggered or configured for continuous conversion mode. For more detailed functional information on the MibADC, see the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

description (continued)

The frequency-modulated zero-pin phase-locked loop (FM_ZPLL) clock module contains a phase-locked loop, a clock-monitor circuit, a clock-enable circuit, and a prescaler (with prescale values of 1–8). The function of the FM_ZPLL is to multiply the external frequency reference to a higher frequency for internal use. The FM_ZPLL provides ACLK to the system (SYS) module. The SYS module subsequently provides system clock (SYSCLK), real-time interrupt clock (RTICLK), CPU clock (MCLK), and peripheral interface clock (ICLK) to all other VF288 device modules. For more detailed functional information on the FM_ZPLL, see the *TMS470R1x Frequency-Modulated Phase-Locked Loop (FMPLL) Clock Module Reference Guide* (literature number SPNU221).

NOTE

ACLK should not be confused with the MibADC internal clock, ADCLK. ACLK is the continuous system clock from an external resonator/crystal reference.

The expansion bus module (EBM) is a standalone module that supports the multiplexing of the GIO functions and the expansion bus interface. For more information on the EBM, see the *TMS470R1x Expansion Bus Module (EBM) Reference Guide* (literature number SPNU222).

The VF288 device also has an external clock prescaler (ECP) module that when enabled, outputs a continuous external clock (ECLK) on a specified GIO pin. The ECLK frequency is a user-programmable ratio of the peripheral interface clock (ICLK) frequency. For more detailed functional information on the ECP, see the *TMS470R1x External Clock Prescaler (ECP) Reference Guide* (literature number SPNU202).

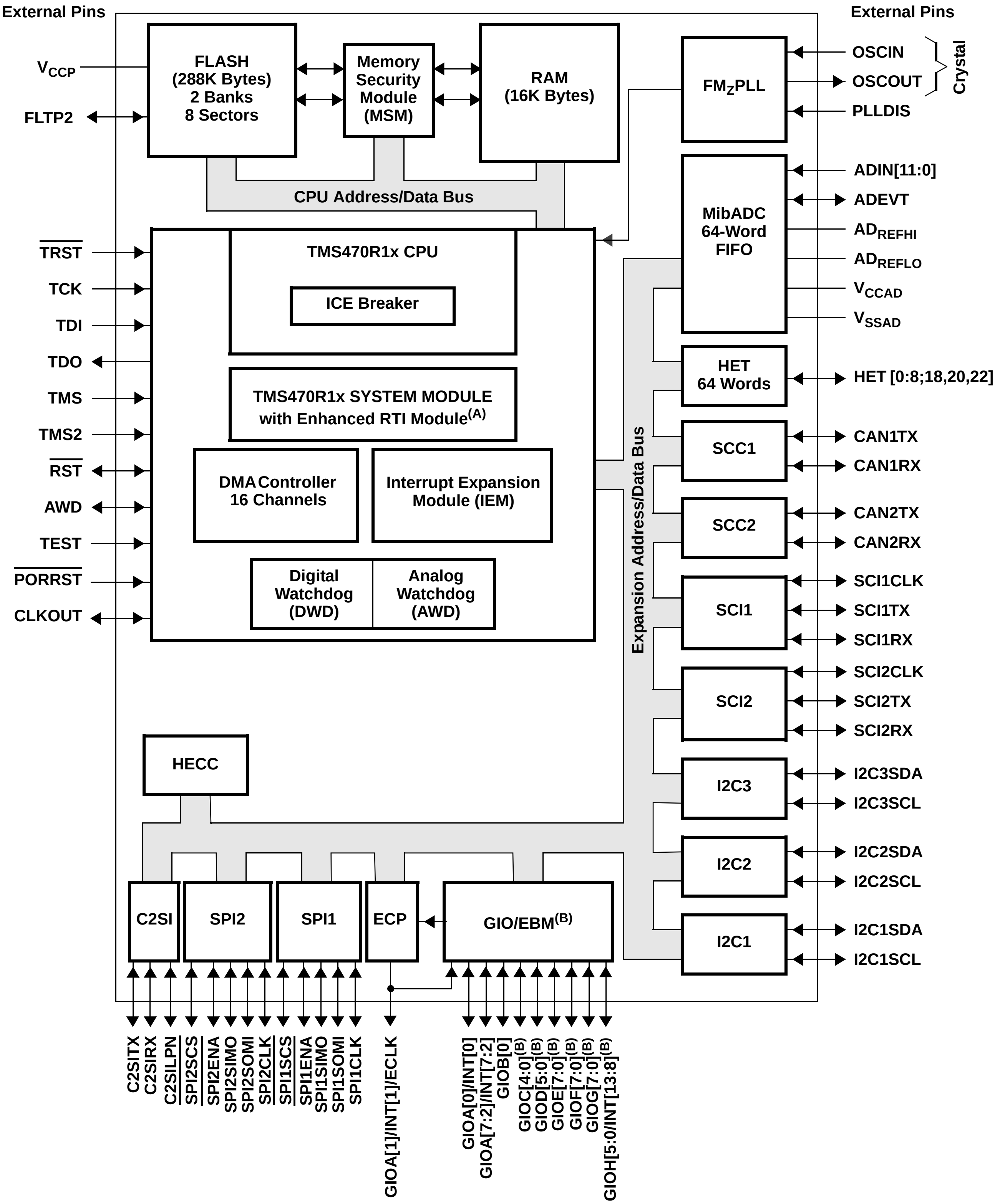
device characteristics

The VF288 device is a derivative of the F05 system emulation device SE470R1VB8AD. Table 1 identifies all the characteristics of the VF288 device except the SYSTEM and CPU, which are generic.

Table 1. Device Characteristics

CHARACTERISTICS	DEVICE DESCRIPTION TMS470R1VF288	COMMENTS FOR VF288
MEMORY		
For the number of memory selects on this device, see the TMS470VF288 Memory Selection Assignment table (Table 2).		
INTERNAL MEMORY	Pipeline/Non-Pipeline 288K-Byte Flash 16K-Byte SRAM Memory Security Module (MSM) JTAG Security Module	Flash is pipeline-capable The VF288 RAM is implemented in one 16K array selected by two memory-select signals (see the TMS470R1VF288 Memory Selection Assignment table, Table 2).
PERIPHERALS		
For the device-specific interrupt priority configurations, see the Interrupt Priority Table (Table 5). And for the 1K peripheral address ranges and their peripheral selects, see the VF288 Peripherals, System Module, and Flash Base Addresses table (Table 3).		
CLOCK	FM$_Z$PLL	Frequency-modulated zero-pin PLL has no external loop filter pins.
Expansion Bus	EBM	Expansion bus module with 42 pins. Supports 8- and 16-bit memories. See Table 6 for details.
GENERAL-PURPOSE I/Os	50 I/O (PGE Suffix) 14 I/O (PZ Suffix)	In the PGE package, Port A has eight (8) external pins, Port B has only one (1) external pin, Port C has five (5) external pins, Port D has six (6) external pins, Ports E, F, and G each have eight (8) external pins, and Port H has six (6) external pins. In the PZ package, Port A has eight (8) external pins, Port B has only one (1) external pin, and Port H has five (5) external pins.
ECP	YES	
SCI	2 (3-pin)	
CAN (HECC and/or SCC)	2 SCC	Two standard CAN controllers
SPI (5-pin, 4-pin or 3-pin)	2 (5-pin)	
C2SIb	1	
I2C	3	
HET with XOR Share	12 I/O	The high-resolution (HR) SHARE feature allows even-numbered HR pins to share the next higher odd-numbered HR pin structures. This HR sharing is independent of whether or not the odd pin is available externally. If an odd pin is available externally and *shared*, then the odd pin can only be used as a general-purpose I/O. For more information on HR SHARE, see the*TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).
HET RAM	64-Instruction Capacity	
MibADC	10-bit, 12-channel 64-word FIFO	Both the logic and registers for a full 16-channel MibADC are present.
CORE VOLTAGE	1.8 V	
I/O VOLTAGE	3.3 V	
PINS	144 100	
PACKAGES	PGE PZ	

functional block diagram



A. The Enhanced RTI module is the System Module with two extra bits to disable the FM_ZPLL while in STANDBY mode.

B. GIOC[4:0], GIOD[5:0], GIOE[5:0], GIOF[7:0], and GIOH[0], which are muxed with EBM, are not available on the PZ package. See Table 6 for EBM to GIO mapping.

Terminal Functions

TERMINAL			INPUT VOLTAGE(1)(2)	OUTPUT CURRENT(1)(2)	INTERNAL PULLUP/ PULLDOWN(3)	DESCRIPTION
NAME	**PZ**	**PGE**				
HIGH-END TIMER (HET)						
HET[0]	51	73	3.3-V	2mA -z		Timer input capture or output compare. The HET[8:0,18,20,22] applicable pins can be programmed as general-purpose input/ output (GIO) pins. All are high-resolution pins. The high-resolution (HR) SHARE feature allows even HR pins to share the next higher odd HR pin structures. This HR sharing is independent of whether or not the odd pin is available externally. If an odd pin is available externally and *shared*, then the odd pin can only be used as a general-purpose I/O. For more information on HR SHARE, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).
HET[1]	50	72				
HET[2]	49	71				
HET[3]	46	66				
HET[4]	45	65				
HET[5]	44	63				
HET[6]	6	9				
HET[7]	7	11				
HET[8]	8	12				
HET[18]	9	15				
HET[20]	12	18				
HET[22]	13	19				
STANDARD CAN CONTROLLER (SCC)						
CAN1SRX	58	83	5V tolerant	4mA		SCC1 receive pin or GIO pin
CAN1STX	59	84	3.3-V	2mA -z		SCC1 transmit pin or GIO pin
CAN2SRX	37	54	5V tolerant	4mA		SCC2 receive pin or GIO pin
CAN2STX	38	55	3.3-V	2mA -z		SCC 2 transmit pin or GIO pin
CLASS II SERIAL INTERFACE (C2SIB)						
C2SIbLPN	14	21	3.3-V	2mA -z		C2SIb module loopback enable pin or GIO pin
C2SIbRX	15	22	5V tolerant	4mA		C2SIb module receive data input pin or GIO pin
C2SIbTX	16	24	3.3-V	2mA -z		C2SIb module transmit data output pin or GIO pin
GENERAL-PURPOSE I/O (GIO)						
GIOA[0]/INT[0]	99	141	5V tolerant	4mA		General-purpose input/output pins. GIOA[7:0]/INT[7:0] are interrupt-capable pins. GIOA[1]/INT[1]/ECLK pin is multiplexed with the external clock-out function of the external clock prescale (ECP) module.
GIOA[1]/INT[1]/ ECLK	96	136				
GIOA[2]/INT[2]	95	134				
GIOA[3]/INT[3]	94	133				
GIOA[4]/INT[4]	89	127				
GIOA[5]/INT[5]	67	98				
GIOA[6]/INT[6]	55	78				
GIOA[7]/INT[7]	56	79				
GIOB[0]/ EBDMAREQ[0]	30	43	3.3-V	2mA -z	IPD (20 µA)	GIOB[0], GIOC[4:0], GIOD[5:0], GIOE[7:0:], GIOF[7:0], GIOG[7:0], AND GIOH[5:0] are multiplexed with the expansion bus module. See Table 6.
GIOC[0]/EBOE	–	135				
GIOC[1]/EBWR[0]	–	128				
GIOC[2]/EBWR[1]	–	126				
GIOC[3]/EBCS[5]	–	120				
GIOC[4]/EBCS[6]	–	119				

1 PWR = power, GND = ground, REF = reference voltage, NC = no connect
2 All I/O pins, except RST, are configured as inputs while PORRST is low and immediately after PORRST goes high.
3 IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the PORRST state.)

Terminal Functions (Continued)

TERMINAL			INPUT VOLTAGE[(1)(2)]	OUTPUT CURRENT[(1)(2)]	INTERNAL PULLUP/PULLDOWN[(3)]	DESCRIPTION
NAME	PZ	PGE				
GENERAL-PURPOSE I/O (GIO) (CONTINUED)						
GIOD[0]/EBADDR[0]	–	42	3.3-V	2mA -z	IPD (20 µA)	GIOB[0], GIOC[4:0], GIOD[5:0], GIOE[7:0:], GIOF[7:0], GIOG[7:0], AND GIOH[5:0] are multiplexed with the expansion bus module. See Table 6.
GIOD[1]/EBADDR[1]	–	39				
GIOD[2]/EBADDR[2]	–	35				
GIOD[3]/EBADDR[3]	–	30				
GIOD[4]/EBADDR[4]	–	27				
GIOD[5]/EBADDR[5]	–	23				
GIOE[0]/EBDATA[0]	–	44				
GIOE[1]/EBDATA[1]	–	47				
GIOE[2]/EBDATA[2]	–	58				
GIOE[3]/EBDATA[3]	–	61				
GIOE[4]/EBDATA[4]	–	64				
GIOE[5]/EBDATA[5]	–	67				
GIOE[6]/EBDATA[6]	–	70				
GIOE[7]/EBDATA[7]	–	77				
GIOF[0]/EBADDR[6]/EBDATA[8]	–	80				
GIOF[1]/EBADDR[7]/EBDATA[9]	–	82				
GIOF[2]/EBADDR[8]/EBDATA[10]	–	89				
GIOF[3]/EBADDR[9]/EBDATA[11]	–	90				
GIOF[4]/EBADDR[10]/EBDATA[12]	–	93				
GIOF[5]/EBADDR[11]/EBDATA[13]	–	96				
GIOF[6]/EBADDR[12]/EBDATA[14]	–	99				
GIOF[7]/EBADDR[13]/EBDATA[15]	–	100				
GIOG[0]/EBADDR[14]/EBADDR[6]	–	20				
GIOG[1]/EBADDR[15]/EBADDR[7]	–	10				
GIOG[2]/EBADDR[16]/EBADDR[8]	–	8				
GIOG[3]/EBADDR[17]/EBADDR[9]	–	6				
GIOG[4]/EBADDR[18]/EBADDR[10]	–	3				
GIOG[5]/EBADDR[19]/EBADDR[11]	–	143				
GIOG[6]/EBADDR[20]/EBADDR[12]	–	142				
GIOG[7]/EBADDR[21]/EBADDR[13]	–	140				

1 PWR = power, GND = ground, REF = reference voltage, NC = no connect
2 All I/O pins, except $\overline{\text{RST}}$, are configured as inputs while $\overline{\text{PORRST}}$ is low and immediately after $\overline{\text{PORRST}}$ goes high.
3 IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{\text{PORRST}}$ state.)

PRODUCT PREVIEW

Terminal Functions (Continued)

TERMINAL			INPUT VOLTAGE[1][2]	OUTPUT CURRENT[1][2]	INTERNAL PULLUP/ PULLDOWN[3]	DESCRIPTION
NAME	PZ	PGE				
GENERAL-PURPOSE I/O (GIO) (CONTINUED)						
GIOH[0]/EBADDR[22]/ EBADDR[14]/INT[8]	–	139	3.3-V	2mA	IPD	GIOB[0], GIOC[4:0], GIOD[5:0], GIOE[7:0:], GIOF[7:0], GIOG[7:0], AND GIOH[5:0] are multiplexed with the expansion bus module. GIOH[5:0]/INT[13:8] are interrupt-capable pins.
GIOH[1]/EBADDR[23]/ EBADDR[15]/INT[9]	29	41				
GIOH[2]/EBADDR[24]/ EBADDR[16]/INT[10]	28	40				
GIOH[3]/EBADDR[25]/ EBADDR[17]/INT[11]	27	38				
GIOH[4]/EBADDR[26]/ EBADDR[18]/INT[12]	26	37				
GIOH[5]/EBHOLD/INT[13]	88	125				
MULTI-BUFFERED ANALOG-TO-DIGITAL CONVERTER (MibADC)						
ADEVT	68	101	3.3-V	2mA -z		MibADC event input. Can be programmed as a GIO pin.
ADIN[0]	84	117	3.3-V			MibADC analog input pins
ADIN[1]	83	116				
ADIN[2]	82	115				
ADIN[3]	81	114				
ADIN[4]	80	113				
ADIN[5]	75	108				
ADIN[6]	74	107				
ADIN[7]	73	106				
ADIN[8]	72	105				
ADIN[9]	71	104				
ADIN[10]	70	103				
ADIN[11]	69	102				
AD_{REFHI}	76	109	3.3-V REF			MibADC module high-voltage reference input
AD_{REFLO}	77	110	GND REF			MibADC module low-voltage reference input
V_{CCAD}	78	111	3.3-V PWR			MibADC analog supply voltage
V_{SSAD}	79	112	GND			MibADC analog ground reference
SERIAL PERIPHERAL INTERFACE 1 (SPI1)						
SPI1CLK	3	4	5V tolerant	4mA		SPI1 clock. SPI1CLK can be programmed as a GIO pin.
SPI1ENA	2	2				SPI1 chip enable. Can be programmed as a GIO pin.
SPI1SCS	1	1				SPI1 slave chip select. Can be programmed as a GIO pin.
SPI1SIMO	4	5				SPI1 data stream. Slave in/master out. Can be programmed as a GIO pin.
SPI1SOMI	5	7				SPI1 data stream. Slave out/master in. Can be programmed as a GIO pin.
SERIAL PERIPHERAL INTERFACE 2 (SPI2)						
SPI2CLK	39	56	5V tolerant	4mA		SPI2 clock. Can be programmed as a GIO pin.
SPI2ENA	42	60				SPI2 chip enable. Can be programmed as a GIO pin.
SPI2SCS	43	62				SPI2 slave chip select. Can be programmed as a GIO pin.

1 PWR = power, GND = ground, REF = reference voltage, NC = no connect
2 All I/O pins, except RST, are configured as inputs while PORRST is low and immediately after PORRST goes high.
3 IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the PORRST state.)

Terminal Functions (Continued)

TERMINAL			INPUT VOLTAGE[1][2]	OUTPUT CURRENT[1][2]	INTERNAL PULLUP/ PULLDOWN[3]	DESCRIPTION
NAME	PZ	PGE				
SERIAL PERIPHERAL INTERFACE 2 (SPI2) (CONTINUED)						
SPI2SIMO	41	59	5V tolerant	4mA		SPI2 data stream. Slave in/master out. Can be programmed as a GIO pin.
SPI2SOMI	40	57				SPI2 data stream. Slave out/master in. Can be programmed as a GIO pin.
INTER-INTEGRATED CIRCUIT (I2C)						
I2C1SDA	60	87	5V tolerant	4mA		I2C1 serial data pin or GIO pin
I2C1SCL	61	88				I2C1 serial clock pin or GIO pin
I2C2SDA	64	94				I2C2 serial data pin or GIO pin
I2C2SCL	65	95				I2C2 serial clock pin or GIO pin
I2C3SDA	20	29				I2C3 serial data pin or GIO pin
I2C3SCL	19	28				I2C3 serial clock pin or GIO pin
FREQUENCY-MODULATED ZERO-PIN PHASE-LOCKED LOOP (FM$_Z$PLL)						
OSCIN	23	33	1.8-V			Crystal connection pin or external clock input
OSCOUT	22	32		2mA		External crystal connection pin
PLLDIS	66	97	3.3-V		IPD (20 µA)	Enable/disable the FM$_Z$PLL. The FM$_Z$PLL can be bypassed and the oscillator becomes the system clock.
SERIAL COMMUNICATIONS INTERFACE 1 (SCI1)						
SCI1CLK	33	48	3.3-V	2mA -z		SCI1 clock. SCI1CLK can be programmed as a GIO pin.
SCI1RX	32	46	5V tolerant	4mA		SCI1 data receive. SCI1RX can be programmed as a GIO pin.
SCI1TX	31	45	3.3-V	2mA -z		SCI1 data transmit. SCI1TX can be programmed as a GIO pin.
SERIAL COMMUNICATIONS INTERFACE 2 (SCI2)						
SCI2CLK	36	51	3.3-V	2mA -z		SCI2 clock. SCI2CLK can be programmed as a GIO pin.
SCI2RX	35	50	5V tolerant	4mA		SCI2 data receive. SCI2RX can be programmed as a GIO pin.
SCI2TX	34	49	3.3-V	2mA -z		SCI2 data transmit. SCI2TX can be programmed as a GIO pin.
SYSTEM MODULE (SYS)						
CLKOUT	57	81	3.3-V	8mA		Bidirectional pin. CLKOUT can be programmed as a GIO pin or the output of SYSCLK, ICLK, or MCLK.
$\overline{\text{PORRST}}$	85	118	3.3-V		IPD (20 µA)	Input master chip power-up reset. External V_{CC} monitor circuitry must assert a power-on reset.
$\overline{\text{RST}}$	86	121	3.3-V	4mA	IPU (20 µA)	Bidirectional reset. The internal circuitry can assert a reset, and an external system reset can assert a device reset. On this pin, the output buffer is implemented as an open drain (drives low only). To ensure an external reset is not arbitrarily generated, TI recommends that an external pullup resistor be connected to this pin.
WATCHDOG/REAL-TIME INTERRUPT (WD/RTI)						
AWD	25	36	3.3-V	8mA		Analog watchdog reset. The AWD pin provides a system reset if the WD KEY is not written in time by the system, providing an external RC network circuit is connected. If the user is not using AWD, TI recommends that this pin be connected to ground or pulled down to ground by an external resistor. For more details on the external RC network circuit, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189) and the application note *Analog Watchdog Resistor, Capacitor and Discharge Interval Selection Constraints* (literature number SPNA005).

1 PWR = power, GND = ground, REF = reference voltage, NC = no connect
2 All I/O pins, except $\overline{\text{RST}}$, are configured as inputs while $\overline{\text{PORRST}}$ is low and immediately after $\overline{\text{PORRST}}$ goes high.
3 IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{\text{PORRST}}$ state.)

Terminal Functions (Continued)

TERMINAL			INPUT VOLTAGE(1)(2)	OUTPUT CURRENT(1)(2)	INTERNAL PULLUP/ PULLDOWN(3)	DESCRIPTION
NAME	PZ	PGE				
TEST/DEBUG (T/D)						
TCK	54	76	3.3-V		IPD (20 μA)	Test clock. TCK controls the test hardware (JTAG).
TDI	52	74		8mA	IPU (20 μA)	Test data in. TDI inputs serial data to the test instruction register, test data register, and programmable test address (JTAG).
TDO	53	75		8mA	IPD (20 μA)	Test data out. TDO outputs serial data from the test instruction register, test data register, identification register, and programmable test address (JTAG).
TEST	87	124			IPD (20 μA)	Test enable. Reserved for internal use only. TI recommends that this pin be connected to ground or pulled down to ground by an external resistor.
TMS	11	17		8mA	IPU (20 μA)	Serial input for controlling the state of the CPU test access port (TAP) controller (JTAG).
TMS2	10	16		8mA	IPU (20 μA)	Serial input for controlling the second TAP. TI recommends that this pin be connected to V_{CCIO} or pulled up to V_{CCIO} by an external resistor.
$\overline{\text{TRST}}$	100	144			IPD (20 μA)	Test hardware reset to TAP1 and TAP2. IEEE Standard 1149-1 (JTAG) Boundary-Scan Logic. TI recommends that this pin be pulled down to ground by an external resistor.
FLASH						
FLTP2	93	132	NC	NC		Flash test pad 2. **For proper operation, this pin must not be connected [no connect (NC)].**
V_{CCP}	92	131	3.3-V PWR			Flash external pump voltage (3.3 V)
SUPPLY VOLTAGE CORE (1.8 V)						
V_{CC}	21	13	1.8-V PWR			Core logic supply voltage
	63	31				
	91	53				
	–	92				
	–	123				
	–	130				
SUPPLY VOLTAGE DIGITAL I/O (3.3 V)						
V_{CCIO}	17	25	3.3-V PWR			Digital I/O supply voltage
	48	69				
	–	86				
	97	137				
SUPPLY GROUND CORE						
V_{SS}	90	14	GND			Core supply ground reference
	–	34				
	–	52				
	–	91				
	62	122				
	24	129				
SUPPLY GROUND DIGITAL I/O						
V_{SSIO}	18	26	GND			Digital I/O supply ground reference
	47	68				
	–	85				
	98	138				

1 PWR = power, GND = ground, REF = reference voltage, NC = no connect

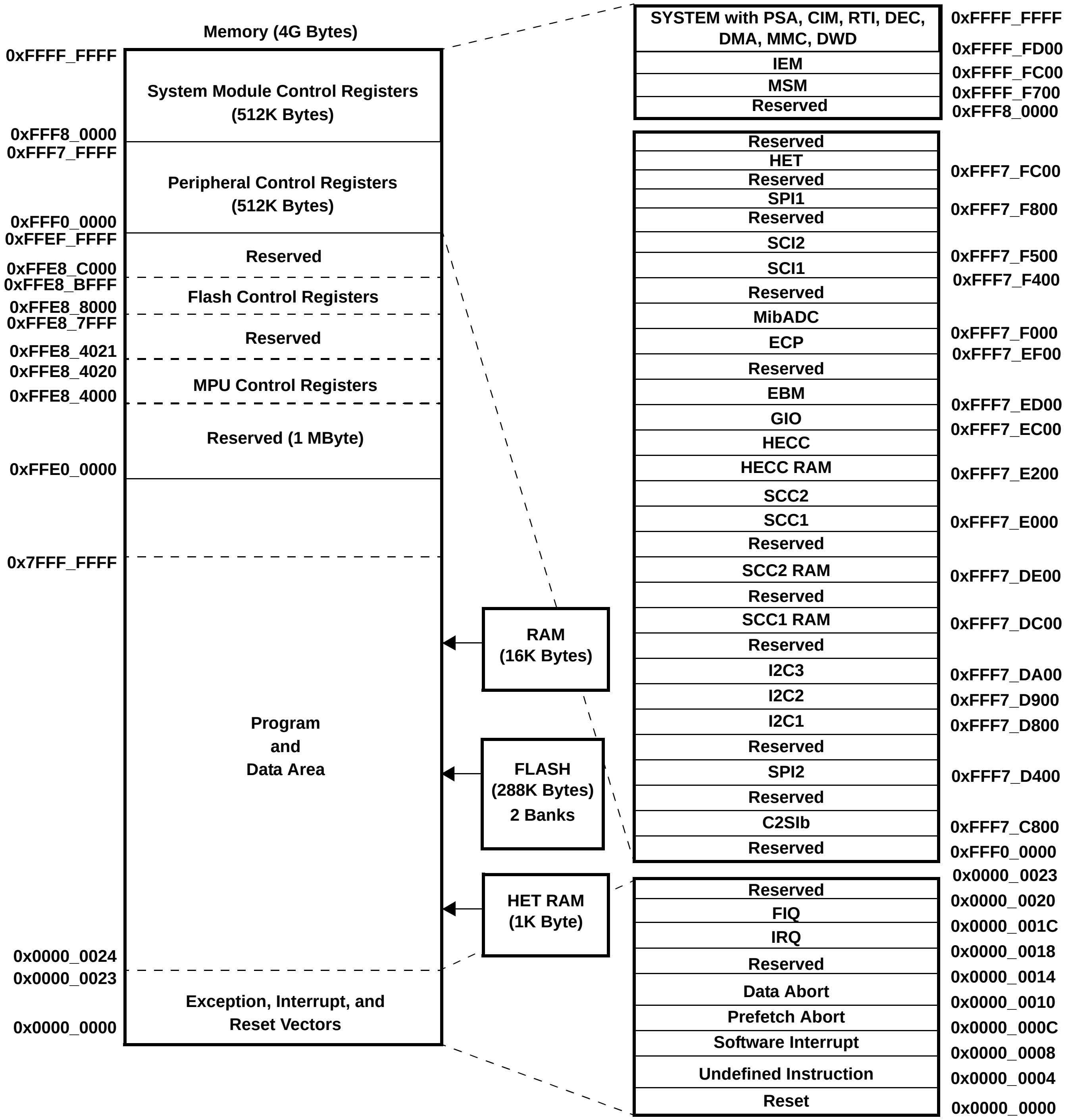
2 All I/O pins, except $\overline{\text{RST}}$, are configured as inputs while $\overline{\text{PORRST}}$ is low and immediately after $\overline{\text{PORRST}}$ goes high.

3 IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{\text{PORRST}}$ state.)

VF288 DEVICE-SPECIFIC INFORMATION

memory

Figure 1 shows the memory map of the VF288 device.



A. Memory addresses are configurable by the system (SYS) module within the range of 0x0000_0000 to 0xFFE0_0000.
B. The CPU registers are not a part of the memory map.

Figure 1. TMS470R1VF288 Memory Map

memory selects

Memory selects allow the user to address memory arrays (i.e., flash, RAM, and HET RAM) at user-defined addresses. Each memory select has its own set (low and high) of memory base address registers (MFBAHRx and MFBALRx) that, together, define the array's starting (base) address, size, and protection.

The base address of each memory select is configurable to any memory address boundary that is a multiple of the decoded block size. The decoded block size for the flash memory on this device is 0x00200000. For more information on how to control and configure these memory select registers, see the bus structure and memory sections of the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

For the memory selection assignments and the memory selected, see Table 2.

Table 2. TMS470R1VF288 Memory Selection Assignment

MEMORY SELECT	MEMORY SELECTED (ALL INTERNAL)	MEMORY SIZE(1)	MPU	MSM	MEMORY BASE ADDRESS REGISTER	STATIC MEM CTL REGISTER
0 (fine)	FLASH/ROM	288K	NO	YES	MFBAHR0 and MFBALR0	
1 (fine)	FLASH/ROM		NO	YES	MFBAHR1 and MFBALR1	
2 (fine)	RAM	16K(2)	YES	YES	MFBAHR2 and MFBALR2	
3 (fine)	RAM		YES	YES	MFBAHR3 and MFBALR3	
4 (fine)	HET RAM	1K	NO	NO	MFBAHR4 and MFBALR4	SMCR1
5 (coarse)	$\overline{\text{CS[5]}}$/GIOC[3]	128MB (x8) 1MB (x16)	NO	NO	MCBAHR2 and MCBALR2	SMCR5
6 (coarse)	$\overline{\text{CS[6]}}$/GIOC[4]	128MB (x8) 1MB (x16)	NO	NO	MCBAHR3 and MCBALR3	SMCR6

1 x8 refers to size of memory in 8-bits; x16 refers to size of memory in 16-bits.
2 The starting addresses for both RAM memory-select signals *cannot* be offset from each other by a multiple of the user-defined block size in the memory-base address register.

JTAG security module

The VF288 device includes a JTAG security module to provide maximum security to the memory contents. The visible unlock code can be chosen to be in the OTP sector or in the first bank of the user-programmable memory. For the VF288, the visible unlock code is in the OTP sector at address 0x0000_01F8.

memory security module

The VF288 device also includes a memory security module (MSM) to provide additional security and flexibility to the memory contents' protection. The password for unlocking the MSM is located in the four words just before the flash protection keys (see page 17).

RAM

The VF288 device contains 16K-bytes of internal static RAM configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. This VF288 RAM is implemented in one 16K array selected by two memory-select signals. This VF288 configuration imposes an additional constraint on the memory map for RAM; the starting addresses for both RAM memory selects *cannot* be offset from each other by the multiples of the size of the physical RAM (i.e., 16K for the VF288 device). The VF288 RAM is addressed through memory selects 2 and 3.

The RAM can be protected by the memory protection unit (MPU) portion of the SYS module, allowing the user finer blocks of memory protection than is allowed by the memory selects. The MPU is ideal for protecting an operating system while allowing access to the current task. For more detailed information on the MPU portion of the SYS module and memory protection, see the memory section of the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

F05 Flash

The F05 flash memory is a nonvolatile electrically erasable and programmable memory implemented with a 32-bit-wide data bus interface. The F05 flash has an external state machine for programming and erase functions. See the *flash read* and *flash program and erase* sections following.

flash protection keys

The VF288 device provides flash protection keys. These four 32-bit protection keys prevent program/erase/compaction operations from occurring until after the four protection keys have been matched by the CPU loading the correct user keys into the FMPKEY control register. The protection keys on the VF288 are located in the last 4 words of the first 8K sector. For more detailed information on the flash protection keys and the FMPKEY control register, see the Optional Quadruple Protection Keys and Programming the Protection Keys portions of the *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213).

flash read

The VF288 flash memory is configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. The Flash is addressed through memory selects 0 and 1.

NOTE

The flash external pump voltage (V_{CCP}) is required for all operations (program, erase, and read).

flash pipeline mode

When in pipeline mode, the flash operates with a system clock frequency of up to 48 MHz (versus a system clock frequency of 24 MHz in normal mode). Flash in pipeline mode is capable of accessing 64-bit words and provides two 32-bit pipelined words to the CPU. Also, in pipeline mode the Flash can be read with no wait states when memory addresses are contiguous (after the initial 1- or 2-wait-state reads).

NOTE

After a system reset, pipeline mode is disabled (ENPIPE bit [FMREGOPT.0] is a "0"). In other words, the VF288 device powers up and comes out of reset in non-pipeline mode. Furthermore, setting the Flash configuration mode bit (GBLCTRL.4) will override pipeline mode.

flash program and erase

The VF288 device Flash contains one 32K-byte memory array (or bank) and one 256K-byte bank, for a total of 288K-bytes of Flash, and consists of eight sectors. These eight sectors are sized as follows:

SECTOR NO.	SEGMENT	LOW ADDRESS	HIGH ADDRESS	MEMORY ARRAYS (OR BANKS)
OTP	2K Bytes	0x0000_0000	0x0000_07FF	BANK0 (32K Bytes)
0	8K Bytes	0x0000_0000	0x0000_1FFF	
1	8K Bytes	0x0000_2000	0x0000_3FFF	
2	8K Bytes	0x0000_4000	0x0000_5FFF	
3	8K Bytes	0x0000_6000	0x0000_7FFF	
0	64K Bytes	0x0004_0000	0x0004_FFFF	BANK1 (256K Bytes)
1	64K Bytes	0x0005_0000	0x0005_FFFF	
2	64K Bytes	0x0006_0000	0x0006_FFFF	
3	64K Bytes	0x0007_0000	0x0007_FFFF	

The minimum size for an erase operation is one sector. The maximum size for a program operation is one 16-bit word.

NOTE

The flash external pump voltage (V_{CCP}) is required for all operations (program, erase, and read).

Execution can occur from one bank while programming/erasing any or all sectors of another bank. However, execution can not occur from any sector within a bank that is being programmed or erased.

NOTE

When the OTP sector is enabled, the rest of the flash memory is disabled. The OTP memory can only be read or programmed from code executed out of RAM.

For more detailed information on Flash program and erase operations, see the *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213).

HET RAM

The VF288 device contains HET RAM. The HET RAM has a 64-instruction capability. The HET RAM is configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. The HET RAM is addressed through memory select 4.

peripheral selects and base addresses

The VF288 device uses ten of the sixteen peripheral selects to decode the base addresses of the peripherals. These peripheral selects are fixed and transparent to the user since they are part of the decoding scheme used by the SYS module.

Control registers for the peripherals, SYS module, and flash begin at the base addresses shown in Table 3.

Table 3. VF288 Peripherals, System Module, and Flash Base Addresses

CONNECTING MODULE	ADDRESS RANGE		PERIPHERAL SELECTS
	BASE ADDRESS	ENDING ADDRESS	
SYSTEM	0xFFFF_FFCC	0xFFFF_FFFF	N/A
RESERVED	0xFFFF_FF70	0xFFFF_FFCB	N/A
DWD	0xFFFF_FF60	0xFFFF_FF6F	N/A
PSA	0xFFFF_FF40	0xFFFF_FF5F	N/A
CIM	0xFFFF_FF20	0xFFFF_FF3F	N/A
RTI	0xFFFF_FF00	0xFFFF_FF1F	N/A
DMA	0xFFFF_FE80	0xFFFF_FEFF	N/A
DEC	0xFFFF_FE00	0xFFFF_FE7F	N/A
RESERVED	0xFFFF_FD80	0xFFFF_FDFF	N/A
MMC	0xFFFF_FD00	0xFFFF_FD7F	N/A
IEM	0xFFFF_FC00	0xFFFF_FCFF	N/A
RESERVED	0xFFFF_FB00	0xFFFF_FBFF	N/A
RESERVED	0xFFFF_FA00	0xFFFF_FAFF	N/A
DMA CMD BUFFER	0xFFFF_F800	0xFFFF_F9FF	N/A
MSM	0xFFFF_F700	0xFFFF_F7FF	N/A
RESERVED	0xFFF8_0000	0xFFFF_F6FF	N/A
RESERVED	0xFFF7_FD00	0xFFF7_FFFF	PS[0]
HET	0xFFF7_FC00	0xFFF7_FCFF	
RESERVED	0xFFF7_F900	0xFFF7_FBFF	PS[1]
SPI1	0xFFF7_F800	0xFFF7_F8FF	
RESERVED	0xFFF7_F600	0xFFF7_F7FF	PS[2]
SCI2	0XFFF7_F500	0XFFF7_F5FF	
SCI1	0xFFF7_F400	0xFFF7_F4FF	
RESERVED	0xFFF7_F100	0xFFF7_F3FF	PS[3]
MibADC	0xFFF7_F000	0xFFF7_F0FF	
ECP	0xFFF7_EF00	0xFFF7_EFFF	PS[4]
RESERVED	0xFFF7_EE00	0xFFF7_EEFF	
EBM	0xFFF7_ED00	0xFFF7_EDFF	
GIO	0xFFF7_EC00	0xFFF7_ECFF	

PRODUCT PREVIEW

Table 3. VF288 Peripherals, System Module, and Flash Base Addresses (Continued)

CONNECTING MODULE	ADDRESS RANGE		PERIPHERAL SELECTS
	BASE ADDRESS	ENDING ADDRESS	
HECC	0xFFF7_EA00	0xFFF7_EBFF	PS[5]
RESERVED	0xFFF7_E800	0xFFF7_E9FF	
HECC RAM	0xFFF7_E600	0xFFF7_E7FF	PS[6]
RESERVED	0xFFF7_E400	0xFFF7_E5FF	
RESERVED	0xFFF7_E300	0xFFF7_E3FF	PS[7]
SCC2	0xFFF7_E200	0xFFF7_E2FF	
RESERVED	0xFFF7_E100	0xFFF7_E1FF	
SCC1	0xFFF7_E000	0xFFF7_E0FF	
RESERVED	0xFFF7_DF00	0xFFF7_DFFF	PS[8]
SCC2 RAM	0xFFF7_DE00	0xFFF7_DEFF	
RESERVED	0xFFF7_DD00	0xFFF7_DDFF	
SCC1 RAM	0xFFF7_DC00	0xFFF7_DCFF	
RESERVED	0xFFF7_DB00	0xFFF7_DBFF	PS[9]
I2C3	0xFFF7_DA00	0xFFF7_DAFF	
I2C2	0xFFF7_D900	0xFFF7_D9FF	
I2C1	0xFFF7_D800	0xFFF7_D8FF	
RESERVED	0xFFF7_D500	0xFFF7_D7FF	PS[10]
SPI2	0xFFF7_D400	0xFFF7_D4FF	
RESERVED	0xFFF7_CC00	0xFFF7_D3FF	PS[11] - PS[12]
RESERVED	0xFFF7_C900	0xFFF7_CBFF	PS[13]
C2SIb	0xFFF7_C800	0xFFF7_C8FF	
RESERVED	0xFFF7_C000	0xFFF7_C7FF	PS[14] - PS[15]
RESERVED	0xFFF0_0000	0xFFF7_BFFF	N/A
Flash Control Registers	0xFFE8_8000	0xFFE8_BFFF	N/A
RESERVED	0xFFF8_4024	0xFFF8_7FFF	N/A
MPU CONTROL REGISTERS	0xFFE8_4000	0xFFE8_4023	N/A
RESERVED	0xFFF8_0000	0xFFF8_3FFF	N/A

PRODUCT PREVIEW

direct-memory access (DMA)

The direct-memory access (DMA) controller transfers data to and from any specified location in the VF288 memory map (except for restricted memory locations like the system control registers area). The DMA manages up to 16 channels, and supports data transfer for both on-chip and off-chip memories and peripherals. The DMA controller is connected to both the CPU and peripheral busses, enabling these data transfers to occur in parallel with CPU activity and thus maximizing overall system performance.

Although the DMA controller has two possible configurations, for the VF288 device, the DMA controller configuration is 32 control packets and 16 channels.

For the VF288 DMA request hardwired configuration, see Table 4.

Table 4. DMA Request Lines Connections(1)

MODULES	DMA REQUEST INTERRUPT SOURCES		DMA CHANNEL
EBM	Expansion Bus DMA request	EBDMAREQ0	DMAREQ[0]
SPI1	SPI1 end-receive	SPI1DMA0	DMAREQ[1]
SPI1	SPI1 end-transmit	SPI1DMA1	DMAREQ[2]
MibADC/I2C1	ADC EV/I2C1 read	MibADCDMA0/I2C1DMA0	DMAREQ[3]
MibADC/SCI1	ADC G1/SCI1 end-receive	MibADCDMA1/SCI1DMA0	DMAREQ[4]
MibADC/SCI1	ADC G2/SCI1 end-transmit	MibADCDMA2/SCI1DMA1	DMAREQ[5]
I2C1	I2C1 write	I2C1DMA1	DMAREQ[6]
SPI2	SPI2 end-receive	SPI2DMA0	DMAREQ[7]
SPI2	SPI2 end-transmit	SPI2DMA1	DMAREQ[8]
I2C2/C2SIb	I2C2 read end-receive/C2SIb end-receive	I2C2DMA0/C2SIDMA0	DMAREQ[9]
I2C2/C2SIb	I2C2 write end-transmit/C2SIb end-transmit	I2C2DMA1/C2SIDMA1	DMAREQ[10]
I2C3	I2C3 read	I2C3DMA0	DMAREQ[11]
I2C3	I2C3 write	I2C3DMA1	DMAREQ[12]
RESERVED			DMAREQ[13]
SCI2	SCI2 end-receive	SCI2DMA0	DMAREQ[14]
SCI2	SCI2 end-transmit	SCI2DMA1	DMAREQ[15]

1 For DMA channels with more than one assigned request source, *only one* of the sources listed can be the DMA request generator in a given application. The device has software control to ensure that there are no conflicts between requesting modules.

Each channel has two control packets attached to it, allowing the DMA to continuously load RAM and generate periodic interrupts so that the data can be read by the CPU. The control packets allow for the interrupt enable, and the channels determine the priority level of the interrupt.

DMA transfers occur in one of two modes:

- Non-request mode (used when transferring from memory to memory)
- Request mode (used when transferring from memory to peripheral)

For more detailed functional information on the DMA controller, see the *TMS470R1x Direct Memory Access (DMA) Controller Reference Guide* (literature number SPNU194).

PRODUCT PREVIEW

interrupt priority (IEM to CIM)

Interrupt requests originating from the VF288 peripheral modules (i.e., SPI1 or SPI2; SCI1 or SCI2; RTI; etc.) are assigned to channels within the 48-channel interrupt expansion module (IEM) where, via programmable register mapping, these channels are then mapped to the 32-channel central interrupt manager (CIM) portion of the SYS module.

Programming multiple interrupt sources in the IEM to the same CIM channel effectively shares the CIM channel between sources.

The CIM request channels are maskable so that individual channels can be selectively disabled. All interrupt requests can be programmed in the CIM to be of either type:

- Fast interrupt request (FIQ)
- Normal interrupt request (IRQ)

The CIM prioritizes interrupts. The precedences of request channels decrease with ascending channel order in the CIM (0 [highest] and 31 [lowest] priority). For IEM-to-CIM default mapping, channel priorities, and their associated modules, see Table 5.

Table 5. Interrupt Priority (IEM and CIM)

MODULES	INTERRUPT SOURCES	DEFAULT CIM INTERRUPT LEVEL/ CHANNEL	IEM CHANNEL
SPI1	SPI1 end-transfer/overrun	0	0
RTI	COMP2 interrupt	1	1
RTI	COMP1 interrupt	2	2
RTI	TAP interrupt	3	3
SPI2	SPI2 end-transfer/overrun	4	4
GIO	GIO interrupt A	5	5
RESERVED		6	6
HET	HET interrupt 1	7	7
I2C1	I2C1 interrupt	8	8
SCI1/SCI2	SCI1 or SCI2 error interrupt	9	9
SCI1	SCI1 receive interrupt	10	10
C2SIb	C2SIb interrupt	11	11
I2C2	I2C2 interrupt	12	12
SCC2	SCC2 interrupt A	13	13
SCC1	SCC1 interrupt A	14	14
RESERVED		15	15
MibADC	MibADC end event conversion	16	16
SCI2	SCI2 receive interrupt	17	17
DMA	DMA interrupt 0	18	18
I2C3	I2C3 interrupt	19	19
SCI1	SCI1 transmit interrupt	20	20
System	SW interrupt (SSI)	21	21
RESERVED		22	22
HET	HET interrupt 2	23	23
SCC2	SCC2 interrupt B	24	24
SCC1	SCC1 interrupt B	25	25

interrupt priority (IEM to CIM) (continued)

Table 5. Interrupt Priority (IEM and CIM) (Continued)

MODULES	INTERRUPT SOURCES	DEFAULT CIM INTERRUPT LEVEL/ CHANNEL	IEM CHANNEL
SCI2	SCI2 transmit interrupt	26	26
MibADC	MibADC end Group 1 conversion	27	27
DMA	DMA Interrupt 1	28	28
GIO	GIO interrupt B	29	29
MibADC	MibADC end Group 2 conversion	30	30
RESERVED		31	31
RESERVED		31	32-37
HECC	HECC interrupt A	31	38
HECC	HECC interrupt B	31	39
RESERVED		31	40-47

For more detailed functional information on the IEM, see the *TMS470R1x Interrupt Expansion Module (IEM) Reference Guide* (literature number SPNU211). For more detailed functional information on the CIM, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

expansion bus module (EBM)

The expansion bus module (EBM) is a standalone module used to bond out both general-purpose input/output pins and expansion bus interface pins. This module supports the multiplexing of the GIO functions and the expansion bus interface functions. The module also supports 8- and 16- bit expansion bus memory interface mappings, as well as mapping of the following expansion bus signals:

- 27-bit address bus (EBADDR[26:0]) for x8, 19-bit address bus (EBADDR[18:0]) for x16
- 8- or 16-bit data bus (EBDATA[7:0] or EBDATA[15:0])
- 2 write strobes ($\overline{\text{EBWR[1:0]}}$)
- 2 memory chip selects ($\overline{\text{EBCS[6:5]}}$)
- 1 output enable ($\overline{\text{EBOE}}$)
- 1 external hold signal for interfacing to slow memories ($\overline{\text{EBHOLD}}$)
- 1 DMA request line (EBDMAREQ[0])

Table 6 shows the multiplexing of I/O signals with the expansion bus interface signals. The mapping of these pins varies depending on the memory mode.

Table 6. Expansion Bus Mux Mapping[1]

GIO	EXPANSION BUS MODULE PINS[2]	
	X8	X16
GIOB[0]	EBDMAREQ[0]	EBDMAREQ[0]
GIOC[0]	$\overline{\text{EBOE}}$	$\overline{\text{EBOE}}$
GIOC[2:1]	$\overline{\text{EBWR[1:0]}}$	$\overline{\text{EBWR[1:0]}}$
GIOC[4:3]	$\overline{\text{EBCS[6:5]}}$	$\overline{\text{EBCS[6:5]}}$
GIOD[5:0]	EBADDR[5:0]	EBADDR[5:0]
GIOE[7:0]	EBDATA[7:0]	EBDATA[7:0]
GIOF[7:0]	EBADDR[13:6]	EBDATA[15:8]
GIOG[7:0]	EBADDR[21:14]	EBADDR[13:6]
GIOH[4:0]	EBADDR[26:22]	EBADDR[18:14]
GIOH[5]	$\overline{\text{EBHOLD}}$	$\overline{\text{EBHOLD}}$

[1] These mappings are controlled by the EBM mux control registers B-H (EBMXCRB - EBMXCRH) and the EBM control register 1 (EBMCR1). For GPIO functions, use GIODIRx, GIODINx, GIODOUTx, GIODSETx, and GIODCLRx. For more detailed information, see the *TMS470R1x General-Purpose Input/Output (GIO) Reference Guide* (literature number SPNU192) and the *TMS470R1x Expansion Bus Module (EBM) Reference Guide* (literature number SPNU222).

[2] X8 refers to size of memory in 8-bits; X16 refers to size of memory in 16-bits.

Table 7 lists the names of the expansion bus interface signals and their functions.

Table 7. Expansion Bus Pins

PIN	DESCRIPTION
EBDMAREQ	Expansion bus DMA request
$\overline{\text{EBOE}}$	Expansion bus pin enable
$\overline{\text{EBWR}}$	Expansion bus write strobe. $\overline{\text{EBWR[1]}}$ controls EBDATA[15:8] and $\overline{\text{EBWR[0]}}$ controls EBDATA[7:0]
$\overline{\text{EBCS}}$	Expansion bus chip select
EBADDR	Expansion bus address pin
EBDATA	Expansion bus data pin
$\overline{\text{EBHOLD}}$	Expansion bus hold. An external device may assert this signal to add wait states to an expansion bus transaction.

MibADC

The multi-buffered analog-to-digital converter (MibADC) accepts an analog signal and converts the signal to a 10-bit digital value.

The VF288 MibADC module can function in two modes: compatibility mode, where its programmer's model is compatible with the TMS470R1x ADC module and its digital results are stored in digital result registers; or in buffered mode, where the digital result registers are replaced with three FIFO buffers, one for each conversion group [event, group1 (G1), and group2 (G2)]. In buffered mode, the MibADC buffers can be serviced by interrupts or by the DMA.

MibADC event trigger enhancements

The MibADC includes two major enhancements over the event-triggering capability of the TMS470R1x ADC.

- Both group 1 and the event group can be configured for event-triggered operation, providing up to two event-triggered groups.
- The trigger source and polarity can be selected individually for both group 1 and the event group from the options identified in Table 8.

Table 8. MibADC Event Hookup Configuration

EVENT #	SOURCE SELECT BITS FOR G1 OR EVENT (G1SRC[1:0] or EVSRC[1:0])	SIGNAL PIN NAME
EVENT1	00	ADEVT
EVENT2	01	HET18
EVENT3	10	Reserved
EVENT4	11	Reserved

For group 1, these event-triggered selections are configured via the group 1 source select bits (G1SRC[1:0]) in the AD event source register (ADEVTSRC.[5:4]). For the event group, these event-triggered selections are configured via the event group source select bits (EVSRC[1:0]) in the AD event source register (ADEVTSRC.[1:0]).

For more detailed functional information on the MibADC, see the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

JTAG interface

There are two main test access ports (TAPs) on the VF748C device:

- TMS470R1x CPU TAP
- Device TAP for factory test

Some of the JTAG pins are shared among these two TAPs. The hookup is illustrated in Figure 2.

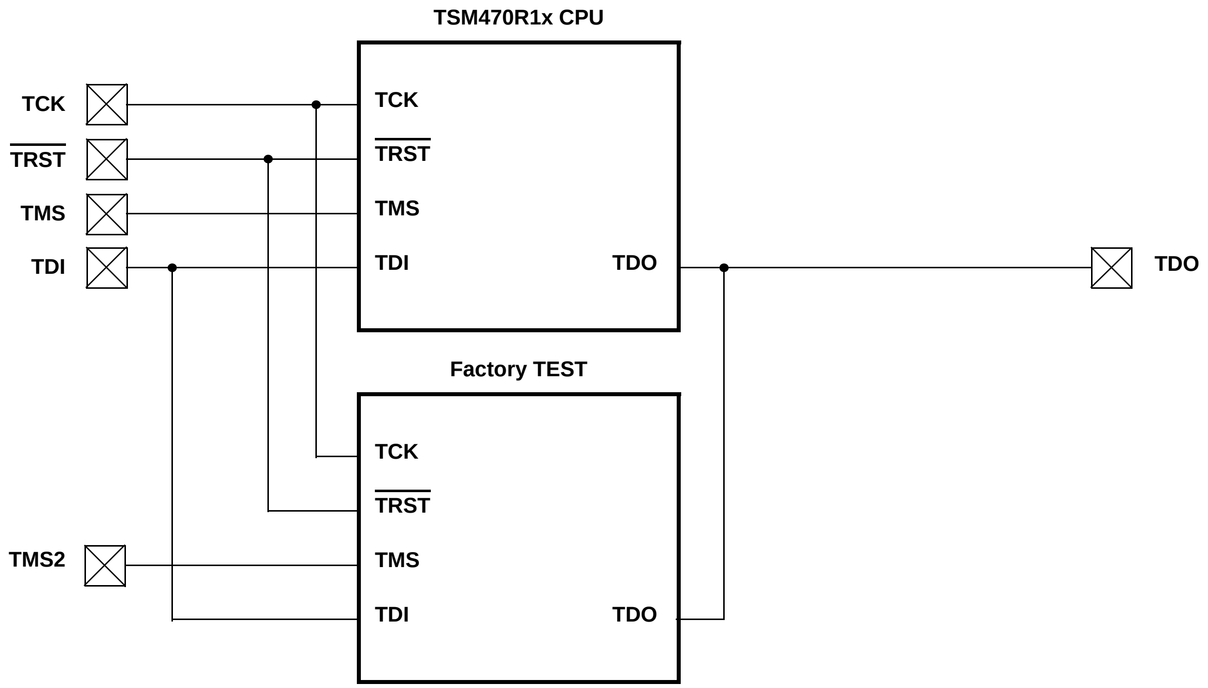


Figure 2. JTAG Interface

development system support

Texas Instruments provides extensive hardware and software development support tools for the TMS470R1x family. These support tools include:

- Code Composer Studio™ Integrated Development Environment (IDE)
  - Fully integrated suite of software development tools
  - Includes Compiler/Assembler/Linker, Debugger, and Simulator
  - Supports Real-Time analysis, data visualization, and open API
- Optimizing C compiler
  - Supports high-level language programming
  - Full implementation of the standard ANSI C language
  - Powerful optimizer that improves code-execution speed and reduces code size
  - Extensive run-time support library included
  - TMS470R1x control registers easily accessible from the C program
  - Interfaces C functions and assembly functions easily
  - Establishes comprehensive, easy-to-use tool set for the development of high-performance microcontroller applications in C/C++
- Assembly language tools (assembler and linker)
  - Provides extensive macro capability
  - Allows high-speed operation
  - Allows extensive control of the assembly process using assembler directives
  - Automatically resolves memory references as C and assembly modules are combined
- TMS470R1x CPU Simulator
  - Provides capability to simulate CPU operation without emulation hardware
  - Allows inspection and modifications of memory locations
  - Allows debugging programs in C or assembly language
- XDS emulation communication kits
  - Allows high-speed JTAG communication to the TMS470R1x emulator or target board

For more information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

Code Composer Studio is a trademark of Texas Instruments.

documentation support

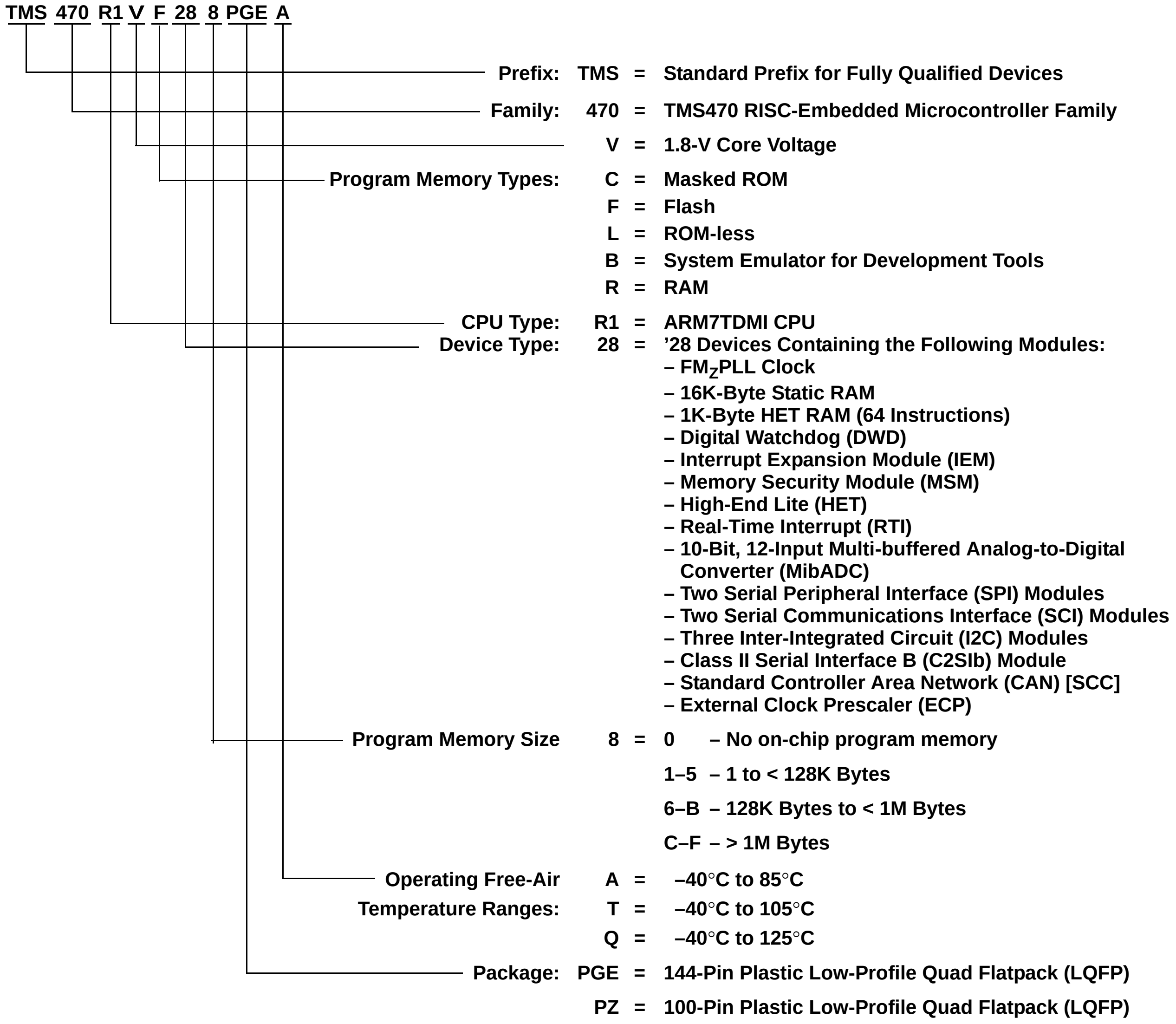
Extensive documentation supports all of the TMS470 microcontroller family generation of devices. The types of documentation available include: data sheets with design specifications; complete user's guides for all devices and development support tools; and hardware and software applications. Useful reference documentation includes:

- User's Guides
  - *TMS470R1x 32-Bit RISC Microcontroller Family User's Guide* (literature number SPNU134)
  - *TMS470R1x C/C++ Compiler User's Guide* (literature number SPNU151)
  - *TMS470R1x Code Generation Tools Getting Started Guide* (literature number SPNU117)
  - *TMS470R1x C Source Debugger User's Guide* (literature number SPNU124)
  - *TMS470R1x Assembly Language Tools User's Guide* (literature number SPNU118)
  - *TMS470R1x System Module Reference Guide* (literature number SPNU189)
  - *TMS470R1x Direct Memory Access (DMA) Controller Reference Guide* (literature number SPNU194)
  - *TMS470R1x Serial Peripheral Interface (SPI) Reference Guide* (literature number SPNU195)
  - *TMS470R1x Serial Communication Interface (SCI) Reference Guide* (literature number SPNU196)
  - *TMS470R1x Controller Area Network (CAN) Reference Guide* (literature number SPNU197)
  - *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199)
  - *TMS470R1x External Clock Prescale (ECP) Reference Guide* (literature number SPNU202)
  - *TMS470R1x Multi-Buffered Analog-to-Digital Converter* (MibADC) *Reference Guide* (literature number SPNU206)
  - *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213)
  - *TMS470R1x Class II Serial Interface B (C2SIb) Reference Guide* (literature number SPNU214)
  - *TMS470R1x Frequency-Modulated Phase-Locked Loop (FMPLL) Clock Module Reference Guide* (literature number SPNU221)
  - *TMS470R1x Expansion Bus Module (EBM) Reference Guide* (literature number SPNU222)
  - *TMS470R1x Inter-Integrated Circuit (I2C) Reference Guide* (literature number SPNU223)
- Application Reports:
  - *Analog Watchdog Resistor, Capacitor and Discharge Interval Selection Constraints* (literature number SPNA005)
  - *F05/C05 Power Up Reset and Power Sequencing Requirements* (literature number SPNA009)

PRODUCT PREVIEW

device numbering conventions

Figure 3 illustrates the numbering and symbol nomenclature for the TMS470R1x family.



Prefix: TMS = Standard Prefix for Fully Qualified Devices
Family: 470 = TMS470 RISC-Embedded Microcontroller Family
V = 1.8-V Core Voltage
Program Memory Types: C = Masked ROM
F = Flash
L = ROM-less
B = System Emulator for Development Tools
R = RAM
CPU Type: R1 = ARM7TDMI CPU
Device Type: 28 = ’28 Devices Containing the Following Modules:
- FM_ZPLL Clock
- 16K-Byte Static RAM
- 1K-Byte HET RAM (64 Instructions)
- Digital Watchdog (DWD)
- Interrupt Expansion Module (IEM)
- Memory Security Module (MSM)
- High-End Lite (HET)
- Real-Time Interrupt (RTI)
- 10-Bit, 12-Input Multi-buffered Analog-to-Digital Converter (MibADC)
- Two Serial Peripheral Interface (SPI) Modules
- Two Serial Communications Interface (SCI) Modules
- Three Inter-Integrated Circuit (I2C) Modules
- Class II Serial Interface B (C2SIb) Module
- Standard Controller Area Network (CAN) [SCC]
- External Clock Prescaler (ECP)

Program Memory Size 8 = 0 – No on-chip program memory
1–5 – 1 to < 128K Bytes
6–B – 128K Bytes to < 1M Bytes
C–F – > 1M Bytes
Operating Free-Air Temperature Ranges: A = –40°C to 85°C
T = –40°C to 105°C
Q = –40°C to 125°C
Package: PGE = 144-Pin Plastic Low-Profile Quad Flatpack (LQFP)
PZ = 100-Pin Plastic Low-Profile Quad Flatpack (LQFP)

Figure 3. TMS470R1x Family Nomenclature

device identification code register

The device identification code register identifies the silicon version, the technology family (TF), a ROM or flash device, and an assigned device-specific part number (see Table 9). The VF288 device identification code register value is 0x095F.

Table 9. TMS470 Device ID Bit Allocation Register

	BIT 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	BIT 16
FFFF_FFF0	Reserved															

BIT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT 0
VERSION				TF	R/F	PART NUMBER							1	1	1
R-K				R-K	R-K	R-K							R-1	R-1	R-1

LEGEND:

For bits 3–15: R = Read only, -K = Value constant after $\overline{\text{RESET}}$

For bits 0–2: R = Read only, -1 = Value after $\overline{\text{RESET}}$

Transmission Request Reset Register (CANTRR) Field Descriptions

Bit	Name	Value	Description
31–16	Reserved		Reads are undefined and writes have no effect.
15–12	VERSION		Silicon version (revision) bits These bits identify the silicon version of the device.
11	TF		Technology family bit This bit distinguishes the technology family core power supply:
		0	3.3 V for F10/C10 devices
		1	1.8 V for F05/C05 devices
10	R/F		ROM/Flash bit This bit distinguishes between ROM and Flash devices:
		0	Flash device
		1	ROM device
9–3	PART NUMBER		Device-specific part number bits These bits identify the assigned device-specific part number. The assigned device-specific part number for the VF288 device is 0101011.
2–0	1 Mandatory High		Bits 2, 1, and 0 are tied high by default.

device part numbers

Table 10 lists all the available TMS470R1VF288 devices.

Table 10. Device Part Number

DEVICE PART NUMBER	PROGRAM MEMORY		PACKAGE TYPE		TEMPERATURE RANGES		
	ROM	FLASH EEPROM	100-PIN LQFP	144-PIN LQFP	–40°C TO 85°C	–40°C TO 105°C	–40°C TO 125°C
TMS470R1VF288PGEA		X		X	X		
TMS470R1VF288PGEQ		X		X			X
TMS470R1VF288PZA		X	X		X		
TMS470R1VF288PZQ		X	X				X
TMS470R1VF288PGEAR		X		X	X		
TMS470R1VF288PGEQR		X		X			X
TMS470R1VF288PZAR		X	X		X		
TMS470R1VF288PZQR		X	X				X

DEVICE ELECTRICAL SPECIFICATIONS AND TIMING PARAMETERS

absolute maximum ratings over operating free-air temperature range[1]

Supply voltage ranges: V_{CC}[2]		–0.3 V to 2.5 V
Supply voltage ranges: V_{CCIO}, V_{CCAD}, V_{CCP} (flash pump)[2]		–0.3 V to 4.1 V
Input voltage range:	All 5 V tolerant input pins	–0.3 V to 6.0 V
	All other input pins	–0.3 V to 4.1 V
Input clamp current:	All 5 V tolerant pins, $\overline{\text{PORRST}}$, $\overline{\text{TRST}}$, TEST and TCK ($V_I < 0$)	–20mA[3]
	ADIN[0:11] I_{IK} ($V_I < 0$ or $V_I > V_{CCAD}$)	±10 mA
	All other pins I_{IK} ($V_I < 0$ or $V_I > V_{CCIO}$)	±20 mA
Operating free-air temperature ranges, T_A:	A version	–40°C to 85°C
	Q version	–40°C to 125°C
Operating junction temperature range, T_J		–40°C to 150°C
Storage temperature range, T_{stg}		–40°C to 150°C

[1] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] All voltage values are with respect to their associated grounds.

[3] These pins do not have an internal clamp diode to a positive supply voltage.

device recommended operating conditions[4]

			MIN	NOM	MAX	UNIT
V_{CC}	Digital logic supply voltage (Core)		1.71		2.05	V
V_{CCIO}	Digital logic supply voltage (I/O)		3		3.6	V
V_{CCAD}	ADC supply voltage		3		3.6	V
V_{CCP}	Flash pump supply voltage		3		3.6	V
V_{SS}	Digital logic supply ground			0		V
V_{SSAD}	ADC supply ground		– 0.1		0.1	V
T_A	Operating free-air temperature	A version	– 40		85	°C
		Q version	– 40		125	°C
T_J	Operating junction temperature		– 40		150	°C

[4] All voltages are with respect to V_{SS}, except V_{CCAD}, which is with respect to V_{SSAD}.

electrical characteristics over recommended operating free-air temperature range[1]

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{hys}	Input hysteresis			0.15			V
V_{IL}	Low-level input voltage	All inputs[2]		-0.3		0.8	V
V_{IH}	High-level input voltage	All inputs		2		$V_{CCIO} + 0.3$	V
V_{th}	Input threshold voltage	AWD only[3]		1.35		1.8	V
V_{OL}	Low-level output voltage[4]		$I_{OL} = I_{OL}$ MAX			$0.2\ V_{CCIO}$	V
			$I_{OL} = 50\ \mu A$			0.2	
V_{OH}	High-level output voltage[4]		$I_{OH} = I_{OH}$ MIN	$0.8\ V_{CCIO}$			V
			$I_{OH} = 50\ \mu A$	$V_{CCIO} - 0.2$			
I_{IC}	Input clamp current (I/O pins)[5]		$V_I < V_{SSIO} - 0.3$ or $V_I > V_{CCIO} + 0.3$	−2		2	mA
I_I	Input current (3.3 V input pins)	I_{IL} Pulldown	$V_I = V_{SS}$	−1		1	µA
		I_{IH} Pulldown	$V_I = V_{CCIO}$	5		40	
		I_{IL} Pullup	$V_I = V_{SS}$	−40		−5	
		I_{IH} Pullup	$V_I = V_{CCIO}$	−1		1	
		All other pins	No pullup or pulldown	−1		1	
	Input current (5 V tolerant input pins)		$V_I = V_{SS}$	−1		1	µA
			$V_I = V_{CCIO}$	−1		1	
			$V_I = 5$ V	0.5		20	
			$V_I = 5.5$ V	1		40	
I_{OL}	Low-level output current	CLKOUT, AWD, TDI, TDO, TMS, TMS2	$V_{OL} = V_{OL}$ MAX			8	mA
		$\overline{RST}$				4	
		All other 3.3 V I/O[6]				2	
		5 V tolerant				4	
I_{OH}	High-level output current	CLKOUT, TDI, TDO, TMS, TMS2	$V_{OH} = V_{OH}$ MIN	−8			mA
		$\overline{RST}$		−4			
		All other 3.3 V I/O[6]		−2			
		5 V tolerant		−4			

1 Source currents (out of the device) are negative while sink currents (into the device) are positive.

2 This does not apply to the $\overline{PORRST}$ pin. For $\overline{PORRST}$ exceptions, see the $\overline{RST}$ and $\overline{PORRST}$ timings section on page 40.

3 These values help to determine the external RC network circuit. For more details, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

4 V_{OL} and V_{OH} are linear with respect to the amount of load current (I_{OL}/I_{OH}) applied.

5 Parameter does not apply to input-only or output-only pins.

6 Some of the 2 mA buffers on this device are zero-dominant buffers, as indicated by a -z in the Output Current column of the Terminal Functions table. If two of these buffers are shorted together and one is outputting a low level and the other is outputting a high level, the resulting value will always be low.

7 For Flash banks/pumps in sleep mode.

8 I_{CC} in halt mode is linear between 30C and 85C.

9 I/O pins configured as inputs or outputs with no load. All pulldown inputs ≤ 0.2 V. All pullup inputs ≥ $V_{CCIO} - 0.2$ V.

PRODUCT PREVIEW

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range(1) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	V_{CC} digital supply current (operating mode)	SYSCLK = 24 MHz, V_{CC} = 2.05 V			90	mA
		SYSCLK = 48 MHz, V_{CC} = 2.05 V			115	mA
	V_{CC} digital supply current (standby mode)(7)	A version (85°C) OSCIN = 4 MHz, V_{CC} = 2.05 V			750	µA
		Q version (125°C) OSCIN = 4 MHz, V_{CC} = 2.05 V			1.25	mA
	V_{CC} digital supply current (halt mode)(7)(8)	T_A = 30°C, V_{CC} = 2.05 V			30	µA
		A version (85°C), V_{CC} = 2.05 V			160	µA
		Q version (125°C), V_{CC} = 2.05 V			550	µA
I_{CCIO}	V_{CCIO} digital supply current (operating mode)	No DC load, V_{CCIO} = 3.6 V(9)			15	mA
	V_{CCIO} digital supply current (standby mode)	No DC load, V_{CCIO} = 3.6 V(9)			10	µA
	V_{CCIO} digital supply current (halt mode)	No DC load, V_{CCIO} = 3.6 V(9)			5	µA
I_{CCAD}	V_{CCAD} supply current (operating mode)	All frequencies, V_{CCAD} = 3.6 V			25	mA
	V_{CCAD} supply current (standby mode)	No DC load, V_{CCAD} = 3.6 V(9)			10	µA
	V_{CCAD} supply current (halt mode)	V_{CCAD} = 3.6 V			5	µA
I_{CCP}	V_{CCP} pump supply current	V_{CCP} = 3.6 V read operation			60	mA
		V_{CCP} = 3.6 V program and erase			70	mA
		V_{CCP} = 3.6 V standby mode operation(7)			10	µA
		V_{CCP} = 3.6 V halt mode operation(7)			5	µA
C_I	Input capacitance			2		pF
C_O	Output capacitance			3		pF

1 Source currents (out of the device) are negative while sink currents (into the device) are positive.

2 This does not apply to the $\overline{\text{PORRST}}$ pin. For $\overline{\text{PORRST}}$ exceptions, see the $\overline{\text{RST}}$ and $\overline{\text{PORRST}}$ timings section on page 40.

3 These values help to determine the external RC network circuit. For more details, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

4 V_{OL} and V_{OH} are linear with respect to the amount of load current (I_{OL}/I_{OH}) applied.

5 Parameter does not apply to input-only or output-only pins.

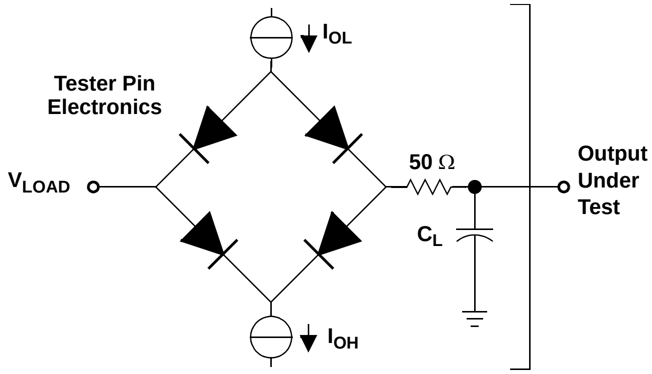
6 Some of the 2 mA buffers on this device are zero-dominant buffers, as indicated by a -z in the Output Current column of the Terminal Functions table. If two of these buffers are shorted together and one is outputting a low level and the other is outputting a high level, the resulting value will always be low.

7 For Flash banks/pumps in sleep mode.

8 I_{CC} in halt mode is linear between 30°C and 85°C.

9I/O pins configured as inputs or outputs with no load. All pulldown inputs ≤ 0.2 V. All pullup inputs ≥ V_{CCIO} – 0.2 V.

PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = I_{OL} MAX for the respective pin(A)
I_{OH} = I_{OH} MIN for the respective pin(A)
V_{LOAD} = 1.5 V
C_L = 150-pF typical load-circuit capacitance(B)

NOTES: A. For these values, see the "electrical characteristics over recommended operating free-air temperature range" table.
B. All timing parameters measured using an external load capacitance of 150 pF unless otherwise noted.

Figure 4. Test Load Circuit

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

CM	Compaction, CMPCT	RD	Read
CO	CLKOUT	RST	Reset, $\overline{\text{RST}}$
ER	Erase	RX	SCInRX
ICLK	Interface clock	S	Slave mode
M	Master mode	SCC	SCInCLK
OSC, OSCI	OSCIN	SIMO	SPInSIMO
OSCO	OSCOUT	SOMI	SPInSOMI
P	Program, PROG	SPC	SPInCLK
R	Ready	SYS	System clock
R0	Read margin 0, RDMRGN0	TX	SCInTX
R1	Read margin 1, RDMRGN1		

Lowercase subscripts and their meanings are:

a	access time	r	rise time
c	cycle time (period)	su	setup time
d	delay time	t	transition time
f	fall time	v	valid time
h	hold time	w	pulse duration (width)

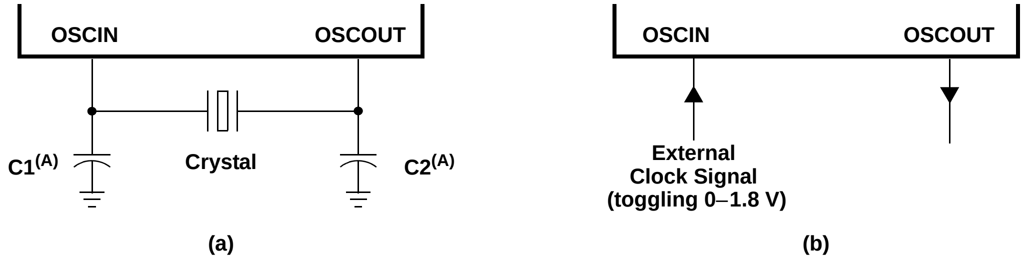
The following additional letters are used with these meanings:

H	High	X	Unknown, changing, or don’t care level
L	Low	Z	High impedance
V	Valid		

external reference resonator/crystal oscillator clock option

The oscillator is enabled by connecting the appropriate fundamental 4–10 MHz resonator/crystal and load capacitors across the external OSCIN and OSCOUT pins as shown in Figure 5a. The oscillator is a single-stage inverter held in bias by an integrated bias resistor. This resistor is disabled during leakage test measurement and HALT mode. **TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation.** The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

An external oscillator source can be used by connecting a 1.8 V clock signal to the OSCIN pin and leaving the OSCOUT pin unconnected (open) as shown in Figure 5b.



A. The values of C1 and C2 should be provided by the resonator/crystal vendor.

Figure 5. Crystal/Clock Connection

FM$_Z$PLL and clock specifications

timing requirements for FM$_Z$PLL circuits enabled or disabled

		MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Input clock frequency	4		10	MHz
$t_{c(OSC)}$	Cycle time, OSCIN	100			ns
$t_{w(OSCIL)}$	Pulse duration, OSCIN low	15			ns
$t_{w(OSCIH)}$	Pulse duration, OSCIN high	15			ns
$f_{(OSCRST)}$	OSC FAIL frequency(1)		53		kHz

1 Causes a device reset (specifically a clock reset) by setting the RST OSC FAIL (GLBCTRL.15) and the OSC FAIL flag (GLBSTAT.1) bits equal to 1. For more detailed information on these bits and device resets, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

switching characteristics over recommended operating conditions for clocks(1)(2)(3)

PARAMETER		TEST CONDITIONS(3)	MIN	MAX	UNIT
$f_{(SYS)}$	System clock frequency(4)	Pipeline mode enabled		48	MHz
		Pipeline mode disabled		24	MHz
$f_{(CONFIG)}$	System clock frequency - Flash config mode			24	MHz
$f_{(ICLK)}$	Interface clock frequency	Pipeline mode enabled		25	MHz
		Pipeline mode disabled		24	MHz
$f_{(ECLK)}$	External clock output frequency for ECP module	Pipeline mode enabled		25	MHz
		Pipeline mode disabled		24	MHz
$t_{c(SYS)}$	Cycle time, system clock	Pipeline mode enabled	20.8		ns
		Pipeline mode disabled	41.6		ns
$t_{c(CONFIG)}$	Cycle time, system clock - flash config mode		41.6		ns
$t_{c(ICLK)}$	Cycle time, interface clock	Pipeline mode enabled	40		ns
		Pipeline mode disabled	41.6		ns
$t_{c(ECLK)}$	Cycle time, ECP module external clock output	Pipeline mode enabled	40		ns
		Pipeline mode disabled	41.6		ns

1 $f_{(SYS)} = M \times f_{(OSC)} / R$, where M = {8}, R = {1,2,3,4,5,6,7,8} when PLLDIS = 0. R is the system-clock divider determined by the CLKDIVPRE [2:0] bits in the global control register (GLBCTRL.[2:0]) and M is the PLL multiplier determined by the MULT4 bit also in the GLBCTRL register (GLBCTRL.3).
$f_{(SYS)} = f_{(OSC)} / R$, where R = {1,2,3,4,5,6,7,8} when PLLDIS = 1.
$f_{(ICLK)} = f_{(SYS)} / X$, where X = {1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16}. X is the interface clock divider ratio determined by the PCR0.[4:1] bits in the SYS module.

2 $f_{(ECLK)} = f_{(ICLK)} / N$, where N = {1 to 256}. N is the ECP prescale value defined by the ECPCTRL.[7:0] register bits in the ECP module.

3 Pipeline mode enabled or disabled is determined by the ENPIPE bit (FMREGOPT.0).

4 Flash Vread must be set to 5V to achieve maximum system clock frequency.

FM_ZPLL and clock specifications (continued)

switching characteristics over recommended operating conditions for external clocks (see Figure 6 and Figure 7)(1)(2)(3)

NO.	PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
1	$t_{w(COL)}$	Pulse duration, CLKOUT low	SYSCLK or MCLK(4)	$0.5t_{c(SYS)} - t_f$		ns
			ICLK: X is even or 1(5)	$0.5t_{c(ICLK)} - t_f$		
			ICLK: X is odd and not 1(5)	$0.5t_{c(ICLK)} + 0.5t_{c(SYS)} - t_f$		
2	$t_{w(COH)}$	Pulse duration, CLKOUT high	SYSCLK or MCLK(4)	$0.5t_{c(SYS)} - t_r$		ns
			ICLK: X is even or 1(5)	$0.5t_{c(ICLK)} - t_r$		
			ICLK: X is odd and not 1(5)	$0.5t_{c(ICLK)} - 0.5t_{c(SYS)} - t_r$		
3	$t_{w(EOL)}$	Pulse duration, ECLK low	N is even and X is even or odd	$0.5t_{c(ECLK)} - t_f$		ns
			N is odd and X is even	$0.5t_{c(ECLK)} - t_f$		
			N is odd and X is odd and not 1	$0.5t_{c(ECLK)} + 0.5t_{c(SYS)} - t_f$		
4	$t_{w(EOH)}$	Pulse duration, ECLK high	N is even and X is even or odd	$0.5t_{c(ECLK)} - t_r$		ns
			N is odd and X is even	$0.5t_{c(ECLK)} - t_r$		
			N is odd and X is odd and not 1	$0.5t_{c(ECLK)} - 0.5t_{c(SYS)} - t_r$		

1 X = {1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16}. X is the interface clock divider ratio determined by the PCR0.[4:1] bits in the SYS module.
2 N = {1 to 256}. N is the ECP prescale value defined by the ECPCTRL.[7:0] register bits in the ECP module.
3 CLKOUT/ECLK pulse durations (low/high) are a function of the OSCIN pulse durations when PLLDIS is active.
4 Clock source bits are selected as either SYSCLK (CLKCNTL.[6:5] = 11 binary) or MCLK (CLKCNTL.[6:5] = 10 binary).
5 Clock source bits are selected as ICLK (CLKCNTL.[6:5] = 01 binary).

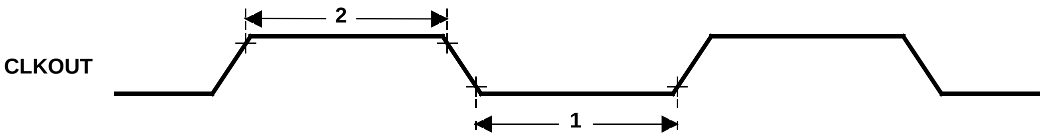


Figure 6. CLKOUT Timing Diagram

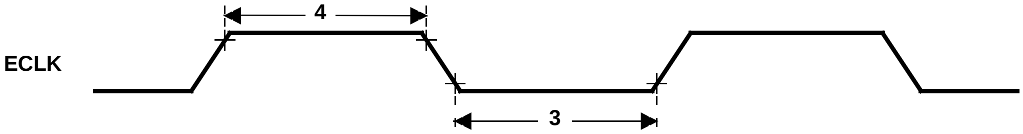


Figure 7. ECLK Timing Diagram

$\overline{\text{RST}}$ and $\overline{\text{PORRST}}$ timings

timing requirements for $\overline{\text{PORRST}}$ (see Figure 8)

NO.			MIN	MAX	UNIT
	V_{CCPORL}	V_{CC} low supply level when $\overline{\text{PORRST}}$ must be active during power up		0.6	V
	V_{CCPORH}	V_{CC} high supply level when $\overline{\text{PORRST}}$ must remain active during power up and become active during power down	1.5		V
	$V_{CCIOPORL}$	V_{CCIO} low supply level when $\overline{\text{PORRST}}$ must be active during power up		1.1	V
	$V_{CCIOPORH}$	V_{CCIO} high supply level when $\overline{\text{PORRST}}$ must remain active during power up and become active during power down	2.75		V
	V_{IL}	Low-level input voltage after $V_{CCIO} > V_{CCIOPORH}$		0.2 V_{CCIO}	V
	$V_{IL(PORRST)}$	Low-level input voltage of $\overline{\text{PORRST}}$ before $V_{CCIO} > V_{CCIOPORL}$		0.5	V
3	$t_{su(PORRST)r}$	Setup time, $\overline{\text{PORRST}}$ active before $V_{CCIO} > V_{CCIOPORL}$ during power up	0		ms
5	$t_{su(VCCIO)r}$	Setup time, $V_{CCIO} > V_{CCIOPORL}$ before $V_{CC} > V_{CCPORL}$	0		ms
6	$t_{h(PORRST)r}$	Hold time, $\overline{\text{PORRST}}$ active after $V_{CC} > V_{CCPORH}$	1		ms
7	$t_{su(PORRST)f}$	Setup time, $\overline{\text{PORRST}}$ active before $V_{CC} \leq V_{CCPORH}$ during power down	8		µs
8	$t_{h(PORRST)rio}$	Hold time, $\overline{\text{PORRST}}$ active after $V_{CCIO} > V_{CCIOPORH}$	1		ms
9	$t_{h(PORRST)d}$	Hold time, $\overline{\text{PORRST}}$ active after $V_{CC} < V_{CCPORL}$	0		ms
10	$t_{su(PORRST)fio}$	Setup time, $\overline{\text{PORRST}}$ active before $V_{CCIO} \leq V_{CCIOPORH}$ during power down	0		ns
11	$t_{su(VCCIO)f}$	Setup time, $V_{CC} < V_{CCPORL}$ before $V_{CCIO} < V_{CCIOPORL}$	0		ns

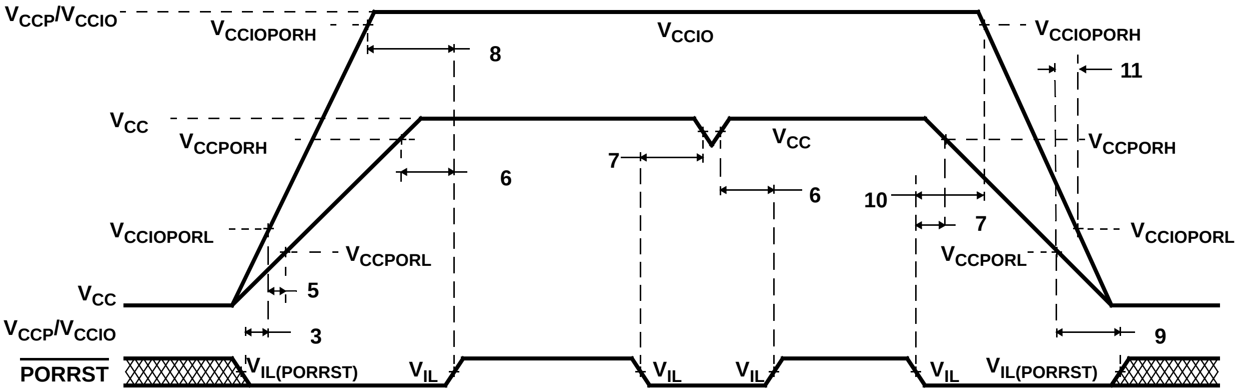


Figure 8. $\overline{\text{PORRST}}$ Timing Diagram

switching characteristics over recommended operating conditions for $\overline{\text{RST}}$[1]

PARAMETER		MIN	MAX	UNIT
$t_{v(RST)}$	Valid time, $\overline{\text{RST}}$ active after $\overline{\text{PORRST}}$ inactive	$4112t_{c(OSC)}$		ns
	Valid time, $\overline{\text{RST}}$ active (all others)	$8t_{c(SYS)}$		
t_{fsu}	Flash start up time, from $\overline{\text{RST}}$ inactive to fetch of first instruction from Flash (Flash pump stabilization time)	$670t_{c(OSC)}$		ns

1 Specified values do NOT include rise/fall times. For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.

JTAG scan interface timing (JTAG clock specification 10-MHz and 50-pF load on TDO output)

NO.			MIN	MAX	UNIT
1	$t_{c(JTAG)}$	Cycle time, JTAG low and high period	50		ns
2	$t_{su(TDI/TMS - TCKr)}$	Setup time, TDI, TMS before TCK rise (TCKr)	15		ns
3	$t_{h(TCKr -TDI/TMS)}$	Hold time, TDI, TMS after TCKr	15		ns
4	$t_{h(TCKf -TDO)}$	Hold time, TDO after TCKf	10		ns
5	$t_{d(TCKf -TDO)}$	Delay time, TDO valid after TCK fall (TCKf)		45	ns

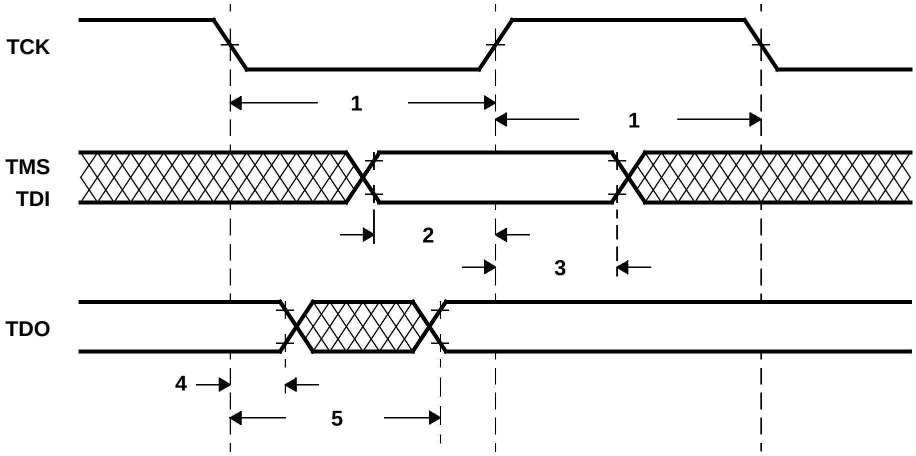


Figure 9. JTAG Scan Timings

output timings

switching characteristics for output timings versus load capacitance (C_L) (see Figure 10)

PARAMETER			MIN	MAX	UNIT
t_r	Rise time, AWD, CLKOUT, TDI, TDO, TMS, TMS2	C_L = 15 pF	0.5	2.5	ns
		C_L= 50 pF	1.5	5.0	
		C_L = 100 pF	3.0	9.0	
		C_L = 150 pF	4.5	12.5	
t_f	Fall time, AWD, CLKOUT, TDI, TDO, TMS, TMS2	C_L = 15 pF	0.5	2.5	ns
		C_L= 50 pF	1.5	5.0	
		C_L = 100 pF	3.0	9.0	
		C_L = 150 pF	4.5	12.5	
t_r	Rise time, $\overline{\text{RST}}$	C_L = 15 pF	2.5	8	ns
		C_L = 50 pF	5	14	
		C_L = 100 pF	9	23	
		C_L = 150 pF	13	32	
t_f	Fall time, $\overline{\text{RST}}$	C_L = 15 pF	2.5	8	ns
		C_L = 50 pF	5	14	
		C_L = 100 pF	9	23	
		C_L = 150 pF	13	32	
t_r	Rise time,4mA, 5 V tolerant pins	C_L = 15 pF	3	10	ns
		C_L = 50 pF	3.5	12	
		C_L = 100 pF	7	21	
		C_L = 150 pF	9	28	
t_f	Fall time, 4mA, 5 V tolerant pins	C_L = 15 pF	2	8	ns
		C_L = 50 pF	2.5	9	
		C_L = 100 pF	8	25	
		C_L = 150 pF	11	35	
t_r	Rise time, all other output pins	C_L = 15 pF	2.5	10	ns
		C_L = 50 pF	6.0	25	
		C_L = 100 pF	12	45	
		C_L = 150 pF	18	65	
t_f	Fall time, all other output pins	C_L = 15 pF	3	10	ns
		C_L = 50 pF	8.5	25	
		C_L = 100 pF	16	45	
		C_L = 150 pF	23	65	

Figure 10. CMOS-Level Outputs

input timings

timing requirements for input timings(1) (see Figure 11)

		MIN	MAX	UNIT
t_{pw}	Input minimum pulse width	$t_{c(ICLK)} + 10$		ns

1 $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$

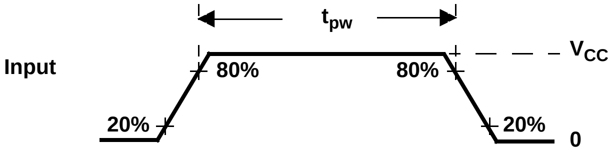


Figure 11. CMOS-Level Inputs

PRODUCT PREVIEW

flash timings

timing requirements for program flash(1)(2)

		MIN	TYP	MAX	UNIT
$t_{prog(16\text{-}bit)}$	Half word (16-bit) programming time	4	16	200	µs
$t_{prog(Total)}$	288K-byte programming time(3)		2	8	s
$t_{erase(sector)}$	Sector erase time		5	15	s
t_{wec}	Write/erase cycles	1000	10000		cycles
$t_{fp(\overline{RST})}$	Flash pump settling time from $\overline{RST}$ to SLEEP		$134t_{c(SYS)}$		ns
$t_{fp(SLEEP)}$	Initial flash pump settling time from SLEEP to STANDBY		$134t_{c(SYS)}$		ns
$t_{fp(STANDBY)}$	Initial flash pump settling time from STANDBY to ACTIVE		$67t_{c(SYS)}$		ns

1 For more detailed information on the flash core sectors, see the flash program and erase section of this data sheet.

2 Flash program/erase is specified only at the temperature range of 25°C to 85°C (A version), or 25°C to 125°C (Q version).

3 The 288K-byte programming time includes overhead of state machine.

PRODUCT PREVIEW

SPIn master mode timing parameters

SPIn master mode external timing parameters (CLOCK PHASE = 0, SPInCLK = output, SPInSIMO = output, and SPInSOMI = input)(1)(2)(3)(see Figure 12)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPInCLK (4)	100	$256t_{c(ICLK)}$	ns
2(5)	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	
	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	
3(5)	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	
	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	
4(5)	$t_{d(SPCH\text{-}SIMO)M}$	Delay time, SPInCLK high to SPInSIMO valid (clock polarity = 0)		10	
	$t_{d(SPCL\text{-}SIMO)M}$	Delay time, SPInCLK low to SPInSIMO valid (clock polarity = 1)		10	
5(5)	$t_{v(SPCL\text{-}SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 0)	$t_{c(SPC)M} - 5 - t_f$		
	$t_{v(SPCH\text{-}SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 1)	$t_{c(SPC)M} - 5 - t_r$		
6(5)	$t_{su(SOMI\text{-}SPCL)M}$	Setup time, SPInSOMI before SPInCLK low (clock polarity = 0)	6		
	$t_{su(SOMI\text{-}SPCH)M}$	Setup time, SPInSOMI before SPInCLK high (clock polarity = 1)	6		
7(5)	$t_{v(SPCL\text{-}SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 0)	4		
	$t_{v(SPCH\text{-}SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 1)	4		

1 The MASTER bit (SPInCTRL2.3) is set and the CLOCK PHASE bit (SPInCTRL2.0) is cleared.
2 $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$
3 For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.
4 When the SPI is in Master mode, the following must be true:
For PS values from 1 to 255:$t_{c(SPC)M} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1.[12:5] register bits.
For PS values of 0:$t_{c(SPC)M} = 2t_{c(ICLK)} \geq 100$ ns.
5 The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2.1).

SPIn master mode timing parameters (continued)

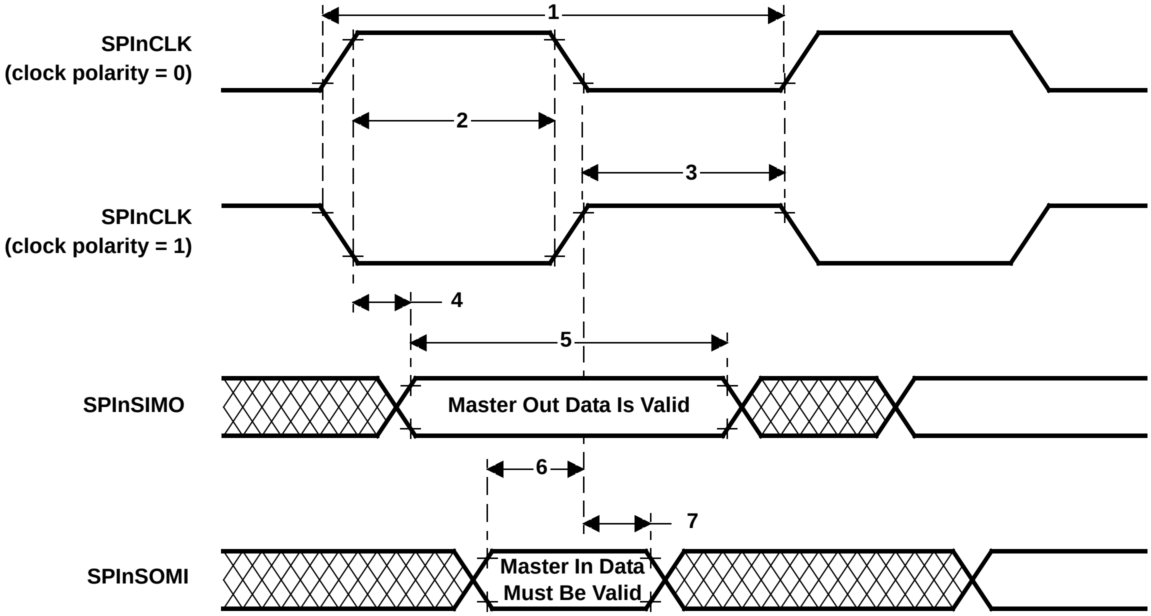


Figure 12. SPIn Master Mode External Timing (CLOCK PHASE = 0)

SPIn master mode timing parameters (continued)

SPIn master mode external timing parameters (CLOCK PHASE = 1, SPInCLK = output, SPInSIMO = output, and SPInSOMI = input)$^{(1)(2)(3)}$ (see Figure 13)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPInCLK $^{(4)}$	100	$256t_{c(ICLK)}$	ns
$2^{(5)}$	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	
	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	
$3^{(5)}$	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	
	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	
$4^{(5)}$	$t_{v(SIMO\text{-}SPCH)M}$	Valid time, SPInCLK high after SPInSIMO data valid (clock polarity = 0) at 85°C	$0.5t_{c(SPC)M} - 10$		
	$t_{v(SIMO\text{-}SPCH)M}$	Valid time, SPInCLK high after SPInSIMO data valid (clock polarity = 0) at 125°C	$0.5t_{c(SPC)M} - 12$		
	$t_{v(SIMO\text{-}SPCL)M}$	Valid time, SPInCLK low after SPInSIMO data valid (clock polarity = 1)	$0.5t_{c(SPC)M} - 10$		
$5^{(5)}$	$t_{v(SPCH\text{-}SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 5 - t_r$		
	$t_{v(SPCL\text{-}SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 5 - t_f$		
$6^{(5)}$	$t_{su(SOMI\text{-}SPCH)M}$	Setup time, SPInSOMI before SPInCLK high (clock polarity = 0)	6		
	$t_{su(SOMI\text{-}SPCL)M}$	Setup time, SPInSOMI before SPInCLK low (clock polarity = 1)	6		
$7^{(5)}$	$t_{v(SPCH\text{-}SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0)	4		
	$t_{v(SPCL\text{-}SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1)	4		

1 The MASTER bit (SPInCTRL2.3) is set and the CLOCK PHASE bit (SPInCTRL2.0) is set.

2 $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$

3 For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.

4 When the SPI is in Master mode, the following must be true:
For PS values from 1 to 255:$t_{c(SPC)M} \geq (PS+1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1.[12:5] register bits.
For PS values of 0:$t_{c(SPC)M} = 2t_{c(ICLK)} \geq 100$ ns.

5 The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2.1).

SPIn master mode timing parameters (continued)

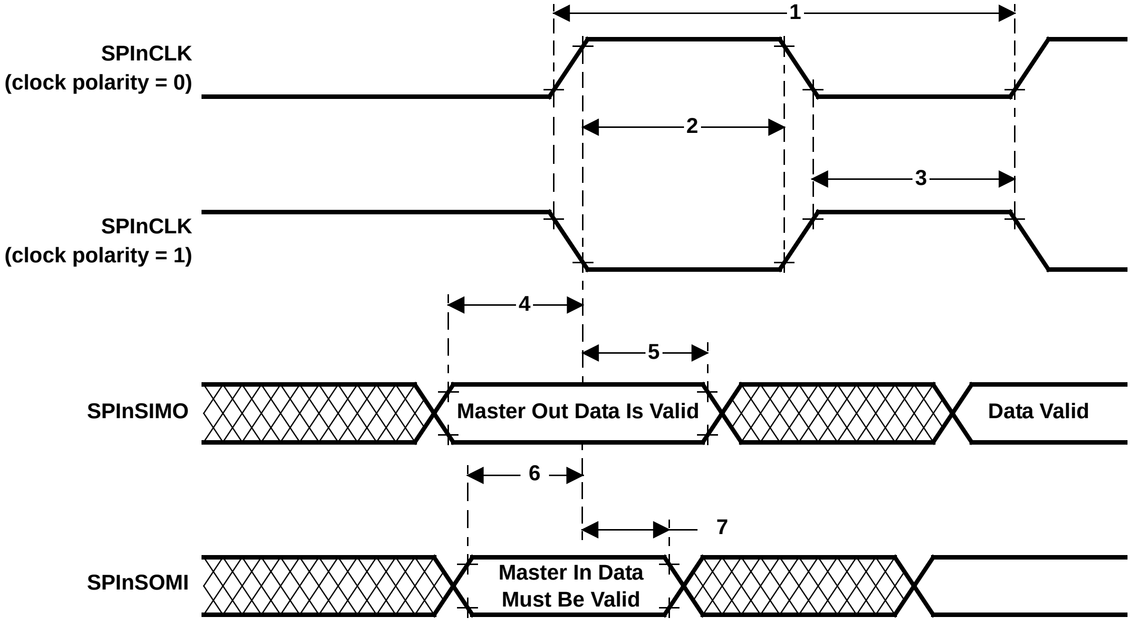


Figure 13. SPIn Master Mode External Timing (CLOCK PHASE = 1)

PRODUCT PREVIEW

SPIn slave mode timing parameters

SPIn slave mode external timing parameters (CLOCK PHASE = 0, SPInCLK = input, SPInSIMO = input, and SPInSOMI = output)(1)(2)(3)(4)(see Figure 14)

NO			MIN	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPInCLK(5)	100	$256t_{c(ICLK)}$	ns
2(6)	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	
	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	
3(6)	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	
	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	
4(6)	$t_{d(SPCH-SOMI)S}$	Delay time, SPInCLK high to SPInSOMI valid (clock polarity = 0)		$6 + t_r$	
	$t_{d(SPCL-SOMI)S}$	Delay time, SPInCLK low to SPInSOMI valid (clock polarity = 1)		$6 + t_f$	
5(6)	$t_{v(SPCH-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0)	$t_{c(SPC)S} - 6 - t_r$		
	$t_{v(SPCL-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1)	$t_{c(SPC)S} - 6 - t_f$		
6(6)	$t_{su(SIMO-SPCL)S}$	Setup time, SPInSIMO before SPInCLK low (clock polarity = 0)	6		
	$t_{su(SIMO-SPCH)S}$	Setup time, SPInSIMO before SPInCLK high (clock polarity = 1)	6		
7(6)	$t_{v(SPCL-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 0)	6		
	$t_{v(SPCH-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 1)	6		

1 The MASTER bit (SPInCTRL2.3) is cleared and the CLOCK PHASE bit (SPInCTRL2.0) is cleared.

2 If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(ICLK)}$, where PS = prescale value set in SPInCTL1.[12:5].

3 For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.

4 $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$

5 When the SPIn is in Slave mode, the following must be true:
For PS values from 1 to 255:$t_{c(SPC)S} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1.[12:5] register bits.
For PS values of 0:$t_{c(SPC)S} = 2t_{c(ICLK)} \geq 100$ ns.

6 The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2.1).

SPIn slave mode timing parameters (continued)

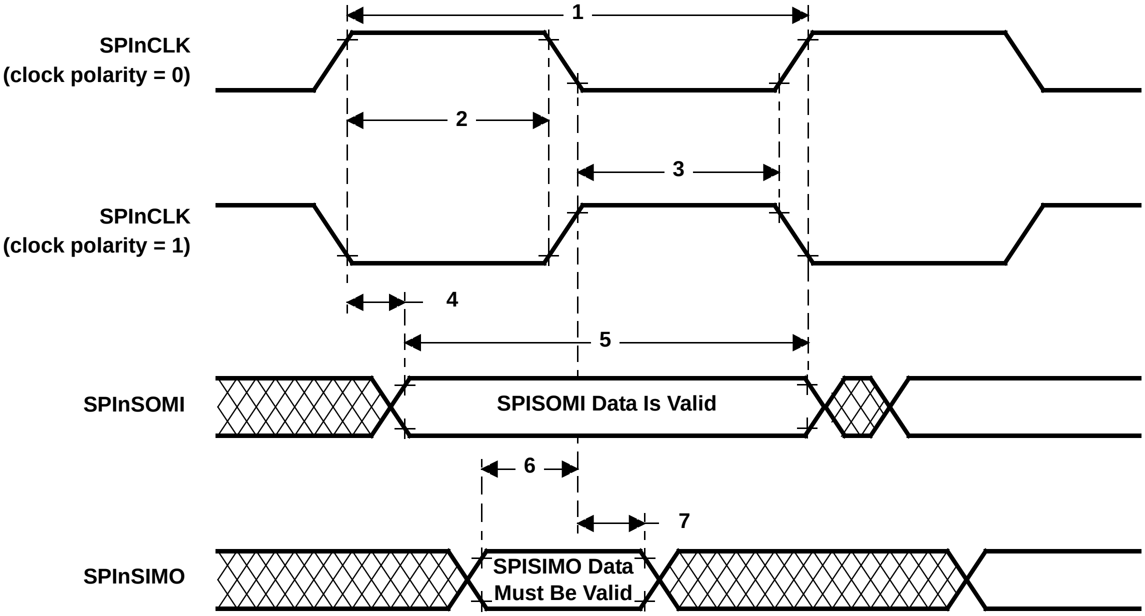


Figure 14. SPIn Slave Mode External Timing (CLOCK PHASE = 0)

SPIn slave mode timing parameters (continued)

SPIn slave mode external timing parameters (CLOCK PHASE = 1, SPInCLK = input, SPInSIMO = input, and SPInSOMI = output)(1)(2)(3)(4)(see Figure 15)

NO			MIN	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPInCLK(5)	100	$256t_{c(ICLK)}$	ns
2(6)	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)S}-0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S}+0.25t_{c(ICLK)}$	
	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)S}-0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S}+0.25t_{c(ICLK)}$	
3(6)	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)S}-0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S}+0.25t_{c(ICLK)}$	
	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)S}-0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S}+0.25t_{c(ICLK)}$	
4(6)	$t_{v(SOMI-SPCH)S}$	Valid time, SPInCLK high after SPInSOMI data valid (clock polarity = 0)	$0.5t_{c(SPC)S}-6-t_r$		
	$t_{v(SOMI-SPCL)S}$	Valid time, SPInCLK low after SPInSOMI data valid (clock polarity = 1)	$0.5t_{c(SPC)S}-6-t_f$		
5(6)	$t_{v(SPCH-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)S}-6-t_r$		
	$t_{v(SPCL-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)S}-6-t_f$		
6(6)	$t_{su(SIMO-SPCH)S}$	Setup time, SPInSIMO before SPInCLK high (clock polarity = 0)	6		
	$t_{su(SIMO-SPCL)S}$	Setup time, SPInSIMO before SPInCLK low (clock polarity = 1)	6		
7(6)	$t_{v(SPCH-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 0)	6		
	$t_{v(SPCL-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 1)	6		

1 The MASTER bit (SPInCTRL2.3) is cleared and the CLOCK PHASE bit (SPInCTRL2.0) is set.

2 If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(ICLK)}$, where PS = prescale value set in SPInCTL1.[12:5].

3 For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.

4 $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$

5 When the SPIn is in Slave mode, the following must be true:
For PS values from 1 to 255:$t_{c(SPC)S} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1.[12:5] register bits.
For PS values of 0:$t_{c(SPC)S} = 2t_{c(ICLK)} \geq 100$ ns.

6 The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2.1).

PRODUCT PREVIEW

SPIn slave mode timing parameters (continued)

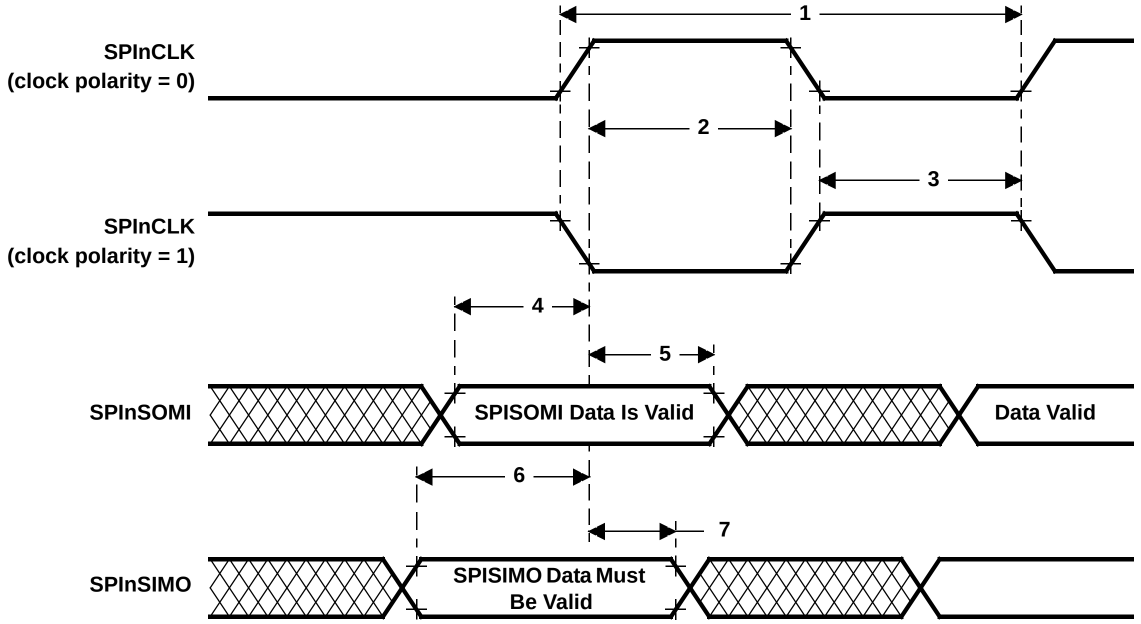


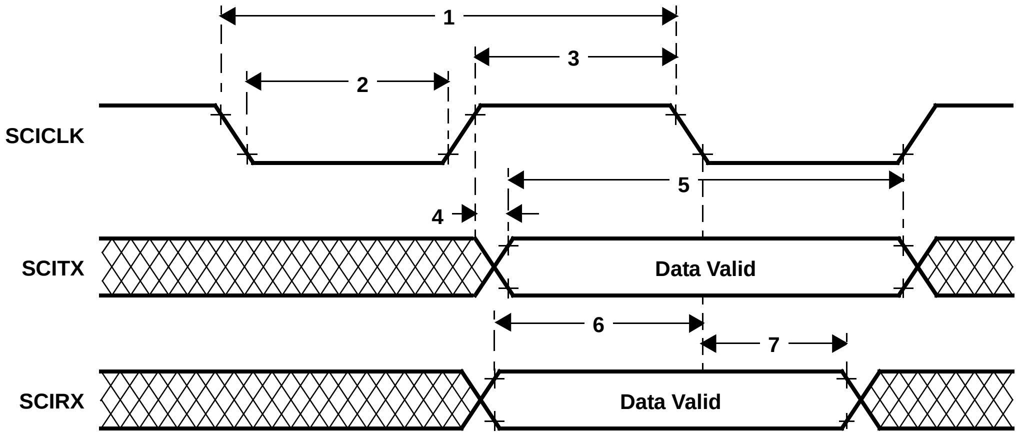
Figure 15. SPIn Slave Mode External Timing (CLOCK PHASE = 1)

SCIn isosynchronous mode timings — internal clock

timing requirements for internal clock SCIn isosynchronous mode[(1)(2)(3)] (see Figure 16)

NO.			(BAUD + 1) IS EVEN OR BAUD = 0		(BAUD + 1) IS ODD AND BAUD ≠ 0		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SCC)}$	Cycle time, SCInCLK	$2t_{c(ICLK)}$	$2^{24}t_{c(ICLK)}$	$3t_{c(ICLK)}$	$(2^{24} - 1)\ t_{c(ICLK)}$	ns
2	$t_{w(SCCL)}$	Pulse duration, SCInCLK low	$0.5t_{c(SCC)} - t_f$	$0.5t_{c(SCC)} + 5$	$0.5t_{c(SCC)} + 0.5t_{c(ICLK)} - t_f$	$0.5t_{c(SCC)} + 0.5t_{c(ICLK)}$	ns
3	$t_{w(SCCH)}$	Pulse duration, SCInCLK high	$0.5t_{c(SCC)} - t_r$	$0.5t_{c(SCC)} + 5$	$0.5t_{c(SCC)} - 0.5t_{c(ICLK)} - t_r$	$0.5t_{c(SCC)} - 0.5t_{c(ICLK)}$	ns
4	$t_{d(SCCH\text{-}TXV)}$	Delay time, SCInCLK high to SCInTX valid		10		10	ns
5	$t_{v(TX)}$	Valid time, SCInTX data after SCInCLK low	$t_{c(SCC)} - 10$		$t_{c(SCC)} - 10$		ns
6	$t_{su(RX\text{-}SCCL)}$	Setup time, SCInRX before SCInCLK low	$t_{c(ICLK)} + t_f + 20$		$t_{c(ICLK)} + t_f + 20$		ns
7	$t_{v(SCCL\text{-}RX)}$	Valid time, SCInRX data after SCInCLK low	$- t_{c(ICLK)} + t_f + 20$		$- t_{c(ICLK)} + t_f + 20$		ns

1 BAUD = 24-bit concatenated value formed by the SCI[H,M,L]BAUD registers.
2 $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$
3 For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.



NOTE : Data transmission/reception characteristics for isosynchronous mode with internal clocking are similar to the asynchronous mode. Data transmission occurs on the SCICLK rising edge, and data reception on the SCICLK falling edge.

Figure 16. SCIn Isosynchronous Mode Timing Diagram for Internal Clock

PRODUCT PREVIEW

SCIn isosynchronous mode timings — external clock

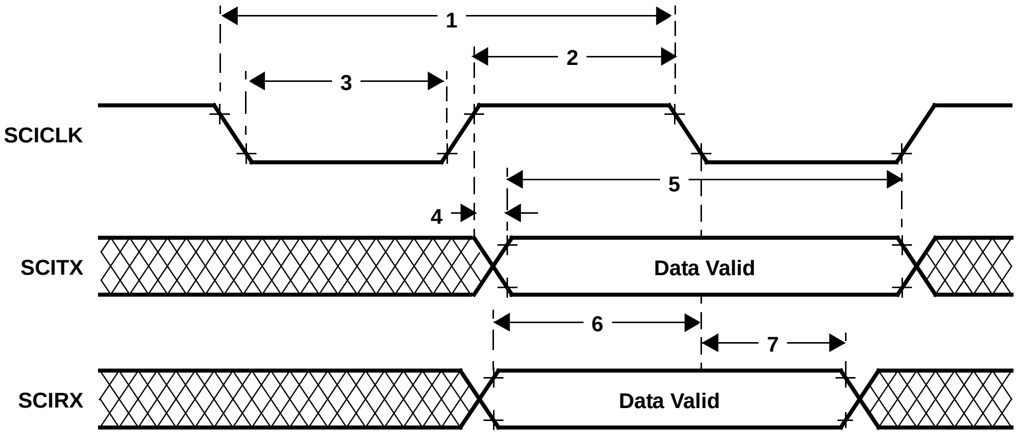
timing requirements for external clock SCIn isosynchronous mode(1)(2) (see Figure 17)

NO.			MIN	MAX	UNIT
1	$t_{c(SCC)}$	Cycle time, SCInCLK(3)	$8t_{c(ICLK)}$		ns
2	$t_{w(SCCH)}$	Pulse duration, SCInCLK high	$0.5t_{c(SCC)} - 0.25t_{c(ICLK)}$	$0.5t_{c(SCC)} + 0.25t_{c(ICLK)}$	ns
3	$t_{w(SCCL)}$	Pulse duration, SCInCLK low	$0.5t_{c(SCC)} - 0.25t_{c(ICLK)}$	$0.5t_{c(SCC)} + 0.25t_{c(ICLK)}$	ns
4	$t_{d(SCCH\text{-}TXV)}$	Delay time, SCInCLK high to SCInTX valid		$2t_{c(ICLK)} + 12 + t_r$	ns
5	$t_{v(TX)}$	Valid time, SCInTX data after SCInCLK low	$2t_{c(SCC)}-10$		ns
6	$t_{su(RX\text{-}SCCL)}$	Setup time, SCInRX before SCInCLK low	0		ns
7	$t_{v(SCCL\text{-}RX)}$	Valid time, SCInRX data after SCInCLK low	$2t_{c(ICLK)} + 10$		ns

1 $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$

2 For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.

3 When driving an external SCInCLK, the following must be true: $t_{c(SCC)} \geq 8t_{c(ICLK)}$



NOTE : Data transmission/reception characteristics for isosynchronous mode with external clocking are similar to the asynchronous mode. Data transmission occurs on the SCICLK rising edge, and data reception on the SCICLK falling edge.

Figure 17. SCIn Isosynchronous Mode Timing Diagram for External Clock

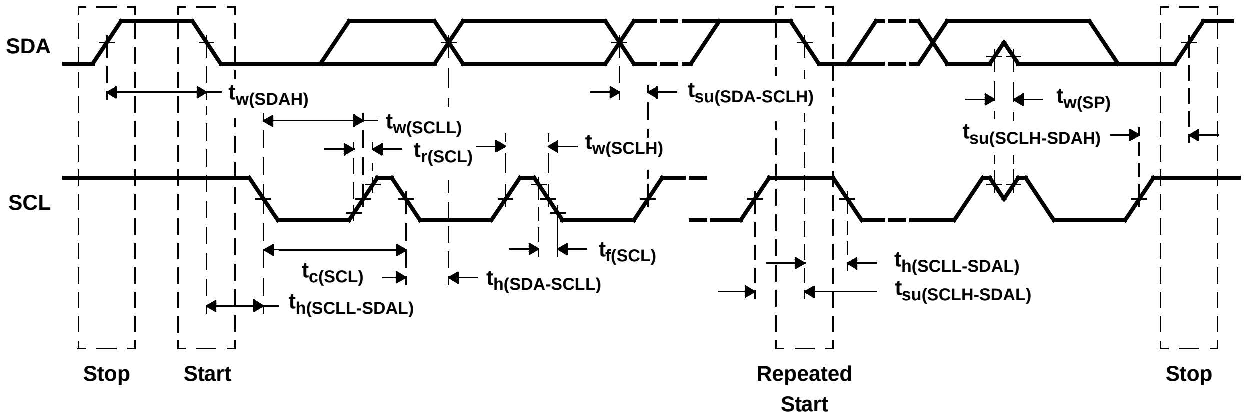
I2C timing

Table 11 below assumes testing over recommended operating conditions.

Table 11. I2C Signals (SDA and SCL) Switching Characteristics(1)

PARAMETER			STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(I2CCLK)}$	Cycle time, I2C module clock		75	150	75	150	ns
$t_{c(SCL)}$	Cycle time, SCL		10		2.5		µs
$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)		4.7		0.6		µs
$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a repeated START condition)		4		0.6		µs
$t_{w(SCLL)}$	Pulse duration, SCL low		4.7		1.3		µs
$t_{w(SCLH)}$	Pulse duration, SCL high		4		0.6		µs
$t_{su(SDA-SCLH)}$	Setup time, SDA valid before SCL high		250		100		ns
$t_{h(SDA-SCLL)}$	Hold time, SDA valid after SCL low	For I2C bus devices	0	3.45(2)	0	0.9	µs
$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions		4.7		1.3		µs
$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)		4.0		0.6		µs
$t_{w(SP)}$	Pulse duration, spike (must be suppressed)				0	50	ns
C_b(3)	Capacitive load for each bus line			400		400	pF

1 The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
2 The maximum $t_{h(SDA-SCLL)}$ for I2C bus devices needs only be met if the device does not stretch the low period ($t_{w(SCLL)}$) of the SCL signal.
3 C_b = The total capacitance of one bus line in pF.



NOTE:A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

NOTE:The maximum $t_{h(SDA-SCLL)}$ needs only be met if the device does not stretch the LOW period ($t_{w(SCLL)}$) of the SCL signal.

NOTE:A Fast-mode I2C-bus device can be used in a standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r max + $t_{su(SDA-SCLH)}$.

NOTE:C_b = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed.

Figure 18. I2C Timings

standard CAN controller (SCC) mode timings

dynamic characteristics for the CANSTX and CANSRX pins

PARAMETER		MIN	MAX	UNIT
t_d(CANSTX)	Delay time, transmit shift register to CANSTX pin(1)		15	ns
t_d(CANSRX)	Delay time, CANSRX pin to receive shift register		5	ns

1 These values do not include rise/fall times of the output buffer.

expansion bus timing parameters, –40°C $\le T_J \le$ 150°C, 3.0 V $\le V_{CC} \le$ 3.6 V (see figure 19 and figure 20)

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{c(\text{CO})}$	Cycle time, CLKOUT	20.8		ns
2	$t_{d(\text{COH-EBADV})}$	Delay Time, CLKOUT high to EBADDR valid		26	ns
3	$t_{h(\text{COH-EBADIV})}$	Hold Time, EBADDR invalid after CLKOUT high	(– 8)		ns
4	$t_{d(\text{COH-EBOE})}$	Delay Time, CLKOUT high to $\overline{\text{EBOE}}$ fall		15	ns
5	$t_{h(\text{COH-EBOEH})}$	Hold Time, $\overline{\text{EBOE}}$ rise after CLKOUT high	2		ns
6	$t_{d(\text{COL-EBWR})}$	Delay Time, CLKOUT low to write strobe ($\overline{\text{EBWR}}$) low		17	ns
7	$t_{h(\text{COL-EBWRH})}$	Hold Time, $\overline{\text{EBWR}}$ high after CLKOUT low	3		ns
8	$t_{su(\text{EBRDATV-COH})}$	Setup time, EBDATA valid before CLKOUT high (READ)(2)	25		ns
9	$t_{h(\text{COH-EBRDATIV})}$	Hold time, EBDATA invalid after CLKOUT high (READ)	(– 6)		ns
10	$t_{d(\text{COL-EBWDATV})}$	Delay time, CLKOUT low to EBDATA valid (WRITE)(3)		19	ns
11	$t_{h(\text{COL-EBWDATIV})}$	Hold time, EBDATA invalid after CLKOUT low (WRITE)	(– 12)		ns
SECONDARY TIMES					
12	$t_{d(\text{COH-EBCS0})}$	Delay, CLKOUT high to $\overline{\text{EBCS0}}$ fall	6	20	ns
13	$t_{h(\text{COH-EBCS0H})}$	Hold, $\overline{\text{EBCS0}}$ rise after CLKOUT high		21	ns
14	$t_{su(\text{COH-EBHOLDL})}$	Setup time, $\overline{\text{EBHOLD}}$ low to CLKOUT high(2)	25		ns
15	$t_{su(\text{COH-EBHOLDH})}$	Setup time, $\overline{\text{EBHOLD}}$ high to CLKOUT high(2)	25		ns

2 Setup time is the minimum time under worst case conditions. Data with less setup time will not work.
3 Valid after CLKOUT goes low for write cycles.

expansion bus module timing

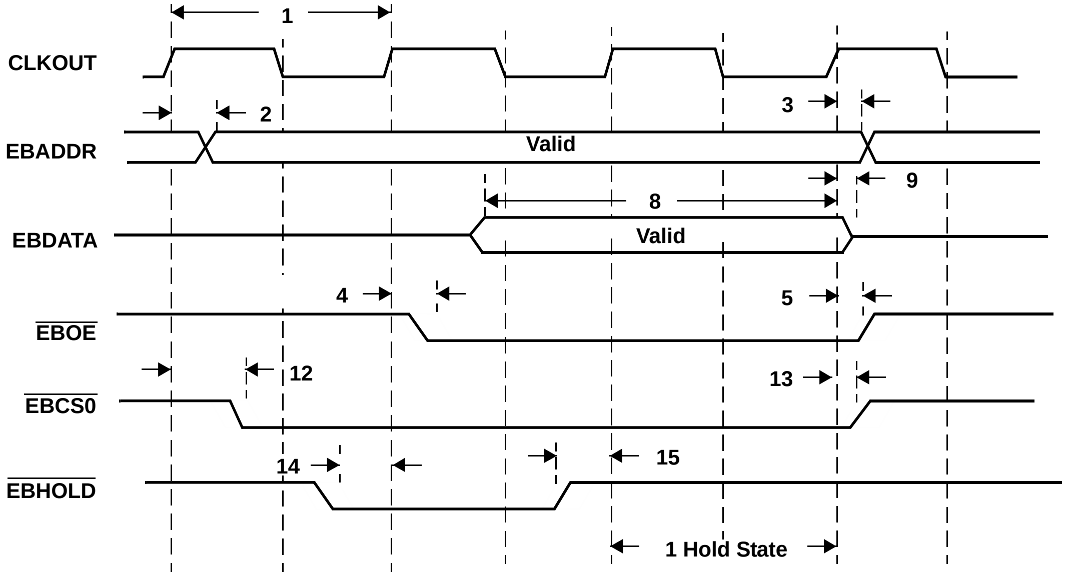


Figure 19. Expansion Memory Signal Timing - Reads

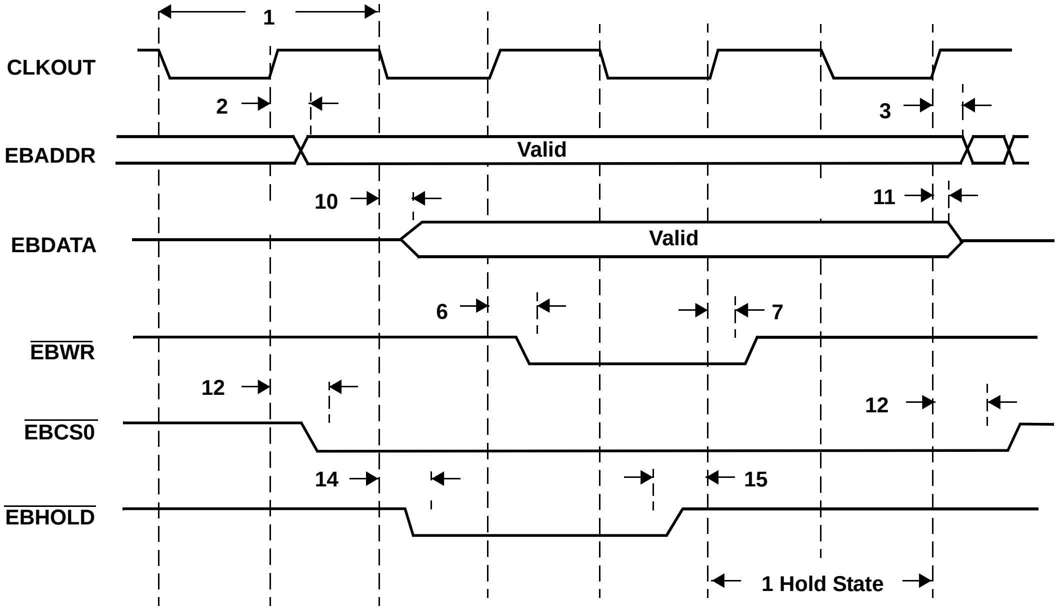


Figure 20. Expansion Memory Signal Timing - Writes

high-end timer (HET) timings

minimum PWM output pulse width:

This is equal to one high resolution clock period (HRP). The HRP is defined by the 6-bit high resolution prescale factor (hr) which is user defined, giving prescale factors of 1 to 64, with a linear increment of codes.

Therefore, the minimum PWM output pulse width = HRP(min) = hr(min)/SYSCLK = 1/SYSCLK

For example, for a SYSCLK of 30 MHz, the minimum PWM output pulse width = 1/30 = 33.33ns

minimum input pulses we can capture:

The input pulse width must be greater or equal to the low resolution clock period (LRP), i.e., the HET loop (the HET program must fit within the LRP). The LRP is defined by the 3-bit loop-resolution prescale factor (lr), which is user defined, with a power of 2 increment of codes. That is, the value of lr can be 1, 2, 4, 8, 16, or 32.

Therefore, the minimum input pulse width = LRP(min) = hr(min) * lr(min)/SYSCLK = 1 * 1/SYSCLK

For example, with a SYSCLK of 30 MHz, the minimum input pulse width = 1 * 1/30 = 33.33 ns

NOTE

Once the input pulse width is greater than LRP, the resolution of the measurement is still HRP. (That is, the captured value gives the number of HRP clocks inside the pulse.)

Abbreviations:

High resolution clock period = HRP = hr/SYSCLK

Loop resolution clock period = LRP = hr*lr/SYSCLK

hr = HET high resolution divide rate = 1, 2, 3,...63, 64

lr = HET low resolution divide rate = 1, 2, 4, 8, 16, 32

multi-buffered A-to-D converter (MibADC)

The multi-buffered A-to-D converter (MibADC) has a separate power bus for its analog circuitry that enhances the A-to-D performance by preventing digital switching noise on the logic circuitry which could be present on V_{SS} and V_{CC} from coupling into the A-to-D analog stage. All A-to-D specifications are given with respect to AD_{REFLO} unless otherwise noted.

Resolution	10 bits (1024 values)
Monotonic	Assured
Output conversion code	00h to 3FFh [00 for $V_{AI} \leq AD_{REFLO}$; 3FF for $V_{AI} \geq AD_{REFHI}$]

MibADC recommended operating conditions(1)

		MIN	MAX	UNIT
AD_{REFHI}	A-to-D high -voltage reference source	V_{SSAD}	V_{CCAD}	V
AD_{REFLO}	A-to-D low-voltage reference source	V_{SSAD}	V_{CCAD}	V
V_{AI}	Analog input voltage	$V_{SSAD} - 0.3$	$V_{CCAD} + 0.3$	V
I_{AIC}	Analog input clamp current(2) ($V_{AI} < V_{SSAD} - 0.3$ or $V_{AI} > V_{CCAD} + 0.3$)	− 2	2	mA

1 For V_{CCAD} and V_{SSAD} recommended operating conditions, see the "device recommended operating conditions" table.

2 Input currents into any ADC input channel outside the specified limits could affect conversion results of other channels.

operating characteristics over full ranges of recommended operating conditions(1)(2)

PARAMETER		DESCRIPTION/CONDITIONS		MIN	TYP	MAX	UNIT
R_i	Analog input resistance	See Figure 21			250	500	Ω
C_i	Analog input capacitance	See Figure 21	Conversion			10	pF
			Sampling			30	pF
I_{AIL}	Analog input leakage current	See Figure 21		–1		1	μA
$I_{ADREFHI}$	AD_{REFHI} input current	$AD_{REFHI} = 3.6$ V, $AD_{REFLO} = V_{SSAD}$				5	mA
CR	Conversion range over which specified accuracy is maintained	$AD_{REFHI} - AD_{REFLO}$		3		3.6	V
E_{DNL}	Differential nonlinearity error	Difference between the actual step width and the ideal value. (See Figure 22)				±2	LSB
E_{INL}	Integral nonlinearity error	Maximum deviation from the best straight line through the MibADC. MibADC transfer characteristics, excluding the quantization error. (See Figure 23)				±2	LSB
E_{TOT}	Total error/Absolute accuracy	Maximum value of the difference between an analog value and the ideal midstep value. (See Figure 24)				±2	LSB

1 $V_{CCAD} = AD_{REFHI}$

2 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{10}$ for the MibADC

PRODUCT PREVIEW

multi-buffered A-to-D converter (MibADC) (continued)

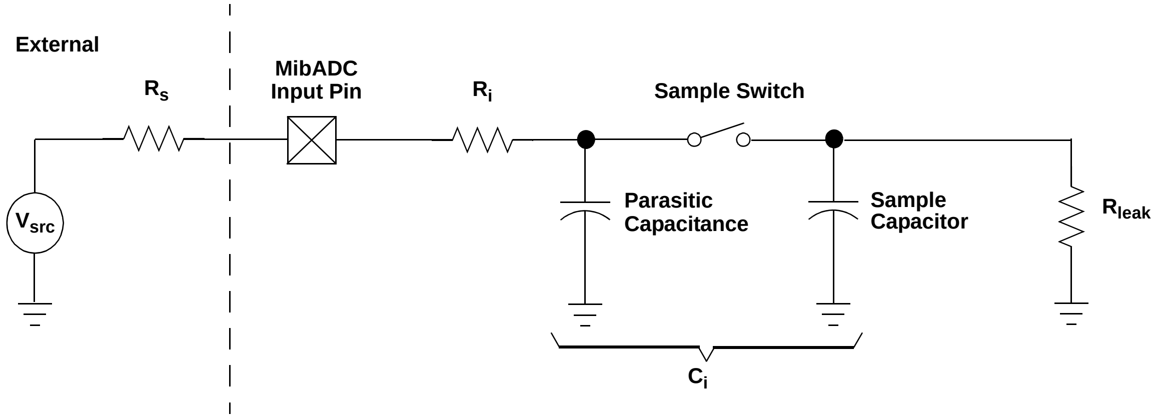


Figure 21. MibADC Input Equivalent Circuit

multi-buffer ADC timing requirements

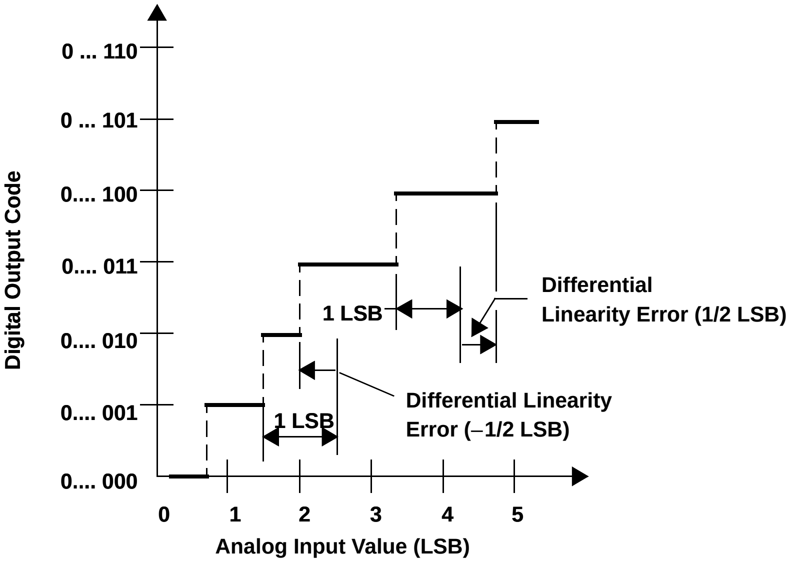
		MIN	NOM	MAX	UNIT
$t_{c(ADCLK)}$	Cycle time, MibADC clock	0.05			µs
$t_{d(SH)}$	Delay time, sample and hold time	1			µs
$t_{d(C)}$	Delay time, conversion time	0.55			µs
$t_{d(SHC)}$(1)	Delay time, total sample/hold and conversion time	1.55			µs

---

1 This is the minimum sample/hold and conversion time that can be achieved. These parameters are dependent on many factors; for more details, see the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

multi-buffered A-to-D converter (MibADC) (continued)

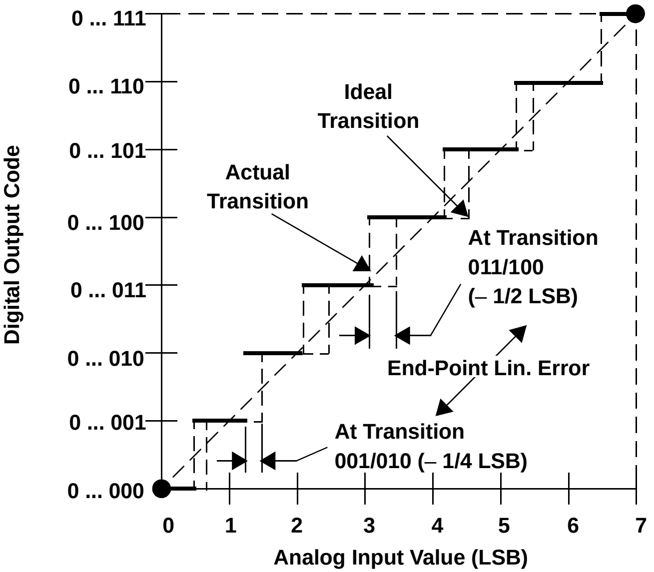
The differential nonlinearity error shown in Figure 22 (sometimes referred to as differential linearity) is the difference between an actual step width and the ideal value of 1 LSB.



NOTE A: 1 LSB = $(AD_{REFHI} – AD_{REFLO})/2^{10}$

Figure 22. Differential Nonlinearity (DNL)

The integral nonlinearity error shown in Figure 23 (sometimes referred to as linearity error) is the deviation of the values on the actual transfer function from a straight line.

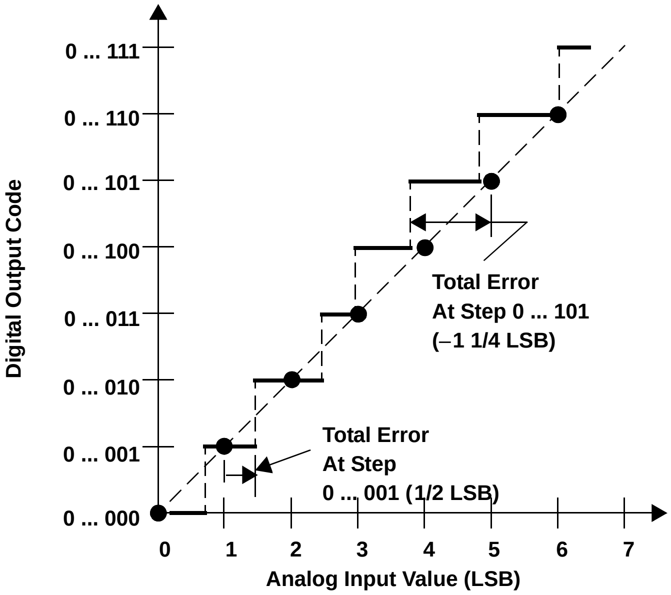


NOTE A: 1 LSB = $(AD_{REFHI} – AD_{REFLO})/2^{10}$

Figure 23. Integral Nonlinearity (INL) Error

multi-buffer A-to-D converter (MibADC) (continued)

The absolute accuracy or total error of an MibADC as shown in Figure 24 is the maximum value of the difference between an analog value and the ideal midstep value.

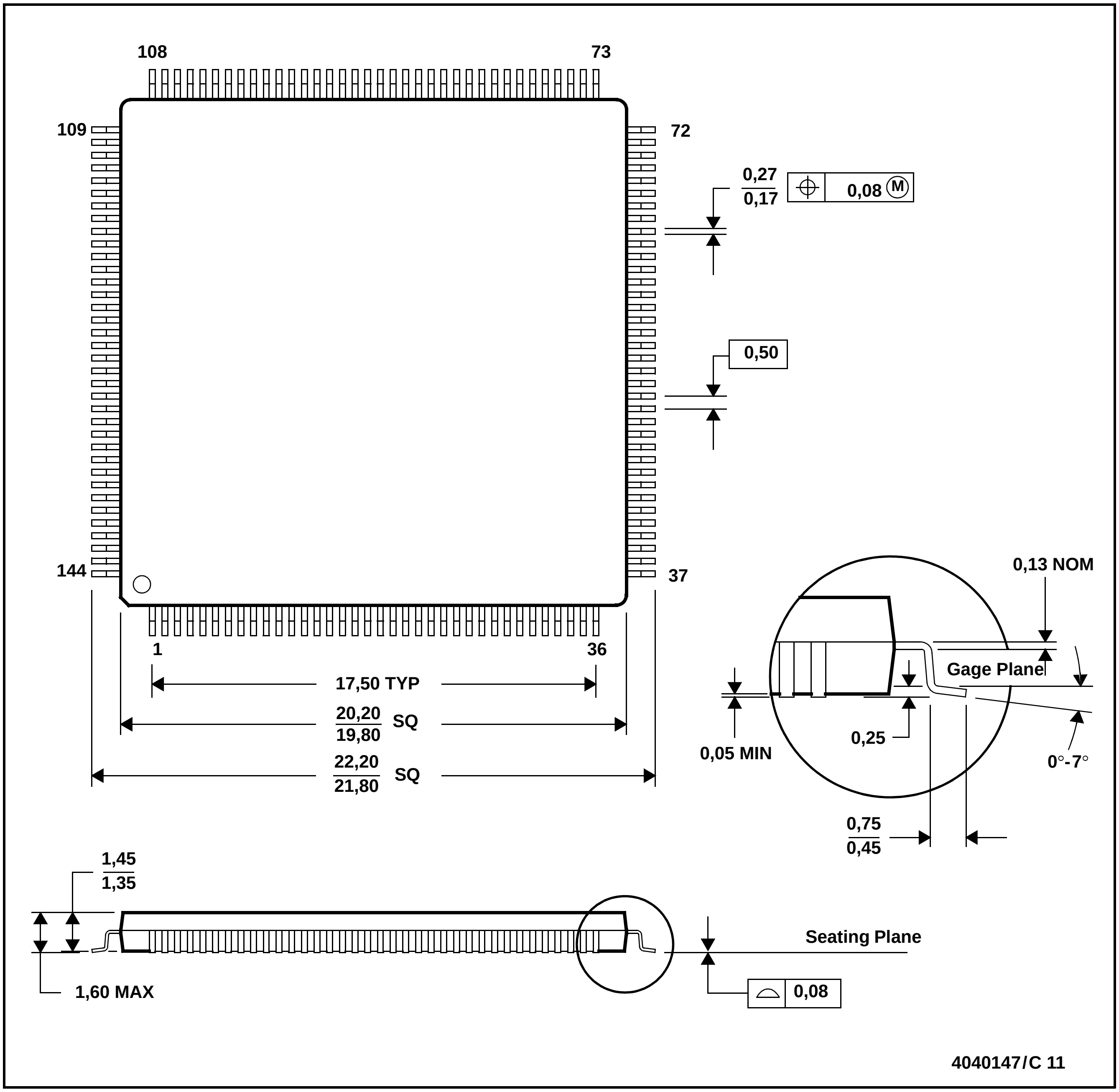


NOTE A: 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{10}$

Figure 24. Absolute Accuracy (Total) Error

MECHANICAL DATA

PGE (S-PQFP-G144) **PLASTIC QUAD FLATPACK**



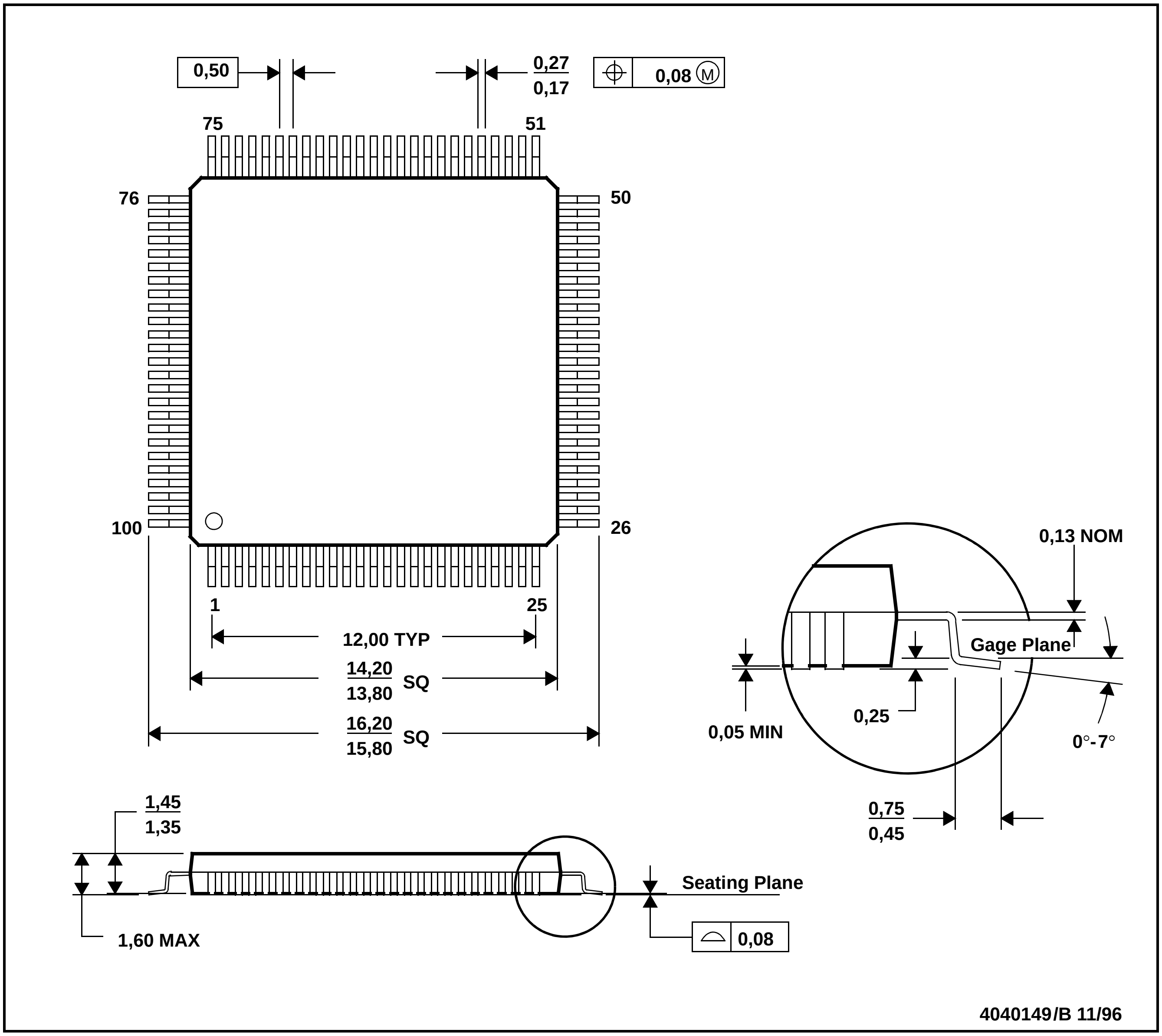
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-026

Thermal Resistance Characteristics

PARAMETER	°C/W
$R_{\Theta JA}$	43
$R_{\Theta JC}$	5

MECHANICAL DATA

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

Thermal Resistance Characteristics

PARAMETER	°C/W
$R_{\Theta JA}$	48
$R_{\Theta JC}$	5

List of Figures

TMS470R1VF288 144-Pin PGE Package (TOP VIEW) (without Expansion Bus)
TMS470R1VF288 144-Pin PGE Package (TOP VIEW) (with Expansion Bus)
TMS470R1VF288 100-Pin PZ Package (TOP VIEW)
Functional Block Diagram
Figure 1. TMS470R1VF288 Memory Map
Figure 2. JTAG Interface
Figure 3. TMS470R1x Family Nomenclature
Figure 4. Test Load Circuit
Figure 5. Crystal/Clock Connection
Figure 6. CLKOUT Timing Diagram
Figure 7. ECLK Timing Diagram
Figure 8. $\overline{\text{PORRST}}$ Timing Diagram
Figure 9. JTAG Scan Timings
Figure 10. CMOS-Level Outputs
Figure 11. CMOS-Level Inputs
Figure 12. SPIn Master Mode External Timing (CLOCK PHASE = 0)
Figure 13. SPIn Master Mode External Timing (CLOCK PHASE = 1)
Figure 14. SPIn Slave Mode External Timing (CLOCK PHASE = 0)
Figure 15. SPIn Slave Mode External Timing (CLOCK PHASE = 1)
Figure 16. SCIn Isosynchronous Mode Timing Diagram for Internal Clock
Figure 17. SCIn Isosynchronous Mode Timing Diagram for External Clock
Figure 18. I2C Timings
Figure 19. Expansion Memory Signal Timing - Reads
Figure 20. Expansion Memory Signal Timing - Writes
Figure 21. MibADC Input Equivalent Circuit
Figure 22. Differential Nonlinearity (DNL)
Figure 23. Integral Nonlinearity (INL) Error
Figure 24. Absolute Accuracy (Total) Error
Mechanical Data
Mechanical Data

List of Tables

Table 1. Device Characteristics
Table 2. TMS470R1VF288 Memory Selection Assignment
Table 3. VF288 Peripherals, System Module, and Flash Base Addresses
Table 4. DMA Request Lines Connections
Table 5. Interrupt Priority (IEM and CIM)
Table 6. Expansion Bus Mux Mapping
Table 7. Expansion Bus Pins
Table 8. MibADC Event Hookup Configuration
Table 9. TMS470 Device ID Bit Allocation Register
Table 10. Device Part Number
Table 11. I2C Signals (SDA and SCL) Switching Characteristics

REVISION HISTORY

REV	DATE	NOTES
E	12/05	Updates: Page 44, temperature condition removed from t_{wec} parameter. Page 44, note #2 revised. Page 56, expansion bus timing parameters updated.

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