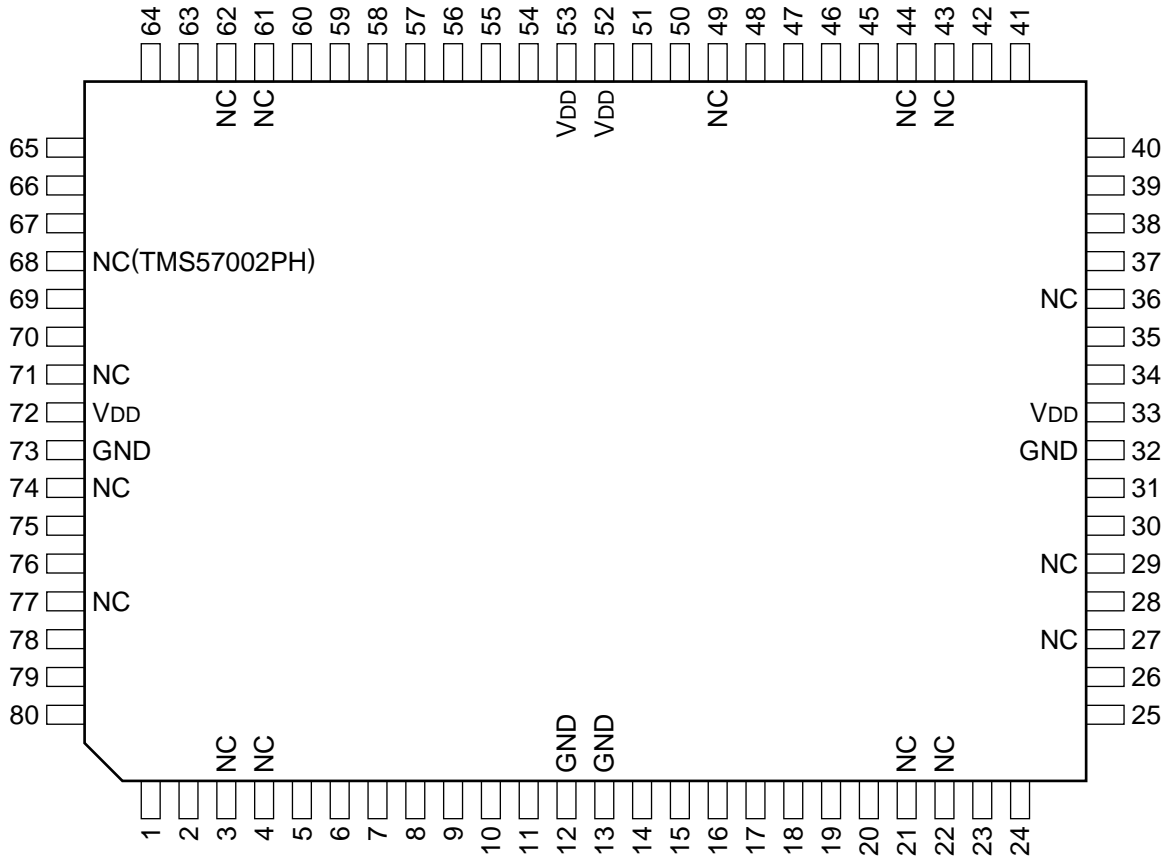


C-MOS DIGITAL AUDIO SIGNAL PROCESSOR

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	SYNPOL	21	—	NC	41	O	EA8	61	—	NC
2	I	BCKO	22	—	NC	42	O	EA9 (MSB)	62	—	NC
3	—	NC	23	I/O	ED6	43	—	NC	63	O	EMPTY
4	—	NC	24	I/O	ED7 (MSB)	44	—	NC	64	I	MUTE
5	I	LRCKO	25	O	EA0 (LSB)	45	I	D0 (LSB)	65	I	CS
6	O	SO0	26	O	EA1	46	I	D1	66	I	WR
7	O	SO1	27	—	NC	47	I	D2	67	I	PLOAD
8	O	CAS	28	O	EA2	48	I	D3	68	O	NC/DREADY*
9	O	RAS	29	—	NC	49	—	NC	69	I	CLOAD
10	I	CLKSEL	30	O	EA3	50	I	D4	70	I	STRB
11	I	CLKIN	31	O	EA4	51	I	D5	71	—	NC
12	—	GND	32	—	GND	52	—	VDD	72	—	VDD
13	—	GND	33	—	VDD	53	—	VDD	73	—	GND
14	O	WE	34	O	EA5	54	I	D6	74	—	NC
15	I/O	ED0 (LSB)	35	O	EA6	55	I	D7 (MSB)	75	I	BCKI
16	I/O	ED1	36	—	NC	56	O	PC0	76	I	LRCKI
17	I/O	ED2	37	O	EA7	57	I	BIO	77	—	NC
18	I/O	ED3	38	I	TEST0	58	O	OVFA	78	I	SI0
19	I/O	ED4	39	I	TEST1	59	O	OVFM	79	I	SI1
20	I/O	ED5	40	I	TEST2	60	I	RS	80	I	SYNC

* : TMS57002PH ; NC.

78	SI0	SO0	6
79	SI1	SO1	7
75	BCKI	PC0	56
2	BCKO	EMPTY	63
76	LRCKI		
5	LRCKO	EA9	42
80	SYNC	EA8	41
11	CLKIN	EA7	37
10	CLKSEL	EA6	35
1	SYNPOL	EA5	34
		EA4	31
60	RS	EA3	30
66	WR	EA2	28
65	CS	EA1	26
67	PLOAD	EA0	25
69	CLOAD	CAS	8
64	MUTE	RAS	9
57	BIO	WE	14
55	D7	ED7	15
54	D6	ED6	16
51	D5	ED5	17
50	D4	ED4	18
48	D3	ED3	19
47	D2	ED2	20
46	D1	ED1	23
45	D0	ED0	24
70	STRB	OVFA	58
		OVFM	59
38	TEST0		
39	TEST1	DREADY	68
40	TEST2		

INPUT

BCKI ; BIT CLOCK FOR SERIAL INPUT
BCKO ; BIT CLOCK FOR SERIAL OUTPUT
 $\overline{\text{BIO}}$; BRANCH CONTROL
CLKIN ; MASTER CLOCK
CLKSEL ; CLKIN FREQUENCY SELECT (L ; 512 fs H ; 256 fs)
 $\overline{\text{CLOAD}}$; COUNTING LOAD
 $\overline{\text{CS}}$; CHIP ENABLE FOR PARALLEL PORT
D0 - 7 ; PARALLEL PORT
 $\overline{\text{DREADY}}$; DATA READY SIGNAL TO HOST CONTROLLER
LRCKI ; RIGHT AND LEFT CHANNEL THRESHOLD CLOCK FOR SERIAL INPUT
LRCKO ; RIGHT AND LEFT CHANNEL THRESHOLD CLOCK FOR SERIAL OUTPUT
 $\overline{\text{MUTE}}$; MUTE
 $\overline{\text{PLOAD}}$; PROGRAM LOAD
 $\overline{\text{RS}}$; RESET (L ; RESET H ; NORMAL OPERATION)
SI0, 1 ; SERIAL INPUT DATA 0, 1
 $\overline{\text{STRB}}$; DATA STROBE FOR PARALLEL PORT
SYNC ; PROGRAM SYNC SIGNAL
SYNPOL ; SYNC SIGNAL EFFECTIVE EDGE SELECT (L ; DOWN H ; UP)
TEST0 - 2 ; FOR TEST
 $\overline{\text{WR}}$; RIGHT ENABLE FOR PARALLEL PORT

OUTPUT

$\overline{\text{CAS}}$; COL ADDRESS STROBE FOR OUTER EXTERNAL RAM
EA0 - 9 ; OUTER EXTERNAL RAM ADDRESS
EMPTY ; COUNTING BUFFER EMPTY
 $\overline{\text{OVFA}}$; ALU OVERFLOW FLAG (OPEN DRAIN OUTPUT)
 $\overline{\text{OVFM}}$; MAC OVERFLOW FLAG (OPEN DRAIN OUTPUT)
PC0 ; PROGRAM COUNTER 0
 $\overline{\text{RAS}}$; ROW ADDRESS STROBE FOR OUTER EXTERNAL RAM
SO0, 1 ; SERIAL OUTPUT DATA 0, 1
 $\overline{\text{WE}}$; RIGHT ENABLE FOR OUTER EXTERNAL RAM

INPUT/OUTPUT

ED0 - 7 ; OUTER EXTERNAL RAM DATA

