- **Organization**
  1M Words × 8 Bits × 2 Banks
- **3.3-V Power Supply (±10% Tolerance)**
- **Two Banks for On-Chip Interleaving (Gapless Accesses)**
- **High Bandwidth − Up to 100-MHz Data Rates**
- **CAS Latency (CL) Programmable to 2 or 3 Cycles From Column-Address Entry**
- **Burst Sequence Programmable to Serial or Interleave**
- **Burst Length Programmable to 1, 2, 4, or 8**
- **Chip Select and Clock Enable for Enhanced-System Interfacing**
- **Cycle-by-Cycle DQ-Bus Mask Capability**
- **Auto-Refresh and Self-Refresh Capabilities**
- **4K Refresh (Total for Both Banks)**
- **High-Speed, Low-Noise, Low-Voltage TTL (LVTTL) Interface**
- **Power-Down Mode**
- **Compatible With JEDEC Standards**
- **Pipeline Architecture**
- **Temperature Ranges**
  Operating, 0°C to 70°C
  Storage, − 55°C to 150°C
- **Performance Ranges:**

	SYNCHRONOUS CLOCK CYCLE TIME		ACCESS TIME (CLOCK TO OUTPUT)		REFRESH TIME INTERVAL
	t_{CK3} (CL† = 3)	t_{CK2} (CL = 2)	t_{AC3} (CL = 3)	t_{AC2} (CL = 2)	
’626812A-10	10 ns	15 ns	7 ns	7 ns	64 ms

† CL = CAS latency

TMS626812A
DGE PACKAGE
(TOP VIEW)

V_{CC}	1	44	V_{SS}
DQ0	2	43	DQ7
V_{SSQ}	3	42	V_{SSQ}
DQ1	4	41	DQ6
V_{CCQ}	5	40	V_{CCQ}
DQ2	6	39	DQ5
V_{SSQ}	7	38	V_{SSQ}
DQ3	8	37	DQ4
V_{CCQ}	9	36	V_{CCQ}
NC	10	35	NC
NC	11	34	NC
$\overline{\text{W}}$	12	33	DQM
$\overline{\text{CAS}}$	13	32	CLK
$\overline{\text{RAS}}$	14	31	CKE
$\overline{\text{CS}}$	15	30	NC
A11	16	29	A9
A10	17	28	A8
A0	18	27	A7
A1	19	26	A6
A2	20	25	A5
A3	21	24	A4
V_{CC}	22	23	V_{SS}

PIN NOMENCLATURE	
A[0:10]	Address Inputs A0−A10 Row Addresses A0−A8 Column Addresses A10 Automatic-Precharge Select
A11	Bank Select
$\overline{\text{CAS}}$	Column-Address Strobe
CKE	Clock Enable
CLK	System Clock
$\overline{\text{CS}}$	Chip Select
DQ[0:7]	SDRAM Data Input/Output
DQM	Data-Input/Data-Output Mask Enable
NC	No External Connect
$\overline{\text{RAS}}$	Row-Address Strobe
V_{CC}	Power Supply (3.3-V Typical)
V_{CCQ}	Power Supply for Output Drivers (3.3-V Typical)
V_{SS}	Ground
V_{SSQ}	Ground for Output Drivers
$\overline{\text{W}}$	Write Enable

description

The TMS626812A is a high-speed, 16 777 216-bit synchronous dynamic random-access memory (SDRAM) device organized as:

- Two banks of 1 048 576 words with 8 bits per word

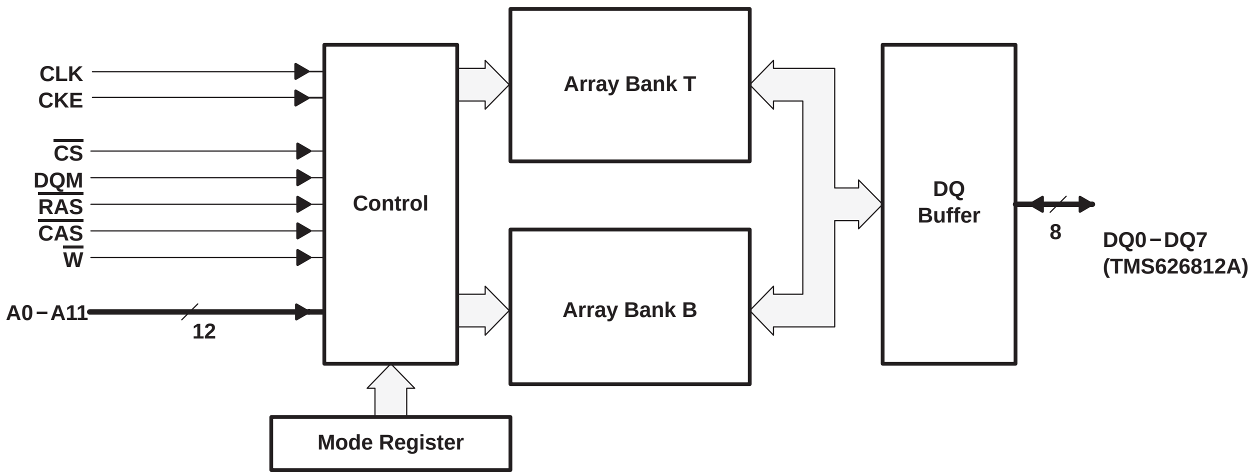
description (continued)

All inputs and outputs of the TMS626812A series are compatible with the LVTTL interface.

The SDRAM employs state-of-the-art technology for high performance, reliability, and low power. All inputs and outputs are synchronized with the CLK input to simplify system design and enhance the use with high-speed microprocessors and caches.

The TMS626812A SDRAM is available in a 400-mil, 44-pin surface-mount TSOP package (DGE suffix).

functional block diagram



operation

All inputs of the ’626812A SDRAM are latched on the rising edge of the system (synchronous) clock. The outputs, DQx, also are referenced to the rising edge of CLK. The ’626812A has two banks that are accessed independently. A bank must be activated before it can be accessed (read from or written to). Refresh cycles refresh both banks alternately.

Six basic commands or functions control most operations of the ’626812A:

- Bank activate / row-address entry
- Column-address entry / write operation
- Column-address entry / read operation
- Bank deactivate
- Auto-refresh
- Self-refresh

Additionally, operations can be controlled by three methods: using chip select ($\overline{CS}$) to select / deselect the devices, using DQM to enable / mask the DQ signals on a cycle-by-cycle basis, or using CKE to suspend the CLK input. The device contains a mode register that must be programmed for proper operation.

Table 1, Table 2, and Table 3 show the various operations that are available on the ’626812A. These truth tables identify the command and / or operations and their respective mnemonics. Each truth table is followed by a legend that explains the abbreviated symbols. An access operation refers to any read or write command in progress at cycle n. Access operations include the cycle upon which the read or write command is entered and all subsequent cycles through the completion of the access burst.

operation (continued)

Table 1. Basic Command Function Table†

COMMAND‡	STATE OF BANK(S)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	A11	A10	A0−A9	MNEMONIC
Mode register set	T = deac B = deac	L	L	L	L	X	X	A0−A6 = V A7−A8 = L A9 = V	MRS
Bank deactivate (precharge)	X	L	L	H	L	BS	L	X	DEAC
Deactivate all banks	X	L	L	H	L	X	H	X	DCAB
Bank activate / row-address entry	SB = deac	L	L	H	H	BS	V	V	ACTV
Column-address entry / write operation	SB = actv	L	H	L	L	BS	L	V	WRT
Column-address entry / write operation with automatic deactivate	SB = actv	L	H	L	L	BS	H	V	WRT-P
Column-address entry / read operation	SB = actv	L	H	L	H	BS	L	V	READ
Column-address entry / read operation with automatic deactivate	SB = actv	L	H	L	H	BS	H	V	READ-P
No operation	X	L	H	H	H	X	X	X	NOOP
Control-input inhibit / no operation	X	H	X	X	X	X	X	X	DESL
Auto-refresh§	T = deac B = deac	L	L	L	H	X	X	X	REFR

† For exception of these commands on cycle n, one of the following must be true:
- CKE(n−1) must be high
- t_{CESP} must be satisfied for power-down exit
- t_{CESP} and t_{RC} must be satisfied for self-refresh exit
- t_{IS} and n_{CLE} must be satisfied for clock-suspend exit.

DQM(n) is a don’t care.

‡ All other unlisted commands are considered vendor-reserved commands or illegal commands.

§ Auto-refresh or self-refresh entry requires that all banks be deactivated or be in an idle state prior to the command entry.

Legend:

n = CLK cycle number
L = Logic low
H = Logic high
X = Don’t care, either logic low or logic high
V = Valid
T = Bank T
B = Bank B
actv = Activated
deac = Deactivated
BS = Logic high to select bank T; logic low to select bank B
SB = Bank selected by A11 at cycle n

operation (continued)

Table 2. Clock-Enable (CKE) Command Function Table†

COMMAND	STATE OF BANK(S)	CKE (n−1)	CKE (n)	$\overline{CS}$ (n)	$\overline{RAS}$ (n)	$\overline{CAS}$ (n)	$\overline{W}$ (n)	MNEMONIC
Self-refresh entry	T = deac B = deac	H	L	L	L	L	H	SLFR
Power-down entry on cycle (n+1)‡	T = no access operation§ B = no access operation§	H	L	X	X	X	X	PDE
Self-refresh exit	T = self-refresh B = self-refresh	L	H	L	H	H	H	—
		L	H	H	X	X	X	—
Power-down exit¶	T = power down B = power down	L	H	X	X	X	X	—
CLK suspend on cycle (n+1)	T = access operation§ B = access operation§	H	L	X	X	X	X	HOLD
CLK suspend exit on cycle (n+1)	T = access operation§ B = access operation§	L	H	X	X	X	X	—

† For execution of these commands, A0 − A11(n) and DQM(n) are don't care entries.
‡ On cycle n, the device executes the respective command (listed in Table 1). On cycle (n+1), the device enters power-down mode.
§ A bank is no longer in an access operation one cycle after the last data-out cycle of a read operation, and two cycles after the last data-in cycle of a write operation. Neither the PDE nor the HOLD command is allowed on the cycle immediately following the last data-in cycle of a write operation.
¶ If setup time from CKE high to the next CLK high satisfies t_{CESP}, the device executes the respective command (listed in Table 1). Otherwise, either the DESL or the NOOP command must be applied before any other command.

Legend:

- n = CLK cycle number
- L = Logic low
- H = Logic high
- X = Don't care, either logic low or logic high
- T = Bank T
- B = Bank B
- deac = Deactivated

operation (continued)

Table 3. Data-Mask (DQM) Command Function Table†

COMMAND	STATE OF BANK(S)	DQM (n)	DATA IN (n)	DATA OUT (n+2)	MNEMONIC
—	T = deac and B = deac	X	N/A	Hi-Z	—
—	T = actv and B = actv (no access operation)‡	X	N/A	Hi-Z	—
Data-in enable	T = write or B = write	L	V	N/A	ENBL
Data-in mask	T = write or B = write	H	M	N/A	MASK
Data-out enable	T = read or B = read	L	N/A	V	ENBL
Data-out mask	T = read or B = read	H	N/A	Hi-Z	MASK

† For exception of these commands on cycle n, one of the following must be true:
- CKE(n−1) must be high
- t_{CESP} must be satisfied for power-down exit
- t_{CESP} and t_{RC} must be satisfied for self-refresh exit
- t_{IS} and n_{CLE} must be satisfied for clock-suspend exit.

$\overline{CS}$(n), $\overline{RAS}$(n), $\overline{CAS}$(n), $\overline{W}$(n), and A0 − A11(n) are don't care except for interrupt conditions.

‡ A bank is no longer in an access operation one cycle after the last data-out cycle of a read operation, and two cycles after the last data-in cycle of a write operation. Neither the PDE nor the HOLD command is allowed on the cycle immediately following the last data-in cycle of a write operation.

Legend:
- n = CLK cycle number
- L = Logic low
- H = Logic high
- Hi-Z = High-impedance state
- X = Don't care, either logic low or logic high
- V = Valid
- M = Masked input data
- N/A = Not applicable
- T = Bank T
- B = Bank B
- actv = Activated
- deac = Deactivated
- write = Activated and accepting data inputs on cycle n
- read = Activated and delivering data outputs on cycle (n + 2)

burst sequence

All data for the ’626812A are written or read in a burst fashion—that is, a single starting address is entered into the device and the ’626812A internally accesses a sequence of locations based on that starting address. After the first access, some subsequent accesses can be at preceding, as well as succeeding, column addresses depending on the starting address entered. This sequence can be programmed to follow either a serial burst or an interleave burst (see Table 4, Table 5, and Table 6). The length of the burst can be programmed to be 1, 2, 4, or 8 accesses (see the section on setting the mode register). After a read burst is complete (as determined by the programmed-burst length), the outputs are in the high-impedance state until the next read access is initiated.

Table 4. 2-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A0			
	DECIMAL		BINARY	
	START	2ND	START	2ND
Serial	0	1	0	1
	1	0	1	0
Interleave	0	1	0	1
	1	0	1	0

Table 5. 4-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A0−A1							
	DECIMAL				BINARY			
	START	2ND	3RD	4TH	START	2ND	3RD	4TH
Serial	0	1	2	3	00	01	10	11
	1	2	3	0	01	10	11	00
	2	3	0	1	10	11	00	01
	3	0	1	2	11	00	01	10
Interleave	0	1	2	3	00	01	10	11
	1	0	3	2	01	00	11	10
	2	3	0	1	10	11	00	01
	3	2	1	0	11	10	01	00

burst sequence (continued)

Table 6. 8-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A0−A2															
	DECIMAL								BINARY							
	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH
Serial	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111
	1	2	3	4	5	6	7	0	001	010	011	100	101	110	111	000
	2	3	4	5	6	7	0	1	010	011	100	101	110	111	000	001
	3	4	5	6	7	0	1	2	011	100	101	110	111	000	001	010
	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011
	5	6	7	0	1	2	3	4	101	110	111	000	001	010	011	100
	6	7	0	1	2	3	4	5	110	111	000	001	010	011	100	101
	7	0	1	2	3	4	5	6	111	000	001	010	011	100	101	110
Interleave	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111
	1	0	3	2	5	4	7	6	001	000	011	010	101	100	111	110
	2	3	0	1	6	7	4	5	010	011	000	001	110	111	100	101
	3	2	1	0	7	6	5	4	011	010	001	000	111	110	101	100
	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011
	5	4	7	6	1	0	3	2	101	100	111	110	001	000	011	010
	6	7	4	5	2	3	0	1	110	111	100	101	010	011	000	001
	7	6	5	4	3	2	1	0	111	110	101	100	011	010	001	000

latency

The beginning data-out cycle of a read burst can be programmed to occur two or three CLK cycles after the read command (see the section on setting the mode register). This feature allows adjustment of the device so that it operates using the capability to latch the data output from the ’626812A. The delay between the READ command and the beginning of the output burst is known as CAS latency. After the initial output cycle begins, the data burst occurs at the CLK frequency without any intervening gaps. Use of minimum read latencies is restricted, based on the maximum frequency rating of the ’626812A.

There is no latency for data-in cycles (write latency). The first data-in cycle of a write burst is entered at the same rising edge of CLK that the WRT command is entered. The write latency is fixed and is not determined by the contents of the mode register.

two-bank operation

The ’626812A contains two independent banks that can be accessed individually or in an interleaved fashion. Each bank must be activated with a row address before it can be accessed. Each bank must then be deactivated before it can be activated again with a new row address. The bank-activate / row-address-entry command (ACTV) is entered by holding $\overline{RAS}$ low, $\overline{CAS}$ high, $\overline{W}$ high, and A11 valid on the rising edge of CLK. A bank can be deactivated either automatically during a READ-P or a WRT-P command or by using bank-deactivate command (DEAC). Both banks can be deactivated at once by using the DCAB command (see Table 1 and the section on bank deactivation).

two-bank row-access operation

The two-bank feature allows access of information on random rows at a higher rate of operation than is possible with a standard DRAM by activating one bank with a row address and, while the data stream is being accessed to/from that bank, activating the second bank with another row address. When the data stream to or from the first bank is completed, the data stream to or from the second bank can begin without interruption. After the second bank is activated, the first bank can be deactivated to allow the entry of a new row address for the next round of accesses. In this manner, operation can continue in an interleaved fashion. Figure 28 shows an example of two-bank row-interleaving read bursts with automatic deactivate for a CAS latency of 3 and a burst length of 8.

two-bank column-access operation

The availability of two banks allows the access of data from random starting columns between banks at a higher rate of operation. After activating each bank with a row address (ACTV command), A11 can be used to alternate READ or WRT commands between the banks to provide gapless accesses at the CLK frequency, provided all specified timing requirements are met. Figure 25 is an example of two-bank column-interleaving read bursts for a CAS latency of three and a burst length of two.

bank deactivation (precharge)

Both banks can be simultaneously deactivated (placed in precharge) by using the DCAB command. A single bank can be deactivated by using the DEAC command. The DEAC command is entered identically to the DCAB command except that A10 must be low and A11 is used to select the bank to be precharged (see Table 1). A bank can also be deactivated automatically by using A10 during a read or write command. If A10 is held high during the entry of a read or write command, the accessed bank (selected by A11) is automatically deactivated upon completion of the access burst. If A10 is held low during the entry of a read or write command, that bank remains active following the burst. The read and write commands with automatic deactivation are signified as READ-P and WRT-P, respectively.

chip select ($\overline{CS}$)

$\overline{CS}$ can be used to select or deselect the ’626812A for command entry, which might be required for multiple memory-device decoding. If $\overline{CS}$ is held high on the rising edge of CLK (DESL command), the device does not respond to $\overline{RAS}$, $\overline{CAS}$, or $\overline{W}$ until the device is selected again by holding $\overline{CS}$ low on the rising edge of CLK. Any other valid command can be entered simultaneously on the same rising CLK edge of the select operation. The device can be selected/deselected on a cycle-by-cycle basis (see Table 1 and Table 2). The use of $\overline{CS}$ does not affect an access burst that is in progress; the DESL command can restrict only $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$ inputs to the ’626812A.

data mask

The MASK command or its opposite, the data-in enable (ENBL) command (see Table 3), is performed on a cycle-by-cycle basis to gate any data cycle within a read burst or a write burst. The application of DQM to a write burst has no latency (n_{DID} = 0 cycle), but the application of DQM to a read burst has a latency of n_{DOD} = 2 cycles. During a write burst, if DQM is held high on the rising edge of CLK, the data input is ignored on that cyce. When DQM is held high at the rising edge of CLK during a read burst, n_{DOD} cycles later, the data goes to the high-impdeance state. Figure 16 and Figure 28 show examples of data-mask operations.

CLK suspend/power-down mode

For normal device operation, CKE should be held high to enable CLK. If CKE goes low during the execution of a READ (READ-P) or WRT (WRT-P) operation, the state of the DQ bus at the immediate next rising edge of CLK is frozen at its current state, and no further inputs are accepted until CKE returns high. This is known

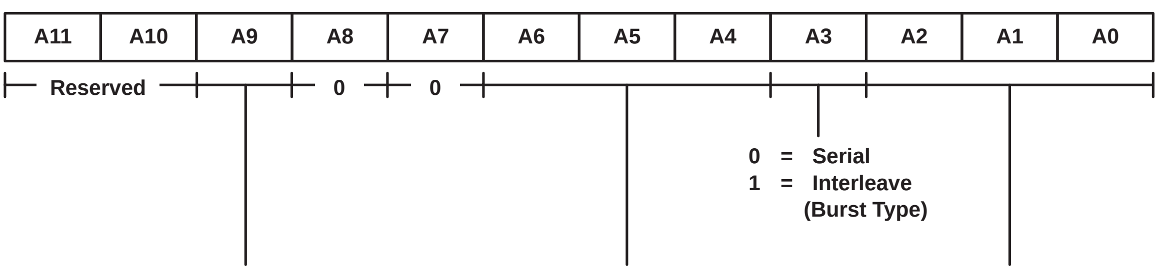
CLK suspend/power-down mode (continued)

as a CLK-suspend operation and its execution indicates a HOLD command. The device resumes operation from the point where it was placed in suspension, beginning with the second rising edge of CLK after CKE returns high.

If CKE is brought low when no read or write command is in progress, the device enters power-down mode. If both banks are deactivated when power-down mode is entered, power consumption is reduced to a minimum. Power-down mode can be used during row-active or auto-refresh periods to reduce input buffer power. After power-down mode is entered, no further inputs are accepted until CKE returns high. To ensure that data in the device remains valid during the power-down mode, the self-refresh command (SLFR) must be executed concurrently with the power-down entry (PDE) command. When exiting power-down mode, new commands can be entered on the first CLK edge after CKE returns high, provided that the setup time (t_{CESP}) is satisfied. Table 2 shows the command configuration for a CLK suspend/power-down operation. Figure 17, Figure 18, and Figure 31 show examples of the procedure.

setting the mode register

The ’626812A contains a mode register that must be programmed with the CAS latency, the burst type, and the burst length. This is accomplished by executing a mode-register set (MRS) command with the information entered on address lines A0−A9. A logic 0 must be entered on A7 and A8, but A10 and A11 are don’t-care entries for the ’626812A. When A9 = 1, the write-burst length is always 1. When A9 = 0, the write-burst length is defined by A0−A2. Figure 1 shows the valid combinations for a successful MRS command. Only valid addresses allow the mode register to be changed. If the addresses are not valid, the contents of the mode register are undefined and a valid MRS command is required for proper operation. The MRS command is executed by holding $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$ low, and the input-mode word valid on A0−A9 on the rising edge of CLK (see Table 1). The MRS command can be executed only when both banks are deactivated.



REGISTER BIT A9	WRITE-BURST LENGTH
0	A2−A0
1	1

REGISTER BITS†			CAS LATENCY‡
A6	A5	A4	
0	1	0	2
0	1	1	3

REGISTER BITS§			BURST LENGTH
A2	A1	A0	
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8

† All other combinations are reserved.
‡ Refer to timing requirements for minimum valid-read latencies based on maximum frequency rating.
§ All other combinations are reserved.

Figure 1. Mode-Register Programming

refresh

The ’626812A must be refreshed such that all 4096 rows are accessed within t_{REF} (see timing requirements) or data cannot be retained. Refresh can be accomplished by performing a series of ACTV and DEAC commands to every row in both banks, by performing 4096 auto-refresh (REFR) commands, or by placing the device in self-refresh mode. Regardless of the method used, all rows must be refreshed before t_{REF} has expired.

auto-refresh (REFR)

Before performing a REFR command, both banks must be deactivated (placed in precharge). To enter a REFR command, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ must be low and $\overline{\text{W}}$ must be high upon the rising edge of CLK (see Table 1). The refresh address is generated internally such that after 4096 REFR commands, both banks of the ’626812A have been refreshed. The external address and bank select (A11) are ignored. The execution of a REFR command automatically deactivates both banks upon completion of the internal auto-refresh cycle, allowing consecutive REFR-only commands to be executed, if desired, without any intervening DEAC commands. The REFR commands do not necessarily have to be consecutive, but all 4096 must be completed before t_{REF} expires.

self refresh (SLFR)

To enter self refresh, both banks of the ’626812A must first be deactivated and a SLFR command must be executed (see Table 2). The SLFR command is identical to the REFR command except that CKE is low. For proper entry of the SLFR command, CKE is brought low for the same rising edge of CLK that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are low and $\overline{\text{W}}$ is high. CKE must be held low to stay in self-refresh mode. In the self-refresh mode, all refreshing signals are generated internally for both banks with all external signals (except CKE) being ignored. Data is retained by the device automatically for an indefinite period when power is maintained and power consumption is reduced to a minimum. To exit self-refresh mode, CKE must be brought high. New commands may be issued only after t_{RC} has expired. If CLK is made inactive during self refresh, it must be returned to an active and stable condition before CKE is brought high to exit self refresh (see Figure 19).

If the burst-refresh scheme is used, 4096 REFR commands must be executed prior to entering and upon exiting self-refresh. However, if the distributed-refresh scheme utilizing auto-refresh is used (for example, two rows every 32 microseconds), the first set of refreshes must be performed upon exiting self-refresh and before continuing with normal device operation. This ensures that the SDRAM is fully refreshed.

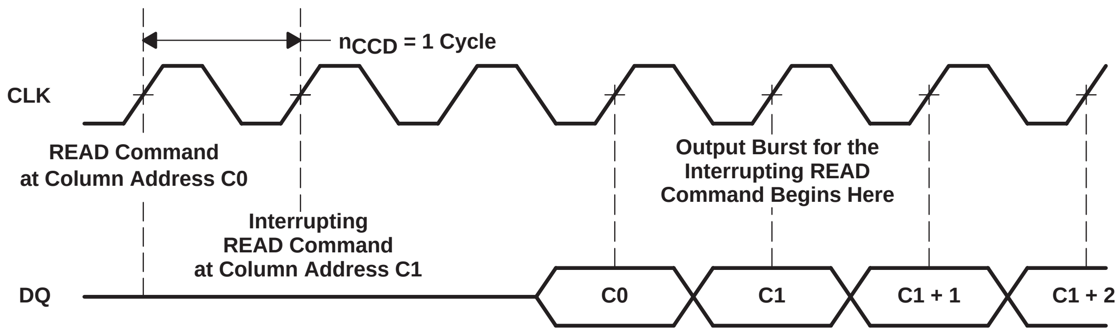
interrupted bursts

A read burst or write burst can be interrupted before the burst sequence has been completed with no adverse effects to the operation. This is accomplished by entering certain superseding commands (see Table 7 and Table 8), provided that all timing requirements are met. A DEAC command is considered an interrupt only if it is issued to the same bank as the preceding READ or WRT command. The interruption of READ-P or WRT-P operations is not supported.

interrupted bursts (continued)

Table 7. Read-Burst Interruption

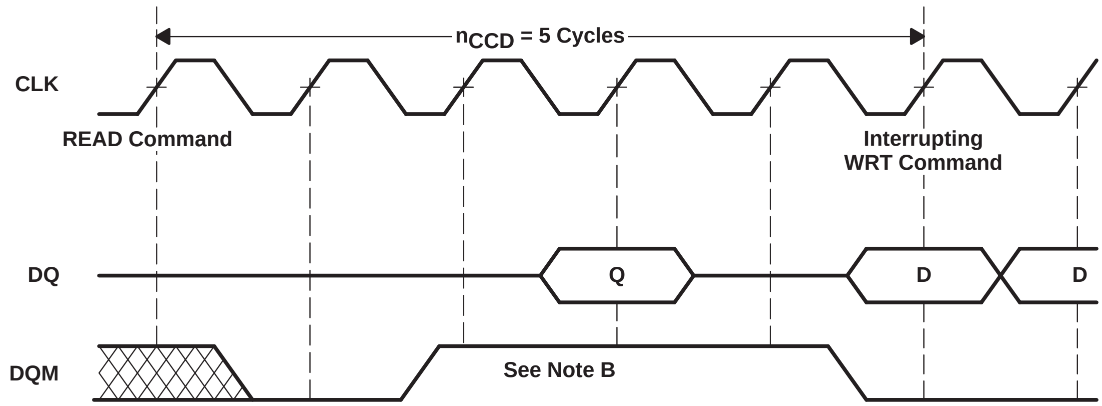
INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING READ BURST
READ, READ-P	Current output cycles continue until the programmed latency from the superseding READ (READ-P) command is met and new output cycles begin (see Figure 2).
WRT, WRT-P	The WRT (WRT-P) command immediately supersedes the read burst in progress. To avoid data contention, DQM must be high before the WRT (WRT-P) command to mask output of the read burst on cycles (n_{CCD}−1), n_{CCD}, and (n_{CCD}+1), assuming that there is any output on these cycles (see Figure 3).
DEAC, DCAB	The DQ bus is in the high-impedance state when n_{HZP} cycles are satisfied or when the read burst completes, whichever occurs first (see Figure 4).



NOTE A: For these examples, assume CAS latency = 3 and burst length = 4.

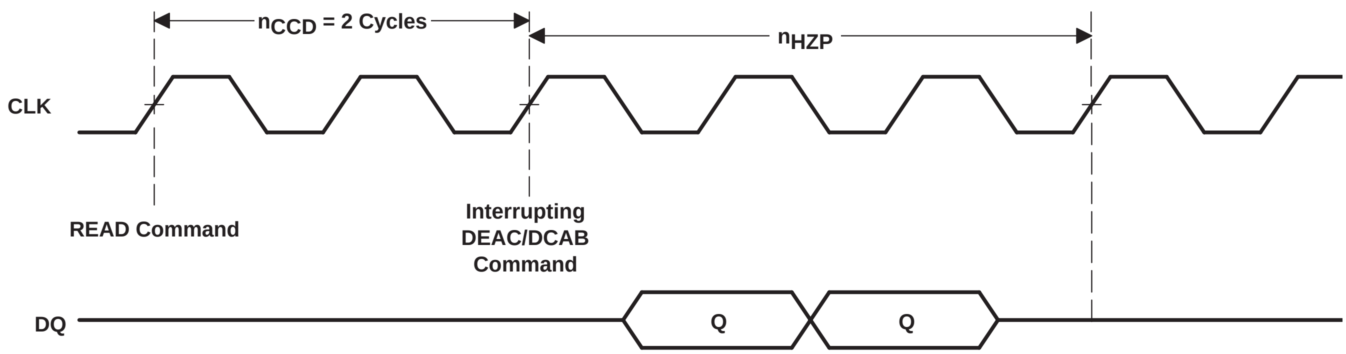
Figure 2. Read Burst Interrupted by Read Command

interrupted bursts (continued)



NOTES: A. For this example, assume CAS latency = 3 and burst length = 4.
B. DQM must be high to mask output of the read burst on cycles (n_{CCD} − 1), n_{CCD}, and (n_{CCD} + 1).

Figure 3. Read Burst Interrupted by Write Command



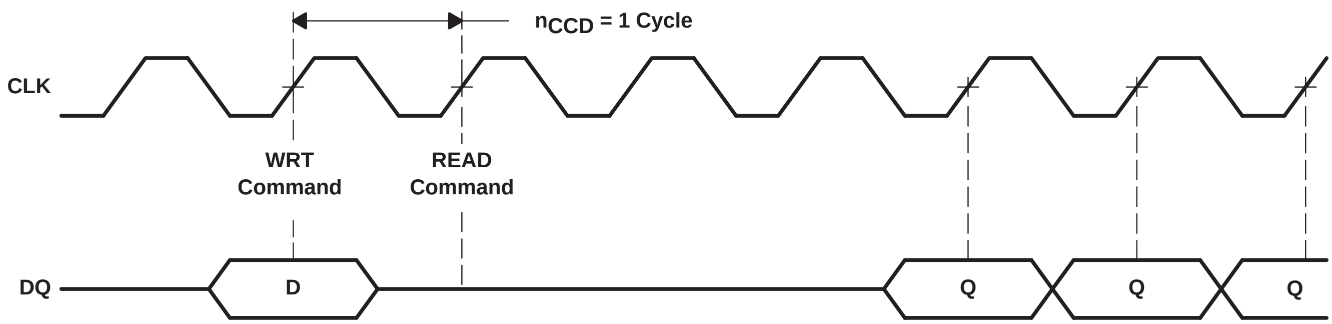
NOTE A: For this example, assume CAS latency = 3 and burst length = 4.

Figure 4. Read Burst Interrupted by DEAC Command

interrupted bursts (continued)

Table 8. Write-Burst Interruption

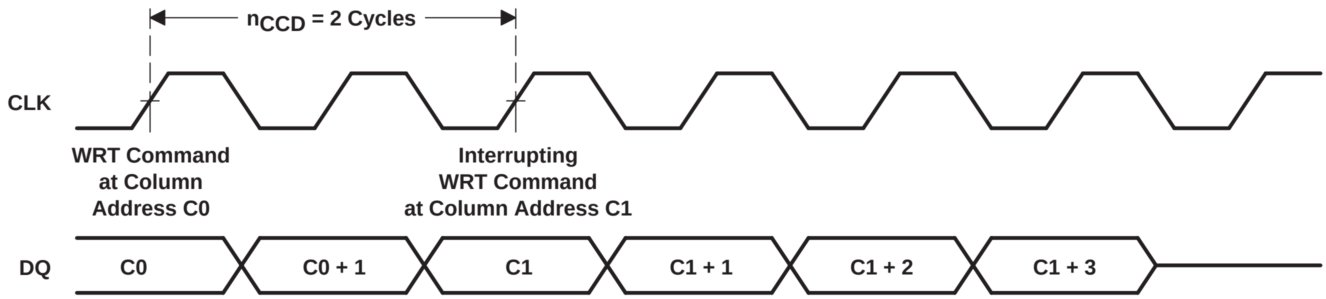
INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING WRITE BURST
READ, READ-P	Data in on the previous cycle is written; however, no further data in is accepted (see Figure 5).
WRT, WRT-P	The new WRT (WRT-P) command and data in immediately supersede the write burst in progress (see Figure 6).
DEAC, DCAB	The DEAC / DCAB command immediately supersedes the write burst in progress. DQM must be used to mask the DQ bus such that the write recovery specification (t_{WR}) is not violated by the interrupt (see Figure 7).



NOTE A: For these examples, assume CAS latency = 3 and burst length = 4.

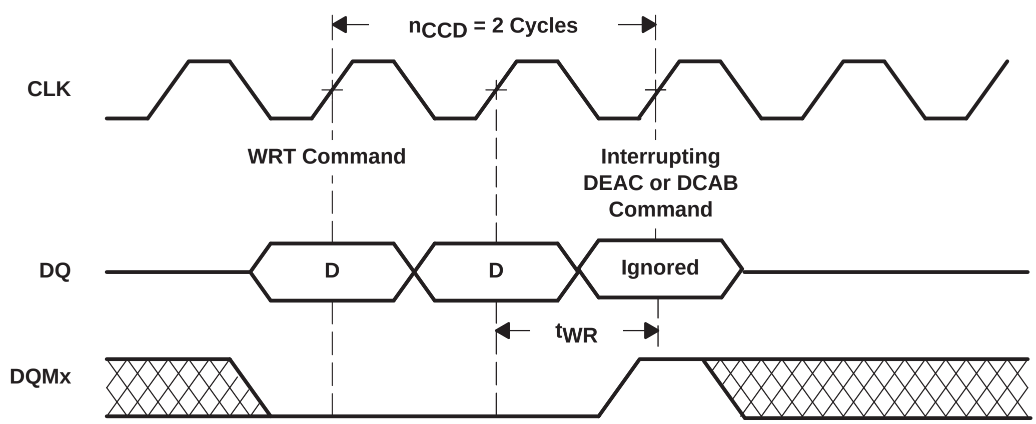
Figure 5. Write Burst Interrupted by Read Command

interrupted bursts (continued)



NOTE A: For this example, assume burst length = 4.

Figure 6. Write Burst Interrupted by Write Command



NOTE A: For this example, assume burst length = 4.

Figure 7. Write Burst Interrupted by DEAC/DCAB Command

power-up sequence

Device initialization should be performed after a power up to the full V_{CC} level. After power is established, a 200-µs interval is required (with no inputs other than CLK). After this interval, both banks of the device must be deactivated. Eight REFR commands must be performed and the mode register must be set to complete the device initialization.

absolute maximum ratings over ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . − 0.5 V to 4.6 V
Supply voltage range for output drivers, V_{CCQ} . . . . − 0.5 V to 4.6 V
Voltage range on any pin (see Note 1) . . . . − 0.5 V to 4.6 V
Short-circuit output current . . . . 50 mA
Power dissipation . . . . 1 W
Ambient temperature range, T_A . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . − 55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{CCQ}	Supply voltage for output drivers	3	3.3	3.6	V
V_{SS}	Supply voltage		0		V
V_{SSQ}	Supply voltage for output drivers		0		V
V_{IH}	High-level input voltage	2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage (see Note 2)	− 0.3		0.8	V
T_A	Ambient temperature	0		70	°C

NOTE 2: V_{IL} MIN = −1.5 V ac (pulse width ≤ 5 ns)

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (see Note 3)

PARAMETER		TEST CONDITIONS		'626812A-10 MIN	'626812A-10 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −2 mA		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
I_I	Input current (leakage)	$0 V \le V_I \le V_{CC} + 0.3 V$, All other pins = 0 V to V_{CC}			±10	µA
I_O	Output current (leakage)	$0 V \le V_O \le V_{CC} + 0.3 V$, Output disabled			±10	µA
I_{CC1}	Operating current	Burst length = 1, $t_{RC} \ge t_{RC}$ MIN I_{OH}/I_{OL} = 0 mA, 1 bank activated (see Note 4)	CAS latency = 2		95	mA
			CAS latency = 3		105	mA
I_{CC2P}	Precharge standby current in power-down mode	CKE $\le V_{IL}$ MAX, t_{CK} = 15 ns (see Note 5)			2	mA
I_{CC2PS}		CKE and CLK $\le V_{IL}$ MAX, $t_{CK} = \infty$ (see Note 6)			2	mA
I_{CC2N}	Precharge standby current in non-power-down mode	CKE $\ge V_{IH}$ MIN, t_{CK} = 15 ns (see Note 5)			25	mA
I_{CC2NS}		CKE $\ge V_{IH}$ MIN, CLK $\le V_{IL}$ MAX, $t_{CK} = \infty$ (see Note 6)			2	mA
I_{CC3P}	Active standby current in power-down mode	CKE $\le V_{IL}$ MAX, t_{CK} = 15 ns (see Note 5)			3	mA
I_{CC3PS}		CKE and CLK $\le V_{IL}$ MAX, $t_{CK} = \infty$ (see Note 6)			3	mA
I_{CC3N}	Active standby current in non-power-down mode	CKE $\ge V_{IH}$ MIN, t_{CK} = 15 ns (see Note 5)			30	mA
I_{CC3NS}		CKE $\ge V_{IH}$ MIN, CLK $\le V_{IL}$ MAX, $t_{CK} = \infty$ (see Note 6)			10	mA
I_{CC4}	Burst current	Page burst, I_{OH}/I_{OL} = 0 mA All banks activated, n_{CCD} = 1 cycle (see Note 7)	CAS latency = 2		100	mA
			CAS latency = 3		130	mA
I_{CC5}	Auto-refresh current	$t_{RC} \le t_{RC}$ MIN	CAS latency = 2		85	mA
			CAS latency = 3		95	mA
I_{CC6}	Self-refresh current	CKE $\le V_{IL}$ MAX			2	mA

NOTES: 3. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.
4. Control, DQ, and address inputs change state only twice during t_{RC}.
5. Control, DQ, and address inputs change state only once every 30 ns.
6. Control, DQ, and address inputs do not change (stable).
7. Control, DQ, and address inputs change state only once every cycle.

capacitance over recommended ranges of supply voltage and ambient temperature, f = 1 MHz (see Note 8)

PARAMETER		MIN	MAX	UNIT
$C_{i(S)}$	Input capacitance, CLK		4	pF
$C_{i(AC)}$	Input capacitance, A0−A11, $\overline{CS}$, DQM, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		5	pF
$C_{i(E)}$	Input capacitance, CKE		5	pF
C_o	Output capacitance		6.5	pF

NOTE 8: V_{CC} = 3.3 ± 0.3 V and bias on pins under test is 0 V.

ac timing requirements† ‡

		’626812A-10		UNIT
		MIN	MAX	
t_{CK2}	Cycle time, CLK, CAS latency = 2	15		ns
t_{CK3}	Cycle time, CLK, CAS latency = 3	10		ns
t_{CH}	Pulse duration, CLK high	3		ns
t_{CL}	Pulse duration, CLK low	3		ns
t_{AC2}	Access time, CLK high to data out, CAS latency = 2 (see Note 9)		7	ns
t_{AC3}	Access time, CLK high to data out, CAS latency = 3 (see Note 9)		7	ns
t_{OH}	Hold time, CLK high to data out	3		ns
t_{LZ}	Delay time, CLK high to DQ in low-impedance state (see Note 10)	2		ns
t_{HZ}	Delay time, CLK high to DQ in high-impedance state (see Note 11)		8	ns
t_{IS}	Setup time, address, control, and data input	3		ns
t_{IH}	Hold time, address, control, and data input	1		ns
t_{CESP}	Power-down/self-refresh exit time (see Note 12)	10		ns
t_{RAS}	Delay time, ACTV command to DEAC or DCAB command	50	100 000	ns
t_{RC}	Delay time, ACTV, REFR, or SLFR exit to ACTV, MRS, REFR, or SLFR command	80		ns
t_{RCD}	Delay time, ACTV command to READ, READ-P, WRT, or WRT-P command (see Note 13)	30		ns
t_{RP}	Delay time, DEAC or DCAB command to ACTV, MRS, REFR, or SLFR command	30		ns
t_{RRD}	Delay time, ACTV command in one bank to ACTV command in the other bank	20		ns
t_{RSA}	Delay time, MRS command to ACTV, MRS, REFR, or SLFR command	20		ns
t_{APR}	Final data out of READ-P operation to ACTV, MRS, SLFR, or REFR command	$t_{RP} - (CL - 1) * t_{CK}$		ns

† See Parameter Measurement Information for load circuits.
‡ All references are made to the rising transition of CLK, unless otherwise noted.

NOTES: 9. t_{AC} is referenced from the rising transition of CLK that precedes the data-out cycle. For example, the first data-out t_{AC} is referenced from the rising transition of CLK0 that is CAS latency minus one cycle after the READ command. Access time is measured at output reference level 1.4 V.
10. t_{LZ} is measured from the rising transition of CLK that is CAS latency minus one cycle after the READ command.
11. t_{HZ} MAX defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.
12. See Figure 18 and Figure 19.
13. For read or write operations with automatic deactivate, t_{RCD} must be set to satisfy minimum t_{RAS}.

ac timing requirements†‡ (continued)

		’626812A-10		UNIT
		MIN	MAX	
t_{APW}	Final data in of WRT-P operation to ACTV, MRS, SLFR, or REFR command	$t_{RP} + t_{CK}$		ns
t_{WR}	Delay time, final data in of WRT operation to DEAC or DCAB command	10		ns
t_T	Transition time (see Note 14)	1	5	ns
t_{REF}	Refresh interval		64	ms
n_{CCD}	Delay time, READ or WRT command to an interrupting command	1		cycle
n_{CDD}	Delay time, $\overline{CS}$ low or high to input enabled or inhibited	0	0	cycle
n_{CLE}	Delay time, CKE high or low to CLK enabled or disabled	1	1	cycle
n_{CWL}	Delay time, final data in of WRT operation to READ, READ-P, WRT, WRT-P	1		cycle
n_{DID}	Delay time, ENBL or MASK command to enabled or masked data in	0	0	cycle
n_{DOD}	Delay time, ENBL or MASK command to enabled or masked data out	2	2	cycle
n_{HZP2}	Delay time, DEAC or DCAB command to DQ in high-impedance state, CAS latency = 2		2	cycle
n_{HZP3}	Delay time, DEAC or DCAB command to DQ in high-impedance state, CAS latency = 3		3	cycle
n_{WCD}	Delay time, WRT command to first data in	0	0	cycle

† See Parameter Measurement Information for load circuits.
‡ All references are made to the rising transition of CLK, unless otherwise noted.
NOTE 14: Transition time, t_T, is measured between V_{IH} and V_{IL}.

PARAMETER MEASUREMENT INFORMATION

The ac timing measurements are based on signal rise and fall times equal to 1 ns (t_T = 1 ns) and a midpoint reference level of 1.4 V for LVTTL. For signal rise and fall times greater than 1 ns, the reference level should be changed to V_{IH} MIN and V_{IL} MAX instead of the midpoint level. All specifications referring to READ commands are also valid for READ-P commands unless otherwise noted. All specifications referring to WRT commands are also valid for WRT-P commands unless otherwise noted. All specifications referring to consecutive commands are specified as consecutive commands for the same bank unless otherwise noted.

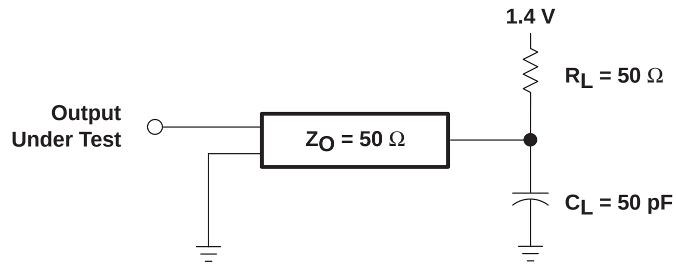


Figure 8. LVTTL-Load Circuit

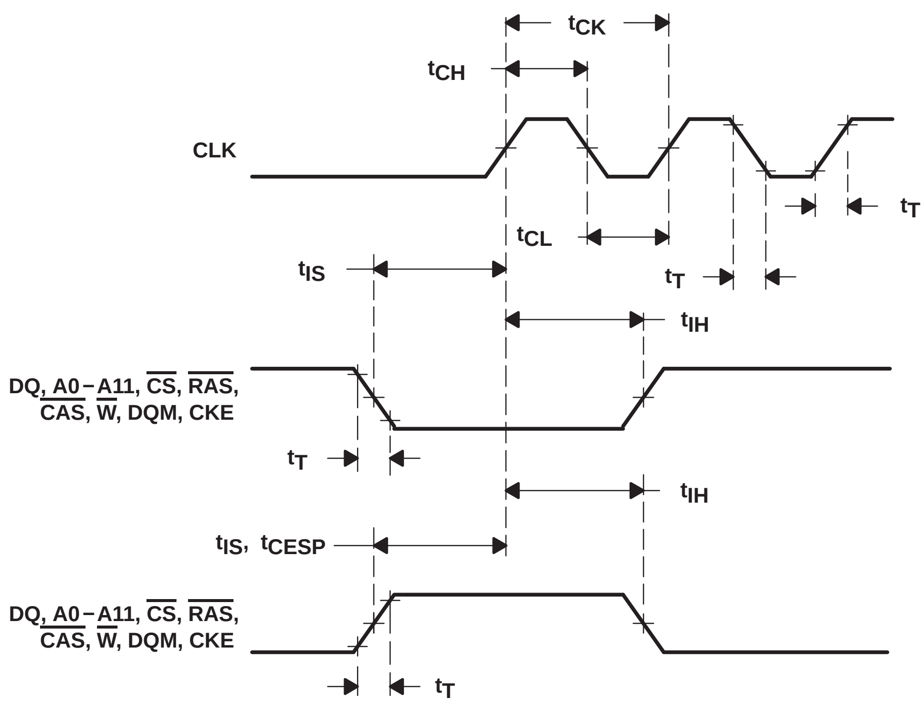


Figure 9. Input-Attribute Parameters

PARAMETER MEASUREMENT INFORMATION

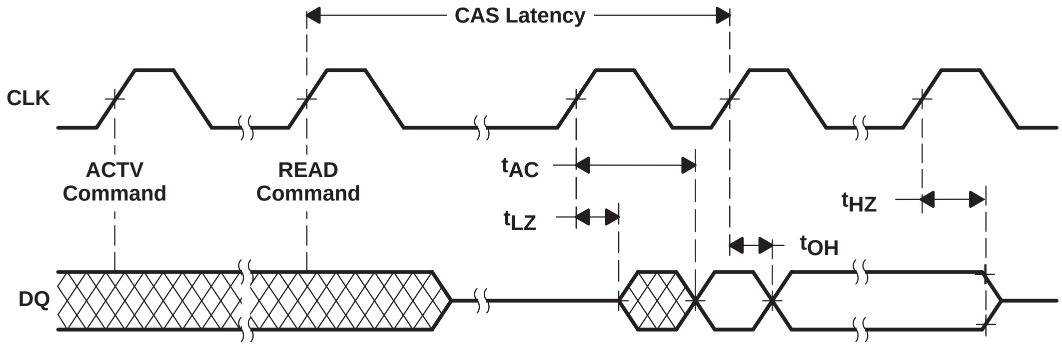


Figure 10. Output Parameters

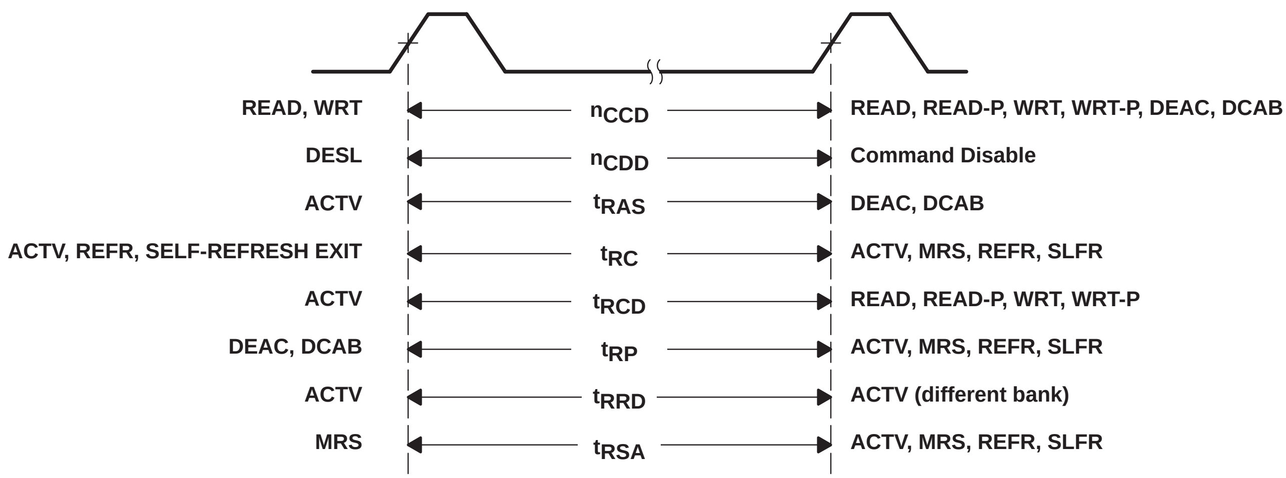
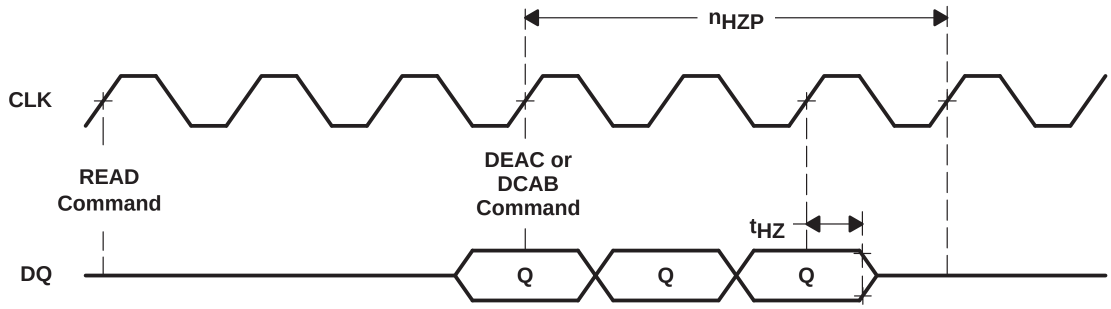


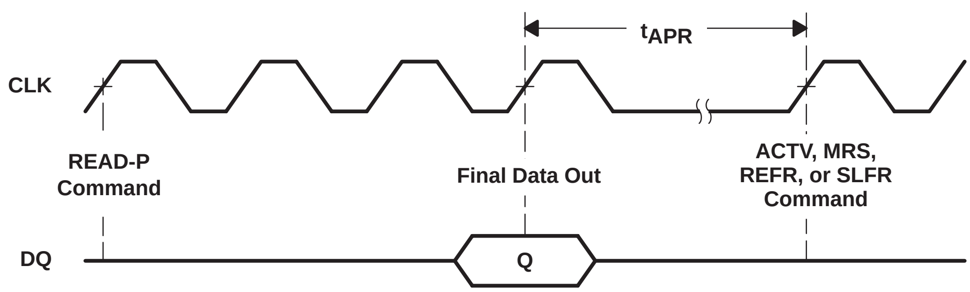
Figure 11. Command-to-Command Parameters

PARAMETER MEASUREMENT INFORMATION



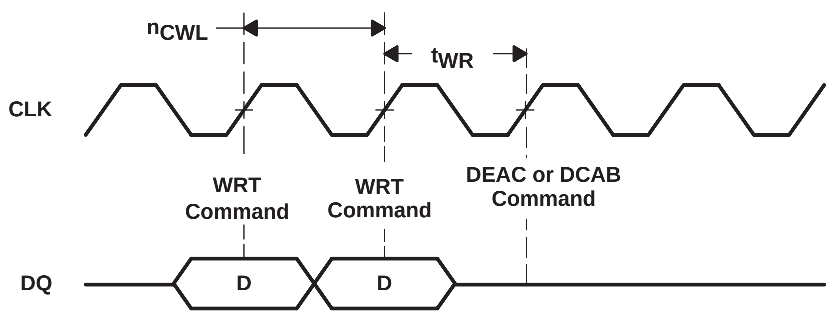
NOTE A: For this example, assume CAS latency = 3 and burst length = 4.

Figure 12. Read Followed by Deactivate



NOTE A: For this example, assume CAS latency = 3 and burst length = 1.

Figure 13. Read With Auto-Deactivate



NOTE A: For this example, assume burst length = 1.

Figure 14. Write Followed By Deactivate

PARAMETER MEASUREMENT INFORMATION

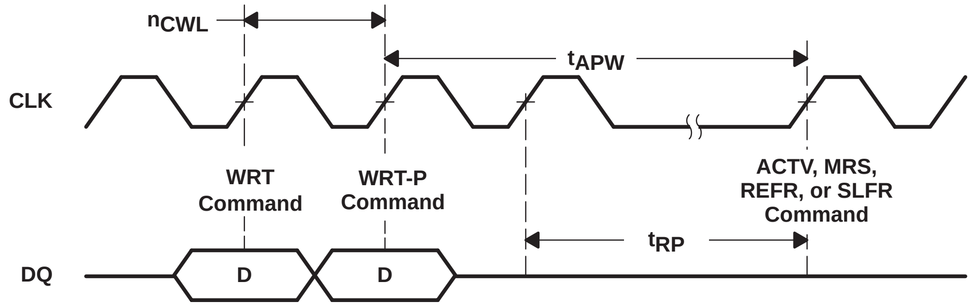
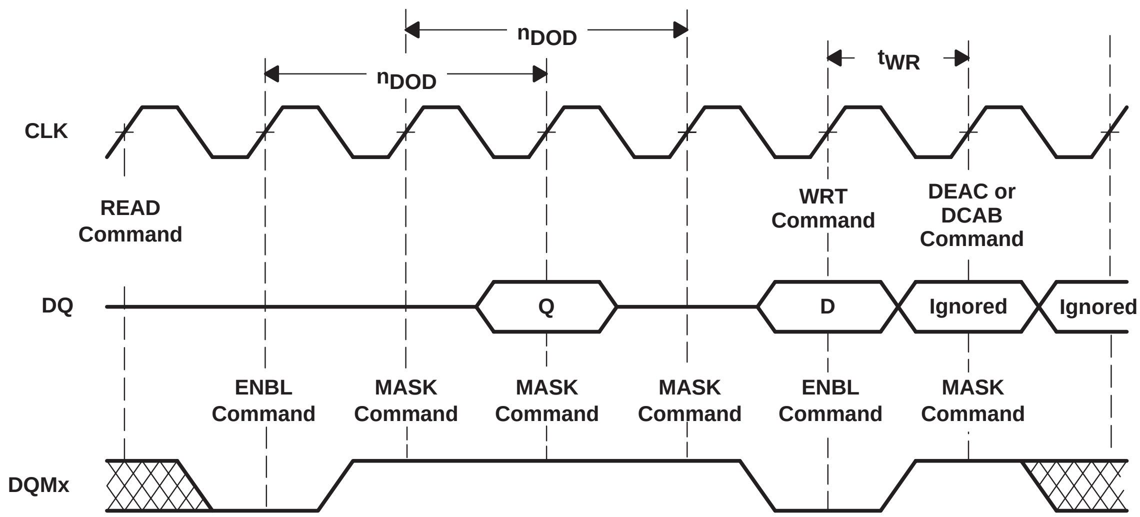


Figure 15. Write With Auto-Deactivate



NOTE A: For this example, assume CAS latency = 3 and burst length = 4.

Figure 16. DQ Masking

PARAMETER MEASUREMENT INFORMATION

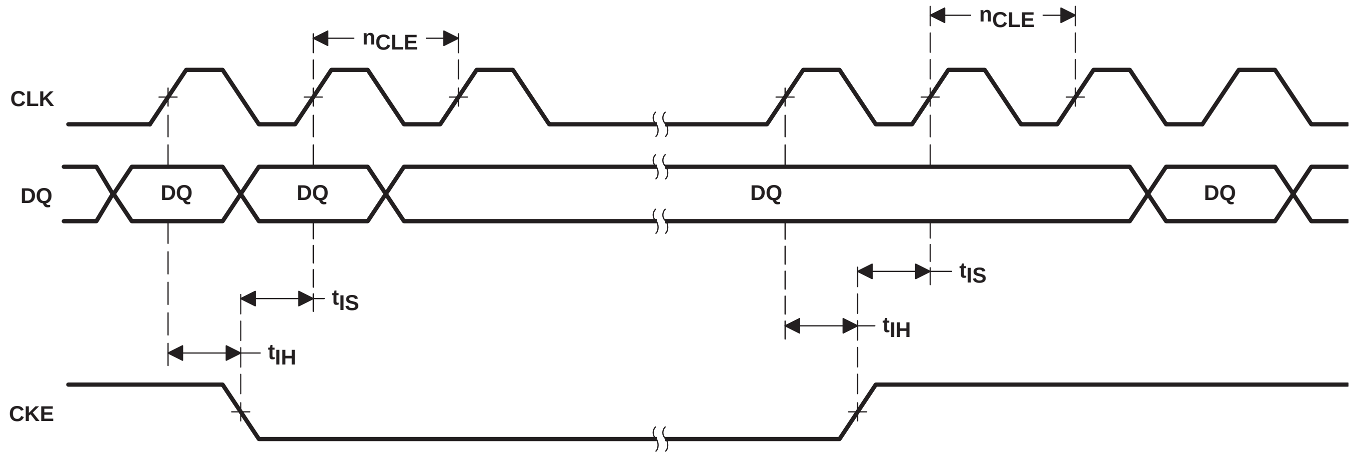


Figure 17. CLK-Suspend Operation

PARAMETER MEASUREMENT INFORMATION

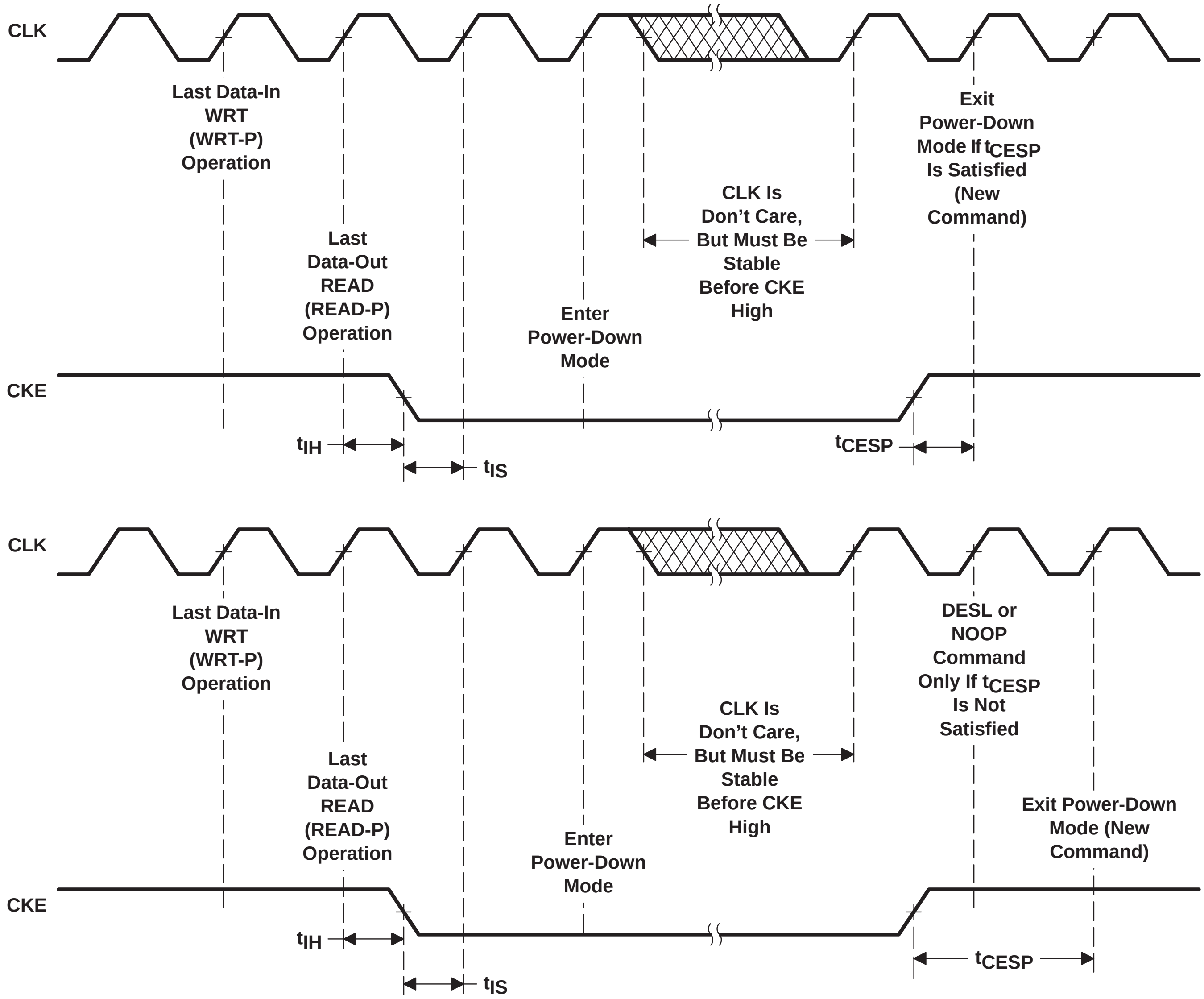


Figure 18. Power-Down Operation

PARAMETER MEASUREMENT INFORMATION

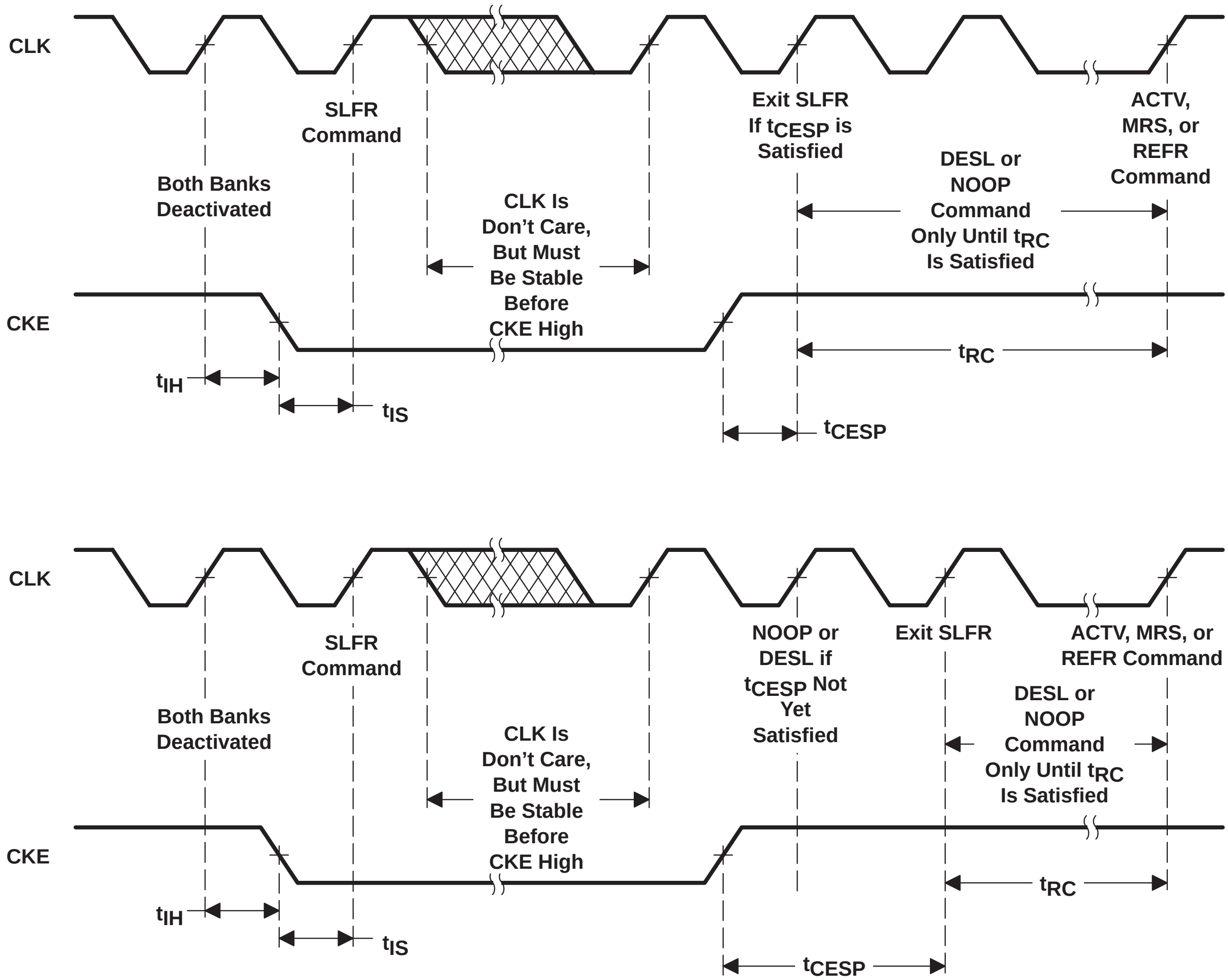
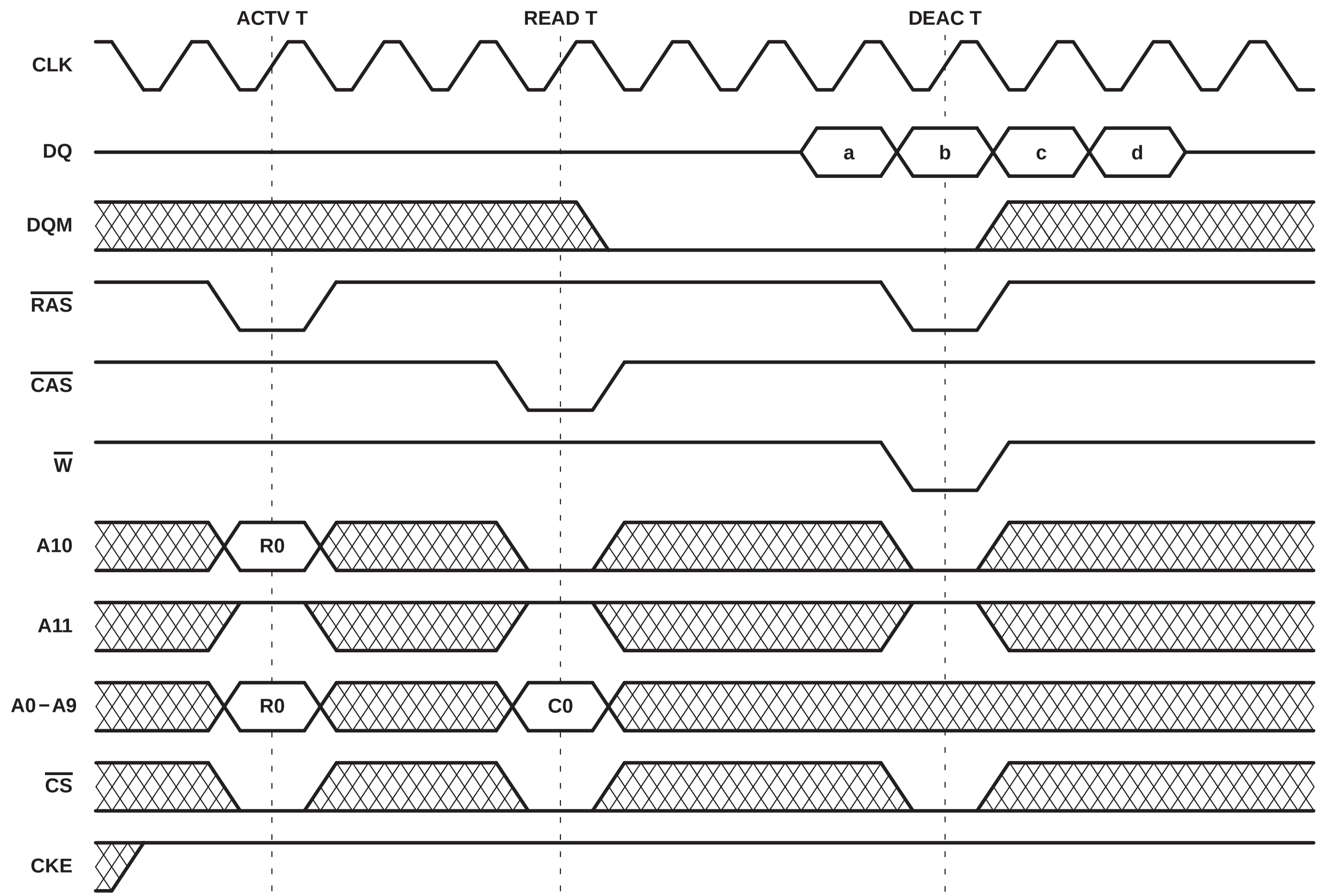


Figure 19. Self-Refresh Operation

PARAMETER MEASUREMENT INFORMATION

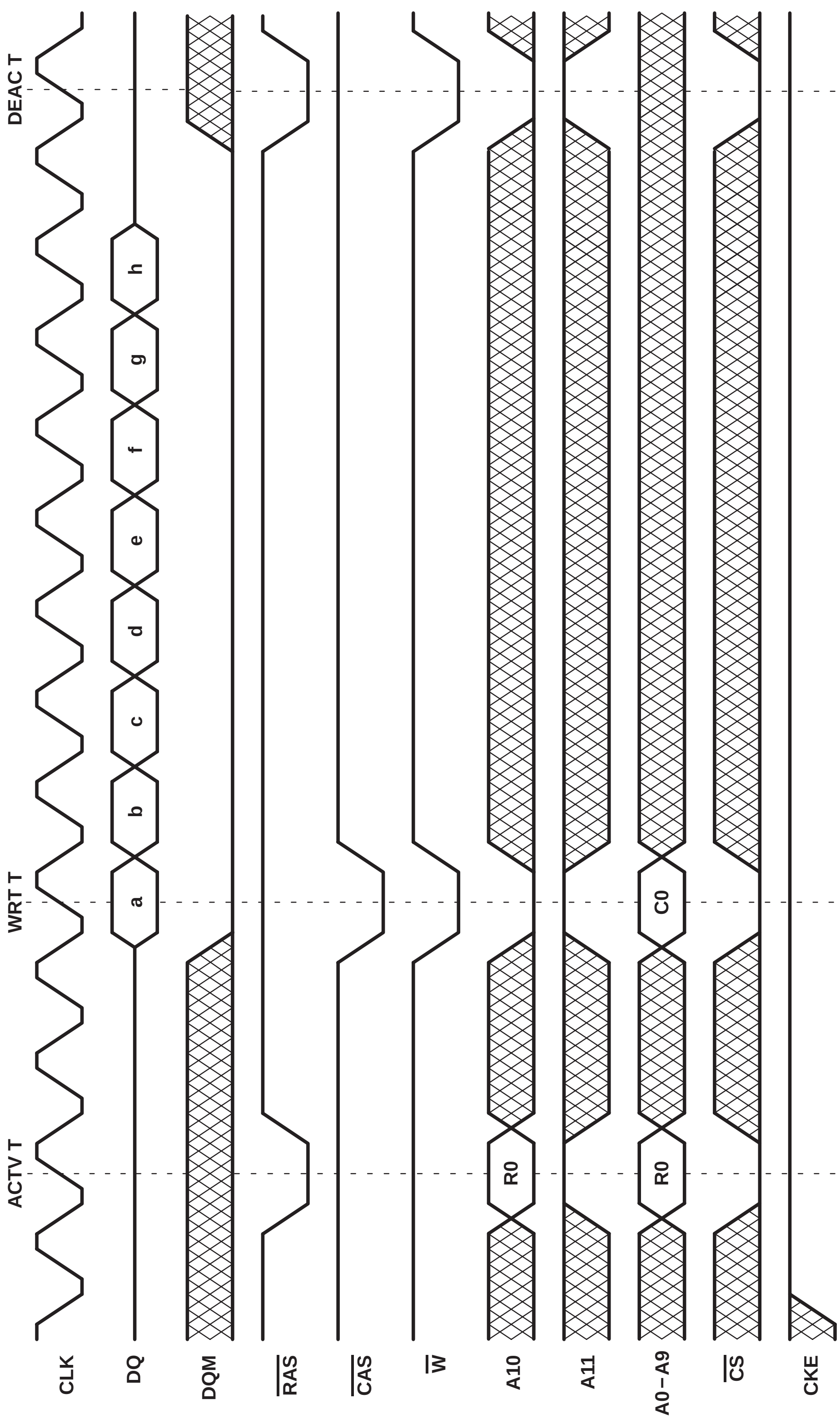


BURST TYPE (D/Q)	BANK (B / T)	ROW ADDR	BURST CYCLE† a	b	c	d
Q	T	R0	C0	C0 + 1	C0 + 2	C0 + 3

† Column-address sequence depends on programmed burst type and starting column address C0 (see Table 5).
NOTE A: This example illustrates minimum t_{RCD} for the ’626812A-10 at 100 MHz.

Figure 20. Read Burst (CAS latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION



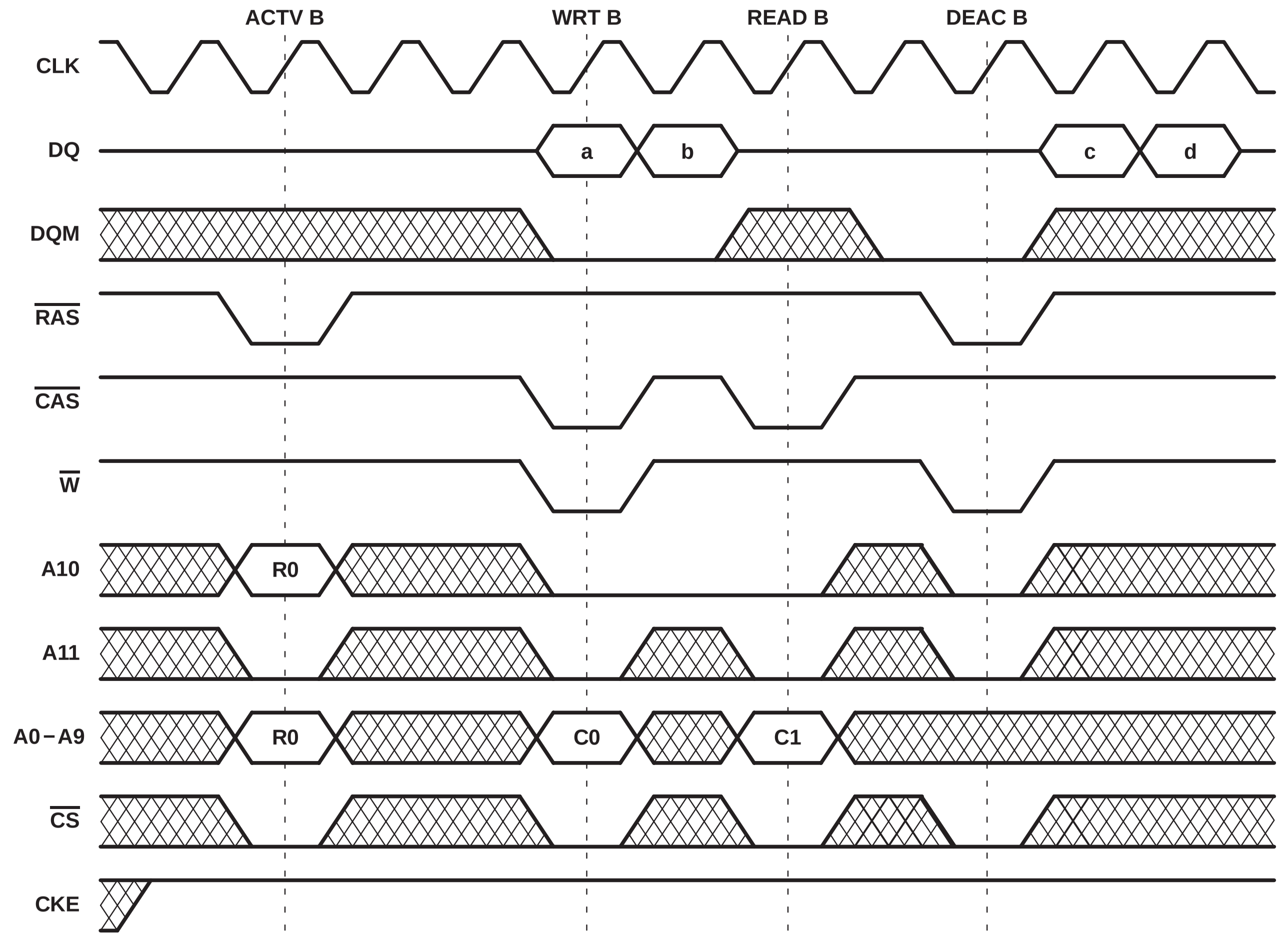
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h
D	T	R0	C0	C0 + 1	C0 + 2	C0 + 3	C0 + 4	C0 + 5	C0 + 6	C0 + 7

† Column-address sequence depends on programmed burst type and starting column address C0 (see Table 6).

NOTE A: This example illustrates minimum t_{RCD} for the ’626812A-10 at 100 MHz.

Figure 21. Write Burst (burst length = 8)

PARAMETER MEASUREMENT INFORMATION

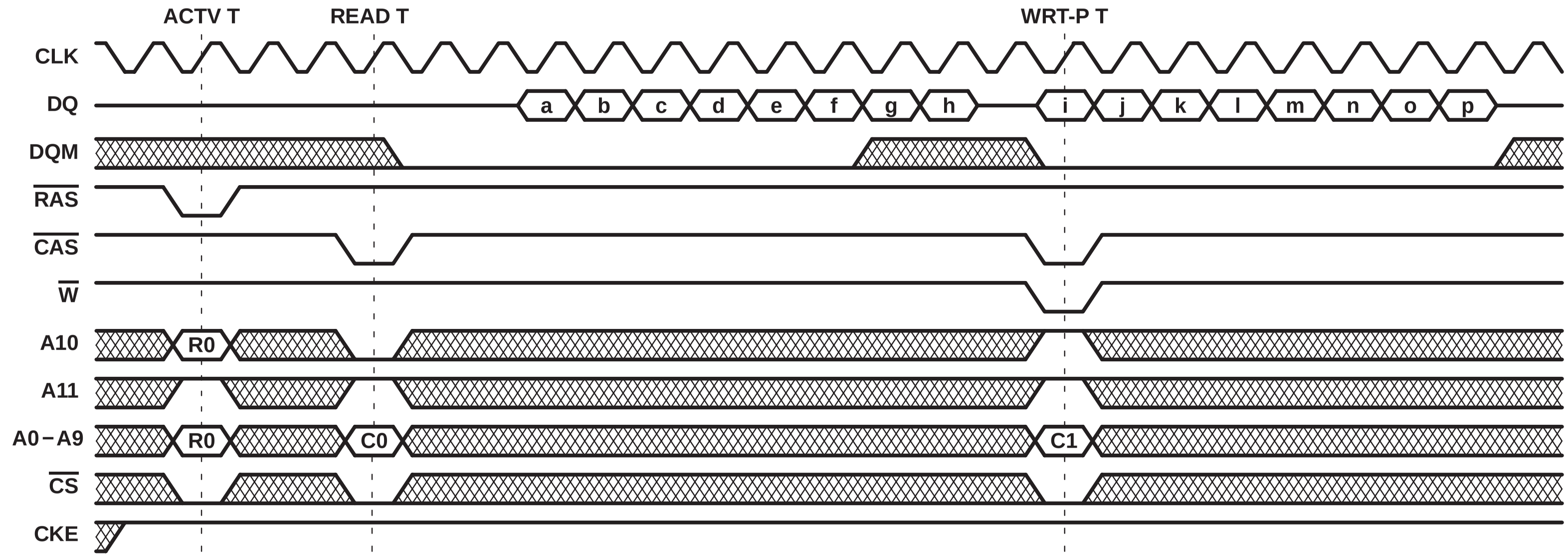


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d
D	B	R0	C0	C0 + 1		
Q	B	R0			C1	C1 + 1

† Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 4).
NOTE A: This example illustrates minimum t_{RCD} and n_{CWL} for the ’626812A-10 at 100 MHz.

Figure 22. Write-Read Burst (CAS latency = 3, burst length = 2)

PARAMETER MEASUREMENT INFORMATION



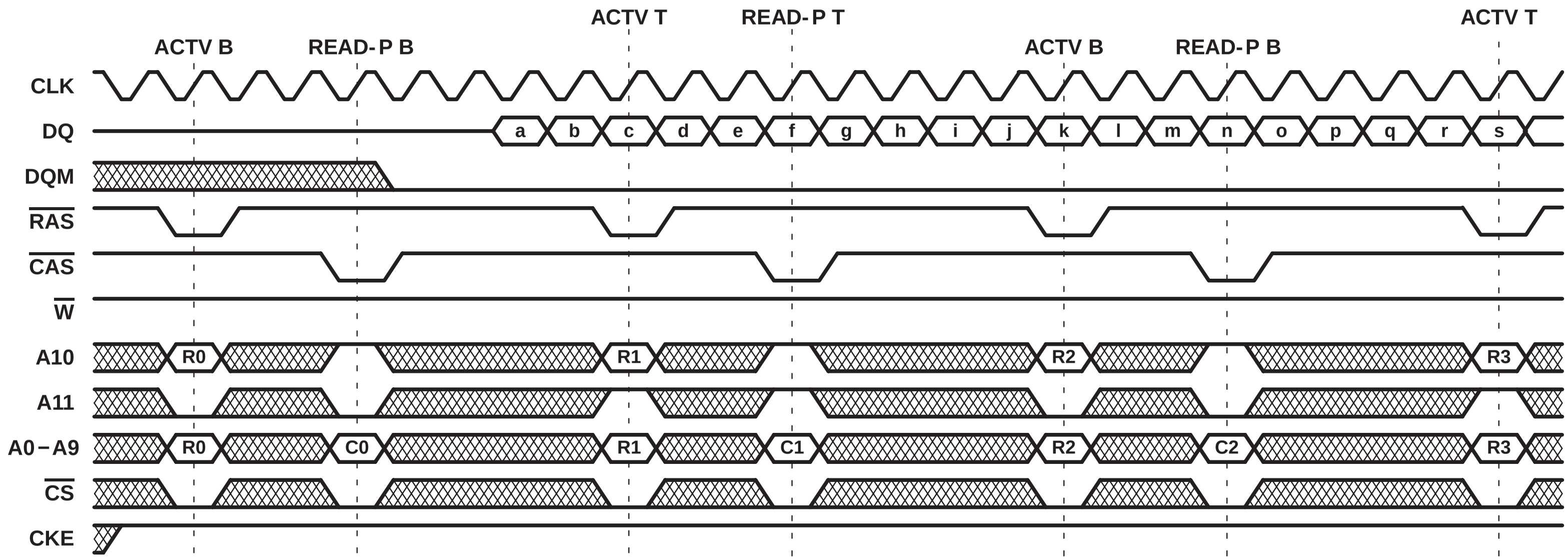
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p
Q	T	R0	C0	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7								
D	T	R0									C1	C1+1	C1+2	C1+3	C1+4	C1+5	C1+6	C1+7

† Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 6).

NOTE A: This example illustrates minimum t_{RCD} for the ’626812A-10 at 100 MHz.

Figure 23. Read-Write Burst With Automatic Deactivate (CAS latency = 3, burst length = 8)

PARAMETER MEASUREMENT INFORMATION



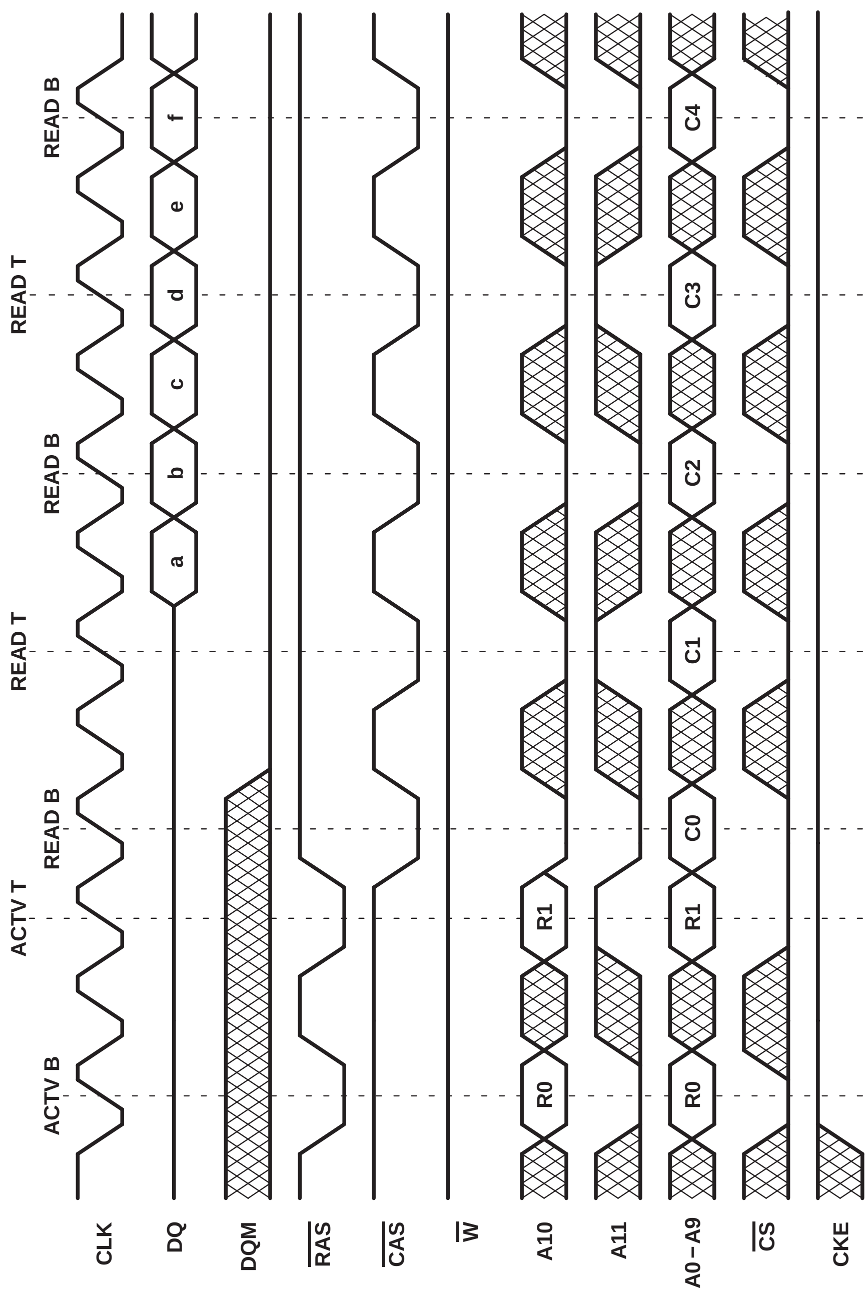
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	. .
Q	B	R0	C0	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7												
Q	T	R1									C1	C1+1	C1+2	C1+3	C1+4	C1+5	C1+6	C1+7				
Q	B	R2																	C2	C2+1	C2+2	. .

† Column-address sequence depends on programmed burst type and starting column address C0, C1, and C2 (see Table 6).

NOTE A: This example illustrates minimum t_{RCD} for the ’626812A-10 at 100 MHz.

Figure 24. Two-Bank Row-Interleaving Read Bursts With Automatic Deactivate (CAS latency = 3, burst length = 8)

PARAMETER MEASUREMENT INFORMATION

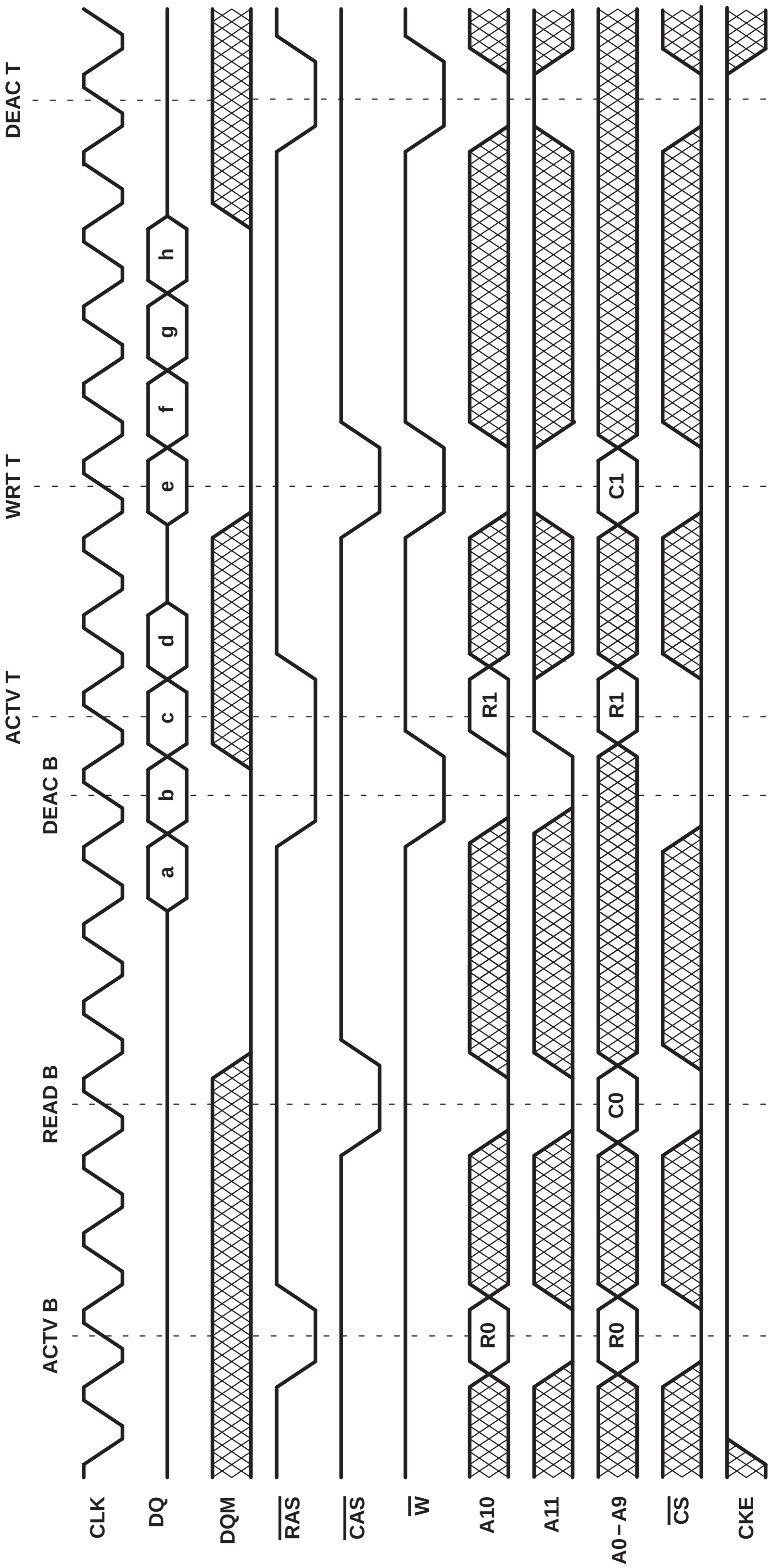


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	
Q	B	R0	C0	C0 + 1					
Q	T	R1			C1	C1 + 1			
Q	B	R0					C2	C2 + 1	
.	. . .	. . .						. . .	. . .

† Column-address sequence depends on programmed burst type and starting column addresses C0, C1 and C2 (see Table 4).

Figure 25. Two-Bank Column-Interleaving Read Bursts (CAS latency = 3, burst length = 2)

PARAMETER MEASUREMENT INFORMATION



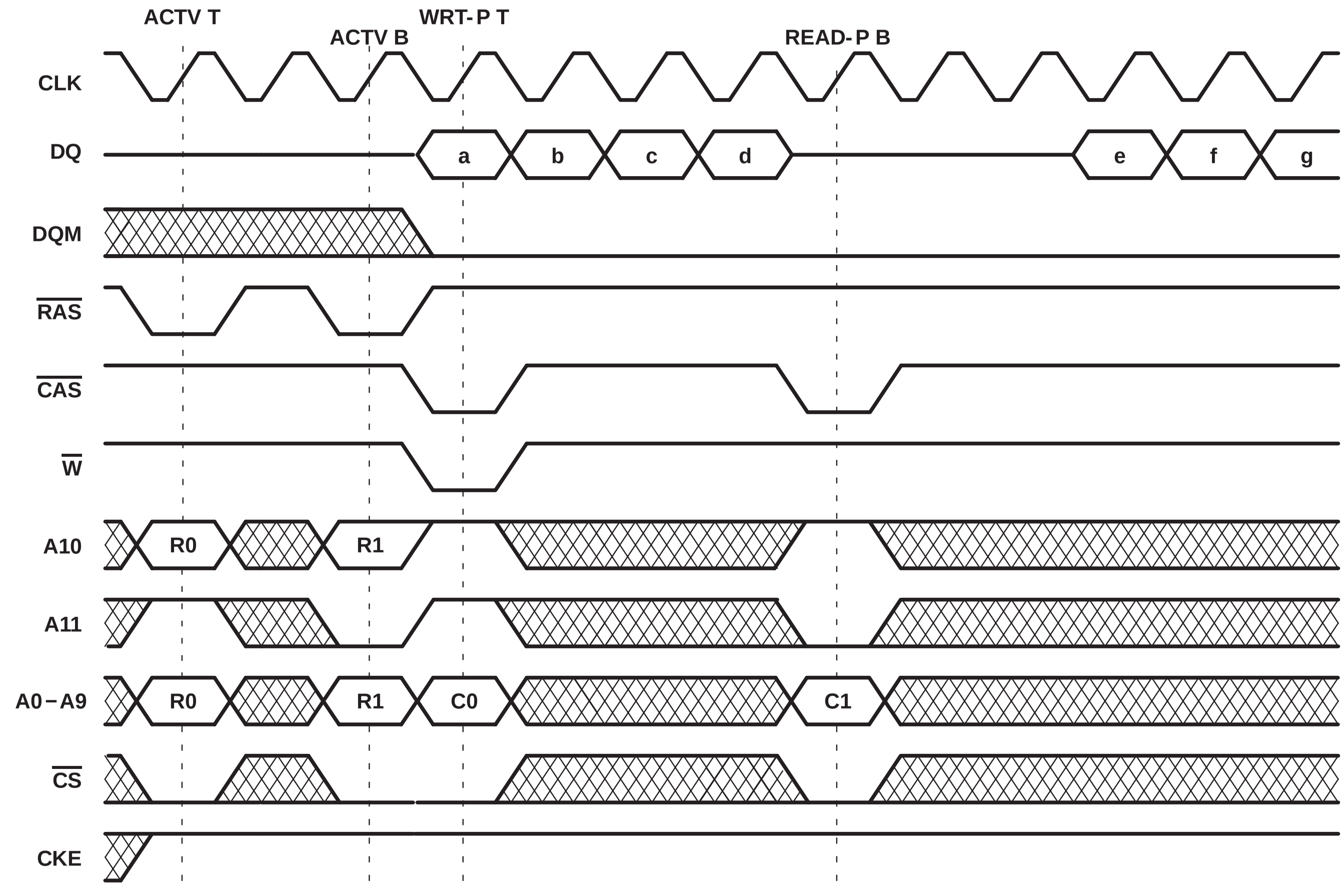
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	a	b	c	d	e	f	g	h
			BURST CYCLE†							
Q	B	R0	C0	C0 + 1	C0 + 2	C0 + 3				
D	T	R1					C1	C1 + 1	C1 + 2	C1 + 3

† Column-address sequence depends on programmed burst type and starting column addresses C0 and C1 (see Table 5).

NOTE A: This example illustrates a minimum t_{RCD} for the ′626812A-10 at 100 MHz.

Figure 26. Read-Burst Bank B, Write-Burst Bank T (CAS latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION



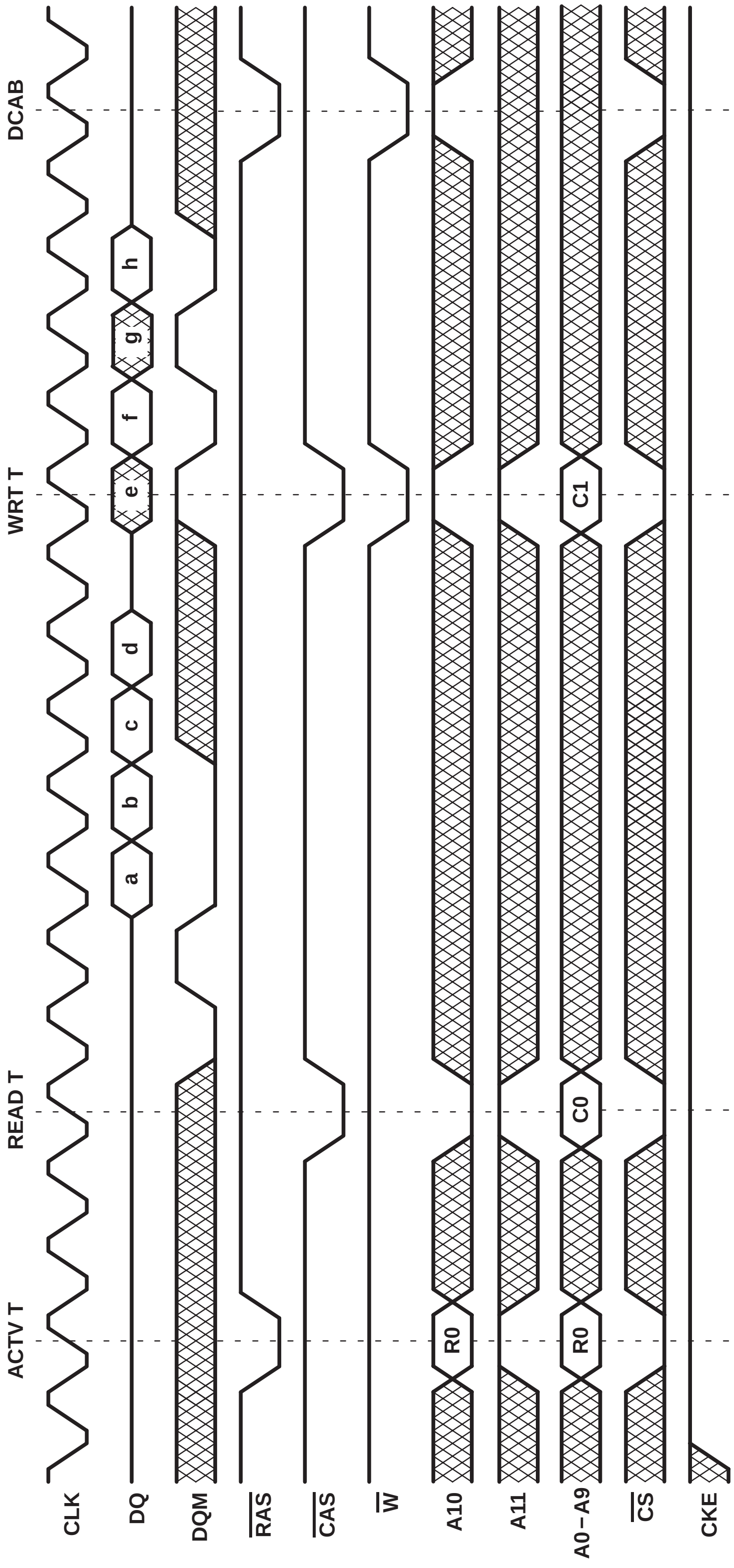
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h
D	T	R0	C0	C0 + 1	C0 + 2	C0 + 3				
Q	B	R1					C1	C1 + 1	C1 + 2	C1 + 3

† Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 5).

NOTE A: This example illustrates minimum n_{CWL} for the ’626812A-10 at 100 MHz.

Figure 27. Write-Burst Bank T, Read-Burst Bank B With Automatic Deactivate (CAS latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION



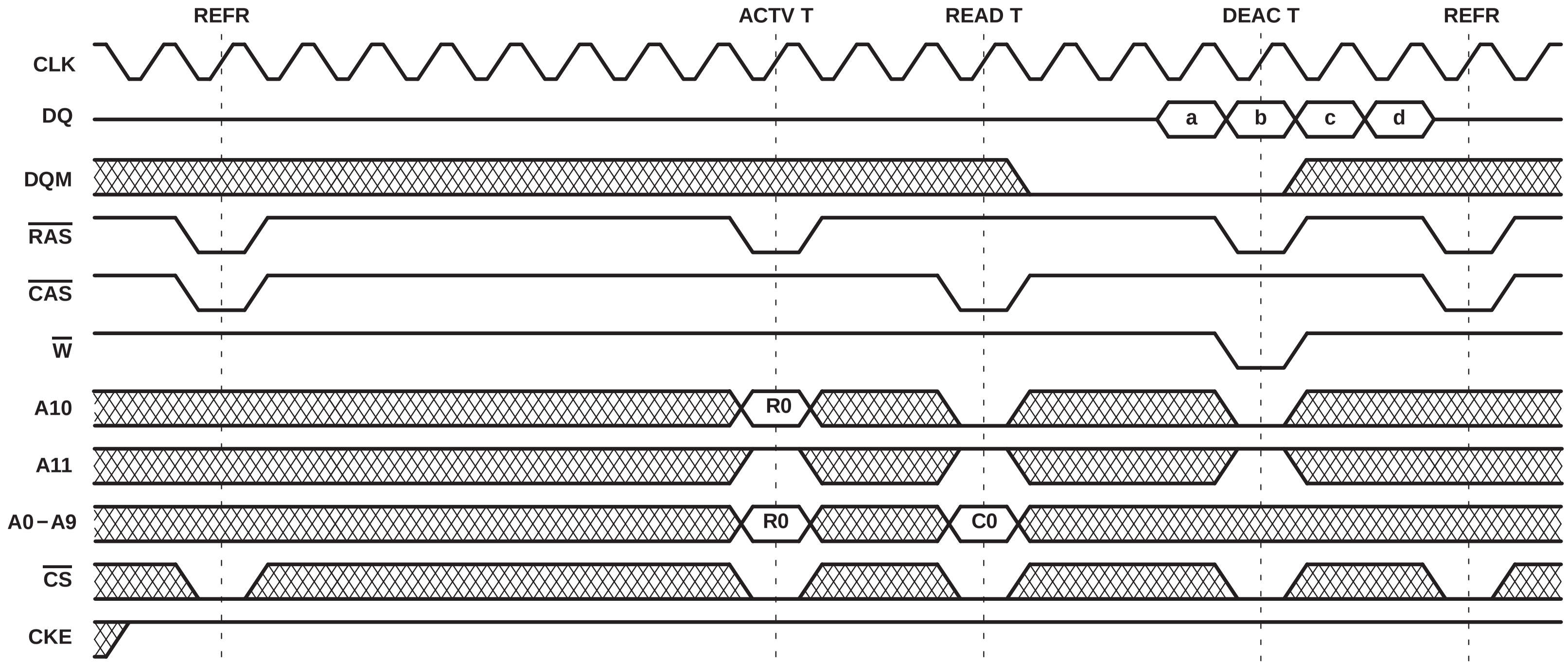
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h
Q	T	R0	C0	C0+1	C0+2	C0+3				
D	T	R1					C1	C1+1	C1+2	C1+3

† Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 5).

NOTE A: This example illustrates minimum t_{RCD} for the '626812A-10 at 100 MHz.

Figure 28. Data Mask (CAS latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION



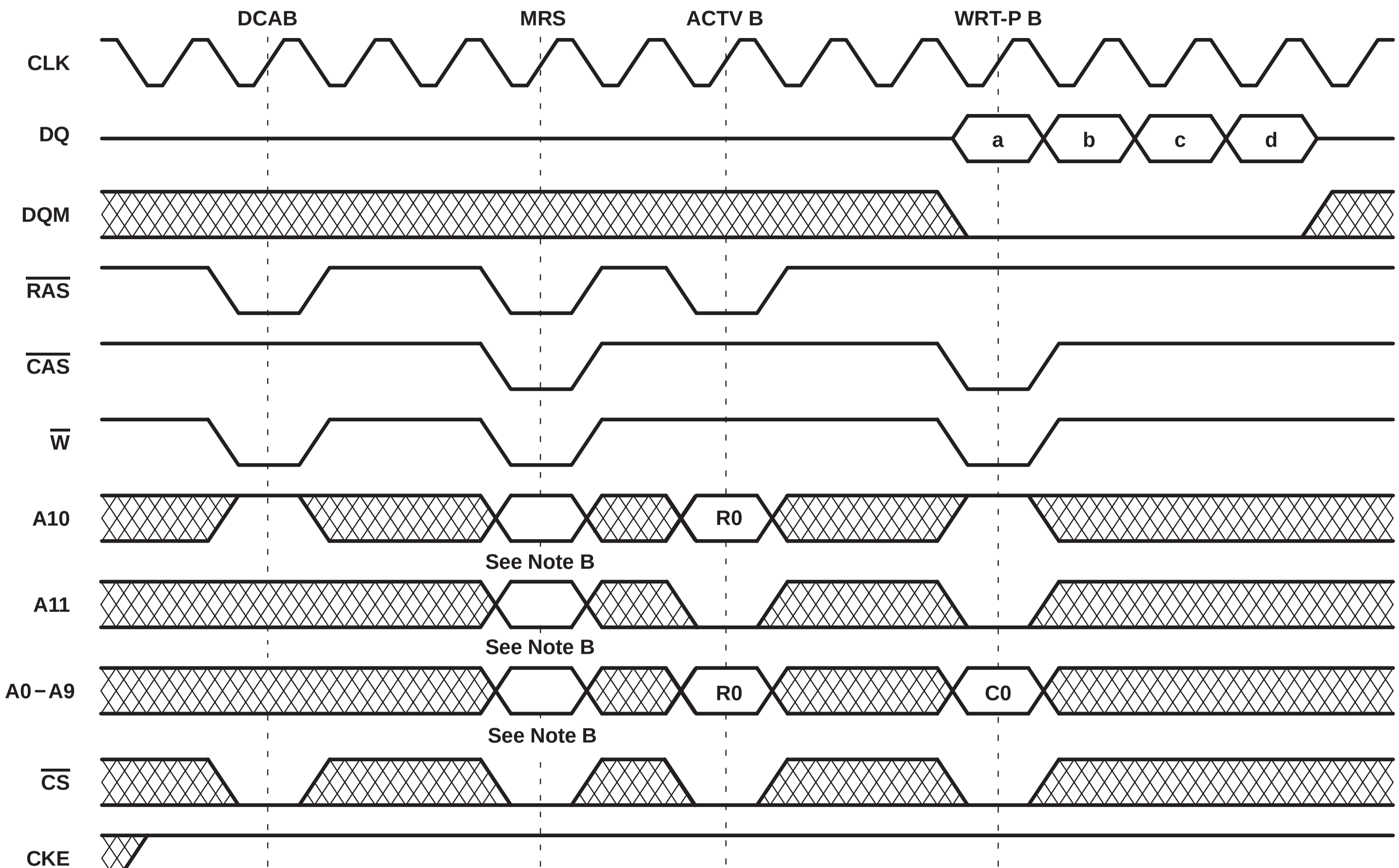
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d
Q	T	R0	C0	C0 + 1	C0 + 2	C0 + 3

† Column-address sequence depends on programmed burst type and starting column address C0 (see Table 5).

NOTE A: This example illustrates minimuim t_{RC} and t_{RCD} for the '626812A-10 at 100 MHz.

Figure 29. Refresh Cycles (CAS latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION



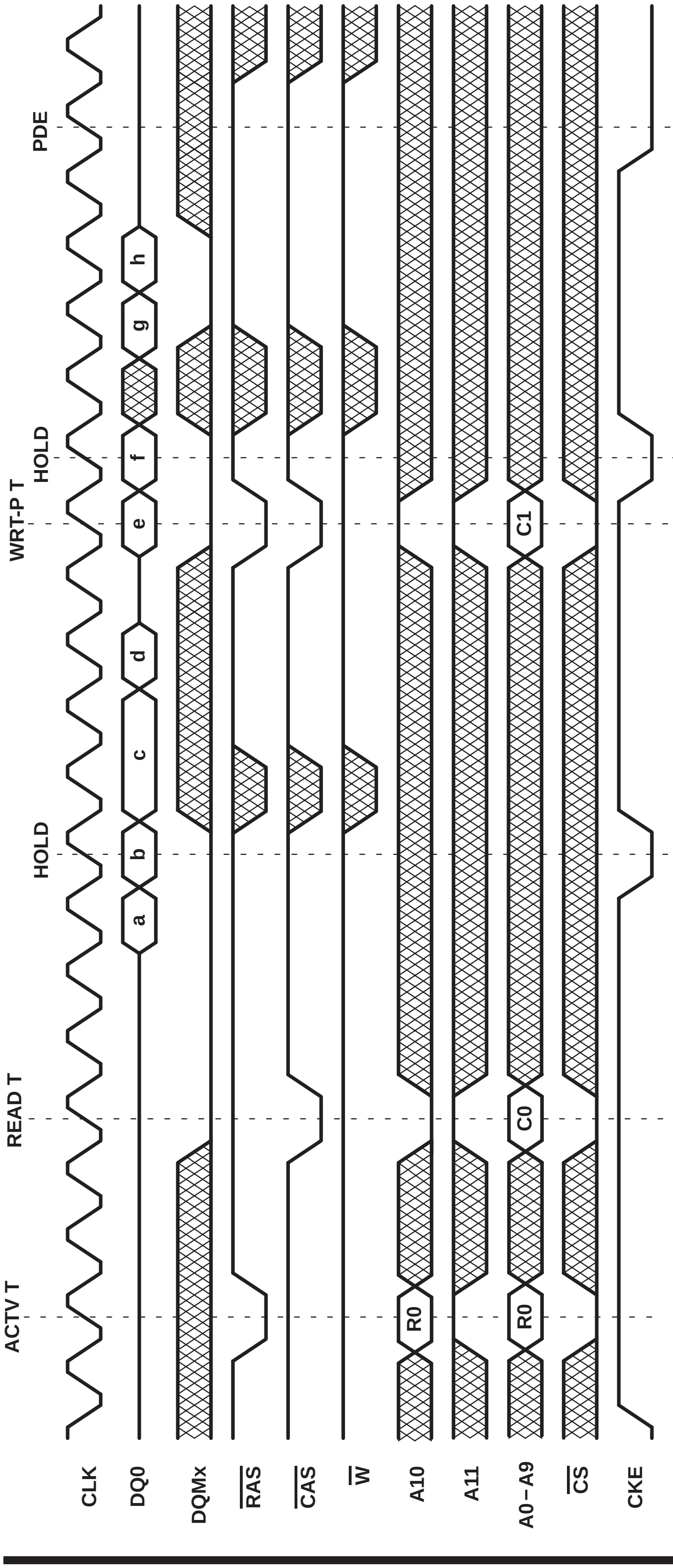
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d
D	B	R0	C0	C0 + 1	C0 + 2	C0 + 3

† Column-address sequence depends on programmed burst type and starting column address C0 (see Table 5).

NOTES: A. This example illustrates minimum t_{RP}, t_{RSA}, and t_{RCD} for the '626812A-10 at 100 MHz.
B. See Figure 1

Figure 30. Set Mode Register (deactivate all, set mode register, write burst with automatic deactivate) (burst length = 4)

PARAMETER MEASUREMENT INFORMATION

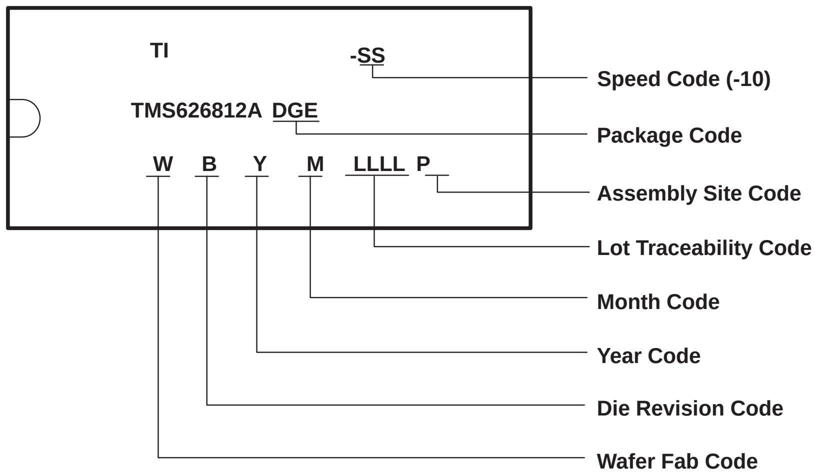


BURST-TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h
Q	T	R0	C0	C0+1	C0+2	C0+3				
D	T	R1					C1	C1+1	C1+2	C1+3

† Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 5).

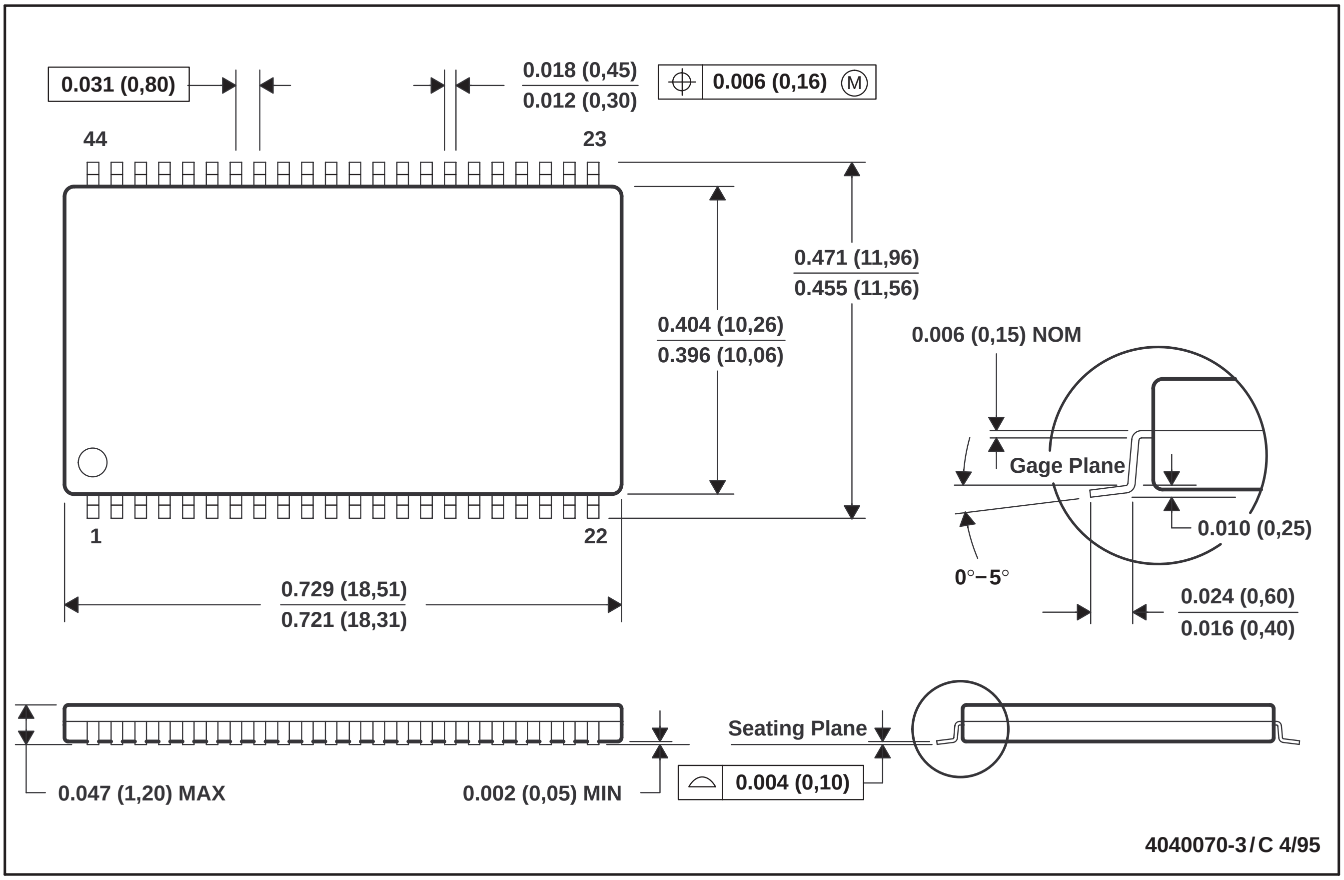
Figure 31. CLK Suspend (HOLD) During Read Burst and Write Burst (CAS latency = 3, burst length = 4)

device symbolization



MECHANICAL DATA

DGE (R-PDSO-G44) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

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