5. TMS9918A/9928A/9929A ELECTRICAL SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (unless otherwise noted)*

Supply voltage, V_{CC} ..... −0.3 to 20 V
All input voltages ..... −0.3 to 20 V
Output voltage ..... −2 to 7 V
Continuous power dissipation ..... 1.3 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −55°C to +150°C

*Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions section of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

5.2 RECOMMENDED OPERATING CONDITIONS*

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75		5.25	V
Supply voltage, V_{SS}			0		V
Input Voltage, V_I, $\overline{\text{RESET}}$/SYNC pin	SYNC active	10		12	V
	RESET active			0.6	V
	SYNC and RESET inactive	3		6	V
High-level input, V_{IH}	XTAL1, XTAL2	2.75			V
	All other inputs	2.2			V
Input voltage, V_I, EXT VDP pin (TMS9918A only)	SYNC level		2.6		V
	White level		3.7		V
	Black level		3		V
Low-level input voltage, V_{IL}				0.8	V
Operating free-air temperature, T_A		0		70	°C

* All voltage values are with respect to V_{SS}.

5.3 ELECTRICAL CHARACTERISTICS OVER FULL RANGES OF RECOMMENDED OPERATING CONDITION (unless otherwise noted)

TMS9918A/9928A/9929A

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$\overline{RAS}$, $\overline{CAS}$, R/$\overline{W}$	I_{OH} = 400 μA	2.7	3.4		V
		All other outputs		2.4	3.2		
V_{OL}	Low-level output voltage	CPU data	I_{OL} = 1.2 mA		0.3	0.6	V
		DRAM interface	I_{OL} = 800 μA			0.6	
I_{OZH}	Off-state output current high-level voltage applied, D0-D7 outputs		V_O = 5.25 V		1	100	μA
I_{OZL}	Off-state output current high-level voltage applied, D0-D7 outputs		V_O = 0.4 V		1	-100	μA
I_{IH}	High-level input current		V_I = 5.25 V, all other pins at 0 V			10	μA
I_{IL}	Low-level input current		V_I = 0 V, All other pins at 0 V			-10	μA

TMS9918A Only (Figure 5-1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{white}	Video voltage level of white, COMVID	R_L = 470 Ω	2.8	3.0	3.2 V	
V_{black}	Video voltage level of black (blank), COMVID		2.1	2.3	2.5 V	
V_{sync}	Video voltage level of sync, COMVID		1.85	2.0	2.1 V	

† All typical values are at V_{CC} = 5.25 V, T_A = 25°C.

5.3 ELECTRICAL CHARACTERISTICS OVER FULL RANGES OF RECOMMENDED OPERATING CONDITIONS (unless otherwise noted) (Continued)

TMS9928A/9929A Only (Figure 5-1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{white}	Video voltage level of white, Y, R-Y, B-Y outputs	R_L = 470 Ω	2.5	3	3.6	V
V_{black}	Video voltage level of black (blank), Y, R-Y, B-Y outputs		1.6	2.3	2.5	V
V_{sync}	Video voltage level of sync, Y output		1.2	1.8	2	V

TMS9929A Only

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PS}	Color burst video voltage level with respect to V no color	R-Y output		0.25		V
V_{neg}	Color burst video voltage level with respect to V no color	B-Y output		-0.25		V

TMS9918A/9928A/9929A (Figure 5-2)

PARAMETER			TEST CONDITIONS	MIN	NOM	MAX	UNIT
	Video voltage difference, white-black, Y, R-Y, B-Y outputs			0.7	1.0		V
I_{CC}	Average supply current from V_{CC}		T_A = 25°C		200	250	mA
C_i	Input capacitance	D0-D7	unmeasured f = 11 MHz, pins at 0 V			20	pF
		All other inputs				10	
						10	
C_o	Output capacitance		unmeasured f = 11 MHz, pins at 0 V			20	pF

† All typical values are at V_{CC} = 5.25 V, T_A = 25°C.

5.4 TIMING REQUIREMENTS OVER FULL RANGES OF RECOMMENDED OPERATING CONDITIONS (TMS9918A/9928A/9929A)

CPU - VDP Interface (Figures 5-3 and 5-4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{su(A-RL)}$	Address setup time before CSR low		0		ns
$t_{su(A-WL)}$	Address setup time before CSW low		30		ns
$t_{h(WL-A)}$	Address hold time after CSW low		30		ns
$t_{su(D-WH)}$	Data setup time before CSW high		100		ns
$t_{h(WH-D)}$	Data hold time after CSW high		30		ns
$t_{w(WL)}$	Pulse width, CSW low		200		ns
$t_{w(CS-H1)}$	Pulse width, chip select high (requesting memory access)		8		μs
$t_{w(CS-H2)}$	Pulse width, chip select high (not requesting memory access)		2		μs

VDP-VRAM Interface (Figure 5-5 and 5-6)

PARAMETER		MIN	NOM	MAX	UNIT
t_c	Memory read or write cycle time	372			ns
$t_{su(D-CH)}$	Input data setup time before CAS high	60			ns
$t_{h(CH-D)}$	Input data hold time after CAS high	0			ns

External Clock Source (Figure 5-7)

PARAMETER		MIN	TYP	MAX	UNIT
f_{ext}	External source frequency	10.738098	10.738635	10.739172	MHz
t_r/t_f	External source rise/fall time		10	15	ns
t_{wH}	External source high-level pulse width	42	47	52	ns
t_{wL}	External source low-level pulse width	42	47	52	ns
t_{pD}	External source phase delay from XTAL1 falling edge to XTAL2 falling edge	42	47	52	ns

5.5 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (TMS9918A/9928A/9929A)

CPU-VDP Interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{A(CSR)}$	Data access time from CSR low	C_L = 300 pF		100	150	ns
t_{PVX}	Data disable time after CSR high			65	100	ns
$t_{PVX,A}$	Data invalid time from address changes			0		ns
f_{CPUCLK}	CPU clock output clock frequency (f_{ext} ÷ 3)		3.4	3.58	3.76	MHz
$f_{GROMCLK}$	GROM clock output clock frequency (f_{ext} ÷ 24)		425.12	447.5	469.88	kHz

VDP-VRAM Interface (Figures 5-5 and 5-6)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_W	Pulse width, $\overline{CAS}$ high	C_L = 50 pF	80	100	120	ns
$t_{W(CL)}$	Pulse width, $\overline{CAS}$ low		220	230	250	ns
$t_{W(RH)}$	Pulse width, $\overline{RAS}$ high		100	125	150	ns
$t_{W(RL)}$	Pulse width, $\overline{RAS}$ low		190	210	230	ns
$t_{W(W)}$	Pulse width, write pulse		170	190	210	ns
t_{CA-CL}	Delay time, column address to $\overline{CAS}$ low		-10	-2		ns
t_{RA-RL}	Delay time, row address to $\overline{RAS}$ low		25	45	65	ns
t_{d-WL}	Delay time, data to R/$\overline{W}$ low		0	6	20	ns
t_{WH-CL}	Delay time, R/$\overline{W}$ high to $\overline{CAS}$ low		25	50	75	ns
t_{W-CH}	Delay time, R/$\overline{W}$ low to $\overline{CAS}$ high		120	140	160	ns
t_{W-RH}	Delay time, R/$\overline{W}$ low to $\overline{RAS}$ high		60	75	90	ns

5.5 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (TMS9918A/9928A/9929A) (Continued)

TMS9918A Composite video output (Figures 5-8 and 5-9)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CL-CA}	Column address valid after $\overline{CAS}$ low	C_L = 50 pF	45	65	85	ns
t_{RL-RA}	Row address valid after $\overline{RAS}$ low		20	25	30	ns
t_{RL-CA}	Column address valid after $\overline{RAS}$ low		95	110	130	ns
t_{CL-D}	Data valid after $\overline{CAS}$ low		240	260	280	ns
t_{RL-D}	Data valid after $\overline{RAS}$ low		95	110	125	ns
t_{WL-D}	Data valid after R/$\overline{W}$ low		135	165	195	ns
t_{CH-WL}	Read command valid after $\overline{CAS}$ high		0			ns
t_{CL-W}	Write command valid after $\overline{CAS}$ low		270	290	310	ns
t_{CH-RL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		45	65		ns
t_{CL-RH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high		150	170	190	ns
t_{RL-CL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low		30	40	50	ns

5.5 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (TMS9918A/9928A/9929A) (Continued)

TMS9918A Composite video output (Figures 5-8 and 5-9)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{fl}	Fall time, V_{black} to V_{sync}	R_L = 470 Ω C_L = 150 pF		10		ns
$t_{w(HS)}$	Pulse width, horizontal sync			4.84		µs
t_{rl}	Rise time, V_{sync} to V_{black}			20		ns
t_{HS-CD}	Delay time, sync to color burst			372		ns
$t_{w(CB)}$	Width, color burst			261		µs
t_{CB-LB}	Delay time, color burst to left border			1.49		µs
t_{r2}	Rise time, V_{black} to V_{white}			60		ns
$t_{w(LB)}$	Left border video width			2.42		µs
t_{f2}	Fall time, V_{white} to V_{black}			110		ns
$t_{w(AD)}$	Width of active display area			47.68		µs
$t_{w(RB)}$	Right border video width			2.79		µs
t_{RB-HS}	Delay time, right border to horizontal sync			1.49		µs µs
t_{VFB}	Vertical front blanking			191.1		µs
t_{VS}	Vertical sync			191.1		µs
V_{VBB}	Vertical back blanking			828		µs
t_{ABA}	Active plus border area time			18.8		ms

NOTE: Fall times depend on external pull-down resistor

5.5 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (TMS9918A/9928A/9929A) (Continued)

TMS9928A/9929A Y, R-Y, B-Y outputs (Figures 5-10 through 5-13)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{f3}	Fall time, V_{black} to V_{sync}	R_L = 470 Ω C_L = 15 pF		100		ns
$t_{w(HSI)}$	Pulse width, horizontal sync			4.84		µs
t_{r3}	Rise time, V_{sync} to V_{black}			150		ns
$t_{w(BP)}$	Width, back porch			4.47		µs
$t_{w(LBI)}$	Width, left border			2.8		µs
$t_{w(P)}$	Pulse width, pixel			186.24		ns
$t_{w(horz)}$	Width, horizontal line			63.695		µs
$t_{w(ADI)}$	Width, active display area			47.67		µs
t_{r4}	Rise time, V_{black} to V_{white}			75		ns
t_{r4}	Fall time, V_{white} to V_{black}			50		ns
$t_{w(RBI)}$	Width, right border			2.42		µs
$t_{w(FP)}$	Width, front porch			1.49		µs
t_{r5}	Rise time, V no color to V pos CB			150		ns
$t_{w(CB1)}$	Pulse width, pos color burst			2.6		µs
t_{f5}	Fall time, V pos CB to V no color			100		ns
$t_{w(CB-LBI)}$	Delay time, pos CB to left border			1.49		µs
t_{f6}	Fall time, V no color to V neg CB			100		ns
t_{r6}	Rise time, V neg CB to V no color			150		ns
$t_{w(VSI)}$	Pulse width, vertical sync			465		ns
t_{VFBI}	Vertical front blanking			191.09		µs
t_{VSI}	Vertical sync			191.09		µs
t_{VBBI}	Vertical back blanking			828.04		µs
t_{ABAI}	Active area plus border area total			18.70		mS
	Vertical time			19.91		mS

NOTE: Fall times depend on external pull-down resistor.

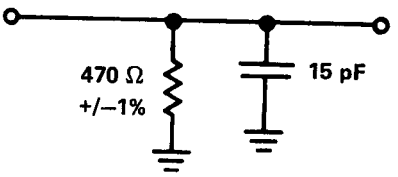


FIGURE 5-1 – LOAD CIRCUIT FOR COMVID (ALL DEVICES) AND R-Y, Y, B-Y SWITCHING CHARACTERISTICS (TMS9928A/9929A)

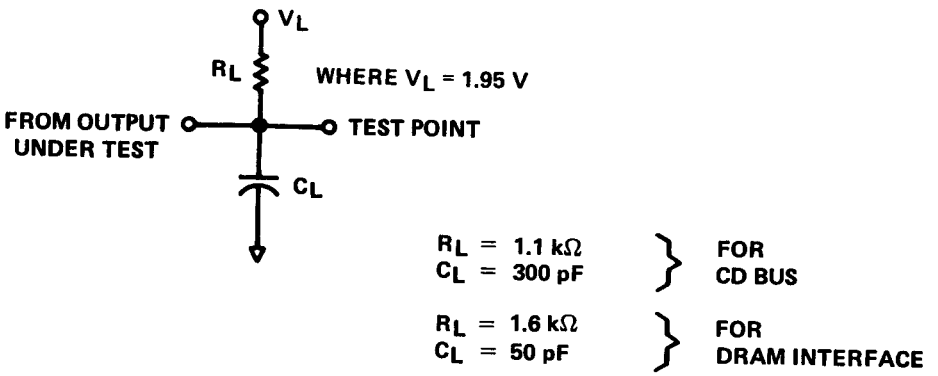


FIGURE 5-2 – LOAD CIRCUITS FOR ALL OUTPUTS EXCEPT COMVID, R-Y, Y, B-Y

WRITE CYCLE

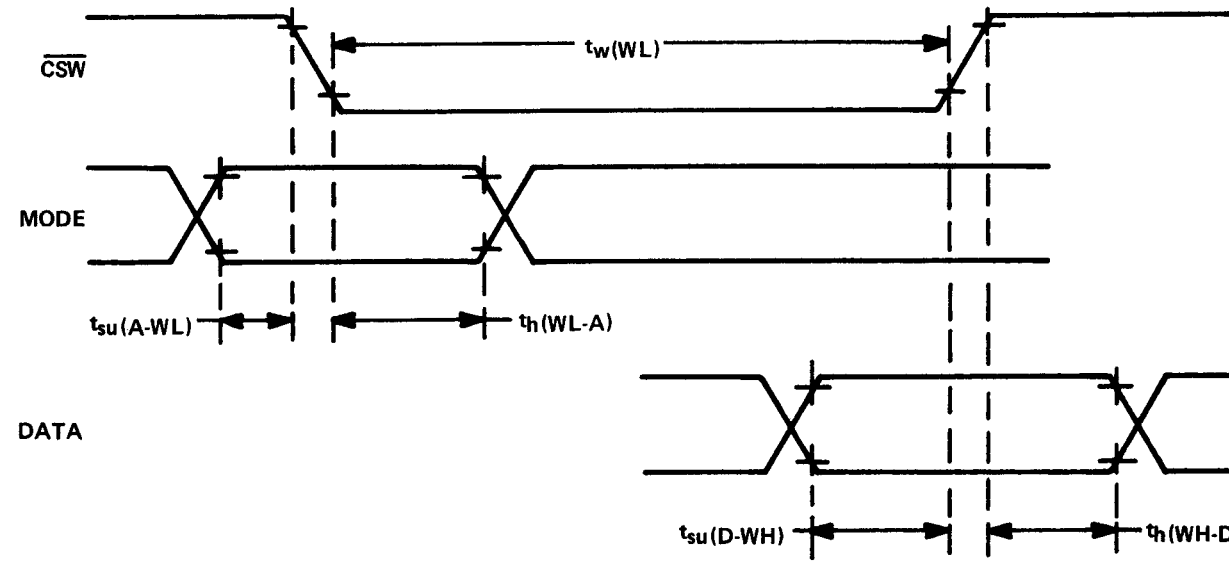
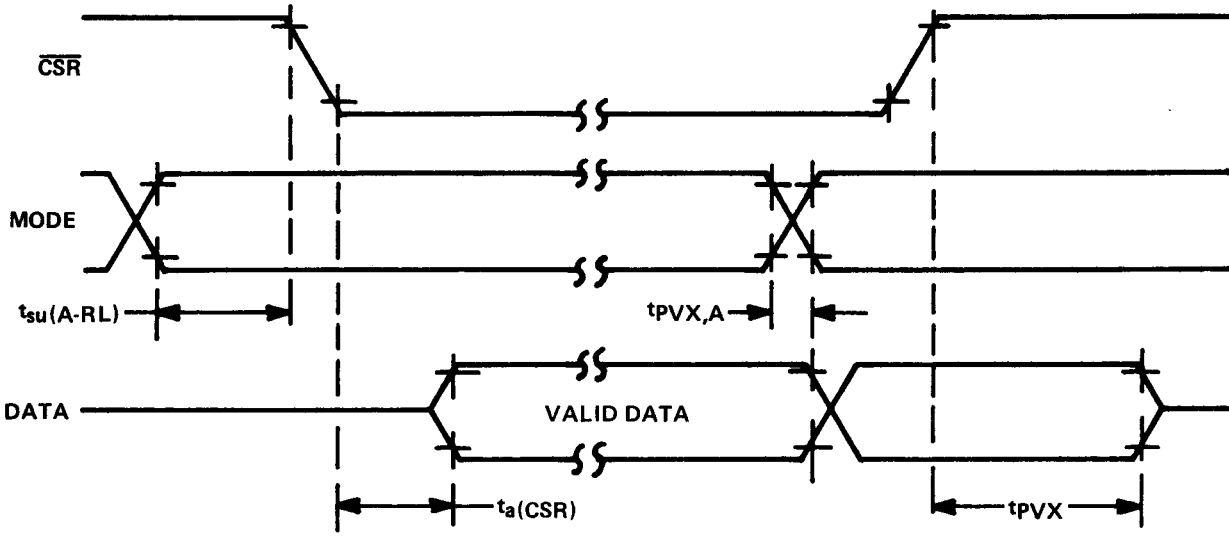


FIGURE 5-3 — CPU-VDP WRITE CYCLE FOR TMS9918A/9928A/9929A

READ CYCLE



NOTE: All measurements are made at 10% and 90% points.

FIGURE 5-4 — CPU-VDP READ CYCLE FOR TMS9918A/9928A/9929A

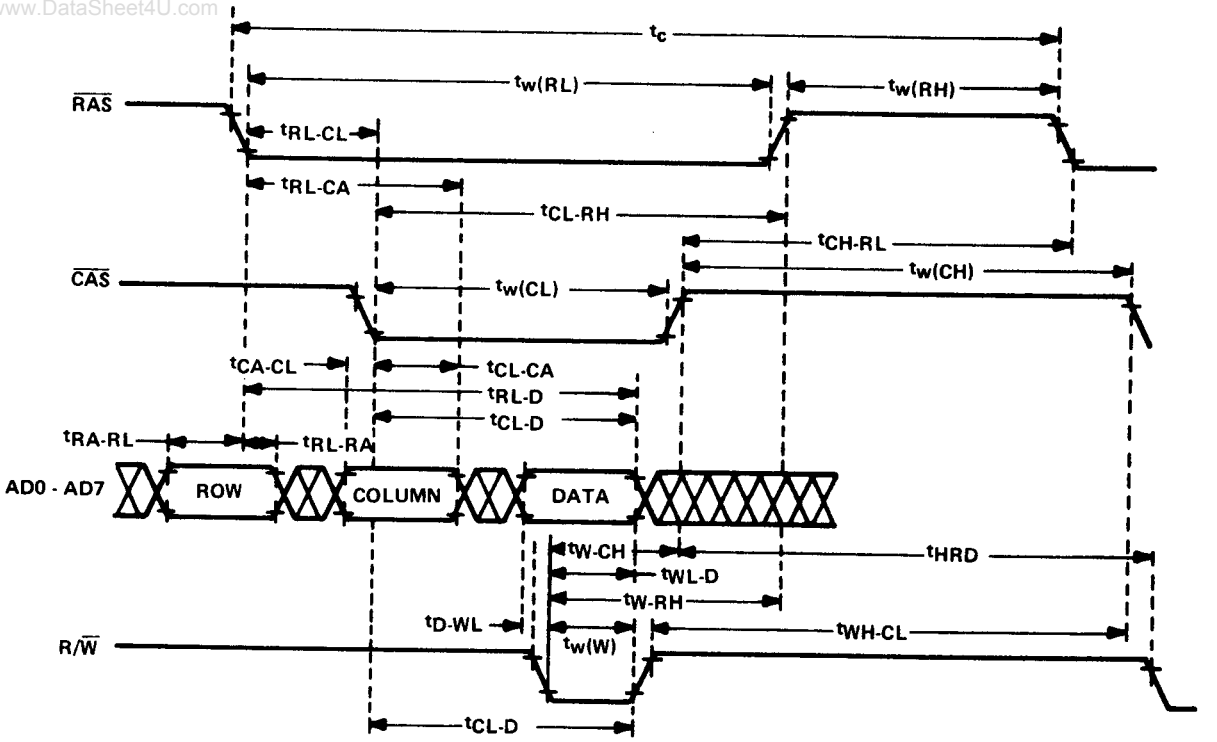
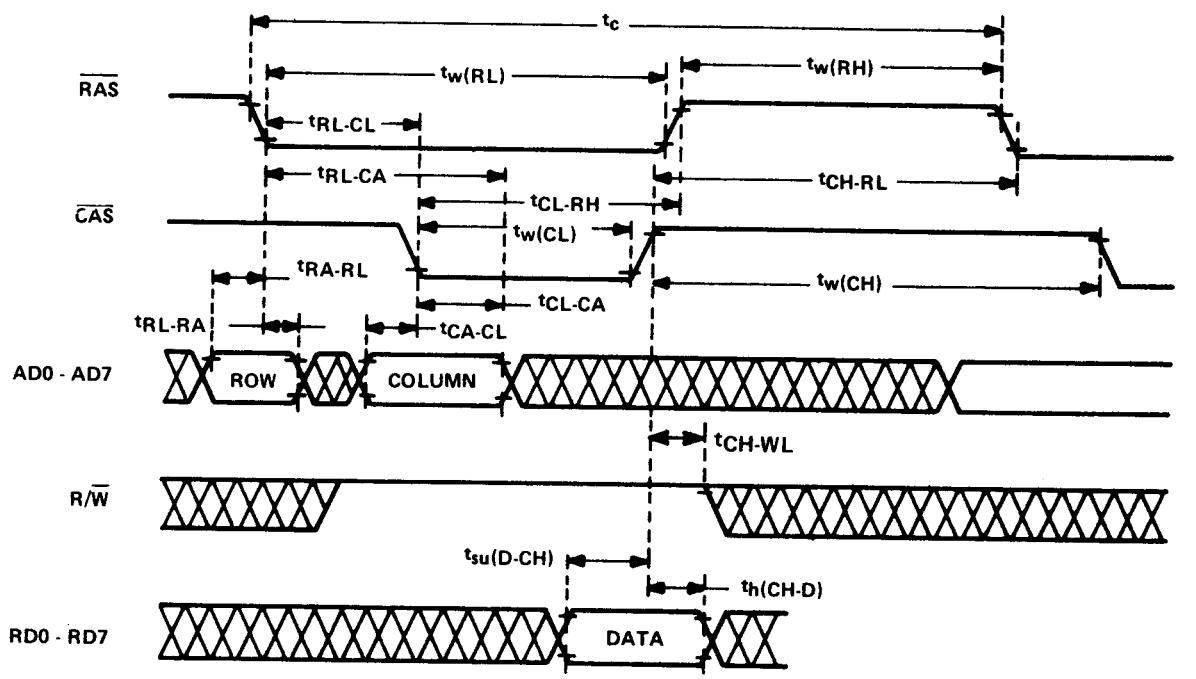
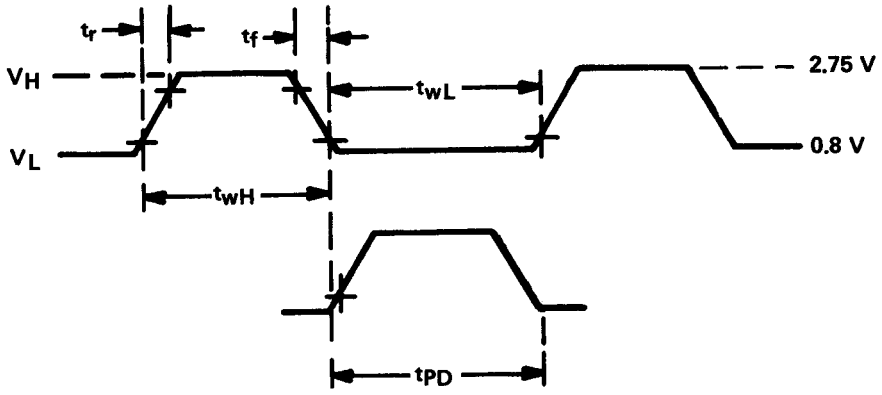


FIGURE 5-5 – VRAM WRITE CYCLE



NOTE: All measurements are made at 10% and 90% points.

FIGURE 5-6 – VRAM READ CYCLE



NOTE: All measurements are made at 10% and 90% points.

FIGURE 5-7 – EXTERNAL CLOCK TIMING WAVEFORM

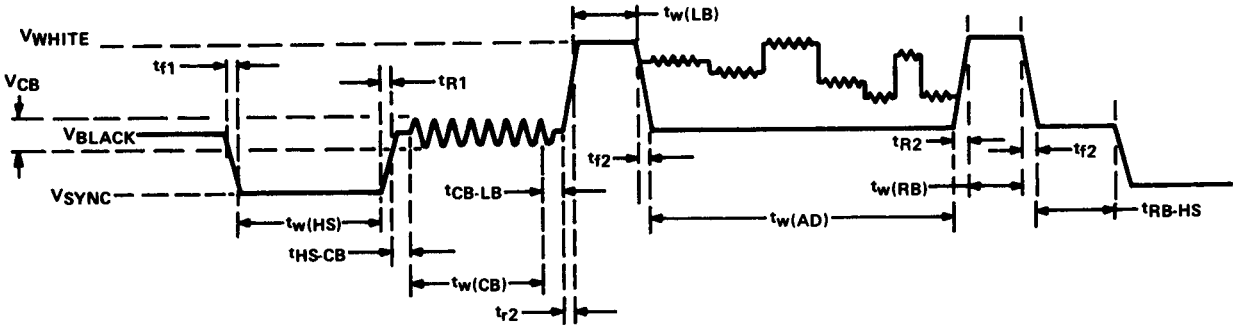
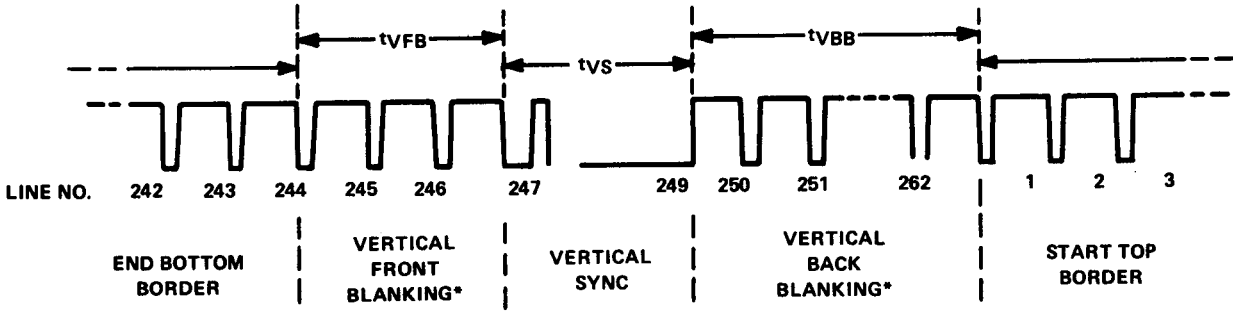


FIGURE 5-8 – TMS9918A COMVID HORIZONTAL TIMING



*Color burst output suppressed

FIGURE 5-9 – TMS9918A VERTICAL TIMING

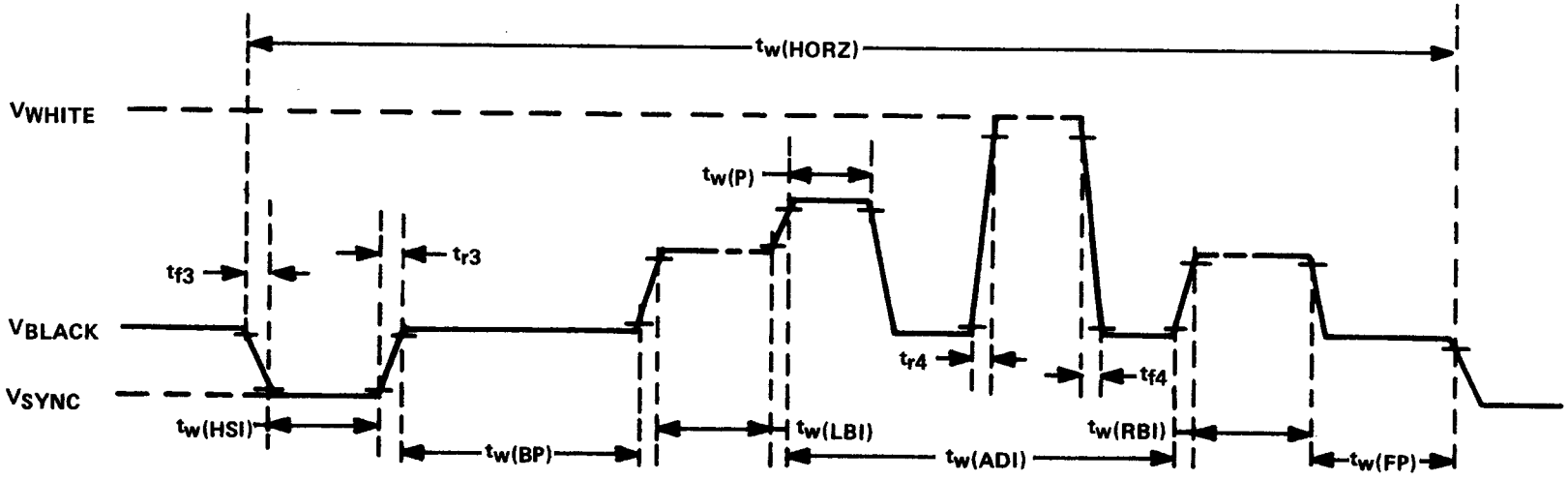
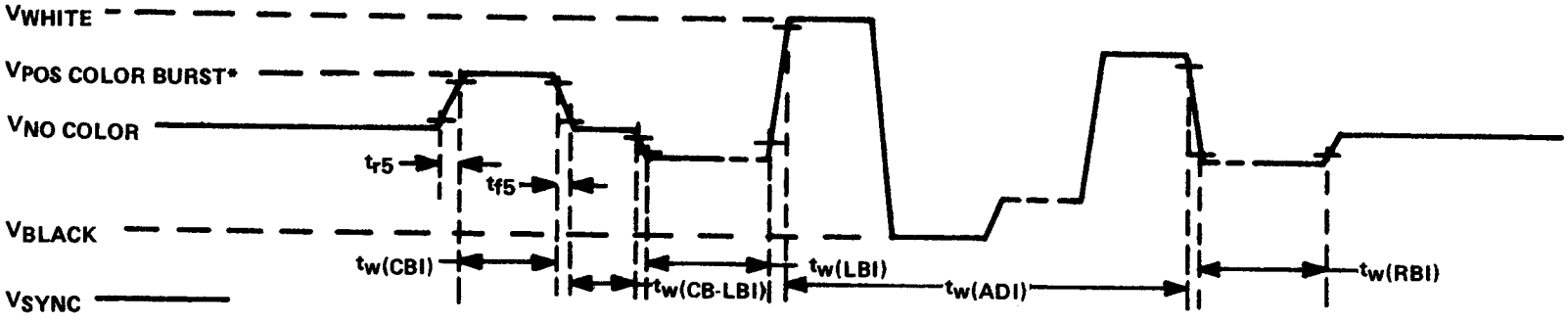
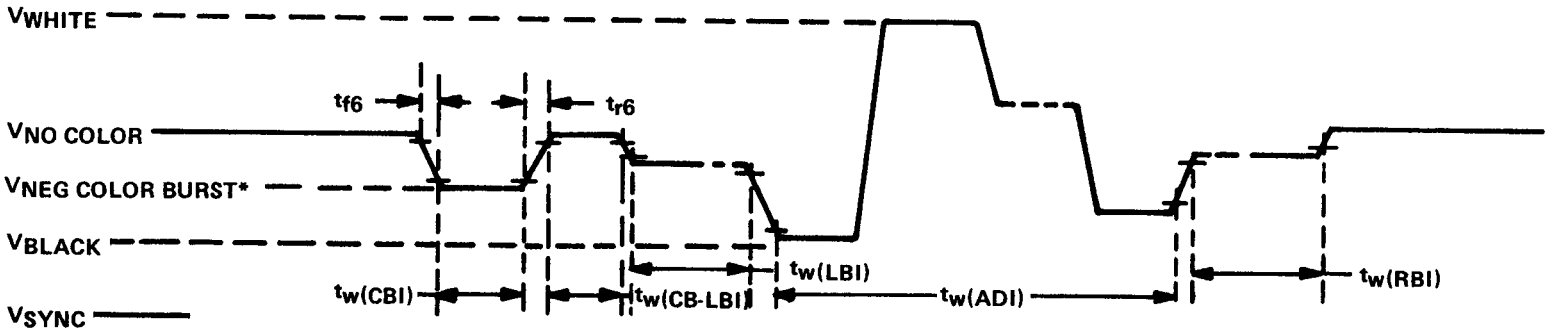


FIGURE 5-10 — TMS9928A/9929A Y HORIZONTAL TIMING



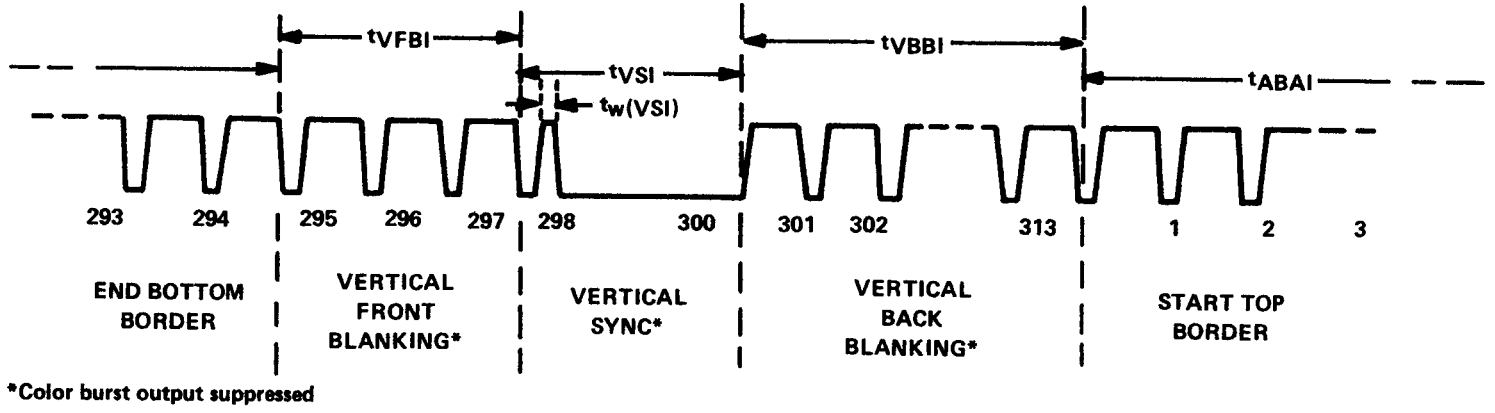
*Absent for the TMS9928A

FIGURE 5-11 — TMS9928A/9929A R-Y HORIZONTAL TIMING



*Absent for the TMS9928A

FIGURE 5-12 — TMS9928A/9929A B-Y HORIZONTAL TIMING



*Color burst output suppressed

FIGURE 5-13 — TMS9929A VERTICAL TIMING