TMU3100MS

USB Controller

Data Sheet

AMENDMENT HISTORY

Version	Date	Description
V1.0	Nov, 2004	New release
V1.1	June, 2006	1. Removed I/O drive/sink capacity description. 2. Modified DC ELECTRICAL CHARACTERISTICS DC CHARACTERISTICS.
V1.2	JAN,2012	Add Ordering Information table in the Packaging Information section.

CONTENTS

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GENERAL DESCRIPTION

The TMU3100MS is an 8-bit microprocessor embedded device tailored to the USB general application. It includes an 8-bit RISC CPU core, 192-byte SRAM, Low Speed USB Interface and an 8K x 14 internal program MASK ROM.

FEATURE

- Compliance with the Universal Serial Bus specification v1.1

- Built-in USB Transceiver and 3.3V regulator

- Support USB Suspend and Resume function

- One Control IN/OUT and two Interrupt IN endpoints

- 192 byte internal SRAM

- 8K x 14 internal program MASK ROM

- 8-bit RISC CPU core with only 36 instruction

- 3MHz instruction rate with 6MHz crystal oscillation

- Dice form, 40 pin DIP and 48 pin SSOP package

BLOCK DIAGRAM

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Preliminary
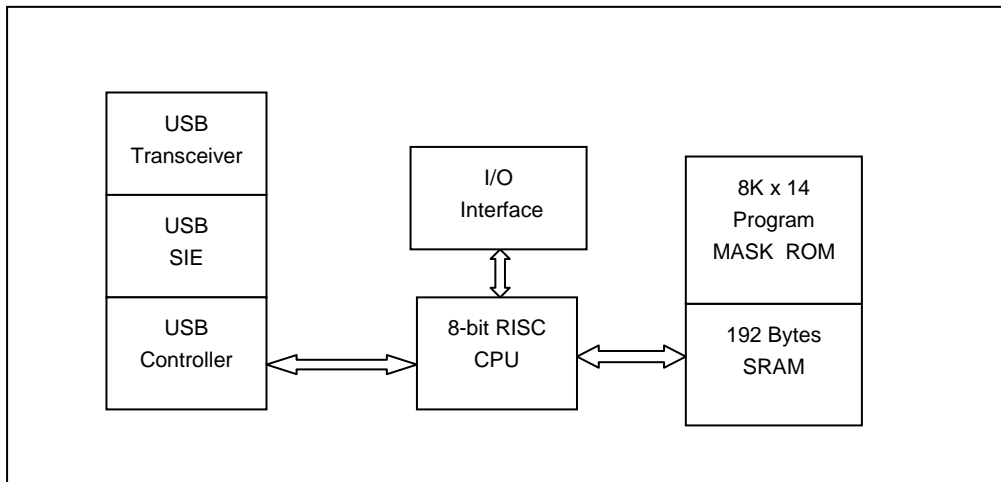
PIN DESCRIPTION

Name	I/O	Description
VDD	P	5V Power from USB cable
VSS	P	Ground
X1	I	Crystal in (6MHz)
X2	O	Crystal out
RESETn	I	Chip reset (active low)
TESTn	I	Test Mode control (active low)
DP/PB[3]	I/O	USB positive data signal / General purpose I/O (pseudo open-drain)
DM/PB[2]	I/O	USB negative data signal / General purpose I/O (pseudo open-drain)
KSI[7:0]	I	Input pins with built-in pull-up resistor
KSO[15:0]	O	Output pins with open drain with pull up resistor
PA[3:0]	I/O	General purpose I/O (open drain with pull up resistor)
PB[1:0]	I/O	General purpose I/O (pseudo open-drain)
LED[3:0]	O	LED output (with serial 450 ohm resistor)
V33	O	3.3V regulator output

Preliminary

PIN ASSIGNMENT

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                    ┌───────⌣───────┐
        VSS  □│1            40│□ X2
        V33  □│2            39│□ X1
     DP/PB[3] □│3            38│□ VDD
     DM/PB[2] □│4            37│□ LED[0]
       PB[1]  □│5            36│□ LED[1]
       PB[0]  □│6   TMU3100MS 35│□ LED[2]
       PA[1]  □│7    PDIP 40  34│□ KSI[0]
       PA[0]  □│8            33│□ KSI[1]
       TESTn  □│9            32│□ KSI[2]
     RESETn   □│10           31│□ KSI[3]
      KSO[0]  □│11           30│□ KSI[4]
      KSO[1]  □│12           29│□ KSI[5]
      KSO[2]  □│13           28│□ KSI[6]
      KSO[3]  □│14           27│□ KSI[7]
      KSO[4]  □│15           26│□ KSO[15]
      KSO[5]  □│16           25│□ KSO[14]
      KSO[6]  □│17           24│□ KSO[13]
      KSO[7]  □│18           23│□ KSO[12]
      KSO[8]  □│19           22│□ KSO[11]
      KSO[9]  □│20           21│□ KSO[10]
                    └───────────────┘
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                    ┌───────⌣───────┐
        VSS  □│1            48│□ X2
        V33  □│2            47│□ X1
     DP/PB[3] □│3            46│□ VDD
     DM/PB[2] □│4            45│□ PA[2]
       PB[1]  □│5            44│□ LED[0]
       PB[0]  □│6            43│□ N.C.
       N.C.   □│7   TMU3100MS 42│□ LED[1]
       N.C.   □│8    SSOP 48  41│□ LED[2]
       PA[1]  □│9            40│□ KSI[0]
       PA[0]  □│10           39│□ KSI[1]
       TESTn  □│11           38│□ KSI[2]
     RESETn   □│12           37│□ KSI[3]
      KSO[0]  □│13           36│□ KSI[4]
      KSO[1]  □│14           35│□ KSI[5]
      KSO[2]  □│15           34│□ KSI[6]
      KSO[3]  □│16           33│□ KSI[7]
      KSO[4]  □│17           32│□ LED[3]
      KSO[5]  □│18           31│□ N.C.
       N.C.   □│19           30│□ KSO[15]
       PA[3]  □│20           29│□ KSO[14]
      KSO[6]  □│21           28│□ KSO[13]
      KSO[7]  □│22           27│□ KSO[12]
      KSO[8]  □│23           26│□ KSO[11]
      KSO[9]  □│24           25│□ KSO[10]
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FUNCTIONAL DESCRIPTION

1. CPU Core

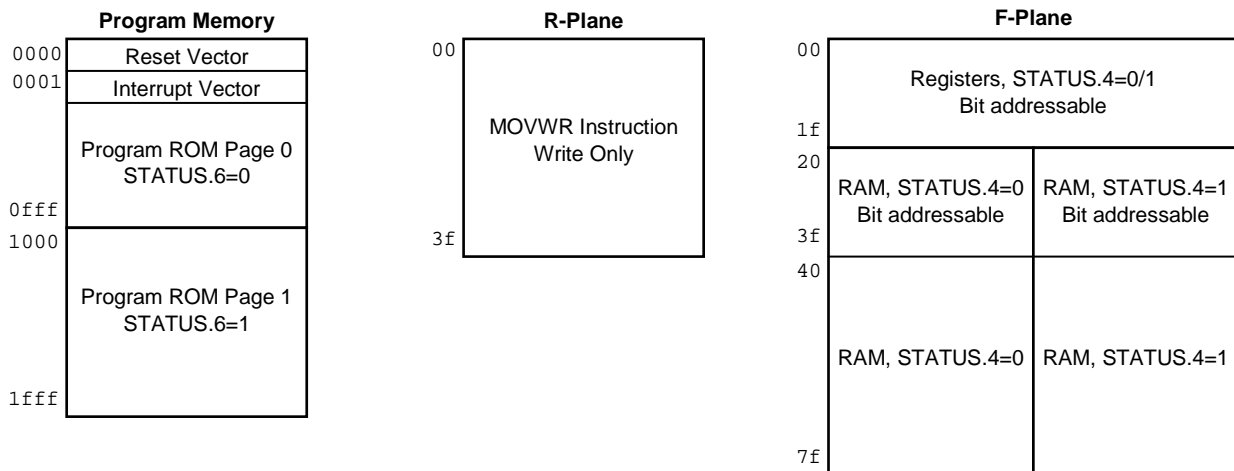### 1.1 Clock Scheme and Instruction Cycle

The clock input (X1) is internally divided by two to generate Q1 state and Q2 state for each instruction cycle. The Programming Counter (PC) is updated at Q1 and the instruction is fetched from program ROM and latched into the instruction register in Q2. It is then decoded and executed during the following Q1-Q2 cycle.

1.2 Programming Counter (PC) and Stack

The Programming Counter is 13-bit wide capable of addressing a 8K x 14 program ROM. As a program instruction is executed, the PC will contain the address of the next program instruction to be executed. The PC value is normally increased by one except the followings. The Reset Vector (0) and the Interrupt Vector (1) are provided for PC initialization. For CALL/GOTO instructions, PC loads its lower 12 bits from instruction word and the MSB from STATUS's bit 6. For RET/RETI/RETLW instructions, PC retrieves its content from the top level STACK. For the other instructions updating PC[7:0], the PC[12:8] keeps unchanged.
The STACK is 13-bit wide and 6-level in depth. The CALL instruction and Hardware interrupt will push STACK level in order, While the RET/RETI/RETLW instruction pops the STACK level in order.

1.3 Addressing Mode

There are two Data Memory Plane in CPU, R-Plane and F-Plane. The registers in R-Plane are write-only. The "MOVWR" instruction copy the W-register's content to those registers by direct addressing mode. Registers in F-Plane can be addressed directly or indirectly. Indirect Addressing is made by address "0", where FSR points to an actual address. The first half of F-Plane is also bit-addressable.

Program Memory

0000	Reset Vector
0001	Interrupt Vector
	Program ROM Page 0 STATUS.6=0
0fff	
1000	
	Program ROM Page 1 STATUS.6=1
1fff	

R-Plane

00	
	MOVWR Instruction Write Only
3f	

F-Plane

00	Registers, STATUS.4=0/1 Bit addressable
1f	
20	RAM, STATUS.4=0 Bit addressable / RAM, STATUS.4=1 Bit addressable
3f	
40	RAM, STATUS.4=0 / RAM, STATUS.4=1
7f	

1.4 ALU and Working (W) Register

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. In two-operand instructions, typically one operand is the W register, which is an 8-bit non-addressable register used for ALU operations. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either W register or a file register.

Depending on the instruction executed, the ALU may affect the values of Carry(C), Digit Carry(DC), and Zero(Z) Flags in the STATUS register. The C and DC flags operate as a /Borrow and /Digit Borrow, respectively, in subtraction.

1.5 STATUS Register

This register contains the arithmetic status of ALU and the page select for Program ROM and Data RAM. The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. It is recommended, therefore, that only BCF, BSF and MOVWF instructions be used to alter the STATUS Register because these instructions do not affect those bits.

1.6 Interrupt

Each interrupt source has its own enable control bit. An interrupt event will set its individual flag. If the corresponding interrupt enable bit has been set, it would trigger CPU to service the interrupt. CPU accepts interrupt in the end of current executed instruction cycle. In the mean while, A "CALL 0001" instruction is inserted to CPU, and the I-flag is set to prevent recursive interrupt nesting. The I-flag is cleared in the instruction after the "RETI" instruction. That is, at least one instruction in main program is executed before service the pending interrupt. The interrupt event is level trigged. F/W must clear the interrupt event register while serves the interrupt routine.

1.7 Instruction Set

Each instruction is a 14-bit word divided into an OPCODE, which specified the instruction type, and one or more operands, which further specify the operation of the instruction. The instructions can be categorized as byte-oriented, bit-oriented and literal operations list in the following table.

For byte-oriented instructions, "f" represents address designator and "d" represents destination designator. The address designator is used to specify which address in F-Plane is to be used by the instruction. The destination designator specifies where the result of the operation is to be placed. If "d" is "0", the result is placed in the W register. If "d" is "1", the result is placed in the address specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator, which selects the number of the bit affected by the operation, while "f" represents the address designator.

For literal operations, "k" represents the literal or constant value.

For "MOVWR" instruction, "r" specifies which address in R-Plane is to be used by the instruction.

All instructions are single cycle except for program branches, which are two-cycle.

Mnemonic	Op Code	Cycles	Flag Affect	Description
NOP	00 0000 0 0000000	1	-	No operation
SLEEP	00 0000 0 0000011	1		Go into standby mode, Clock oscillation stops
CLRWDT	00 0000 0 0000100	1		Clear and enable Watch Dog Timer
MOVWR r	00 0000 0 0rrrrrr	1	-	Move W to "r"
RET	00 0000 0 1000000	2	-	Return
RETI	00 0000 0 1100000	2	-	Return from interrupt
MOVWF f	00 0000 1 fffffff	1	-	Move W to "f"
CLRW	00 0001 0 1000000	1	Z	Clear W
CLRF f	00 0001 1 fffffff	1	Z	Clear "f"
SUBWF f,d	00 0010 d fffffff	1	C,DC,Z	Subtract W from "f"
DECF f,d	00 0011 d fffffff	1	Z	Decrement "f"
IORWF f,d	00 0100 d fffffff	1	Z	OR W with "f"
ANDWF f,d	00 0101 d fffffff	1	Z	AND W with "f"
XORWF f,d	00 0110 d fffffff	1	Z	XOR W with "f"
ADDWF f,d	00 0111 d fffffff	1	C,DC,Z	Add W and "f"
MOVFW f	00 1000 0 fffffff	1	-	Move "f" to "w"
TESTZ f	00 1000 1 fffffff	1	Z	Test if "f" is zero
COMF f,d	00 1001 d fffffff	1	Z	Complement "f"
INCF f,d	00 1010 d fffffff	1	Z	Increment "f"
DECFSZ f,d	00 1011 d fffffff	1 or 2	-	Decrement "f", skip if zero
RRF f,d	00 1100 d fffffff	1	C	Rotate right "f" through carry
RLF f,d	00 1101 d fffffff	1	C	Rotate left "f" through carry
SWAPF f,d	00 1110 d fffffff	1	-	Swap high/low nibble of "f"
INCFSZ f,d	00 1111 d fffffff	1 or 2	-	Increment "f", skip if zero
BCF f,b	010 00 bbb fffff	1	-	Clear "b" bit of "f"
BSF f,b	010 01 bbb fffff	1	-	Set "b" bit of "f"
BTFSC f,b	010 10 bbb fffff	1 or 2	-	Test "b" bit of "f", skip if clear
BTFSS f,b	010 11 bbb fffff	1 or 2	-	Test "b" bit of "f", skip if set
RETLW k	011 000 kkkkkkkk	2	-	Return, place Literal "k" in W
MOVLW k	011 001 kkkkkkkk	1	-	Move Literal "k" to W
IORLW k	011 010 kkkkkkkk	1	Z	OR Literal "k" with W
ANDLW k	011 011 kkkkkkkk	1	Z	AND Literal "k" with W
ADDLW k	011 100 kkkkkkkk	1	C,DC,Z	Add Literal "k" to W
XORLW k	011 111 kkkkkkkk	1	Z	XOR Literal "k" with W
CALL k	10 kkkk kkkkkkkk	2	-	Call subroutine "k"
GOTO k	11 kkkk kkkkkkkk	2	-	Jump to branch "k"

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2. I/O Port

2.1 KSO[15:0]

These pins are used as keyboard scan outputs. They have at least 4mA drive and sink strength.

KSO[15:0]
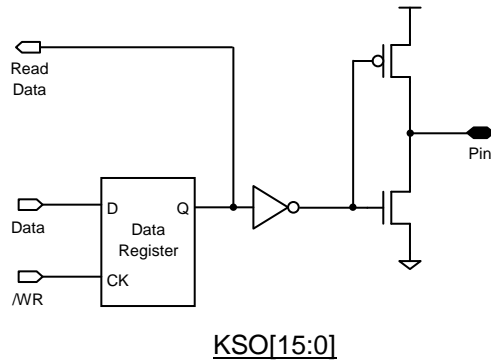
2.2 KSI[7:0]

These pins are used as keyboard scan inputs. Each one of them has a pull up resistor. In addition, each KSI pin can cause Keyboard interrupt (KBDint) if the corresponding interrupt mask bit (KBDmask) is 0. The KBDint is asserted at the falling edge of KSI pin.


KSI[7:0]
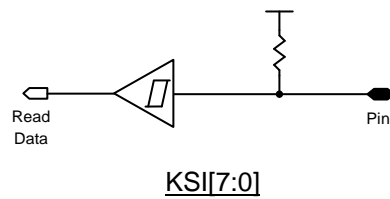
2.3 PA[3:0]

These pins are similar to KSO pins, except data are read from pin. They can be used as input or open drain output.

PA[3:0]

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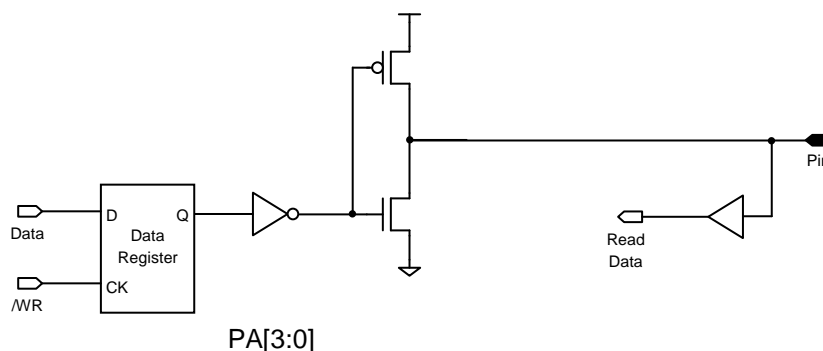
2.4 PB[1:0]

These pins are "Pseudo-Open-Drain" structure. In "Read-Modify-Write" instruction, CPU actually reads the output data register. In the others instructions, CPU reads the pin data. The so-called "Read-Modify-Writenstruction includes BSF, BCF and all instructions using F-Plane as destination.

The PB[0] pin can also generate interrupt (PB0int) at its falling edge.
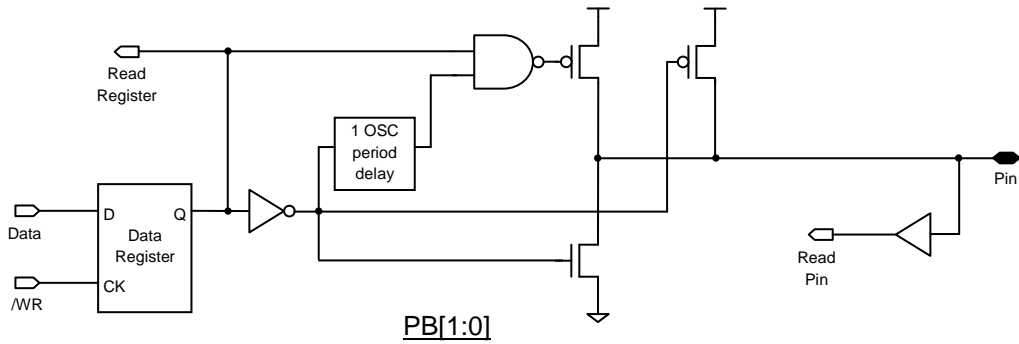
PB[1:0]

2.5 DP/PB[3] and DM/PB[2]

These pins are similar to PB[1:0], except they share the pin with USB function. An extra control bit "PS2kbd" is used to enable the small pull-up current.

DP/PB[3] and DM/PB[2]
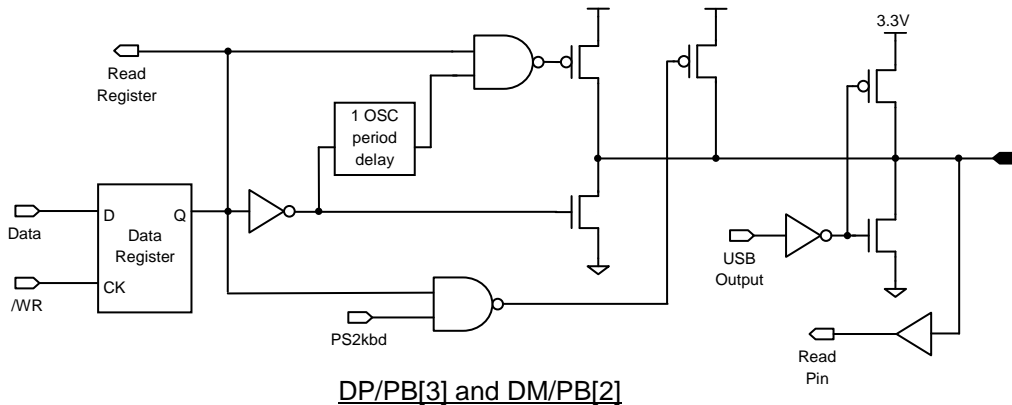
2.6 LED[3:0]

These pins are used to drive LED. They are open-drain structure with a serial resistor. The typical resistor value is 420 ohm.

LED[3:0]

3. Power Down Mode

The power down mode is activated by SLEEP instruction. In power down mode, the crystal clock oscillation stops to minimize power consumption. Power down mode can be terminated by Reset or enabled Interrupts.
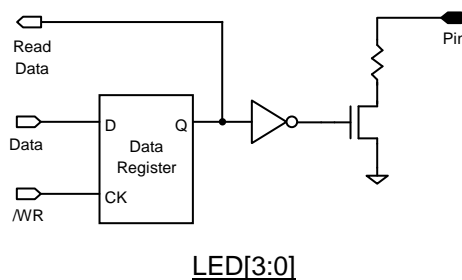
4. Watch Dog Timer

The Watch Dog Timer (WDT) is disabled after Reset. F/W can use the CLRWDT instruction to clear and enable the Watch Dog Timer. Once enabled, the Watch Dog Timer overflow and generate a chip reset signal if no CLRWDT executed in a period of 4000000 oscillator's cycle (0.66 second for 6MHz crystal). The WDT does not work in Power Down Mode to provide wake-up function. It is only designed to prevent F/W goes into endless loop.

5. Timer 0

The Timer 0 is an 8-bit wide register of F-Plane. It can be read or written as any other register of F-Plane. Besides, Timer 0 increases itself periodically and reloads itself with a special value every time while roll over. The value to be load at roll over point is defined by "Timer 0 Reload" (T0RLD) register in the R-Plane. The period which Timer 0 increases itself is defined by "Timer 0 Pre-Scale" (T0PSCL) register in R-Plane, the default (0) mean 4 instruction cycles increase Timer 0. The Timer 0 also generates interrupt (T0int) while it rolls over.

6. USB Engine

The USB engine includes the Serial Interface Engine (SIE), the low-speed USB I/O transceiver and the 3.3 Volt Regulator. The SIE block performs most of the USB interface function with only minimum support from F/W. Three endpoints are supported. Endpoint 0 is used to receive and transmit control (including SETUP) packets while Endpoint 1 and endpoint 2 are only used to transmit data packets.

The USB SIE handles the following USB bus activity independently:

1. Bitstuffing/unstuffing
2. CRC generation/checking
3. ACK/NAK
4. TOKEN type identification
5. Address checking

F/W handles the following tasks:

1. Coordinate enumeration by responding to SETUP packets
2. Fill and empty the FIFOs
3. Suspend/Resume coordination
4. Verify and select DATA toggle values

6.1 USB Device Address

The USB device address register (USBadr) stores the device's address. This register is reset to all 0 after chip reset. F/W must write this register a valid value after the USB enumeration process.

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6.2 Endpoint 0 receive

After receiving a packet and placing the data into the Endpoint 0 receive FIFO (RC0FIFO), TMU3100 updates the Endpoint 0 status registers to record the receive status and then generates an Endpoint 0 receive interrupt (RC0int). F/W can read the status register for the recent transfer information, which includes the data byte count (RC0cnt), data direction (EP0dir), SETUP token flag (EP0set), packet toggle (RC0tgl) and data valid flag (RC0err). The received data is always stored into RC0FIFO and the RC0cnt is always updated for DATA packets following SETUP tokens. The data following an OUT token is written into the RC0FIFO, and the RC0cnt is updated unless Endpoint 0 STALL (EP0stall) is set or Endpoint 0 receive ready (RC0rdy) is cleared. The SIE clears the RC0rdy automatically and generates RC0int interrupt when the RC0cnt or RC0FIFO is updated. As long as the RC0rdy is cleared, SIE keep responding NAK to Host's Endpoint 0 OUT packet request. F/W should set the RC0rdy flag after the RC0int interrupt is asserted and RC0FIFO is read out.

6.3 Endpoint 0 transmit

After detecting a valid Endpoint 0 IN token, TMU3100MS automatically transmit the data pre-stored in the Endpoint 0 transmit FIFO (TX0FIFO) to the USB bus if the Endpoint 0 transmit ready flag (TX0rdy) is set and the EP0stall is cleared. The number of byte to be transmitted depends on the Endpoint 0 transmit byte count register (TX0cnt). The DATA0/1 token to be transmitted depends on the Endpoint 0 transmit toggle control bit (TX0tgl). After the TX0FIFO is updated, TX0rdy should be set to 1. This enables the TMU3100MS to respond to an Endpoint 0 IN packet. TX0rdy is cleared and an Endpoint 0 transmit interrupt (TX0int) is generated once the USB host acknowledges the data transmission. The interrupt service routine can check TX0rdy to confirm that the data transfer was successful.

6.4 Endpoint 1/2 transmit

Endpoint1 and Endpoint2 are capable of transmit only. These endpoints are enabled when the Endpoint1 / Endpoint2 configuration control bit (EP1cfg/EP2cfg) is set. After detecting a valid Endpoint 1/2 IN token, TMU3100MS automatically transmit the data pre-stored in the Endpoint 1/2 transmit FIFO (TX1FIFO/TX2FIFO) to the USB bus if the Endpoint 1/2 transmit ready flag (TX1rdy/TX2rdy) is set and the EP1stall/EP2stall is cleared. The number of byte to be transmitted depends on the Endpoint 1/2 transmit byte count register (TX1cnt/TX2cnt). The DATA0/1 token to be transmitted depends on the Endpoint 1/2 transmit toggle control bit (TX1tgl/TX2tgl). After the TX1FIFO/TX2FIFO is updated, TX1rdy/TX2rdy should be set to 1. This enables the TMU3100MS to respond to an Endpoint 1/2 IN packet. TX1rdy/TX2rdy is cleared and an Endpoint 1/2 transmit interrupt (TX1int/TX2int) is generated once the USB host acknowledges the data transmission. The interrupt service routine can check TX1rdy/TX2rdy to confirm that the data transfer was successful.

6.5 USB Control and Status

Other USB control bits include the USB enable (ENUSB), Suspend (Susp), Resume output (RsmO), Control Read (CtrRD), and corresponding interrupt enable bits. The CtrRD should be set when program detects the current transfer is an Endpoint0 Control Read Transfer. Once this bit is set, the TMU3100 will stall an Endpoint0 OUT packet with DATA toggle 0 or byte count other than 0. Other USB status flag includes the USB reset interrupt (RSTint), Resume input interrupt (RSMint), and USB Suspend interrupt (SUSPint).

6.6 Suspend and Resume

Once the Suspend condition is asserted, F/W can set the Susp bit to save the power consumption of USB Engine. F/W can further save the device power by force the CPU to go into the Power Down Mode. In the Power Down mode, the X'tal is stop, but CPU can be waken-up by the trigger of enabled interrupt's source, which includes RSMint, KBDint and PB0int.

The TMU3100MS send Resume signaling to USB bus when Susp=1 and RsmO=1. In the suspend mode, if a keyboard interrupt is asserted, F/W should send resume signal to wake up the USB bus.

MEMORY MAP of F-Plane

Name	Address	R/W	Rst	Description
Timer0	01.7~0	R/W	0	Timer 0
PCL	02.7~0	R/W	0	Program Counter [7~0]
ROMpage	03.6	R/W	0	Program ROM Page Select (STATUS.6)
RAMbank	03.4	R/W	0	SRAM Bank Select (STATUS.4)
Z	03.2	R/W	0	Zero Flag (STATUS.2)
DC	03.1	R/W	0	Decimal Carry Flag or Decimal /Borrow Flag (STATUS.1)
C	03.0	R/W	0	Carry Flag or /Borrow Flag (STATUS.0)
FSR	04.6~0	R/W	0	File Select Register to define Address in indirect addressing mode
PAD	05.3~0	R/W	f	Port A output data
PBD	06.3~0	W	f	Port B output data
PBD	06.3~0	R	-	Port B output data or Port B pin data
LED	07.3~0	R/W	-	LED output
KSOL	08.7~0	R/W	ff	Key Scan output [7~0]
KSOH	09.7~0	R/W	ff	Key Scan output [15~8]
KSI	0A.7~0	R		Key Scan input [7~0]
GPR0	0E.7~0	R/W	-	General Purpose Register 0
GPR1	0F.7~0	R/W	-	General Purpose Register 1
ENUSB	10.7	R/W	0	USB function enable (1)
USBadr	10.6~0	R/W	0	USB device address
RC0int	11.7	R/W	0	Endpoint 0 Receive Interrupt flag, write 0 to clear flag.
TX0int	11.6	R/W	0	Endpoint 0 Transmit Interrupt flag, write 0 to clear flag.
TX1int	11.5	R/W	0	Endpoint 1 Transmit Interrupt flag, write 0 to clear flag.
TX2int	11.4	R/W	0	Endpoint 2 Transmit Interrupt flag, write 0 to clear flag.
RSTint	11.3	R/W	0	USB Bus Reset Interrupt flag, write 0 to clear flag.
SUSPint	11.2	R/W	0	USB Suspend Interrupt flag, write 0 to clear flag.
RSMint	12.3	R/W	0	USB Resume Interrupt flag, write 0 to clear flag.
KBDint	12.2	R/W	0	KeyBoard Interrupt flag, write 0 to clear flag.
PB0int	12.1	R/W	0	PB0 interrupt flag, write 0 to clear flag.
T0int	12.0	R/W	0	Timer0 Interrupt flag, write 0 to clear flag.
Susp	13.7	R/W	0	F/W force USB interface to go into suspend mode.
RsmO	13.6	R/W	0	F/W force USB interface send Resume signal in suspend mode.
EP1cfg	13.5	R/W	0	Set Endpoint 1 configuration.
EP2cfg	13.4	R/W	0	Set Endpoint 2 configuration.
CtrRD	13.3	R/W	0	H/W will stall an invalid OUT token during Control Read transfer.
RC0rdy	13.0	R/W	0	Endpoint 0 ready for receive, clear by H/W while RC0int occurs.
RC0tgl	14.7	R		1: received DATA1 packet; 0: received DATA0 Packet.
RC0err	14.6	R		Endpoint 0 received data error.
EP0dir	14.5	R		1: IN transfer; 0: OUT/SETUP transfer.
EP0set	14.4	R		SETUP Token indicator.
RC0cnt	14.3~0	R		Received data byte count.
TX0rdy	15.7	R/W	0	Endpoint 0 ready for transmit, clear by H/W while TX0int occurs.
TX0tgl	15.6	R/W	0	Endpoint 0 transmit DATA1/DATA0 packet.
EP0stall	15.5	R/W	0	Endpoint 0 will stall OUT/IN packet while this bit is 1.
TX0cnt	15.3~0	R/W	0	Endpoint 0 transmit byte count.
TX1rdy	16.7	R/W	0	Endpoint 1 ready for transmit, clear by H/W while TX1int occurs.
TX1tgl	16.6	R/W	0	Endpoint 1 transmit DATA1/DATA0 packet.
EP1stall	16.5	R/W	0	Endpoint 1 will stall IN packet while this bit is 1.
TX1cnt	16.3~0	R/W	0	Endpoint 1 transmit byte count.
TX2rdy	17.7	R/W	0	Endpoint 2 ready for transmit, clear by H/W while TX2int occurs.
TX2tgl	17.6	R/W	0	Endpoint 2 transmit DATA1/DATA0 packet.
EP2stall	17.5	R/W	0	Endpoint 2 will stall IN packet while this bit is 1.
TX2cnt	17.3~0	R/W	0	Endpoint 2 transmit byte count.

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RC0FIFO	18~1F	R		Endpoint 0 Receive Buffer (8 Bytes)
SRAM	20~7F	R/W	-	Internal RAM (96 Bytes x 2 Banks)

MEMORY MAP of R-Plane

Name	Address	R/W	Rst	Description
T0RLD	01.7~0	W	0	Timer0 overflow reload value
T0PSCL	02.3~0	W	0	Timer0 Pre-Scale, 0:divided by 2, 1:divided by 4, … 7:divided by 256, 8:divided by 1 (Time base is 2*instruction cycle)
PWRdwn	03	W	0	Write this register to enter Power-Down Mode
WDTe	04	W	0	Write this register to clear WDT and enable WDT
KBDmask	05.7~0	W	0	Mask KSI[7:0] interrupt function while the corresponding bit is "1"
TESTreg	0F.3~0	W	0	Test Mode control, keep 0 in normal mode
TX0FIFO	18~1F	W	-	Endpoint 0 Transmit Buffer (8 Bytes)
TX1FIFO	20~27	W	-	Endpoint 1 Transmit Buffer (8 Bytes)
TX2FIFO	28~2F	W	-	Endpoint 2 Transmit Buffer (8 Bytes)
RC0ie	11.7	W	0	RC0 Interrupt enable
TX0ie	11.6	W	0	TX0 Interrupt enable
TX1ie	11.5	W	0	TX1 Interrupt enable
TX2ie	11.4	W	0	TX2 Interrupt enable
RSTie	11.3	W	0	USB Reset Interrupt enable
SUSPie	11.2	W	0	Suspend Interrupt enable
PS2kbd	12.4	W	0	Select PS2 keyboard Mode
RSMie	12.3	W	0	RSM Interrupt enable
KBDie	12.2	W	0	Keyboard Interrupt enable
PB0ie	12.1	W	0	PB[0] Interrupt enable
T0ie	12.0	W	0	Timer 0 Interrupt enable

ABSOLOUTE MAXIMUM RATINGS

GND= 0V

Name	Symbol	Range	Unit
Maximum Supply Voltage	VDD	-0.3 to 5.5	V
Maximum Input Voltage	Vin	-0.3 to VDD+0.3	V
Maximum output Voltage	Vout	-0.3 to VDD+0.3	V
Maximum Operating Temperature	Topg	-5 to +70	℃
Maximum Storage Temperature	Tstg	-25 to +125	℃

RECOMMEND OPERATING CONDITION

at Ta=-20　　　　　℃ to 70℃,GND= 0V

Name	Symb.	Min.	Max.	Unit
Supply Voltage	VDD	4.5	5.5	V

DC CHARACTERISTICS

at Ta=25 ℃,VDD=5.0V, VSS= 0V, Fosc=6MHz

Name	Symb.	Min.	Typ.	Max.	Unit	Condition
Operating current	Icc		5.5		mA	Fosc=6MHz
Suspend current	Isus		360		uA	No load
Output High Voltage	Voh1		4.0		V	Ioh=30uA
	Voh2		4.5		V	Ioh=4mA
Output Low Voltage	Vol		0.4		V	Iol=15mA
RESET pull up resistor	Rrst		31		Kohm	(Vrst=3.38v)
KSI pull up resistor	Rksi		46		Kohm	
LED sink current	Iled		5.5		mA	Vled=3.2V
V33 output voltage	V33		3.28		V	
Input "H" Voltage	Vih	2.0			V	

AC CHARACTERISTICS

at Ta=25 ℃,VDD=5.0V, VSS= 0V, Fosc=6MHz

Name	Symb.	Min.	Max.	Unit	Note
DP/DM rising time	Trise	75	300	ns	
DP/DM falling time	Tfall	75	300	ns	
DP,DM cross point	Vx	1.3	2.0	V	

Note: All USB transceiver characteristics can meet USB1.1 spec.

Package Diagrams

40 PIN P_ DIP
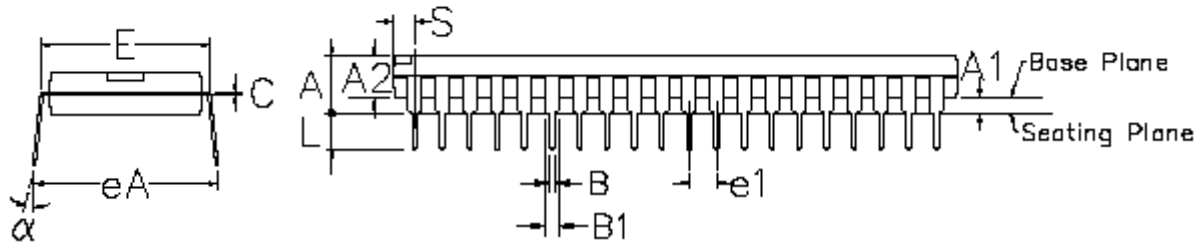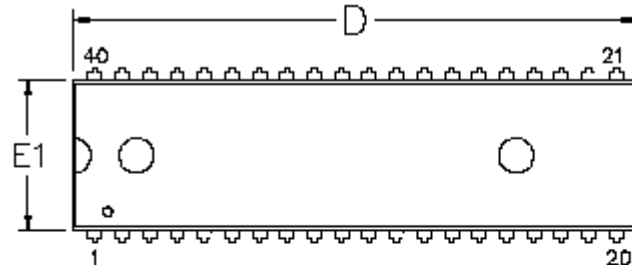
Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	——	——	0.210	——	——	5.33
A1	0.010	——	——	0.25	——	——
A2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	——	2.055	2.070	——	52.20	52.58
E	0.590	0.600	0.610	14.99	15.24	15.49
E1	0.540	0.545	0.552	13.72	13.84	14.02
e1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
α	0°	——	15°	0°	——	15°
eA	0.630	0.650	0.670	16.00	16.51	17.02
S	——	——	0.090	——	——	2.29

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48 PIN SSOP

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.413	2.591	2.794	0.095	0.102	0.110
A1	0.203	0.305	0.406	0.008	0.012	0.016
b	0.203		0.343	0.008		0.0135
c	0.127		0.254	0.005		0.010
e	0.635BASIC			0.025BASIC		
E	10.033		10.668	0.395		0.420
E1	7.391	7.493	7.595	0.291	0.295	0.299
h	0.381		0.635	0.015		0.025
L	0.508		1.016	0.020		0.040
α	0	8	2.473	0		8

N	D DIMENSION(IN INCH)			JEDEC
48	0.620	0.625	0.630	MO-118(AA)
56	0.720	0.725	0.730	MO-118(AB)

NOTE:

1. DIMENSION "D" DONE NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

2. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006 INCH(0.1524mm) PER SIDE.
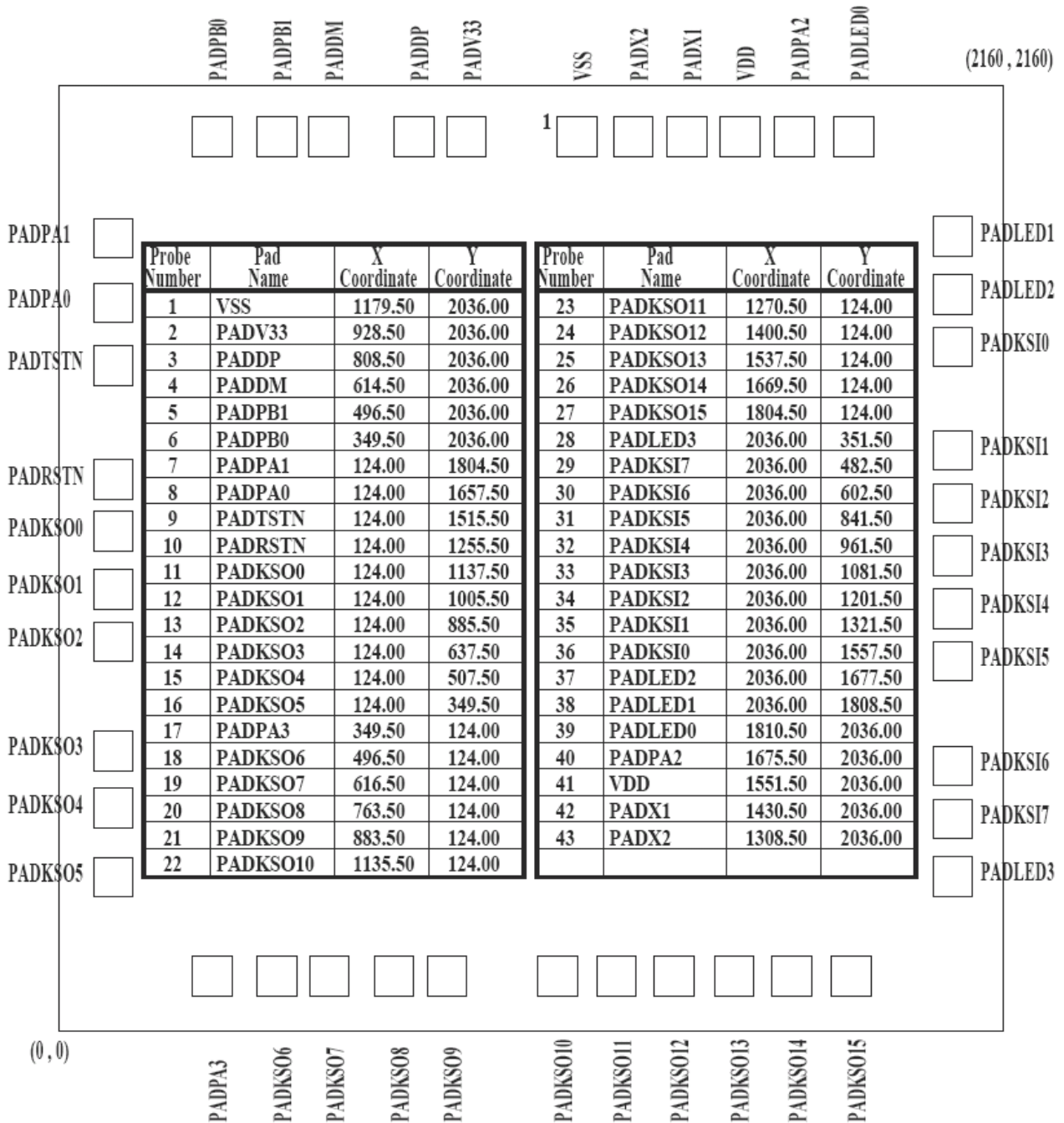
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PAD Locations

Probe Number	Pad Name	X Coordinate	Y Coordinate	Probe Number	Pad Name	X Coordinate	Y Coordinate
1	VSS	1179.50	2036.00	23	PADKSO11	1270.50	124.00
2	PADV33	928.50	2036.00	24	PADKSO12	1400.50	124.00
3	PADDP	808.50	2036.00	25	PADKSO13	1537.50	124.00
4	PADDM	614.50	2036.00	26	PADKSO14	1669.50	124.00
5	PADPB1	496.50	2036.00	27	PADKSO15	1804.50	124.00
6	PADPB0	349.50	2036.00	28	PADLED3	2036.00	351.50
7	PADPA1	124.00	1804.50	29	PADKSI7	2036.00	482.50
8	PADPA0	124.00	1657.50	30	PADKSI6	2036.00	602.50
9	PADTSTN	124.00	1515.50	31	PADKSI5	2036.00	841.50
10	PADRSTN	124.00	1255.50	32	PADKSI4	2036.00	961.50
11	PADKSO0	124.00	1137.50	33	PADKSI3	2036.00	1081.50
12	PADKSO1	124.00	1005.50	34	PADKSI2	2036.00	1201.50
13	PADKSO2	124.00	885.50	35	PADKSI1	2036.00	1321.50
14	PADKSO3	124.00	637.50	36	PADKSI0	2036.00	1557.50
15	PADKSO4	124.00	507.50	37	PADLED2	2036.00	1677.50
16	PADKSO5	124.00	349.50	38	PADLED1	2036.00	1808.50
17	PADPA3	349.50	124.00	39	PADLED0	1810.50	2036.00
18	PADKSO6	496.50	124.00	40	PADPA2	1675.50	2036.00
19	PADKSO7	616.50	124.00	41	VDD	1551.50	2036.00
20	PADKSO8	763.50	124.00	42	PADX1	1430.50	2036.00
21	PADKSO9	883.50	124.00	43	PADX2	1308.50	2036.00
22	PADKSO10	1135.50	124.00				

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Ordering Information

The ordering information:

Ordering number	Package
TMU3100MS-COD	Wafer / Dice with code