TMU3113MS

USB Full Speed Controller

Data Sheet

AMENDMENT HISTORY

Version	Date	Description
V1.0	Mar, 2010	New release
V1.1	JAN,2012	Add Ordering Information table.

CONTENTS

1. GENERAL DESCRIPTION

The TMU3113MS is an 8-bit high performance MCU with mask type. It is 8051-based embedded device tailored to the USB full speed general purpose application. TMU3113MS is designed for connecting the PC or operating in stand-alone (non-PC) mode. It supports the powerful functions and interfaces, such as master/slave SPI and external parallel bus (I80 interface).

2. FEATURES

(1). Dual Power System

- USB 5V and/or battery-in dual power systems

(2). Operation Frequency

- FAST mode
  - 6MHz crystal oscillator for PLL clock source, PLL generate 48MHz for USB data transaction and 24MHz/6MHz for CPU clock
- SLOW mode
  - External resistor, RC oscillator at 2.0V~3.6V for battery system (optional)
  - 32KHz crystal oscillator for CPU clock and accuracy timing in low power mode (optional)
- STOP mode

(3). On-Chip Memory

- 24k x 8 internal Mask-ROM for program memory
- Internal RAM 256 bytes and external XRAM up to 320 bytes

(4). USB interface

- Compliance with the Universal Serial Bus specification v2.0 Full Speed
- Built-in USB Transceiver, 3.3V regulator
- Software Control USB pull-up resister
- Support USB Suspend /Resume and Remote Wakeup function
- Endpoint 0: Control SETUP transfer (8 bytes)
- Endpoint 0: Control IN/OUT transfer (64 bytes)
- Endpoint 1: BULK-IN transfer with Pin-Pong feature (2*64 bytes)
- Endpoint 2: BULK-OUT transfer with Pin-Pong feature (2*64 bytes)
- Endpoint 3: INTERRUPT IN transfer (8 bytes)

(9). I80 Interface (a.k.a. NAND-Flash interface)

- Data transfer for all of External XRAMs
- Write DMA (up to 64 bytes per time)
- Read DMA (up to 64 bytes per time)
- Compatible with 8-bit parallel interface

(10). SPI Interface

- Mode0, 1, 2, 3
- Master or Slave mode
- Clock Rate up to 12Mbps
- Read DMA (up to 64 bytes per time)
- Write DMA (up to 64 bytes per time)

(11). PWM

- Support 2 channels of Pulse Width Modulation (PWM) function with 8-bit resolution

(12). Reset Controller

- Power On Reset
- Low Voltage Reset
- Watch-Dog Timer
- USB Plug-in Reset
- Plug-out Reset

(13). Keep SRAM data when USB un-plug (need battery)

(14). I/O Ports

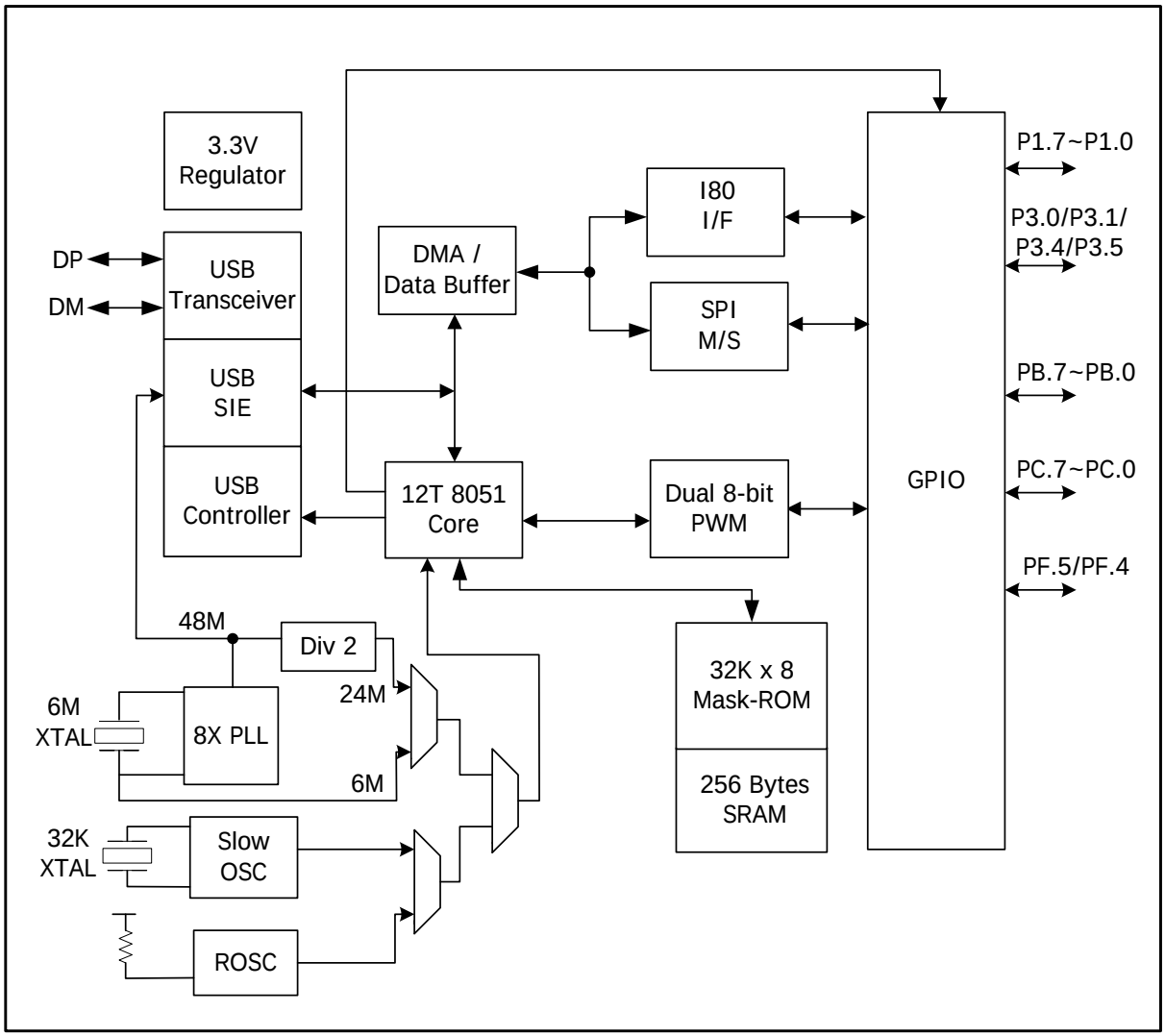
- Max. 30 GPIOs to flexible application
- 4 external Interrupts with wakeup function

(15). LQFP48 / Die Form / Customer Request

(16). Application

- USB full speed general purpose devices
- Portable picture viewer equipment (Digital Portable Framer)

3. Functional LOCK DIAGRAM



4. PIN DESCRIPTION

Name	I/O	Description			
VDD	P	5V Power from USB cable			
VSS	P	Ground			
VUSB	I	USB 5V detection pin, should connect to USB power			
VBAT	P	Battery power in			
V33	O	3.3V regulator output			
DP	I/O	USB positive data signal			
DM	I/O	USB negative data signal			
RSTN	I	Chip reset pin (internal pull-up)			
TSTN	I	Test Mode control (internal pull-up)			
FX1	I	Crystal in (6MHz)			
FX2	O	Crystal out			
VDDX	P	PLL power			
FLTC	I	PLL filter			
VSSX	P	PLL ground			
LX1	I	Crystal in (32KHz)			
LX2	O	Crystal out			
VR	I	RCLK clock, external resistor			
P1[7:0]	I/O	8051's Port1			
P3[1:0]	I/O	8051's Port3[1:0]			
P3.5/T0	I/O	8051's Port3.5 / Timer 0			
P3.4/T1	I/O	8051's Port3.4 / Timer 1			
PB[7:0]	I/O	GPIO (b)		I80_DIO[7:0] (b)	
PC[0]	I/O	GPIO with wake-up interrupt (b)		I80_WRN (o)	
PC[1]	I/O	GPIO with wake-up interrupt (b)		I80_RDN (o)	
PC[2]	I/O	GPIO with wake-up interrupt (b)			
PC[3]	I/O	GPIO with wake-up interrupt (b)			
PC[4]	I/O	GPIO (b)			PWMB out (o)
PC[5]	I/O	GPIO (b)			PWMA out (o)
PC[6]	I/O	GPIO (b)			SPICLK M(o), S(i)
PC[7]	I/O	GPIO (b)			SPI DOUT (o)
PF[4]	I/O	GPIO			SPI DIN (i)
PF[5]	I/O	GPIO			SPI CSN (i)

All I/O ports are pseudo open-drain type, unless otherwise specified function.

5. CPU Operation Mode V.S. Peripheral Clock

	DUAL MODE[1]		SIGNLE MODE[1]	NOTE
	SLOW [2]	FAST [2]		
CPUCLK(CPU51)	RCLK/32KHz	6M/24MHz	6M/24MHz	
USB function	N/A	48MHz	48MHz	XTAL_EN = 1
NAND(I80) DMA	N/A	6MHz	6MHz	
SPI	CPUCLK	CPUCLK	CPUCLK	
WDT	CPUCLK	CPUCLK	CPUCLK	
PWMA/B	CPUCLK	CPUCLK	CPUCLK	
0.5sec timer wakeup Interrupt	0.5sec	0.5sec	0.5sec	If 32KHz Xtal[3] is available

Notes:

(1) & (3) Function enable/disable control in FUSE option.

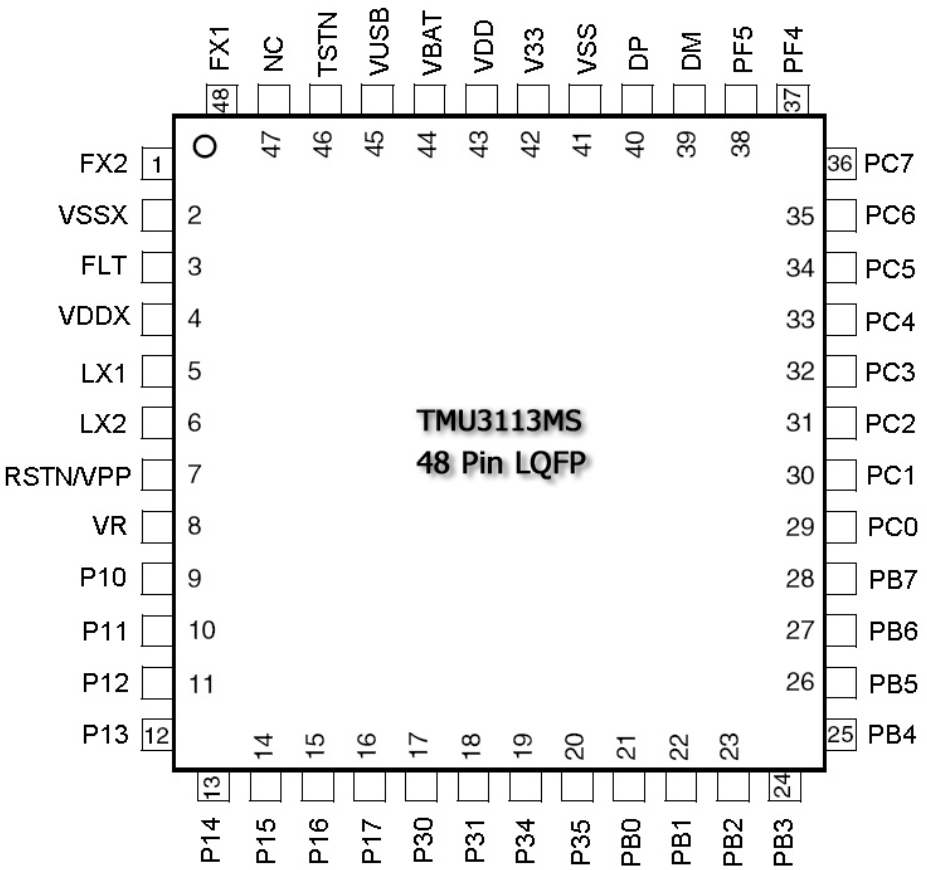
(2) CPU clock mode switching control by firmware

6. Code Options Fuse

	MOPT1	MOPT2	MOPT3
Name	**ENFLT[1]**	**ONLY_FAST**	**NO_USE_LX32K**
1	Use Internal PLL Filter	Fast Clock Only	Disable Low Crystal
0	Use External PLL Filter	FXT/PLL/R-OSC/LXT Selectable	Enable Low Crystal

Note:
(1): ENFLT fuse only be implemented in TMU3113MS, not in its OTP version, TMU3113.

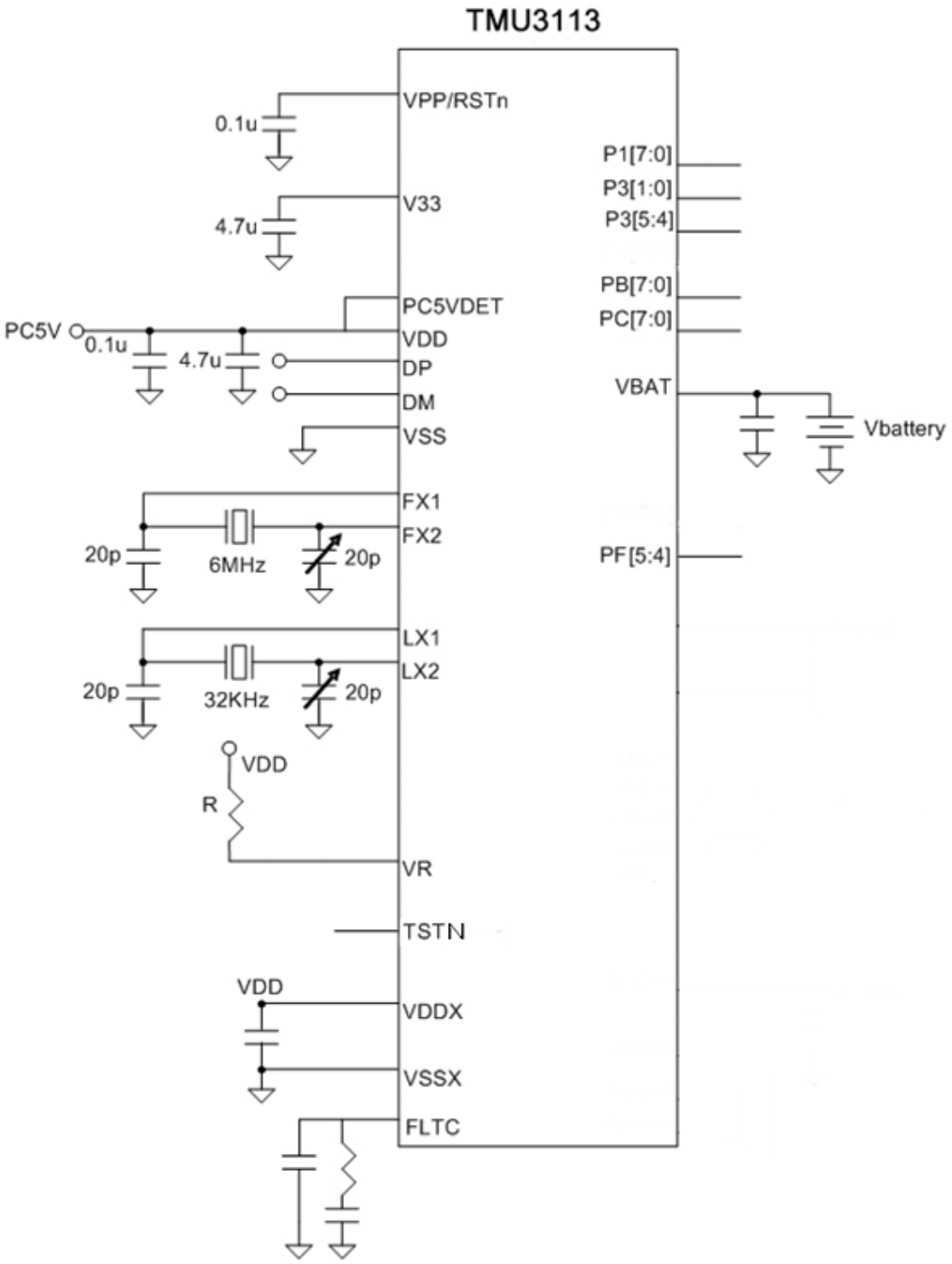
7. Package



CAUTION:

The VDD power pin is located at pin-43, however, the VDD pin is located at pin-42 in OTP version (TMU3113). The 3.3V internal regulator output (V33) is located at pin-42 while the same pin of OTP version is located at pin-43. User can design their application PCB carefully if the PCB is designed to support both OTP and MASK version of TMU3113.

8. Application Circuit



9. ELECTRICAL CHARACTERISTICS

(1). ABSOLOUTE MAXIMUM RATINGS (GND = 0V)

Name	Symbol	Range	Unit
Maximum Supply Voltage	VDD	-0.3 to 5.5	V
Maximum Input Voltage	Vin	-0.3 to VDD + 0.3	V
Maximum output Voltage	Vout	-0.3 to VDD + 0.3	V
Maximum Operating Temperature	Topg	-10 to + 70	℃
Maximum Storage Temperature	Tstg	-25 to + 125	℃

(2). RECOMMEND OPERATING CONDITION (at Ta = -10℃ to 70℃, GND = 0V)

Name	Symb.	Min.	Max.	Unit
Supply Voltage	VDD	2.2	5.5	V
Battery Voltage, if apply	Vbat	2.2	4.2	V
Input “H” Voltage	Vih	0.9 x VDD	VDD	V
Input “L” Voltage	Vil	0	0.1 x VDD	V

(3). DC CHARACTERISTICS

(at Ta = 25℃, VDD = 5.0V, VSS = 0V, unless otherwise specify)

Name	Symb.	Min.	Typ.	Max.	Unit	Condition	Note
FAST clock	fclk1		24		MHz	XT6MHz On, PLL enable	
	fclk2		6		MHz	XT6MHz On	
SLOW clock	sclk1	0.1		10	MHz	VBAT = 3.0V, VDD = N.C.	
	sclk2		32		KHz	XT32KHz On	
Operating current	Icc1		10		mA	fclk1 = 24MHz, XT6MHz On	No load
	Icc2		0.8		mA	XT6MHz Off, RCLK = 3MHz VBAT = 3.0V, VDD = N.C.	No load
Suspend current	Isus		360	500	uA	USB mode	No load
Power down current	Ipd1		3	5	uA	VDD = 3.0v, XT32KHz Off	No load
Output high current	Ioh1	2.5	3.8	-	mA	Voh = 3.0v, Vbat = 3.3v, VDD = N.C.	One clk time
	Ioh2	4	6	-	uA		
	Ioh3	2.5	3.8	-	mA		PWMA/B
	Ioh4	60	70	-	mA	VDD = 3.3V, Voh = VDD/2	Sph. PWM
Output low current	Iol1	10	15	-	mA	Vol = VSS + 0.4v,	GPIO
	Iol2	20	25	-	mA	Vol = VSS + 0.4v	PWMA/B
Input high voltage	Vih1	1.6		VDD	V	VDD = 3.2V, Vio = V33 = 3.2V PC5V = 0, Schmitt trigger	GPIO
	Vih2	1.7		VDD	V	VDD = 5.0V, Vio = V33 = 3.3V, PC5V > Vih3, Schmitt trigger	GPIO
	Vih3	2.8		VDD	V	Schmitt trigger	PC5V
Pull up resistance	Rup1	5	10	15	KΩ	VDD = 3.3 or 5V	VPP/RSTn
	Rup2	40	50	60	KΩ	VDD = 5V	TEST pin
Pull down resistance	Rdn1	50	100	150	KΩ	PC5V	
V33 pin voltage	V33	3.0	3.3	3.6	V	130mA, PC5V > Vih3	

(4). USB AC CHARACTERISTICS

(at Ta = 25℃, VDD = AVDD = 5.0V, VSS = AGND = 0V)

Name	Symb.	Min.	Typ.	Max.	Unit	Note
DP/DM rising time	Trise	4		20	ns	
DP/DM falling time	Tfall	4		20	ns	
DP,DM cross point	Vx	1.3		2.0	V	
V33 output voltage	Vreg	3.2	3.3	3.4	V	

Note: All USB transceiver characteristics can meet USB1.1 spec.

Ordering Information

The ordering information:

Ordering number	Package
TMU3113MS-COD	Wafer / Dice