



N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV _{DSS} / BV _{DGS}	R _{DS(ON)} (max)	I _{D(ON)} (min)	V _{GS(th)} (max)	Order Number / Package		
				TO-39	TO-92	DICE
60V	3Ω	2A	1.6V	TN0106N2	TN0106N3	TN0106ND
100V	3Ω	2A	1.6V	TN0110N2	TN0110N3	TN0110ND

Features

- Low threshold
- High input impedance
- Low input capacitance
- Fast switching speeds
- Low on resistance
- Freedom from secondary breakdown
- Low input and output leakage

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

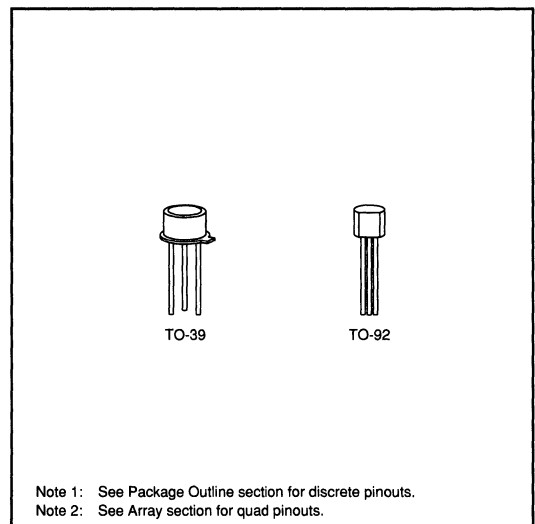
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- Solid state relays
- Battery operated systems
- Photo voltaic drive
- Analog switch
- General purpose line driver

Package Options

(Notes 1 and 2)



Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Note 1: See Package Outline section for discrete pinouts.

Note 2: See Array section for quad pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ $T_c = 25^\circ\text{C}$	θ_{jc} $^\circ\text{C/W}$	θ_{ja} $^\circ\text{C/W}$	I_{DR}	I_{DRM}^*
TO-92	0.5A	2.0A	1.0W	170	125	1.0A	4.0A
TO-39	0.8A	2.5A	3.5W	125	35	2.5A	5.0A

* I_D (continuous) is limited by max rated T_j .

Electrical Characteristics (@ 25°C unless otherwise specified)

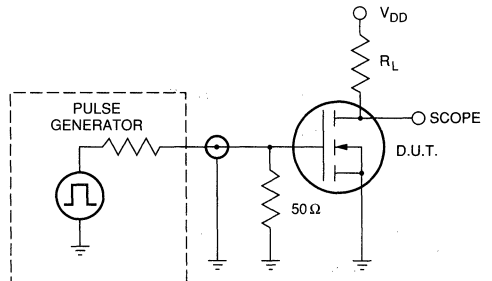
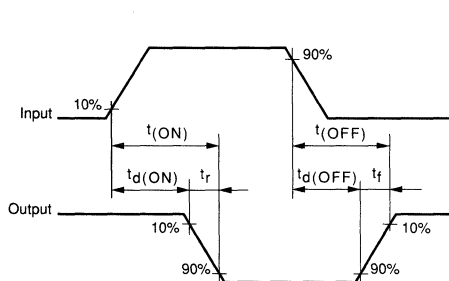
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN0110	100			V $I_D = 1\text{mA}, V_{GS} = 0$
		TN0106	60			
$V_{GS(th)}$	Gate Threshold Voltage	0.6		1.6	V	$V_{GS} = V_{DS}, I_D = 0.5\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-3.2	-5.0	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = 1.0\text{mA}$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current			10	μA	$V_{GS} = 0, V_{DS} = \text{Max Rating}$
				500		$V_{GS} = 0, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	0.75	1.5		A	$V_{GS} = 5\text{V}, V_{DS} = 25\text{V}$
		2.0	3.5			$V_{GS} = 10\text{V}, V_{DS} = 25\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		2.5	4.5	Ω	$V_{GS} = 5\text{V}, I_D = 250\text{mA}$
			2.0	3.0		$V_{GS} = 10\text{V}, I_D = 500\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		0.6	1.1	%/ $^\circ\text{C}$	$I_D = 0.5\text{A}, V_{GS} = 10\text{V}$
G_{FS}	Forward Transconductance	225	400		m Ω	$V_{DS} = 25\text{V}, I_D = 500\text{mA}$
C_{ISS}	Input Capacitance		50	60	pF	$V_{GS} = 0, V_{DS} = 25\text{V}$ $f = 1\text{MHz}$
C_{OSS}	Common Source Output Capacitance		25	35		
C_{RSS}	Reverse Transfer Capacitance		4	8		
$t_{d(ON)}$	Turn-ON Delay Time		2	5		
t_r	Rise Time		3	5	ns	$V_{DD} = 25\text{V}$ $I_D = 1.0\text{A}$ $R_S = 50\Omega$
$t_{d(OFF)}$	Turn-OFF Delay Time		6	7		
t_f	Fall Time		3	5		
V_{SD}	Diode Forward Voltage Drop		1	1.5	V	$I_{SD} = 0.5\text{A}, V_{GS} = 0$
t_{rr}	Reverse Recovery Time		400		ns	$I_{SD} = 0.5\text{A}, V_{GS} = 0$

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

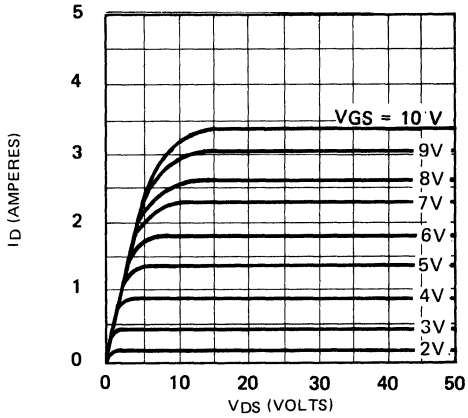
Switching Waveforms and Test Circuit



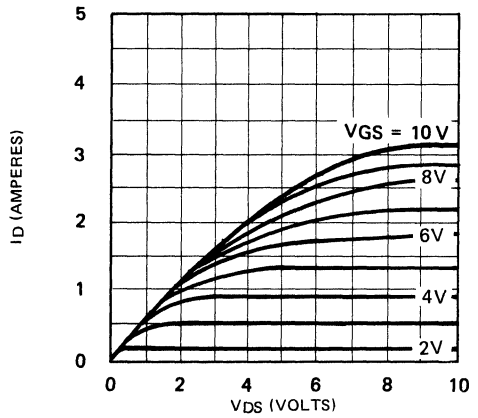
Typical Performance Curves

TN01A

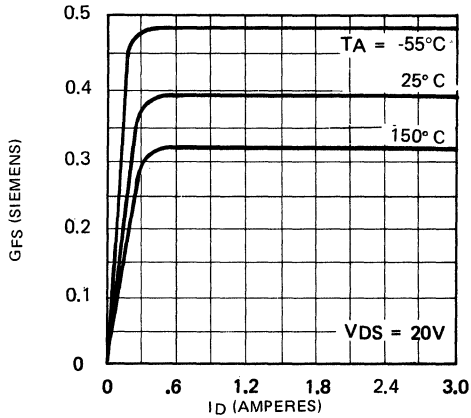
Output Characteristics



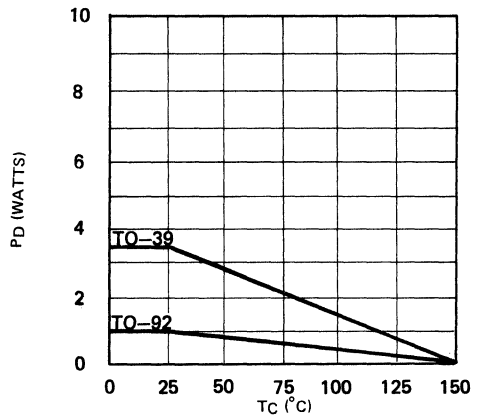
Saturation Characteristics



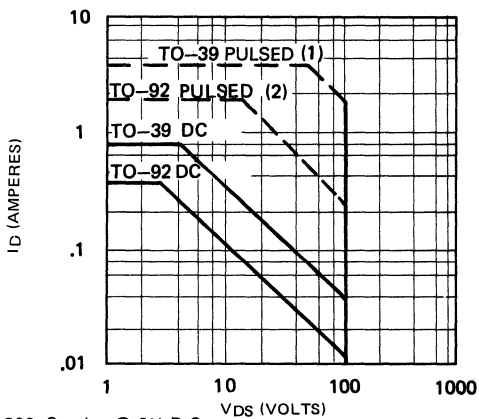
Transconductance Vs. Drain Current



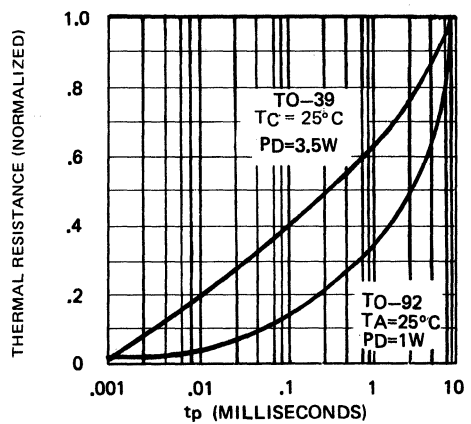
Power Dissipation Vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



- (1) 300 μs pulse @ 2% D.C.
- (2) 10 μs pulse @ 2% D.C.

Typical Performance Curves

