Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package					
				TO-39	TO-92	TO-220	Quad P-DIP	Quad C-DIP	DICE
60V	1.5Ω	3.0A	1.6V	TN0606N2	TN0606N3	TN0606N5	TN0606N6	TN0606N7	TN0606ND
100V	1.5Ω	3.0A	1.6V	TN0610N2	TN0610N3	TN0610N5	—	—	TN0610ND

Features

- ☐ Low threshold
- ☐ High input impedance
- ☐ Low input capacitance
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Freedom from secondary breakdown
- ☐ Low input and output leakage

Advanced DMOS Technology

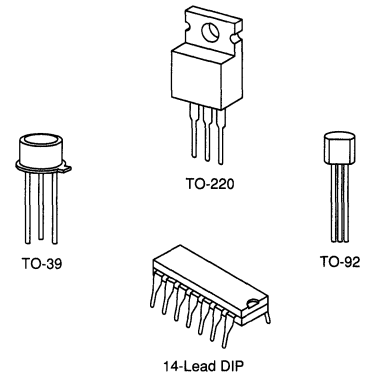
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Logic level interface
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switch
- ☐ General purpose line driver

Package Options (Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-92	0.8A	4A	1W	125	170	0.8A	4.0A
TO-39	1.5A	4A	—	20	125	1.5A	4.0A
T0-220	3.0A	4A	28W	2.7	70	3.0A	4.0A
PLASTIC DIP	Refer to Arrays & Special Functions Section.						
CERAMIC DIP							

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

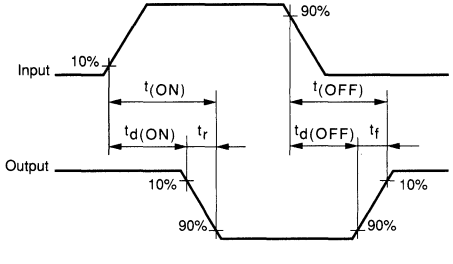
(Notes 1 and 2)

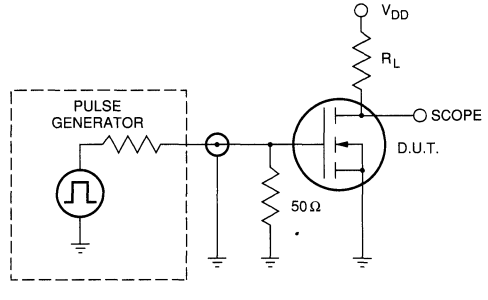
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN0610	100			V	V_{GS} = 0, I_D = 1mA
		TN0606	60				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.6	V	V_{GS} = V_{DS}, I_D = 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-4.5	mV/°C	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				10	μA	V_{GS} = 0, V_{DS} = Max Rating
					1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C (note 2)
$I_{D(ON)}$	ON-State Drain Current		1.2	2.0		A	V_{GS} = 5V, V_{DS} = 25V
			3.0	6.0			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			1.5	2.0	Ω	V_{GS} = 5V, I_D = 0.75A
				1.0	1.5		V_{GS} = 10V, I_D = 0.75A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				0.75	%/°C	
G_{FS}	Forward Transconductance		0.4	0.6		℧	V_{DS} = 25V, I_D = 1.0A
C_{ISS}	Input Capacitance			85	150	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			50	85		
C_{RSS}	Reverse Transfer Capacitance			10	35		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = 25V, I_D = 1.5A, R_S = 50Ω
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				10		
V_{SD}	Diode Forward Voltage Drop			0.8	1.8	V	V_{GS} = 0, I_{SD} = 1.5A
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = 1.5A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

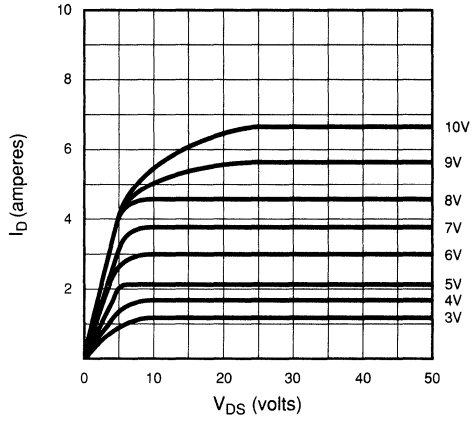
Switching Waveforms and Test Circuit



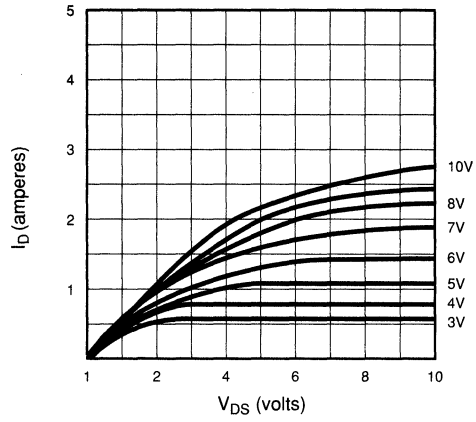


Typical Performance Curves

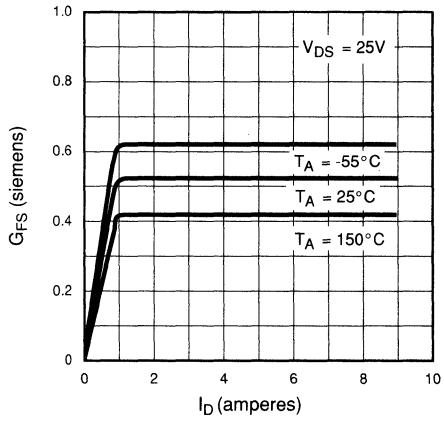
Output Characteristics



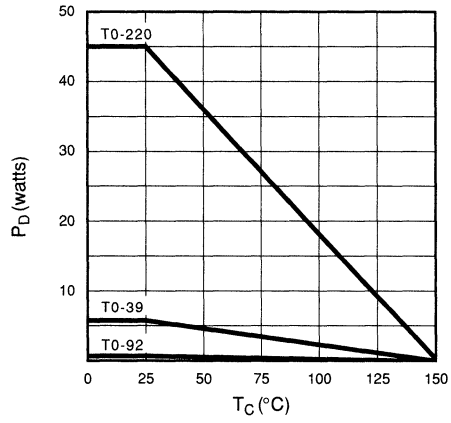
Saturation Characteristics



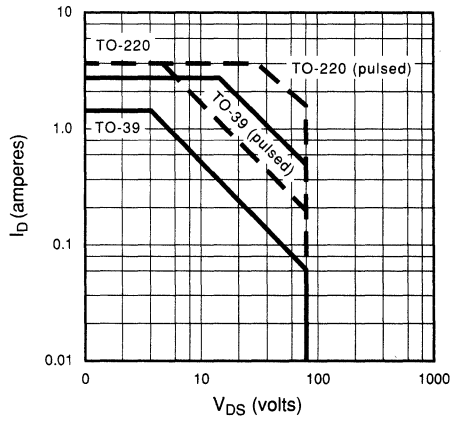
Transconductance vs. Drain Current



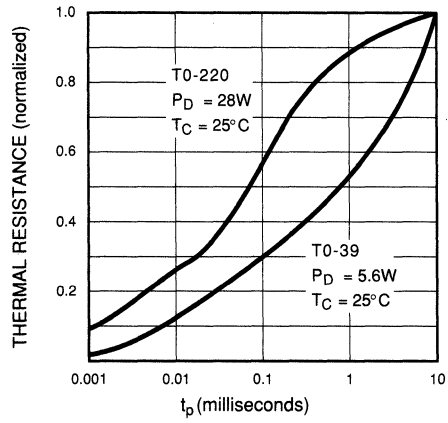
Power Dissipation vs. Case Temperature



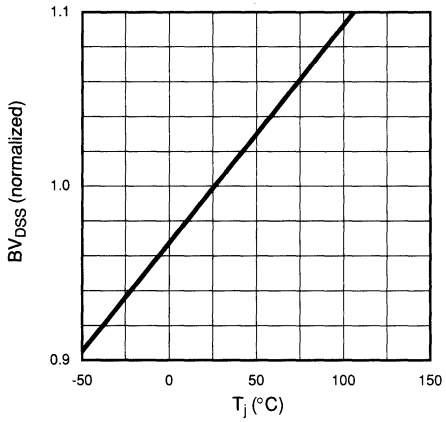
Maximum Rated Safe Operating Area



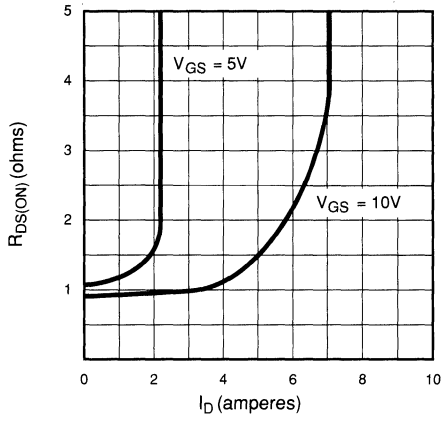
Thermal Response Characteristics



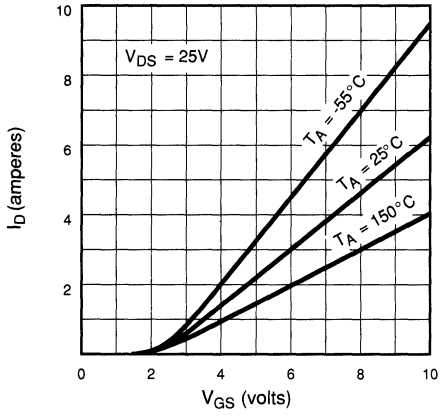
BV$_{DSS}$ Variation with Temperature



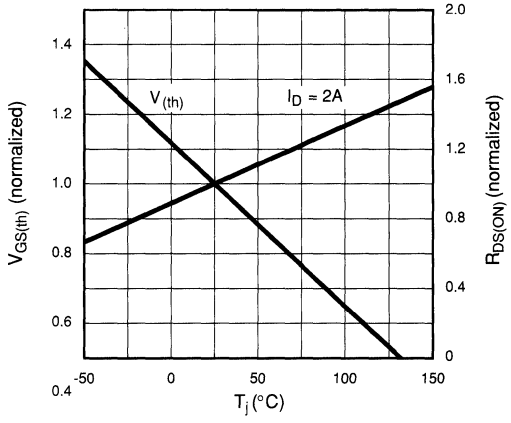
On-Resistance vs. Drain Current



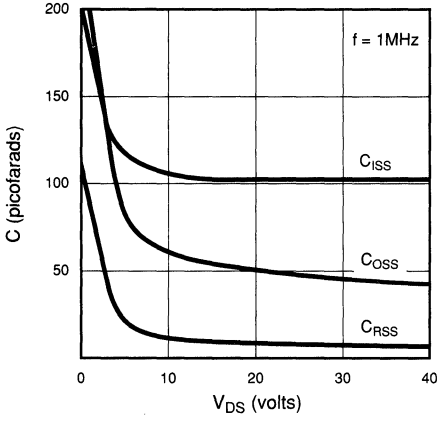
Transfer Characteristics



$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics