N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package			
				TO-39	TO-92	SOW-20*	DICE
20V	0.75Ω	4.0A	1.6V	TN0602N2	TN0602N3	—	TN0602ND
40V	0.75Ω	4.0A	1.6V	TN0604N2	TN0604N3	TN0604WG	TN0604ND

*Same as SO-20 with 300 mil wide body.

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

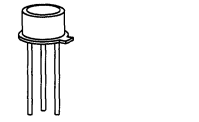
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

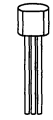
Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps Memories, Displays, Bipolar Transistors, etc.)

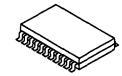
Package Options (Notes 1 and 2)



TO-39



TO-92



SOW-20

Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-39	2.5A	4.6A	4W	35	125	2.5A	4.6A
TO-92	1.0A	4.6A	1W	125	170	1.0A	4.6A
SOW-20	Refer to Arrays & Special Functions Section.						

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

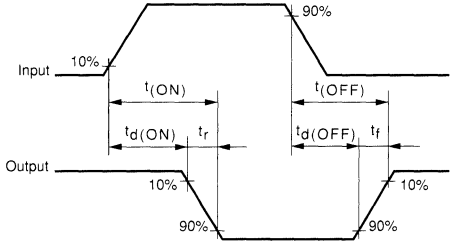
(Notes 1 and 2)

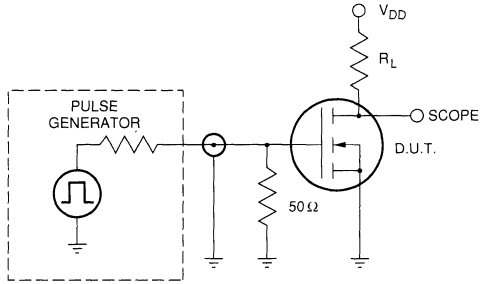
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN0604	40			V	V_{GS}= 0, I_D = 2.0mA
		TN0602	20				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.6	V	V_{GS} = V_{DS}, I_D = 1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-4.5	mV/°C	V_{GS} = V_{DS}, I_D = 2.5mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Crain Current				10	µA	V_{GS} = 0, V_{DS} = Max Rating
					1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		1.5	2.1		A	V_{GS} = 5V, V_{DS} = 25V
			4.0	7.0			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			0.8	1.5	Ω	V_{GS} = 5V, I_D = 0.75A
				0.60	0.75		V_{GS} = 10V, I_D = 1.5A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.5	0.75	%/°C	V_{GS} = 10V, I_D = 2.0A
G_{FS}	Forward Transconductance		0.5	1.0		℧	V_{DS} = 25V, I_D = 2.0A
C_{ISS}	Input Capacitance			85	150	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			50	85		
C_{RSS}	Reverse Transfer Capacitance			12	35		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = 25V, I_D = 0.5A, R_S = 50Ω
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				25		
t_f	Fall Time				13		
V_{SD}	Diode Forward Voltage Drop			-1.2	-1.8	V	V_{GS} = 0, I_{SD} = 1.5A
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = 1A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

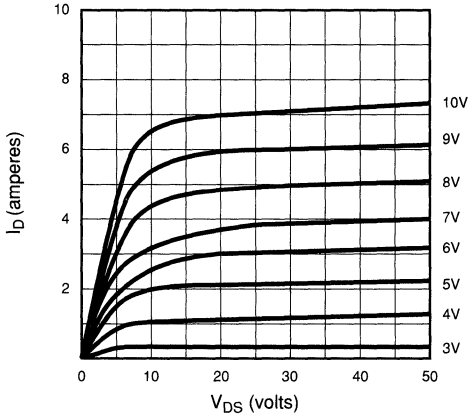
Switching Waveforms and Test Circuit



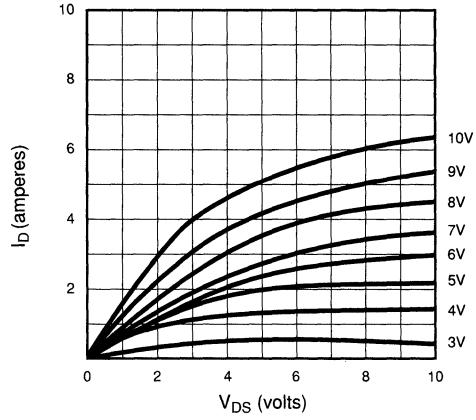


Typical Performance Curves

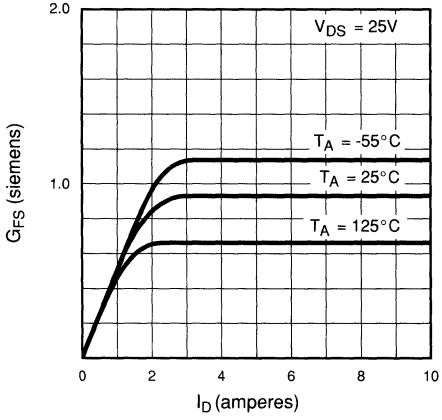
Output Characteristics



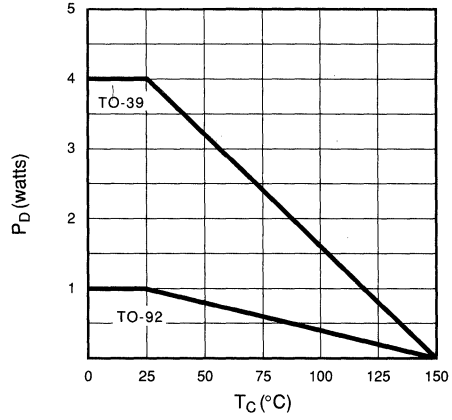
Saturation Characteristics



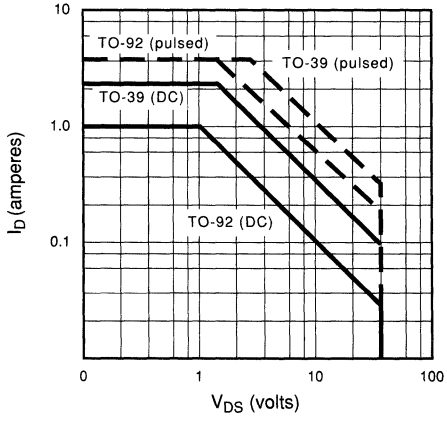
Transconductance vs. Drain Current



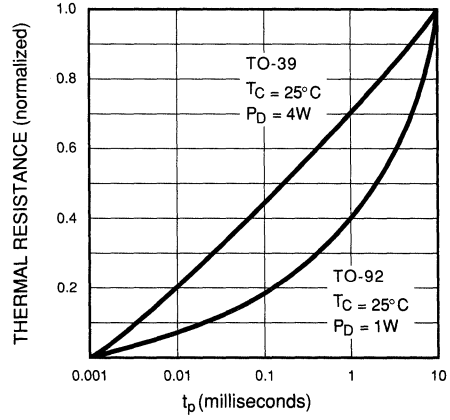
Power Dissipation vs. Case Temperature



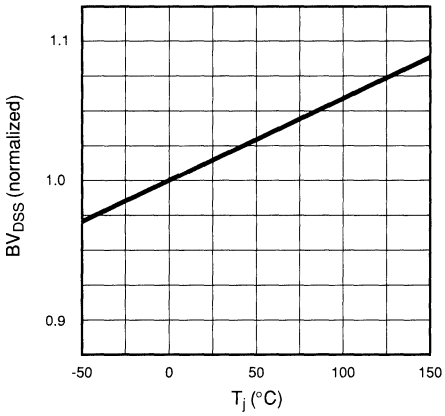
Maximum Rated Safe Operating Area



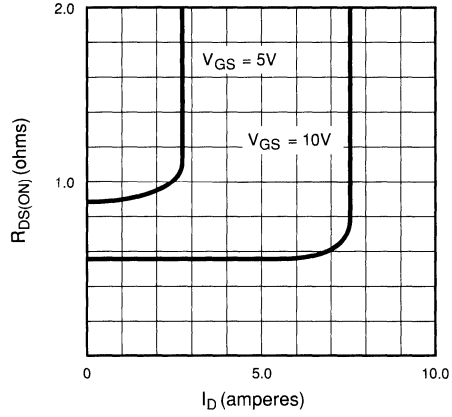
Thermal Response Characteristics



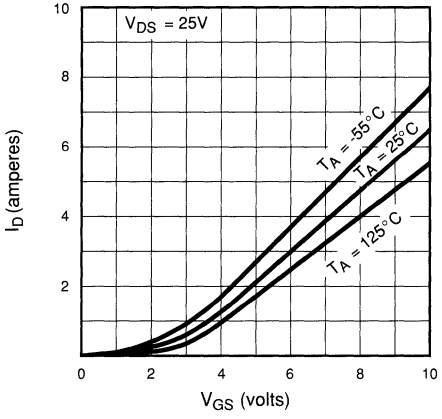
BV$_{DSS}$ Variation with Temperature



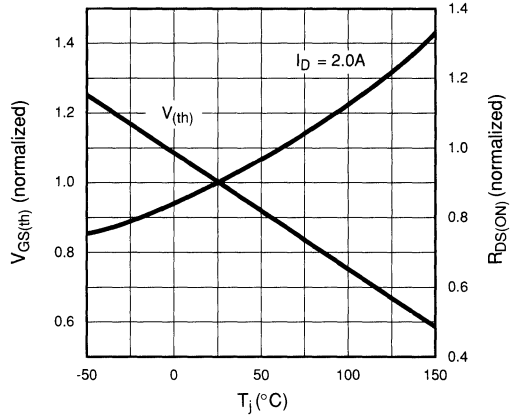
On-Resistance vs. Drain Current



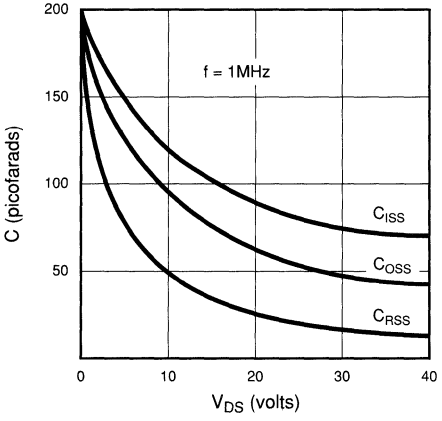
Transfer Characteristics



$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics