TN2130

N-Channel Enhancement-Mode Vertical DMOS FET

Features

- · Free from Secondary Breakdown
- · Low Power Drive Requirement
- · Ease of Paralleling
- Low C_{ISS} and Fast Switching Speeds
- · Excellent Thermal Stability
- · Integral Source-Drain Diode
- · High Input Impedance and High Gain

Applications

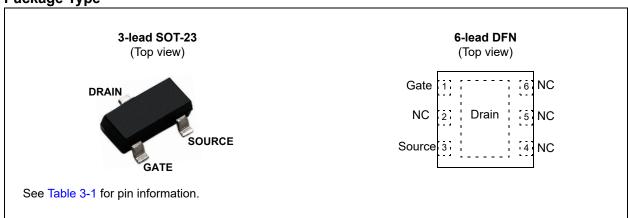
- Logic-Level Interfaces (Ideal for TTL and CMOS)
- · Solid-State Relays
- · Battery-Operated Systems
- · Photovoltaic Drives
- · Analog Switches
- · General Purpose Line Drivers
- · Telecommunication Switches

General Description

The TN2130 low-threshold, Enhancement-mode (normally-off) transistor uses a vertical DMOS structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Type



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	±20V
Operating Ambient Temperature, T _A	55°C to +150°C
Storage Temperature, T _S	55°C to +150°C
ESD Protection (HBM) TN2130MF-G	
Drain-to-Source	±8 kV
Gate-to-Drain	500V
Gate-to-Source	<±250V
ESD Protection (CDM) TN2130MF-G	±1 kV

[†] Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended.

Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS - COMMERCIAL

Electrical Specifications: $T_A = T_J = 25^{\circ}\text{C}$ unless otherwise specified. All DC parameters are 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μ s pulse, 2% duty cycle)

Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	BV _{DSS}	300	_	_	V	$V_{GS} = 0V$, $I_D = 1 \text{ mA}$
Gate Threshold Voltage	V _{GS(th)}	8.0	_	2.4	V	$V_{GS} = V_{DS}$, $I_D = 1 \text{ mA}$
Change in V _{GS(th)} with Temperature	$\Delta V_{GS(th)}$	_	_	-5.5	mV/°C	V _{GS} = V _{DS} , I _D = 1 mA (Note 1)
Gate Body Leakage Current	I _{GSS}	_	_	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
	I _{DSS}	_		10	μΑ	V _{GS} = 0V, V _{DS} = Maximum rating
Zero-Gate Voltage Drain Current				100	μΑ	V_{DS} = 0.8 Maximum rating, V_{GS} = 0V, T_A = 125°C (Note 1)
On-State Drain Current	I _{D(ON)}	250		_	mA	$V_{GS} = 10V, V_{DS} = 25V$
Static Drain-to-Source On-State Resistance	R _{DS(ON)}	_	_	25	Ω	$V_{GS} = 4.5V, I_D = 120 \text{ mA}$
Change in R _{DS(ON)} with Temperature	ΔR _{DS(ON)}	_		1.1	%/°C	V _{GS} = 4.5V, I _D = 120 mA (Note 1)

Note 1: Specification is obtained by characterization and is not 100% tested.

DC ELECTRICAL CHARACTERISTICS - AUTOMOTIVE

Electrical Specifications: Boldface specification limits apply over the full operating temperature range of $T_A = T_J = -55$ °C, 25°C, and 150°C unless otherwise specified. Non-boldfaced specification limits apply only to $T_A = T_J = 25$ °C unless otherwise specified. All DC parameters are 100% tested at all three temperatures unless otherwise specified. (Pulse test: 300 µs pulse, 2% duty cycle.)

Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	BV _{DSS}	300	_	_	V	V_{GS} = 0V, I_D = 1 mA
Cata Threshold Voltage	V	0.8	_	2.4	>	$V_{GS} = V_{DS}$, $I_D = 1 \text{ mA}$
Gate Threshold Voltage	V _{GS(th)}	0.7	_	2.4	>	$V_{DS} = V_{GS}$, $I_D = 1 \text{ mA}$
Change in V _{GS(th)} with Temperature	$\Delta V_{GS(th)}$	_	-3.6		mV/°C	$V_{GS} = V_{DS}$, $I_D = 1 \text{ mA}$ (Note 1)

Note 1: Specification is obtained by characterization and is not 100% tested.

DC ELECTRICAL CHARACTERISTICS - AUTOMOTIVE (CONTINUED)

Electrical Specifications: Boldface specification limits apply over the full operating temperature range of $T_A = T_J = -55^{\circ}\text{C}$, 25°C, and 150°C unless otherwise specified. Non-boldfaced specification limits apply only to $T_A = T_J = 25^{\circ}\text{C}$ unless otherwise specified. All DC parameters are 100% tested at all three temperatures unless otherwise specified. (Pulse test: 300 µs pulse, 2% duty cycle.)

Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions
Gate Body Leakage Current	1	_	_	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
Gate Body Leakage Current	I _{GSS}	_	_	200	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
Zoro Cata Valtaga Prain Current	oin Current		_	10	μA	V _{GS} = 0V, V _{DS} = Maximum rating
Zero-Gate Voltage Drain Current	I _{DSS}	_	_	100	μA	V _{GS} = 0V, V _{DS} = Maximum rating
On-State Drain Current	I _{D(ON)}	250	_	_	mA	$V_{GS} = 10V, V_{DS} = 25V$
Static Drain-to-Source On-State	В	_	_	25	Ω	V_{GS} = 4.5V, I_{D} = 120 mA
Resistance R _{DS(ON)}		_	_	66	Ω	V_{GS} = 4.5V, I_{D} = 120 mA
Change in R _{DS(ON)} with Temperature	$\Delta R_{DS(ON)}$	_	1.1	_	%/°C	V _{GS} = 4.5V, I _D = 120 mA (Note 1)

Note 1: Specification is obtained by characterization and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS - COMMERCIAL

Electrical Specifications: T_A = T_J = 25°C unless otherwise specified. Specification is obtained by characterization and is not 100% tested.

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Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions			
Forward Transconductance	G _{FS}	_	250	_	mmho	V _{DS} = 25V, I _D = 100 mA			
Input Capacitance	C _{ISS}	_	_	50	pF	V _{GS} = 0V,			
Common Source Output Capacitance	Coss	_	_	15	pF	$V_{DS} = 25V$,			
Reverse Transfer Capacitance	C _{RSS}	_	_	5	pF	f = 1 MHz			
Turn-On Delay Time	t _{d(ON)}	_	_	10	ns				
Rise Time	t _r	_	_	7	ns	V _{DD} = 25V, I _D = 120 mA,			
Turn-Off Delay Time	t _{d(OFF)}	_	_	12	ns	$R_{GEN} = 25\Omega$			
Fall Time	t _f	_	_	15	ns	GEN			
DIODE PARAMETER									
Diode Forward Voltage Drop	V _{SD}		_	1.8	٧	V _{GS} = 0V, I _{SD} = 120 mA (Note 1)			
Reverse Recovery Time	t _{rr}	_	400	_	ns	V _{GS} = 0V, I _{SD} = 120 mA			

Note 1: All DC parameters are 100% tested at 25°C unless otherwise stated. (Pulse test: 300 µs pulse, 2% duty cycle)

AC ELECTRICAL CHARACTERISTICS – AUTOMOTIVE

Electrical Specifications: T _A = 25°C unless otherwise specified. All AC parameters are sample tested.									
Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions			
Forward Transconductance	G _{FS}	_	205	_	mmho	V _{DS} = 25V, I _D = 100 mA			
Input Capacitance	C _{ISS}	_	29	_	pF	V _{GS} = 0V,			
Common Source Output Capacitance	Coss	_	6	_	pF	V _{DS} = 25V,			
Reverse Transfer Capacitance	C _{RSS}	_	1.2	_	pF	f = 1 MHz			

Note 1: 100% Production Tested at $T_A = T_J = (-55^{\circ}C, 25^{\circ}C, and 150^{\circ}C)$.

AC ELECTRICAL CHARACTERISTICS – AUTOMOTIVE (CONTINUED)

Electrical Specifications: T _A = 25°C unless otherwise specified. All AC parameters are sample tested.								
Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions		
Turn-On Delay Time	t _{d(ON)}		6.8	_	ns			
Rise Time	t _r	_	3		ns	$V_{DD} = 25V,$		
Turn-Off Delay Time	t _{d(OFF)}	_	12	_	ns	$V_{DD} = 25V,$ $I_{D} = 120 \text{ mA},$ $R_{GEN} = 25\Omega$		
Fall Time	t _f	_	7	_	ns	-GEN		
DIODE PARAMETER								
Diode Forward Voltage Drop	V _{SD}	_	_	1.8	V	V _{GS} = 0V, I _{SD} = 120 mA (Note 1)		
Reverse Recovery Time	t _{rr}		450	_	ns	V _{GS} = 0V, I _{SD} = 120 mA		

Note 1: 100% Production Tested at $T_A = T_J = (-55^{\circ}C, 25^{\circ}C, and 150^{\circ}C)$.

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions				
TEMPERATURE RANGE										
Operating Ambient Temperature	T _A	-55	_	+150	°C					
Storage Temperature	T _S	-55	_	+150	°C					
PACKAGE THERMAL RESISTANCE										
3-lead SOT-23	θ_{JA}	_	203	_	°C/W					
6-lead DFN	θ_{JA}	_	102	_	°C/W					

THERMAL CHARACTERISTICS

Package	I _D (Note 1) (Continuous) (mA)	I _D (Pulsed) (mA)	Power Dissipation at T _A = 25°C (W)	I _{DR} (Note 1) (mA)	I _{DRM} (mA)
3-lead SOT-23	85	200	0.36	85	200

Note 1: I_D (continuous) is limited by maximum rated T_J .

2.0 TYPICAL PERFORMANCE CURVES

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

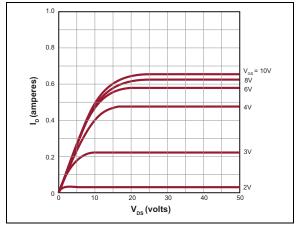


FIGURE 2-1: Output Characteristics.

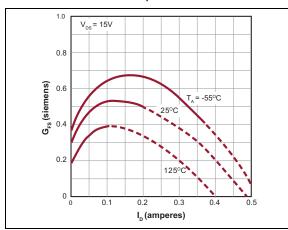


FIGURE 2-2: Transconductance vs. Drain Current.

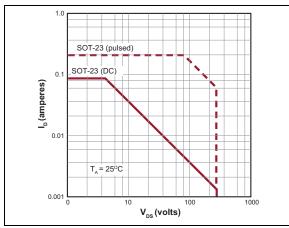


FIGURE 2-3: Maximum Rated Safe Operating Area.

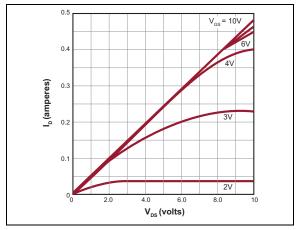


FIGURE 2-4: Saturation Characteristics.

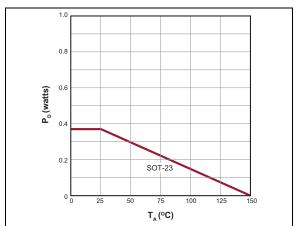


FIGURE 2-5: Power Dissipation vs. Case Temperature.

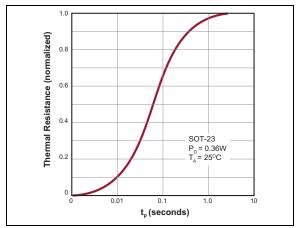


FIGURE 2-6: Thermal Response Characteristics.

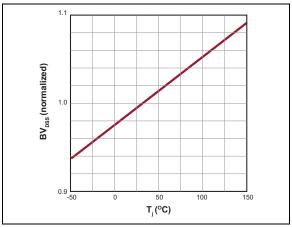


FIGURE 2-7: Temperature.

BV_{DSS} Variation with

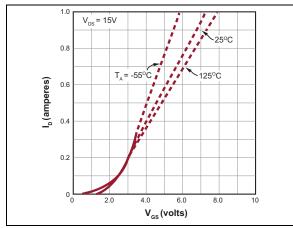


FIGURE 2-8:

Transfer Characteristics.

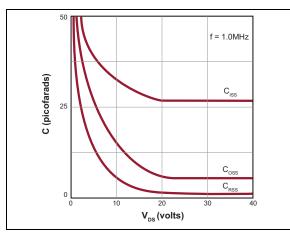


FIGURE 2-9: Capacitance vs Drain-to-Source Voltage.

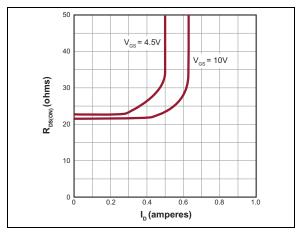


FIGURE 2-10: Current.

On-Resistance vs. Drain

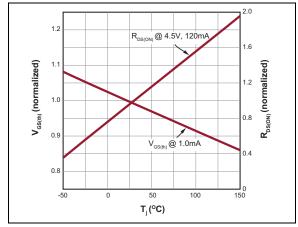


FIGURE 2-11: $V_{GS(th)}$ and R_{DS} Variation with Temperature.

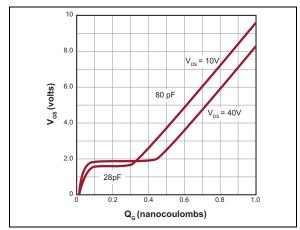


FIGURE 2-12: Characteristics.

Gate Drive Dynamic

3.0 PIN DESCRIPTION

The details on the pins of TN2130 are listed in Table 3-1. Refer to **Package Type** for the location of pins.

TABLE 3-1: PIN FUNCTION TABLE

Pin N	umber	Nama	Description
SOT-23	DFN	Name	Description
1	1	Gate	Gate
2	3	Source	Source
3	4,5,6	NC	Not Connected. Recommended to connect to Drain.
_	2	NC	Not Connected.
_	Exposed Pad	Drain	Drain

4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for TN2130.

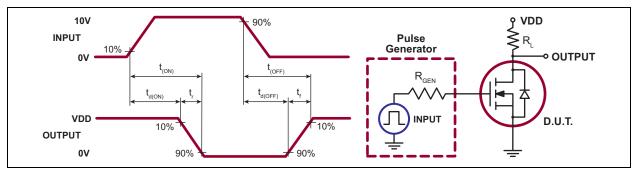


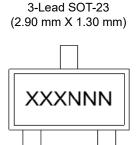
FIGURE 4-1: Switching Waveforms and Test Circuit.

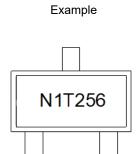
TABLE 4-1: PRODUCT SUMMARY

BV _{DSS} /BV _{DGS} (V)	R _{DS(ON)} (Maximum) (Ω)	V _{GS(th)} (Maximum) (V)
300	25	2.4

5.0 PACKAGING INFORMATION

5.1 Package Marking Information





6-Lead DFN (2.00 mm X 2.00 mm)





ABM 256

Legend: XX...X Product Code or Customer-specific information

Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')

NNN Alphanumeric traceability code

e3 Pb-free JEDEC designator for Matte Tin (Sn)

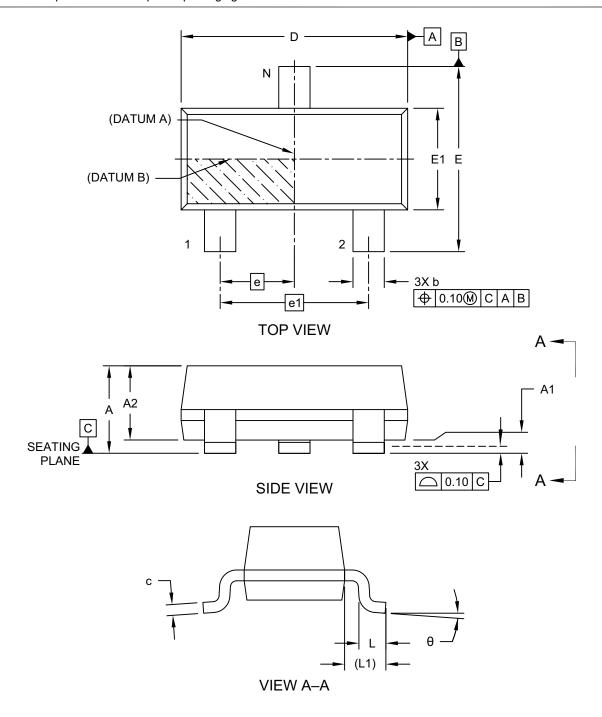
This package is Pb-free. The Pb-free JEDEC designator (@3)

can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.

3-Lead Small Outline Transistor (C6X) - [SOT-23] Supertex Legacy Package (K1/T)

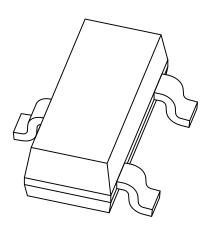
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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3-Lead Small Outline Transistor (C6X) - [SOT-23] Supertex Legacy Package (K1/T)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS			
Dim	ension Limits	MIN	NOM	MAX	
Number of Terminals	N		3		
Pitch	е		0.95 BSC		
Overall Pitch	e1		1.90 BSC		
Overall Height	А	0.89	_	1.12	
Standoff	A1	0.01	_	0.10	
Molded Package Thickness	A2	0.88	0.95	1.02	
Overall Length	D	2.80	2.90	3.04	
Overall Width	E	2.10	_	2.64	
Molded Package Width	E1	1.20	1.30	1.40	
Terminal Width	b	0.30	_	0.50	
Terminal Thickness	С	0.08	_	0.20	
Terminal Length	L	0.20	0.50	0.60	
Footprint	L1	0.54 REF			
Foot Angle	θ	0°	-	8°	

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Dimensioning and tolerancing per ASME Y14.5M

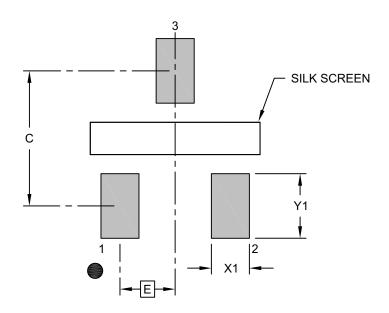
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-17458 Rev A $\,$ Sheet 2 of 2 $\,$

3-Lead Small Outline Transistor (C6X) - [SOT-23] Supertex Legacy Package (K1/T)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch	Е	0.95 BSC		
Contact Pad Spacing	С	2.30		
Contact Pad Width (X3)	X1			0.65
Contact Pad Length (X3) Y1				1.10

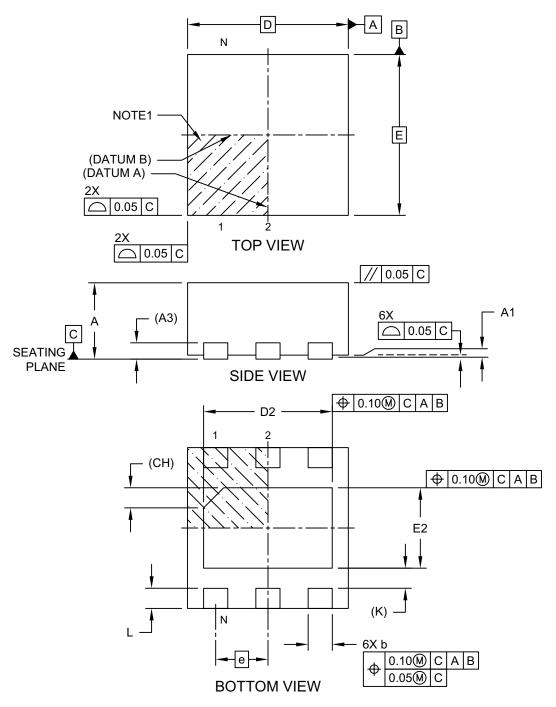
Notes:

- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- 2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-19458 Rev A

6-Lead Plastic Dual Flat, No Lead Package (7AX) - 2x2x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

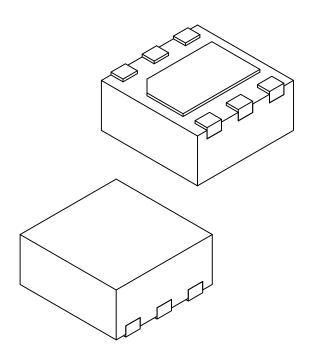


Microchip Technology Drawing C04-120-7AX Rev D Sheet 1 of 2

Note:

6-Lead Plastic Dual Flat, No Lead Package (7AX) - 2x2x0.9 mm Body [DFN]

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimension	MIN	NOM	MAX		
Number of Terminals	N		6		
Pitch	е		0.65 BSC		
Overall Height	Α	0.80	0.87	0.95	
Standoff	A1	0.00 0.02 0.05			
Terminal Thickness	A3	0.203 REF			
Overall Length	D	2.00 BSC			
Exposed Pad Length	D2	1.50 1.60 1.70			
Overall Width	Е	2.00 BSC			
Exposed Pad Width	E2	0.90	1.00	1.10	
Chamfer	CH	0.25 REF			
Terminal Width	b	0.25 0.30 0.35			
Terminal Length	L	0.20 0.25 0.30			
Terminal-to-Exposed-Pad	K	0.25 REF			

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated
- 3. Dimensioning and tolerancing per ASME Y14.5M

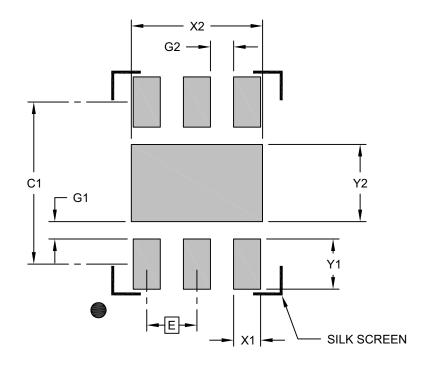
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-120-7AX Rev D Sheet 2 of 2

6-Lead Plastic Dual Flat, No Lead Package (7AX) - 2x2x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch	Е	E 0.65 BSC		
Center Pad Width	X2			1.70
Center Pad Length	Y2			1.00
Contact Pad Spacing	C1		1.70	
Contact Pad Width (X6)	X1			0.35
Contact Pad Length (X6)	Y1			0.65
Contact Pad to Center Pad (X6)		0.20		
Contact Pad to Contact Pad (X4)	G2	0.25		

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- 2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2120-7AX Rev D

Т	N	2	1	3	N
		_		v	v

NOTES:

APPENDIX A: REVISION HISTORY

Revision D (March 2023)

- Added 6-Lead DFN package to Package Type, Pin Function Table and Product Identification System.
- Updated Absolute Maximum Ratings^(†).
- Updated Section 5.1, Package Marking Information.
- Made minor text changes throughout the document.

Revision C (March 2022)

- Updated tables DC Electrical Characteristics Automotive and AC Electrical Characteristics – Automotive.
- Updated Section 5.1, Package Marking Information.
- Updated Product Identification System format.
- · Updated legal and contact information.

Revision B (June 2020)

- Added automotive specifications to the Electrical Characteristics section.
- Added automotive specifications to the Product Information System section.
- Made minor text changes throughout the document.

Revision A (April 2019)

- Converted Supertex Doc# DSFP-TN2130 to Microchip DS20005944A.
- · Changed the package marking format.
- Made minor text changes throughout the document.

TN2	1	3	0
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NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	<u>xx</u>	<u>-X</u>	<u>-XXX</u>	E	xamples:	
Device	Packag	je Environmental	Qualification	а) TN2130K1-G:	N-Channel Enhancement-Mode, Vertical DMOS FET, 3-lead SOT-23 package, 3000/Reel
Device:	TN2130:		i-Mode Vertical DMOS FET) TN2130K1-G-VAO:	N-Channel Enhancement-Mode Vertical DMOS FET, 3-lead SOT-23 package, 3000/Reel, Automotive Grade
Package:	K1 MF	= 3-lead SOT-23 = 6-Lead DFN		C) TN2130MF-G-VAO:	N-Channel Enhancement-Mode Vertical DMOS FET, 6-lead DFN package,
Environmental: Media Type:	G (Blank)	= Lead (Pb)-free/RoHS-c = 3000/Reel for both K1 a		d) TN2130MF-G:	3000/Reel, Automotive Grade N-Channel Enhancement-Mode Vertical DMOS FET, 6-Lead DFN package, 3000/Reel
Qualification:	(Blank) VAO	= Standard Part = Automotive AEC-Q100	Ç			
		, tate means / teo-Q 100	Quality	_		

NOTES:

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not
 mean that we are guaranteeing the product is "unbreakable" Code protection is constantly evolving. Microchip is committed to
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ISBN: 978-1-6683-2161-4



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