Data Sheet of TOH3003
Bluetooth Single Chip for Headset

(Preliminary)

Revise date：11/23/2007

1. Scope

The document is a specification of TOH3003.

1.1 Document Information

Document No. :					
Version :	01	**Total Page:**	34	**Date:**	11/23/2007
Title :	ASIC Data Sheet				
Product Name :	TOH3003				

1.2 Update History

Version	Date/name	Description
01	2006/11/23	Established

Contents

Overview

The TOH3003 is a highly-integrated digital/mixed-signal IC for use as Bluetooth Transceiver. This chip is specifically designed for the headset/hands-free applications. The overall code size is optimized within 128Kbytes. Integrated in conjunction with RF Transceiver and low noise audio CoDec features a high quality voice link. All components with software in this chip conform to Bluetooth Specification v2.0.

Features

- Compliant with Bluetooth Specification V2.0
- Low Power 1.8V operation
- Embedded 8-bits Micro-Controller
- Internal 128 KB mask ROM and 8 KB SRAM
- Includes all essential protocol stacks for headset/hands-free
- Programmable Musical Ring Generator
- 4.2V Tolerant LED Drivers with intensity control
- 9-bit A/D resolution for low power detector
- Integrated Battery Charger
- 14-bit Linear CODEC
- Integrated Switch-mode Regulator
- 56-Pin QFN (8mm x 8mm x 0.9mm)

Block Diagram

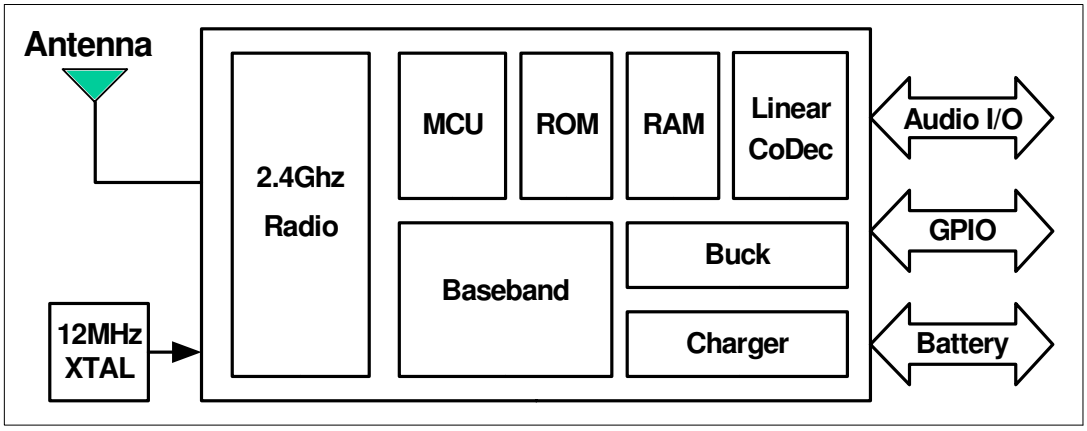


Fig.1 - Block Diagram of Function

Key Features

Radio

- Auxiliary Features
- Crystal oscillator with built-in digital trimming
- Power management includes digital shutdown and wake up commands with an integrated low power oscillator for sniff mode
- 9-bit ADC available to applications
- Battery charger with programmable current (20-120mA) for Lithium Ion/Polymer battery
- LED intensity control for dedicated LED1 and LED0 outputs

Baseband and Software

- Internal 1Mbit ROM
- Allows full speed data transfer and mixed voice and data
- Logic for forward error correction, header error control, access code correlation, CRC, encryption bit stream generation and whitening
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

Physical Interface

- Optional I2C compatible interface

Audio CODEC

- 14-bit resolution, 8kHz sampling frequency
- Digital enhancements to add bass cut and side tone
- Analogue enhancements to support single-ended and differential speaker drive capability

Bluetooth Stack

- Customized builds with embedded application code

Package Options

- 56-pin QFN, 8 * 8 * 0.9 mm, 0.50 mm pitch

Package Information

Pin Assignment Diagram

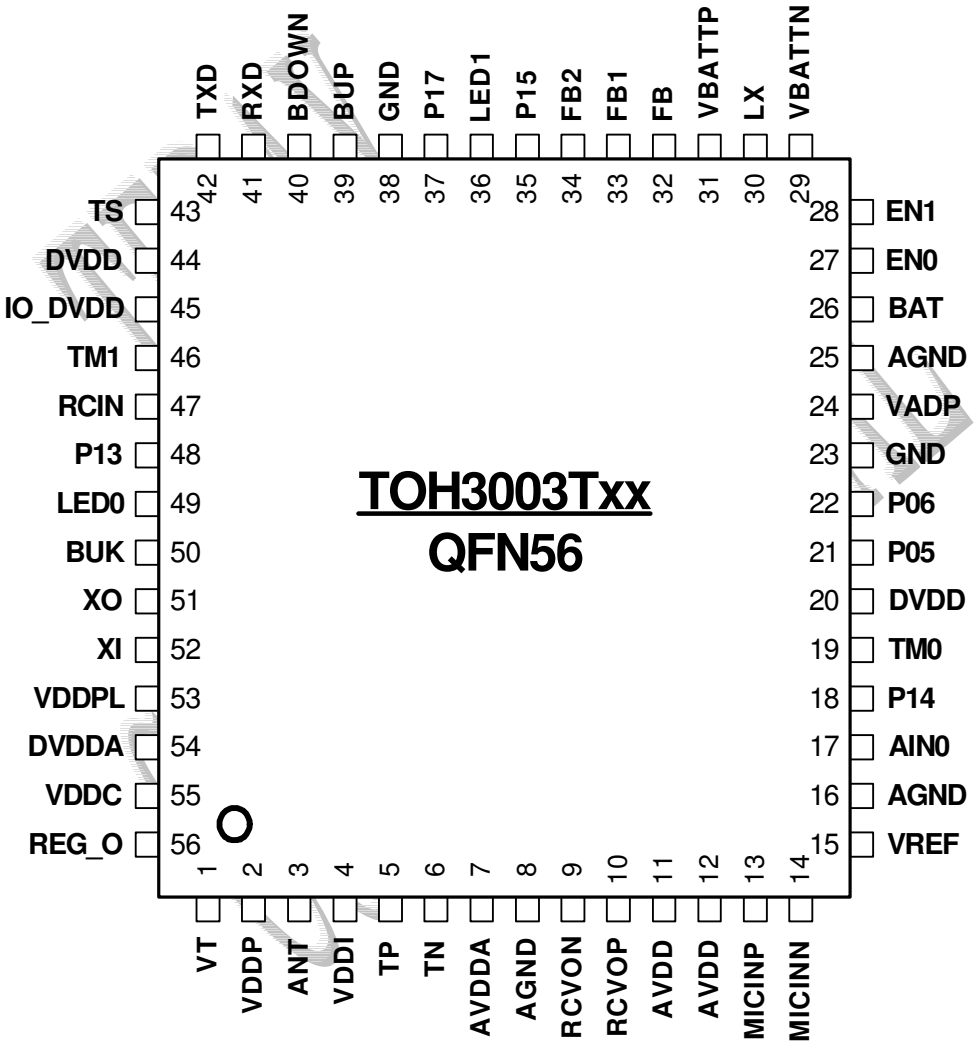


Fig.2 - Pin Assignment Diagram

Pin definition

Oscillator	Pin	Pad Type	Supply Pad	Description
XI	52	AI	RF_DVDD	For crystal
XO	51	AO	RF_DVDD	Drive for crystal

Test	Pin	Pad Type	Supply Pad	Description
TM0	19	I, PD	IO_DVDD	For test mode
TM1	46	I, PD	IO_DVDD	For test mode
TS	43	IO	IO_DVDD	Input for test mode, IO for normal mode.

Switch-mode power regulator	Pin	Pad Type	Supply Pad	Description
LX	30	P	VBATTP	Regulator output
FB	32	AI	VBATTP	Feedback voltage
FB1	33	AI	VBATTP	Voltage bypass 1 for Buck
FB2	34	AI	VBATTP	Voltage bypass 2 for Buck
VBATTP	31	P	VBATTP	Battery + input
VBATTN	29	G	VBATTP	Battery - input

Operational Keys	Pin	Pad Type	Supply Pad	Description
BUP	39	I, PU	IO_DVDD	Speaker Volume Control (Volume up)
BDOWN	40	I, PU	IO_DVDD	Speaker Volume Control (Volume down)
BUK	50	I, PD	IO_DVDD	Universal key
EN0	27	I	VBATTP	Universal key with power enable
EN1	28	I	VBATTP	4-th Key with power enable

Charger	Pin	Pad Type	Supply Pad	Description
VBAT	26	P	VBAT	Voltage 4.2V output
VADP	24	P	VADP	Charger 5V input

RF Interface	Pin	Pad Type	Supply Pad	Description
VDDP	2	P	RF_DVDD	1.8V input for RF power
DVDDI	4	P	RF_DVDD	1.8V input for RF power
AVDDA	7	P	RF_DVDD	1.8V input for RF power
VDDPL	53	P	RF_DVDD	1.8V input for RF power
DVDDA	54	P	RF_DVDD	1.8V input for RF power
VDDC	55	P	RF_DVDD	1.8V input for RF power
REG_O	56	P	RF_DVDD	Regulator out
ANT	3	AIO	RF_DVDD	RF antenna for transceiver
VT	1	AIO	RF_DVDD	Version1
TP	5	AO	RF_DVDD	Test P
TN	6	AO	RF_DVDD	Test N

LED	Pin	Pad Type	Supply Pad	Description
LED0	49	OD	VBATTP IO_DVDD	4.2V Tolerant LED Drivers with intensity control
LED1	36	OD	VBATTP IO_DVDD	4.2V Tolerant LED Drivers with intensity control

GPIO	Pin	Pad Type	Supply Pad	Description
P05	21	IO, PU	IO_DVDD	GPIO of MCU.
P06	22	IO, PU	IO_DVDD	GPIO of MCU
P13	48	IO, PU	IO_DVDD	GPIO of MCU
P14	18	IO, PU	IO_DVDD	Connect to SDA pin of external EEPROM chip with I2C bus
P15	35	IO, PU	IO_DVDD	Connect to SCL pin of external EEPROM chip with I2C bus
P17	37	IO, PU	IO_DVDD	Supply MIC bias voltage

UART	Pin	Pad Type	Supply Pad	Description
TxD	41	O	IO_DVDD	Low speed UART communication port for external controller
RxD	42	IO, PU	IO_DVDD	Low speed UART communication port for external controller

CODEC	Pin	Pad Type	Supply Pad	Description
RCVOP	10	AO	AVDD	Connect to Speaker +
RCVON	9	AO	AVDD	Connect to Speaker -
AVDD	11, 12	P	AVDD	CoDec power supply
AGND	8, 16, 25	G	AVDD	CoDec ground
MICINP	13	AI	AVDD	Microphone input differential +
MICINN	14	AI	AVDD	Microphone input differential -
VREF	15	AO	AVDD	Voltage reference for CoDec

Digital Power	Pin	Pad Type	Supply Pad	Description
DVDD	20, 44	P	DVDD	Positive supply for all digital circuit
IO_DVDD	45	P	IO_DVDD	Positive supply for all digital IO ports
GND	23, 38	G	GND	Ground connections for all digital circuit and IO ports

Auxiliary	Pin	Pad Type	Supply Pad	Description
RCIN	47	I, PU	IO_DVDD	External RC reset input
AIN0	17	AI	AVDD	Low-voltage detector input

Notes:

1. P: power pad, G: ground pad, I: input, O: output,
2. A: analog, OD: open-drain, PU: pull-up, PD: pull-down,
3. AIO: analog I/O,

Electrical Characteristics

Absolute Maximum Ratings

Rating	Min	Max
Storage temperature	-40℃	125℃
Supply voltage: RF power, DVDD, AVDD	0V	2V
Supply voltage: IO_DVDD	0V	3.7V
Supply voltage: VBATTP, VBAT	0V	4.2V
Supply voltage: VADP	0V	6V
Other terminal voltage	0V	DVDD

Recommended Operation Conditions

Operating Condition	Min	Max
Operating temperature (1)	-40℃	85℃
Supply voltage: RF power, DVDD, AVDD	1.7V	1.9V
Supply voltage: IO_DVDD	1.7V	3.6V
Supply voltage: VBATTP, VBAT	3.2V	4.2V
Supply voltage: VADP	4.5V	6V

Note: (1) Design guarantee.

Power Consumption

Typical Average Current

Operation Mode	Connection Type	Average (3V2 Supply)	Average (4V2 Supply)	Unit
Sleep (Shut Down)	-	-	30	uA
Inquiry and page scan	-	2.09	1.39	mA
ACL No traffic	Slave	11.65	9.9	mA
ACL With file transfer	Slave	12.87	10.45	mA
ACL 40ms sniff, attempt=12	Slave	2.49	2.13	mA
ACL 0.5s sniff, attempt=12	Slave	0.59	0.44	mA
ACL 1.28s sniff, attempt=12	Slave	0.49	0.35	mA
SCO HV1 (Mute)	Slave	35.1	28.3	mA
SCO HV3 (Mute)	Slave	14.6	11.25	mA
SCO HV3 30ms sniff	Slave	14.4	10.77	mA
SCO HV3 Play 1k tone with IVT	Slave	19.7	15.5	mA

Switch-mode Regulator

Switch-mode Regulator	Min	Typ	Max	Unit
Input voltage (VIN)	3.2	4.0	5.5	V
Output voltage @ 100mA	1.78	1.85	1.92	V
Normal Operation				
Maximum load current	100	-	110	mA
Power efficiency @ I_{load} =30mA, VIN=4.2V	-	80	-	%
Output capacitor	-	4.7	-	uF
Capacitor ESR	-	-	25	mΩ
Inductor	-	33	-	uH
Inductor ESR	-	-	600	mΩ
Low Power Mode				
Maximum load current	-	15	25	mA
Power efficiency @ I_{load} =2mA, VIN=4.2V	-	85	-	%
Quiescent current	-	-	180	uA
Disable Mode				
Quiescent current	-	-	10	uA

Battery Charger

Battery Charger	Min	Typ	Max	Unit
Input voltage	4.5	5	6	V
Charging Mode				
Supply current	-	2	3	mA
Battery trickle charge current Maximum setting (ICTR=15) Minimum setting IICTR=0)	 - -	 12 2	 - -	 mA mA
Trickle charge voltage threshold	2.8	2.9	3	V
Trickle charge hysteresis voltage	-	50	-	mV
Float voltage (with correct trim value set)	4.05	4.15	4.25	V
Float voltage trim step size	-	30	-	mV
Battery charge termination current Maximum setting (ICTR=15) Minimum setting (ICTR=0)	 - -	 120 20	 - -	 mA mA
Standby Mode				
Supply current	-	-	500	uA
Battery current	-	-	-15	uA
Battery recharge hysteresis	100	-	200	mV
Shutdown Mode				
VADP under-voltage threshold (VADP rising) (VADP falling)	- - -	100 4.3 4.1	- - -	mV V V
VADP – BAT lockout threshold (VADP rising) (VADP falling)	- - -	70 35 -35	- - -	mV mV mV
Supply current	-	-	500	uA
Battery current	-	-	-10	uA
Sleep Mode				
Battery current	-	-	-10	uA

Digital Terminals

Digital Terminals	Min	TYP	Max	Unit
Input Voltage Levels				
Vil @ (2.7v≦IO_DVDD≦3.6v)	0	-	0.8	V
Vil @ (1.7v≦IO_DVDD≦1.9v)	0	-	0.4	V
Vih	IO_DVDD* 0.7	-	IO_DVDD+ 0.4	V
Output Voltage Levels				
Vol @ (2.7v≦IO_DVDD≦3.6v, I = - 4mA)	-	-	0.4	V
Vol @ (1.7v≦IO_DVDD≦1.9v, I = - 4mA)	-	-	0.2	V
Voh @ (2.7v≦IO_DVDD≦3.6v, I = 4mA)	IO_DVDD- 0.4	-	-	V
Voh @ (1.7v≦IO_DVDD≦1.9v, I = 4mA)	IO_DVDD- 0.2	-	-	V
I/O pad leakage current	-1	0	1	µA
Pad Input Capacitance	2	-	5	pF

Auxiliary ADC

Auxiliary ADC	Min	Typ	Max	Unit
Resolution	-	-	9	bits
Minimum input voltage range (A)	0	-	0.1	V
Maximum input voltage range (B)	VDD-0.1	-	VDD	V
INL	-2	-	+2	LSB
DNL	-0.8	-	+0.8	LSB
LSB	-	(B-A)/511	-	mV
Clock	-	1.2	-	MHz

Clocks

Crystal Oscillator	Min	TYP	Max	Unit
Crystal frequency	-	12	-	MHz
Digital trim range	0	3.52	7.04	pF
Trim step size	-	0.11	-	pF
Transconductance	822	-	-	µA/V
Negative resistance @XTAL 12MHz; C0 0.8pF; CL 12pF	120	-	492	Ω
Xtall input capacitance	-	3.87	-	pF
Duty cycle	30:70	50:50	70:30	%

Audio CODEC

Audio CODEC, 14-bit Resolution	Min	Typ	Max	Unit
Microphone Amplifier				
Input scale at maximum gain	-	1.3	-	mVrms
Input scale at minimum gain	-	410	-	mVrms
Gain resolution	2.5	3	3.5	dB
THD @ 1k(Mic Gain=0dB, full scale input)	-	-	-50	dB
Input refer noise (300Hz ~ 3.4KHz, Mic Gain=20dB, include ADC)	-	5	-	uVrms
Bandwidth	-	4	-	kHz
Microphone input impedance	-	20	-	kOhm
Analogue to Digital Converter				
Input sample rate	-	1	-	MHz
Output sample rate	-	8	-	kHz
THD @ 1k(Mic Gain=0dB, full scale input)	-	-	-50	dB
Digital to Analogue Converter				
Input sample rate	-	8	-	kHz
Output sample rate	-	1	-	MHz
Speaker Driver				
Output voltage full scale swing (differential)	-	1.66	-	Vpk-pk
Output full scale current drive (differential, relative to full scale, 32 Ohm, 0.1THD)	-	30	-	mA
Output –3dB bandwidth	300	-	3400	Hz
Distortion and noise (differential, relative to full scale, 32 Ohm)	-	-50	-	dB
Gain resolution	3.5	3	2.5	dB
C load	-	-	200	pF
R load	16	-	40	Ohm
Side tone attenuation				
Gain range	-24	-	+18	dB
Gain step	-	3.5 or 2.5	-	dB

Radio Characteristics

Parameter	Symbol	Specification			Units	Test Condition and Notes
		Min	Typ	Max		
Overall Transceiver						
Operating Frequency Range	$F_{\_OP}$	2400	-	2482	MHz	
Antenna port mismatch	$VSWR_I$	-	<2:1	-	VSWR	Receive mode
	$VSWR_O$	-	<2:1	-	VSWR	Transmit mode
Receive Section						**Rx out on RXDATA pin, using baseband clock recovery, For BER≤0.1%**
Receiver sensitivity		TBD	-80	-72	dBm	Meas. At antenna pin of IC
Maximum		-20	-	-	dBm	
Input 3rd order intercept point	IIP_3	-14	-11	-	dBm	
Data (Symbol) rate	Ts	-	1	-	us	
Min. Carrier/Interference ratio						For BER ≤ 0.1%
Co-Ch. Interference	$CI_{\_cochannel}$	-	9	11	dB	-60 dBm desired signal.
Adjacent Ch. Interference, 1MHz offset	$CI_{\_1}$	-	-1.5	0	dB	-60 dBm desired signal.
Adjacent Ch. Interference, 2MHz offset	$CI_{\_2}$	-	-30	-	dB	-60 dBm desired signal. Interference at 2 MHz below desired signal.
Adjacent Ch. Interference, ≥3MHz offset	$CI_{\_3}$	-	-40	-	dB	-60 dBm desired signal.
Image Frequency Interference	$CI_{\_Image}$	-	-23	-9	dB	-60 dBm desired signal. Image freq. is always 2MHz higher than desired signal.
Adjacent (1MHz) Interference to Image	$CI_{\_Image\_11}$	-	-34	-20	dB	-67 dBm desired signal. Always 3MHz higher than desired signal.

Out-of-Band Blocking						Measure with ACX ceramic filter on antenna pin.	
		OBB_{-1}	-10	-	-	dBm	30 MHz to 2000 MHz
		OBB_{-2}	-27	-	-	dBm	2000 MHz to 2400 MHz
		OBB_{-3}	-27	-	-	dBm	2500 MHz to 3000 MHz
		OBB_{-4}	-10	-	-	dBm	3000 MHz to 12.75 GHz
Transmit section							
RF output power		P_{AV}	-	+2	-	dBm	Under Max. Power level, Measure at antenna pin of IC.
Modulation Characteristics							
Peak FM Deviation	00001111 pattern	$\Delta f1_{avg}$	140	157	175	kHz	
	01010101 pattern	$\Delta f2_{max}$	115	-	-	kHz	For at least 99.9% of all $\Delta f2_{max}$ measure.
ISI, % Eye Open		$\Delta f2_{avg}$ / $\Delta f1_{avg}$	80	-	-	%	1010 data sequence referenced to 00001111 data sequence.
Zero Crossing Error		ZCERR	-125	-	125	ns	+/- 1/8 of symbol period
In-Band Spurious Emission							
(+/- 550 kHz)		IBS_1	-	-	-20	dBc	
2 MHz offset		IBS_2	-	-	-40	dBm	
> 3 MHz offset		IBS_3	-	-	-60	dBm	
Out-of-Band Spurious Emission, Operation							
		OBS_O_1	-	< -60	-36	dBm	30 MHz ~ 1 GHz
		OBS_O_2	-	-45	-30	dBm	1GHz ~ 12.75GHz. excludes desired
		OBS_O_3	-	<-60	-47	dBm	1.8 GHz ~ 1.9 GHz
		OBS_O_4	-	<-65	-47	dBm	5.15 GHz ~ 5.3 GHz
RF VCO and PLL Section							
Typical PLL lock range		F_{LOCK}	2340	-	2560	MHz	
Tx, Rx Frequency tolerance			-20	-	+20	ppm	Same as crystal oscillator frequency tolerance.
Channel (Step) Size			-	1	-	MHz	
SSB Phase Noise			-	-95	-	dBc/Hz	550 KHz offset
			-	-115	-	dBc/Hz	2 MHz offset
RF PLL Settling Time		T_{HOP}	-	75	150	us	
Out-of-Band Spurious Emission		OBS_{-1}	-	<-75	-57	dBm	30 MHZ ~ 1 GHz
		OBS_{-2}	-	-68	-47	dBm	1GHZ ~12.75GHz

IDLE state, Synthesizer and VCO ON

Description of Functional Blocks

RF

TOH3003 RF contains transmit, VCO and PLL functions, including an on-chip channel filter, thus minimizing the need for external components. The receiver utilizes extensive digital processing for excellent overall performance, even in the presence of interference and transmitter impairments.

Switch-mode Regulator

TOH3003 contains a high efficiency step-down switch mode 1.8v regulator, which can be used to power the complete chip from a single Lithium Ion/Polymer battery (or other external voltage source). The circuit has only two external passive filter components and has an internal PID feedback for very low supply ripple.

Battery Charger

TOH3003 contains a fully integrated battery charger circuit, suitable for charging a Lithium Ion/Polymer battery. The circuit requires no external components.

Clock Generation

The operation clock for the system is generated from crystal input 12MHz. The upper limit for the system is 12MHz.

Baseband and Logic

- **Physical Layer Hardware Engine DSP**

  FEC (forward error correction)
  HEC (header error correction)
  CRC (cyclic redundancy check)
  Encryption
  Data whitening
  Access code correlation
  Audio trans-coding
  A-law/μ-law/CVSD (Continuously Variable Slope Delta)

- **Memory (ROM & RAM)**

  8Kbytes RAM: Support the MCU and shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

1Mbits ROM: Provided for system firmware.

- **External FLASH**
  External FLASH pads are available for stacked/external FLASH package.

Micro-controller

The 8-bit micro-controller (MCU), interrupt controlled and event timer run the Bluetooth software stack and control the radio and host interface.

- **Programmable I/O**
  There are 4 Programmable I/O terminals. They are controlled by firmware running on the device.

- **Audio CODEC**
  TOH3003 has a 14-bit Audio CODEC that has an 8kHz sampling frequency. This is designed for voice application. The CODEC has integrated input/output amplifiers capable of driving a microphone and speaker.

- **Auxiliary ADC**
  The 9-bits ADC (analogue to digital converter) is used to digitalize battery voltage for battery check application.

- **LED driver**
  Two LED output pads are provided to control LED indicators. They are open drain pull-downs, controlled by firmware running on the device.

Terax Bluetooth Software Stacks

TOH3003 is supplied with Bluetooth v2.0 compliant stack firmware that runs on the internal MCU.

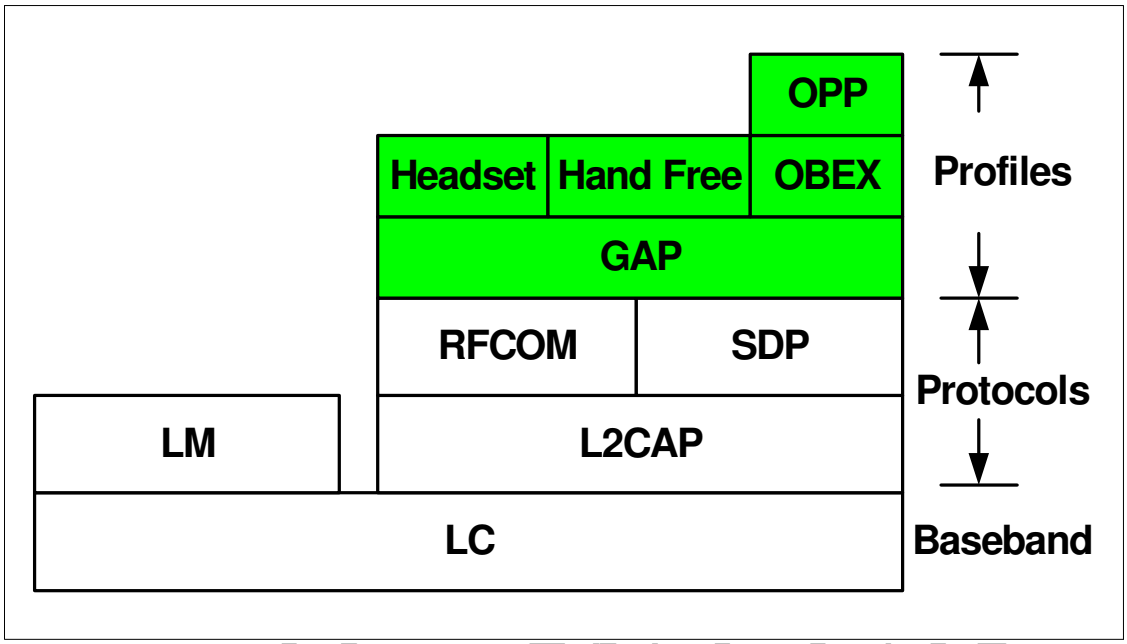


Fig.3 – Terax Bluetooth Software Stacks

Key Feature of the HCI Stack: Standard Bluetooth Functionality

- Bluetooth v2.0 mandatory functionality:
  - Adaptive frequency hopping (AFH), including classifier
  - Faster connection - enhanced inquiry scan (immediate FHS response)
  - LMP improvements
- Optional Bluetooth v2.0 functionality supported:
  - Extended SCO (eSCO), EV3 +CRC, EV4, EV5
  - SCO handle
  - Synchronization
- The firmware was written against the Bluetooth v2.0 specification.
  - Bluetooth components:
  - Baseband (including LC)
  - LM
- All standard radio packet types
- Bluetooth data rate 1Mbps
- Active ACL connections: 1
- Active SCO connections: 1
- All standard SCO voice coding, plus transparent SCO
- Standard operating modes: Page, Inquiry, Page-Scan and Inquiry-Scan
- All standard pairing, authentication, link key and encryption operations

- Standard Bluetooth power saving mechanisms: Sniff
- Master switch to Slave
- Support loop-back test modes

The firmware's supported Bluetooth features are detailed in the standard Protocol Implementation Conformance Statement (PICS) documents.

Device Terminal Descriptions

RF

The RF transmitter is fully compliant with the Bluetooth® Class 2 operation, which allows up to +4 dBm output power. The low-IF receiver architecture produces low DC offsets and a 2 MHz spur below -40 dBc. Digital RSSI values are available to monitor channel quality.

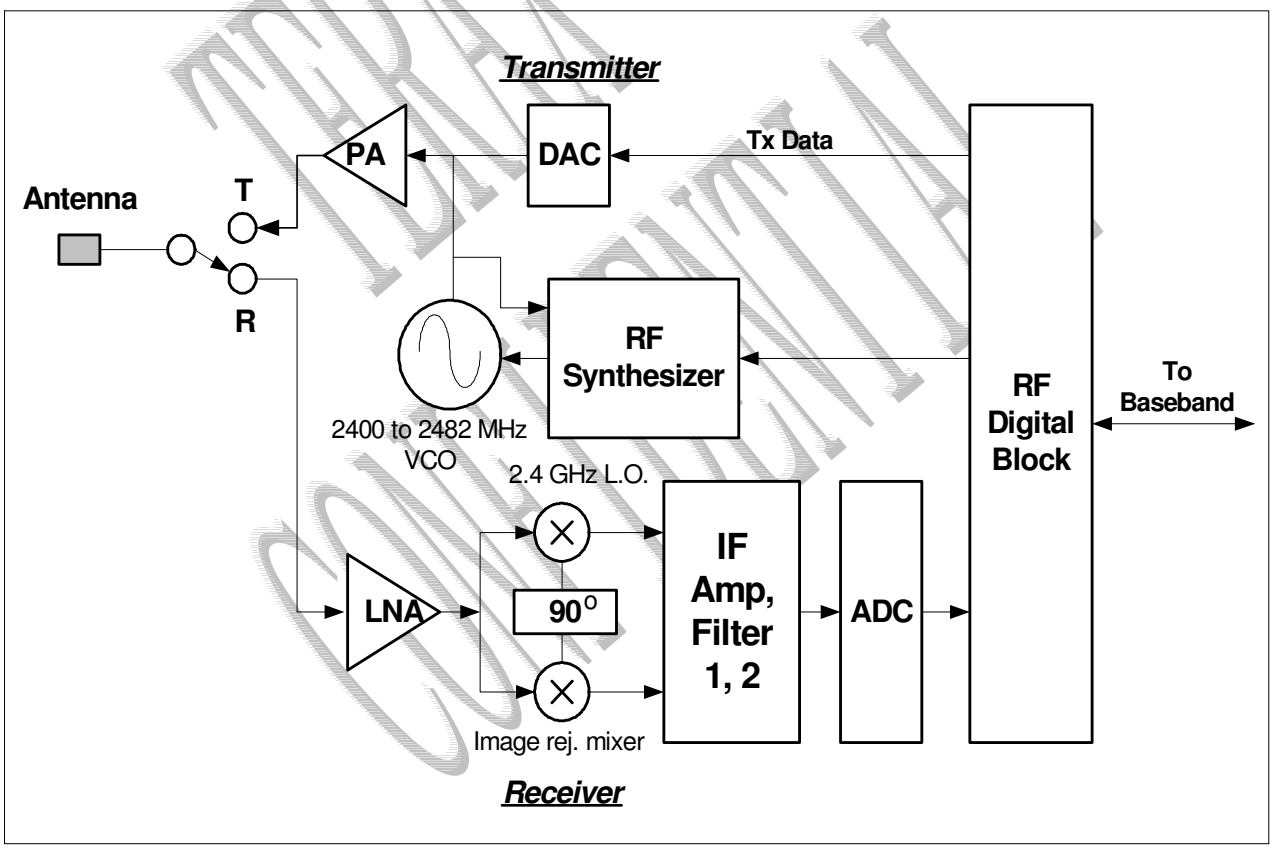


Fig.4 – RF Block Diagram

Crystal Oscillator (Xtall & XtalO)

TOH3003 contains a crystal driver circuit. This operates with an external crystal and capacitors.

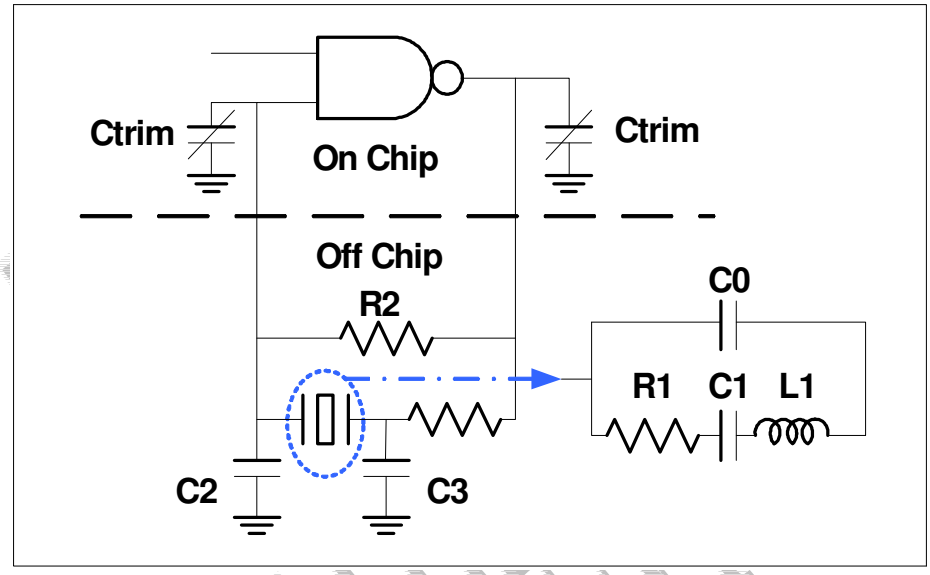


Fig.5 – Crystal Oscillator Block Diagram

- **Load Capacitance**

For resonance at the correct frequency the crystal should be loaded with its specified load capacitance, which is defined for the crystal. This is the total capacitance across the crystal viewed form its terminals. TOH3003 provides some of this load with the capacitor C_{trim} and C_{int}. The remainder should be from the external capacitors labeled C2 and C3. Crystal load capacitance, C_{laod} is calculated by below equation.

$$C_{load} = C_{\text{int}} + \frac{C_{trim}}{2} + \frac{C2 \bullet C3}{C2 + C3}$$

Where:

C_{trim} = 3.52pF nominal (mid-range setting)

C_{int} = 3.88pF

Note:

C_{int} doesn't include the crystal internal self capacitance, it is the driver self capacitance.

- **Frequency Trim**

TOH3003 enable frequency adjustment to be made. This feature is typically used to remove initial tolerance frequency errors associated with the crystal. Frequency trim is achieved by adjusting the crystal load capacitance with on-chip trim capacitors, C_{trim}. The value of C_{trim} is set by a 6-bit word in the CLKTrim (0x1f6). Its value is calculates

$$C_{trim} = 110fF \times CLKTrim$$

There are two C_{trim} capacitors, which are both connected to ground. When views from the crystal terminals, they appear in series so each least significant bit (LSB) increment of frequency trim presents a load across the crystal of 55fF.

The frequency trim is described by

$$\Delta Fx = \text{pull-ability} \times 55fF \times Fx$$

Where Fx is the crystal frequency and pull-ability is a crystal parameter with units of ppm/pF. Total trim range is 63 times the value above.

If not specified, the pull-ability of a crystal may be calculated from its motional capacitance with

$$\text{Pull ability} = \frac{C_m}{2(C_{load} + C_0)^2}$$

Where:

C0 = Crystal self capacitance (shunt capacitance)

Cm = Crystal motional capacitance (series branch capacitance in crystal model)

- **Transconductance Driver Model**

The crystal and its load capacitors should be viewed as a trans-impedance element, whereby a current applied to one terminal generates a voltage at the other. The transconductance amplifier in TOH3003 uses the voltage at its input, XtalI, to generate a current at its output, XtalO. Therefore, the circuit will oscillate if the trans-conductance, trans-impedance product is greater than unity. For sufficient oscillation amplitude, the product should be greater than three. The transconductance requires for oscillation is defined by the relationship shown

$$g_m > \omega^2 R_m \frac{[(C2 + C_{trim})(C3 + C_{trim}) + (C2 + C_{trim})C_{\text{int}} + (C3 + C_{trim})C_{\text{int}}]^2}{(C2 + C_{trim})(C3 + C_{trim})}$$

- **Negative Resistance Model**

An alternative representation of the crystal and its load capacitors is a frequency dependent resistive element. The driver amplifier may be considered as a circuit that provides negative resistance. For oscillation, the value of the negative resistance must be greater than that of the crystal circuit equivalent resistance. Although the TOH3003 crystal driver circuit is based on a trans-impedance amplifier, an equivalent negative resistance may be calculated for it with the following formula in equation

$$R_{neg} > \omega^2 g_m \frac{[(C2+C_{trim})(C3+C_{trim})+(C2+C_{trim})C_{\text{int}}+(C3+C_{trim})C_{\text{int}}]^2}{(C2+C_{trim})(C3+C_{trim})}$$

- **Recommendation for XTAL component spec**

Parameter	Symbol	Min	Typ	Max	Unit	Note
Package		3225	-	5032	mm	3225: L: 32mm W: 25mm 5032: L: 50mm W: 32mm
Nominal Frequency	FL	-	12	-	MHz	
Load Capacitance	CL	-	12	-	pF	
Frequency Tolerance		-10	-	10	ppm	@25±3℃
Frequency Stability		-10	-	10	ppm	Over Operating Temp. Range
Operating Temperature		-20	-	75	℃	
Aging		-3	-	3	ppm	
Drive Level		-	10	-	uW	
Effective Resistance	Rr	-	-	100	Ohm	
Shunt Capacitance C0	C0	-	-	5	pF	

Mono Audio CODEC

The TOH3003 audio CODEC is compatible with the direct speaker drive and microphone input using a minimum number of external components. It is primarily intended for voice applications and it is fully operational from a single 1.8V power supply. A fully differential architecture has been implemented for optimal power supply rejection and low noise performance. The digital format is 14-bit/sample linear PCM with a data rate of 8kHz.

The CODEC has an input stage containing a microphone amplifier, variable gain amplifier and a ΣΔ ADC. Its output stage contains a DAC, low-pass filter and output amplifier. The CODEC functional diagram and applicable gains is shown in below.

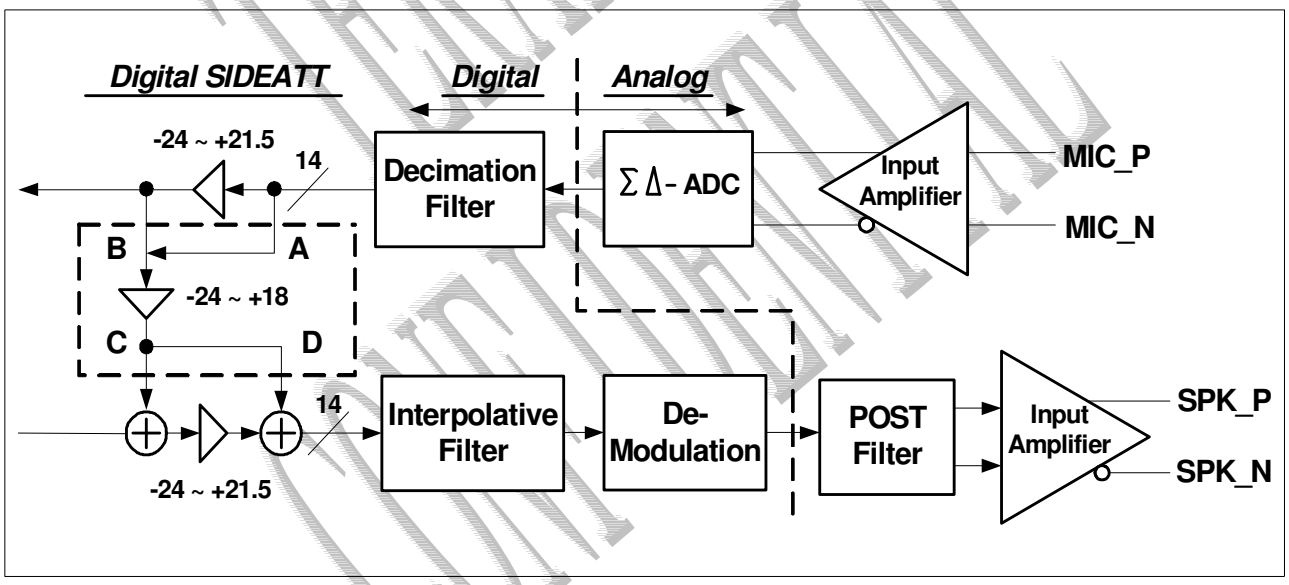


Fig.6 – Mono Audio CODEC Block Diagram

Gain Selection Value (4bit register)	Digital SIDEATT Gain Setting (dB)
0	OFF
1	-24
2	-20.5
3	-18
4	-14.5
5	-12
6	-8.5
7	-6
8	-2.5
9	0
10	3.5
11	6
12	9.5
13	12
14	15.5
15	18
Gain ADC/DAC Path Selection Value (2bit register)	**Digital SIDEATT Gain ADC/DAC Path Setting (dB)**
00	A path SIDEATT C path
01	B path SIDEATT C path
10	A path SIDEATT D path
11	B path SIDEATT D path

Table 1: Digital SIDEATT Gain Rate Selection and path selection

Gain Selection Value (4bit register)	Digital ADC Gain Setting (dB)
0	0
1	3.5
2	6
3	9.5
4	12
5	15.5
6	18
7	21.5
8	-24
9	-20.5
10	-18
11	-14.5
12	-12
13	-8.5
14	-6
15	-2.5

Table 2: Digital ADC Gain Rate Selection

Gain Selection Value (4bit register)	Digital DAC Gain Setting (dB)
0	0
1	3.5
2	6
3	9.5
4	12
5	15.5
6	18
7	21.5
8	-24
9	-20.5
10	-18
11	-14.5
12	-12
13	-8.5
14	-6
15	-2.5

Table 3: Digital DAC Gain Rate Selection

- **Input Stage**

A variable gain amplifier amplifies the signal from MICIN, and then digitized by a second order delta-sigma ADC, it is converted to 14-bit 8kHz linear PCM data by digital circuit.

The gain is programmable and has a 50dB range with 3dB resolution. A bias output from MICPS can provide a DC bias to microphone just like Fig. 7, and then microphone use ac coupling to feed in the MICIN. The CODEC has been designed for use with microphone that has sensitivities between –50 and –40dbV. The MICIN input impedance is typically 20kOhm, C1 should be around 5.6nF within 20% variation for flatten frequency response, RL sets must match with impedance of microphone, MICPS output should be filter with –3dB bandwidth close to DC to provide a low noise DC bias to microphone. The signal to noise ratio is better than 60dB from MICIN to ADC output.

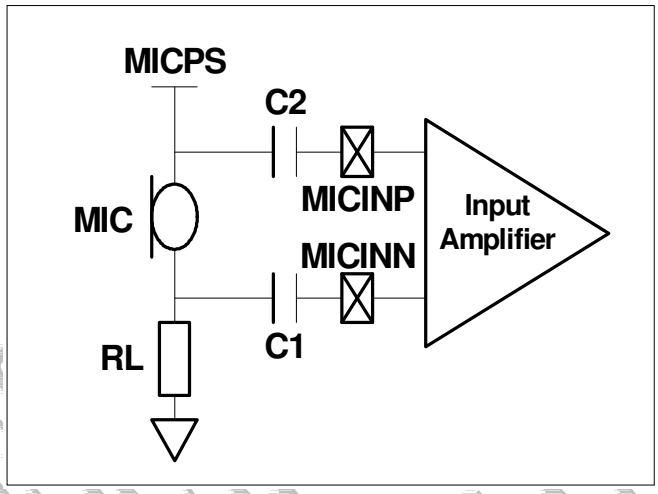


Fig. 7 - Microphone application connection
(RL = around 1k Ohm and must mach to impedance of MIC, C1=C2=5.6 nF)

- **Output Stage**

  The digital data is converted to analogue value by DAC, then out of band noise is filtered by filters without any extra components, then output a differential signal for larger signal level, it will reach 1.66Vpp large, and this output signal path is include gain attenuation/boost stage, the gain range is –24~+6dB, gain step is 3dB when you control attenuation, 3dB for boost.

  There is no DC leakage feed-through the speaker and damage, it need no DC-block capacitor on output path, and we also provide a single-ended output connect in Fig. 8 for reduce the output pin when 3-wire speaker/microphone (common ground) will be used by you.

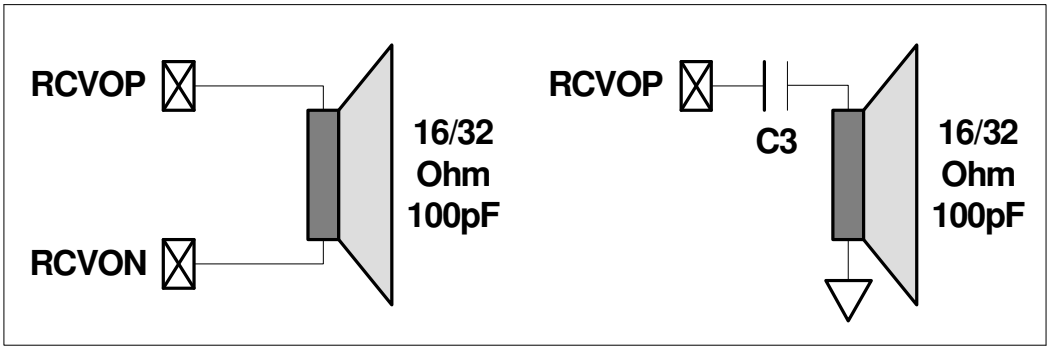


Fig. 8 - Speaker application connection, C3=10uF

- **Base cut**

  Digital enhancements have been made to the TOH3003 mono CODEC to reject low frequencies present in the ADC signal. This is achieved by a digital filter located at the output of the ADC processing chain. The frequency response for bass cut digital enhancement is shown in below.

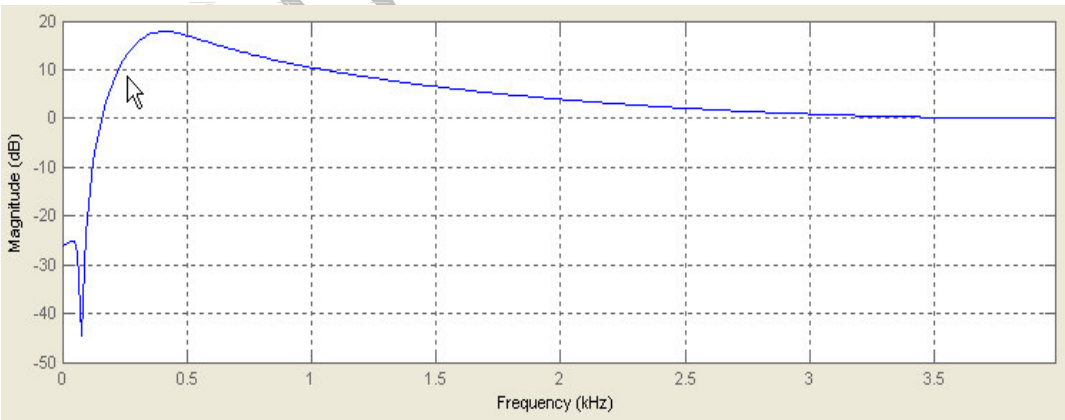


Fig. 9 – Frequency response for bass cut digital enhancement

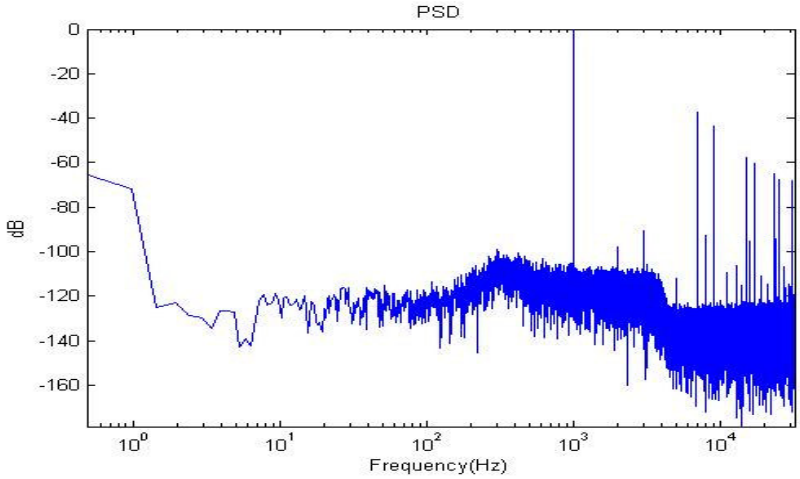


Fig. 10 – SNR chart for 1K tone

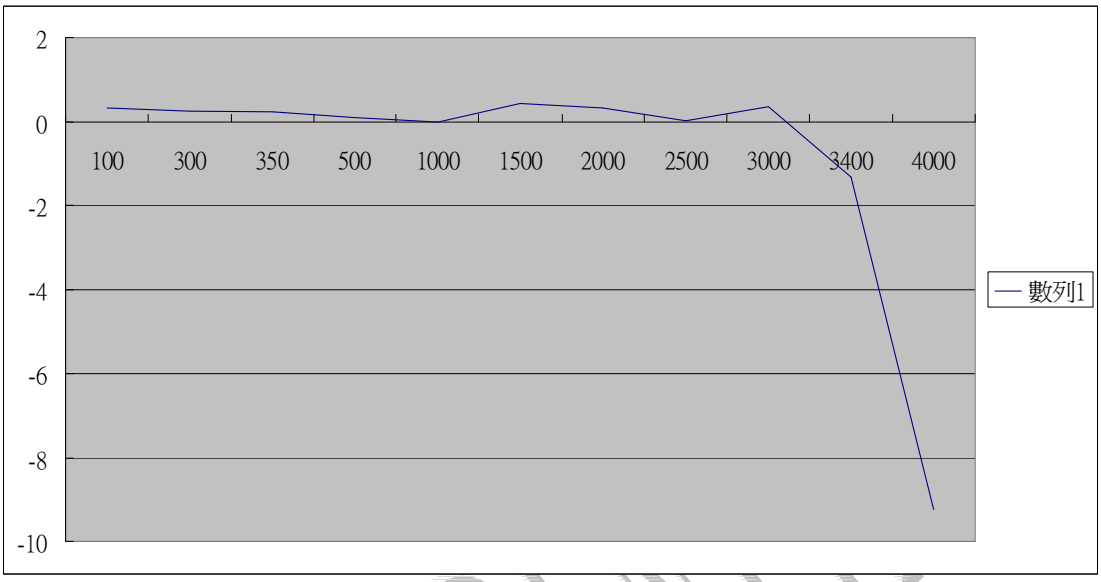


Fig. 11 – Frequency response of Receiver

- **Side Tone**

  In some applications, it is necessary to implement side tone. This involves feeding an attenuated version of the microphone signal to the earpieces.

I/O parallel Ports

Four lines of programmable bi-directional input/outputs (I/O) are provided. They are powered from IO_DVDD. GPIO lines can be configured through software to have either pull-ups or pull-downs. P14, P15 and P17 I/O are configured as inputs with pull-ups at reset. TS I/O is configured as inputs with pull-down at reset.

P14 and P15 are normally dedicated to EEPROM respectively. P17 can be configured as MIC bias control. TS is available for general use.

I2C interface

P14 and P15 can be used to form a master I2C interface. The interface is formed using software to drive these lines. Therefore, it is suited only to relatively slow functions such as driving EEPROM.

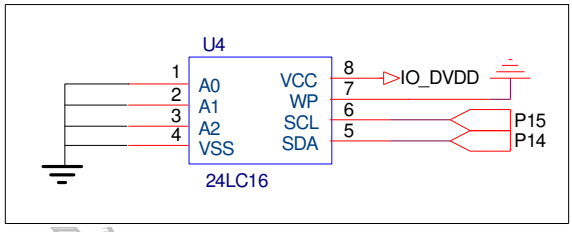


Fig.12 – I2C interface

RESET

The RCIN (reset) pin is an active low reset and is internally filtered using the system clock. A reset will be performed between 1.3 and 1.5s.

The power on reset occurs when the IO_DVDD supply falls below typically 0.9V and is released when IO_DVDD rises above typically 1V. At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are low voltage.

Power Supply

- **Supply Domains and Sequencing**

  The 1.8V supplies are DVDD, RF_VDD and AVDD. It is recommended that the 1.8V supplies are all powered at the same time. The order of powering the 1.8V supplies relative to the other I/O supplies (IO_DVDD) is not important, however if the I/O supplies are powered before the 1.8V supplies all digital IO will have a weak pull-high irrespective of the reset state.

  AVDD and RF_VDD should be connected directly to the 1.8V supply; a simple RC filter is recommended for DVDD to reduce transients put back onto the power supply rails.

- **Switch-mode Regulator**

  The on-chip switch-mode 1.8V regulator can be used to power the 1.8V supplies. An external filter circuit of a low-resistance 33μH series inductor followed by a low ESR 4.7μF shunt capacitor is required between the terminal LX and the 1.8V supply rail. A low ESR 4.7uF shunt capacitor is required between the terminal VBATTP and VBATTN. It is recommended that the series resistance of tracks between the BAT_P and BAT_N terminals, the filter components and the external voltage source are minimized to

maintain high efficiency power conversion and low supply ripple. The regulator may be enabled by the EN0 or EN1 pin, by the device firmware, or by the internal battery charger. The regulator is switched into a low power pulse skipping mode when the device is sent into sniff mode. When this regulator is not used the terminals BAT_P and LX must be grounded of left unconnected.

- **Battery Charger**

The battery charger is a constant current/constant voltage charger circuit and is suitable for Lithium Ion/Polymer batteries only. It must be used in conjunction with the switch-mode regulator as the two circuits share a connection with the battery terminal, VBATTP.

The constant current provided by the charger may be set between 20mA and 120mA allowing different capacity batteries to be charged at their optimum rate. The required current setting is stored in EEPROM and read by the battery charger during the first boot-up sequence.

Whenever the charger is powered the switch-mode regulator is enabled automatically. Internal interfaces are provided to allow firmware to monitor the status of the battery charger. The firmware may also disable the charger.

By default, terminal LED will illuminate at full intensity when a battery is being charged. This behavior may be overridden by the firmware if required. When the charger supply is not connected to VADP the terminal must be left open.

Important Note:

Protection Module:

Lithium Ion/Polymer batteries are capable of delivering high currents of several amperes when short-circuited. This can damage connecting wires and Printed Circuit Board (PCB) components. More seriously, pressure can build up in the cell envelope, causing it to explode and injure the user.

TERAX strongly suggests that Lithium Ion/Polymer batteries incorporate an integral protection module. This is typically a small Integrated Circuit (IC) and Field Effect Transistor (FET) interposed between the battery body and its connecting wires. The protection module limits the short circuit current. Good modules will also prevent

over-charge and over-discharge, which can also cause damage to the battery.

Additional Precautions:

TERAX also suggests that the following additional precautions are observed:

- The direct current (dc) inlet socket used on the appliance should be of a proprietary design, preventing users from attaching the charger or supply connector for another appliance (e.g., a mobile phone or laptop computer). The use of popular 2.1mm and 2.5mm DC jack sockets must be avoided for this reason.
- Never bring the Lithium Ion/Polymer battery connections directly to charging pins on the outside of the appliance casing, where they could be short-circuited by keys in the user's pocket.

Temperature Extremes

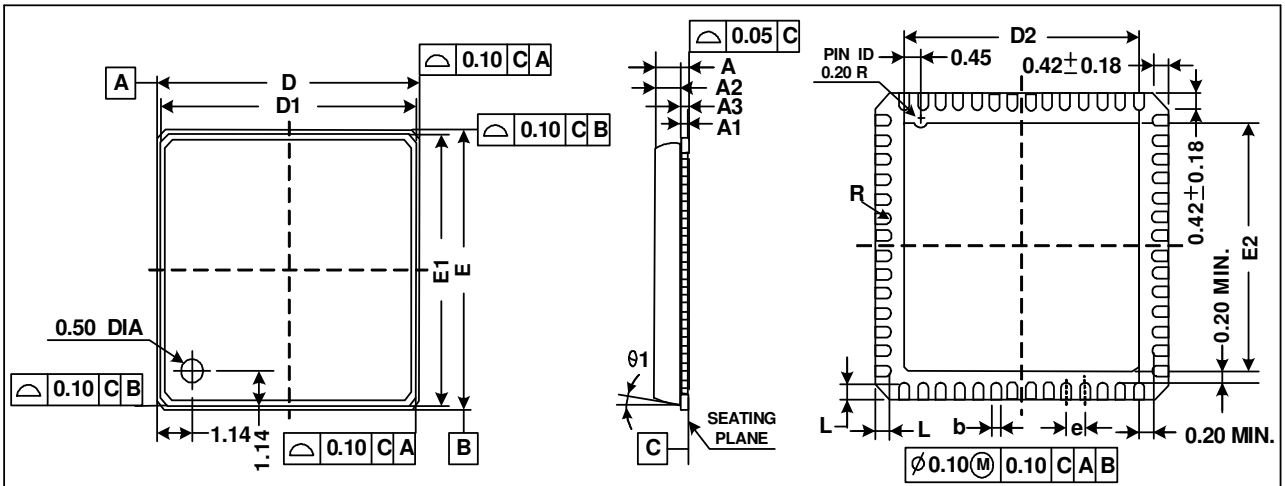
Some Lithium Ion/Polymer cells can be damaged by charging at temperature extremes (e.g., below 0℃ or above 50℃). Consult the battery manufacture for guidance.

LED Drivers

TOH3003 includes two 4.2V tolerant pads dedicated to driving LED indicators. Both pads may be controlled by firmware. The intensity of the LEDs may be adjusted by firmware.

The terminals are low output impedance open-drain outputs, so the LED must be connected in series with a current limiting resistor between the battery terminal or positive supply and the pad.

Package Dimensions



CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	0.90	---	---	0.035
A1	0.00	0.01	0.05	0.00	0.0004	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	8.00 bsc			0.315 bsc		
D1	7.75 bsc			0.305 bsc		
D2	6.30	6.50	6.70	0.248	0.256	0.264
E	8.00 bsc			0.315 bsc		
E1	7.75 bsc			0.305 bsc		
E2	6.30	6.50	6.70	0.248	0.256	0.264
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.50 bsc			0.020 bsc		
θ1	0°	---	12°	0°	---	12°
R	0.09	---	---	0.004	---	---
TOLERANCES OF FROM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

Fig.13 – Package Dimension of 56-pin QFN

Application Schematic

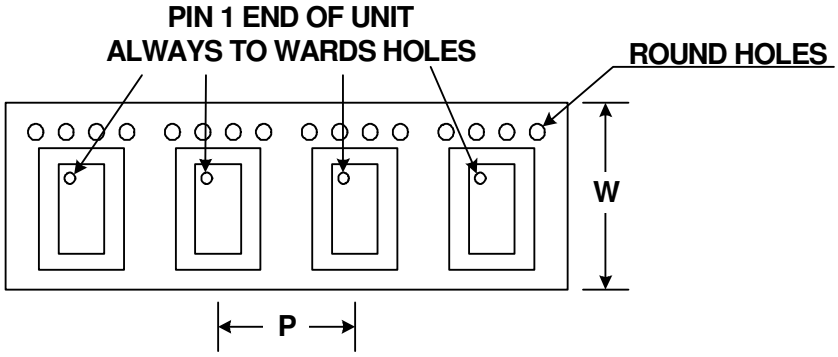
Ordering Information

Part Number # - TOH3003			
Package			
Type	**Size**	**Shipment Method**	**Pieces per Reel**
56-Lead QFN (Pb free)	8 x 8 x 0.9 mm	Tape and reel	2.5Kpcs

Tape & Reel Packing Specification			
Carrier Tape Width (W mm)	**Pocket Pitch (P mm)**	**Trailer# of Pockets (pcs)**	**Leader# of Pockets (pcs)**
16	12	58	88

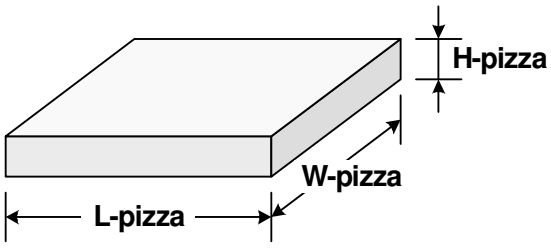
Pizza-Box Packing Specification		
L-pizza (mm)	**W-pizza (mm)**	**H-pizza (mm)**
360	345	50

Carton Packing Specification		
L-carton (mm)	**W-carton (mm)**	**H-carton (mm)**
380	375	290

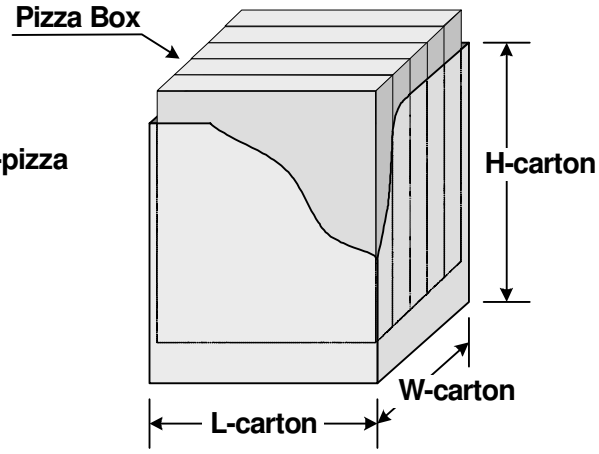


Note:
P --- POCKET PITCH (mm)
W --- CARRIER TAPE WIDTH (mm)

Dimension of Tape & Reel



Dimension of Pizza Box



Dimension of Carton