P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
				TO-39	TO-92	TO-243AA*	Die†
-20V	4.0Ω	-2.4V	-0.85A	—	TP0102N3	—	TP0102ND
-40V	4.0Ω	-2.4V	-0.85A	TP0104N2	TP0104N3	TP0104N8	TP0104ND

* Same as SOT-89. Product supplied on 2000 piece carrier tape reels.
† MIL visual screening available

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Features

- ☐ Low threshold — 2.4V max.
- ☐ High input impedance
- ☐ Low input capacitance
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

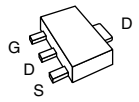
- ☐ Logic level interfaces – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drives
- ☐ Analog switches
- ☐ General purpose line drivers
- ☐ Telecom switches

Absolute Maximum Ratings

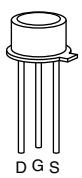
Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* For TO-39 and TO-92, distance of 1.6 mm from case for 10 seconds.

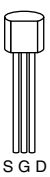
Package Options



TO-243AA
(SOT-89)



TO-39
Case: DRAIN



TO-92

Note: See Package Outline section for dimensions.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-39	-0.9A	-2.0A	3.5W	35	125	-0.90A	-2.0A
TO-92	-0.5A	-2.0A	1.0W	125	170	-0.50A	-2.0A
TO-243AA	-0.26A	-2.0A	1.6W	15	78†	-0.26A	-2.0A

* I_D (continuous) is limited by max rated T_j.
† T_A = 25°C. Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

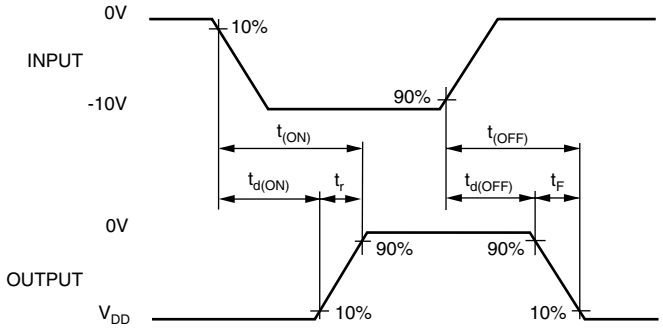
TP0104 – OBSOLETE –

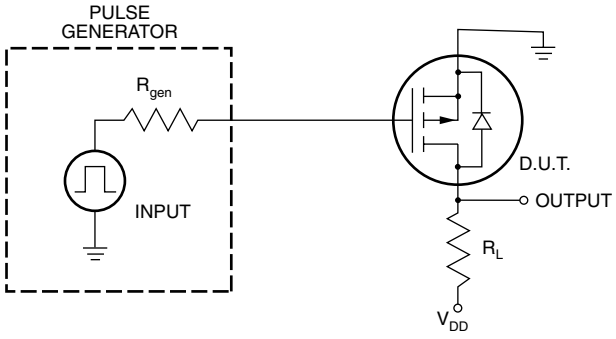
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TP0104	-40			V	V_{GS} = 0V, I_D = -1.0mA
		TP0102	-20				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-2.4	V	V_{GS} = V_{DS}, I_D = -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-5.8	-6.5	mV/°C	V_{GS} = V_{DS}, I_D = -1.0mA
I_{GSS}	Gate Body Leakage			-1.0	-100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	V_{GS} = 0V, V_{DS} = Max Rating
					-1	mA	V_{GS} = 0V, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current			-0.08		A	V_{GS} = -3V, V_{DS} = -20V
			-0.25	-0.50			V_{GS} = -5V, V_{DS} = -20V
			-0.85	-1.70			V_{GS} = -10V, V_{DS} = -20V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			15		Ω	V_{GS} = -3V, I_D = -25mA
				4.7	7.5		V_{GS} = -5V, I_D = -0.1A
				2.5	4.0		V_{GS} = -10V, I_D = -0.5A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.55	1.0	%/°C	V_{GS} = -10V, I_D = -0.5A
G_{FS}	Forward Transconductance		225	250		m℧	V_{DS} = -20V, I_D = -0.5A
C_{ISS}	Input Capacitance				60	pF	V_{GS} = 0V, V_{DS} = -20V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance				50		
C_{RSS}	Reverse Transfer Capacitance				25		
$t_{d(ON)}$	Turn-ON Delay Time			4.0	6.0	ns	V_{DD} = -20V, I_D = -0.85A, R_{GEN} = 25Ω
t_r	Rise Time			7.0	10		
$t_{d(OFF)}$	Turn-OFF Delay Time			3.0	9.0		
t_f	Fall Time			4.0	13		
V_{SD}	Diode Forward Voltage Drop			-1.2	-2.0	V	I_{SD} = -0.25A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time			300		ns	I_{SD} = -0.25A, V_{GS} = 0V

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

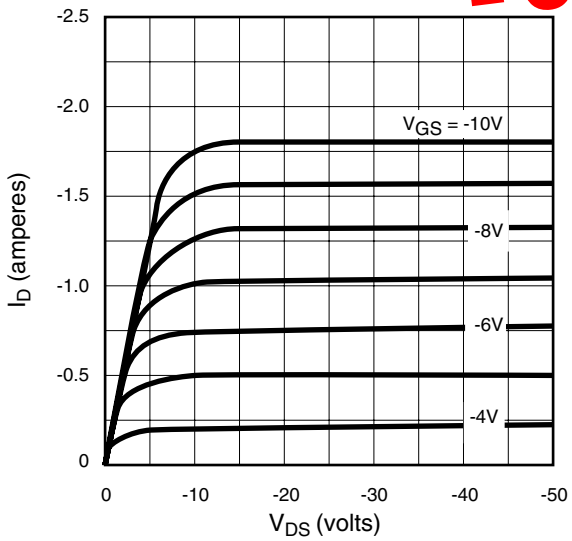




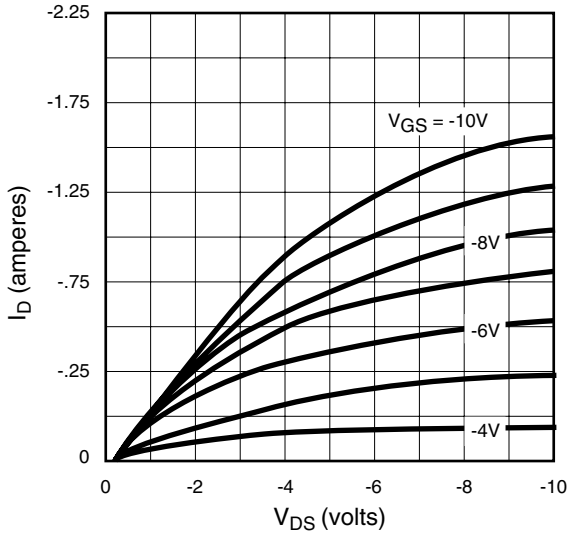
Typical Performance Curves

TP0104 – OBSOLETE –

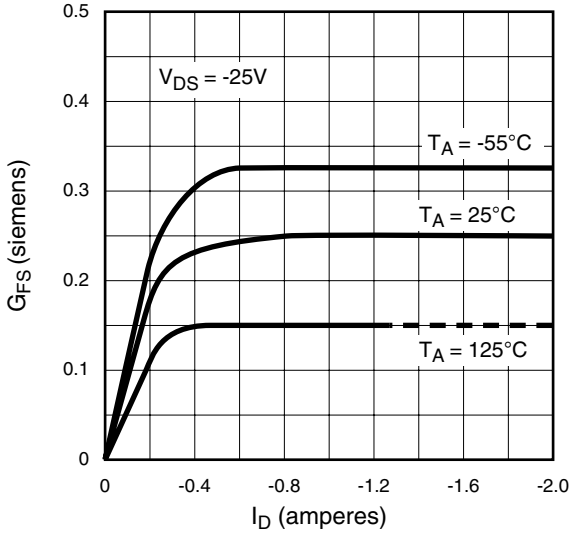
Output Characteristics



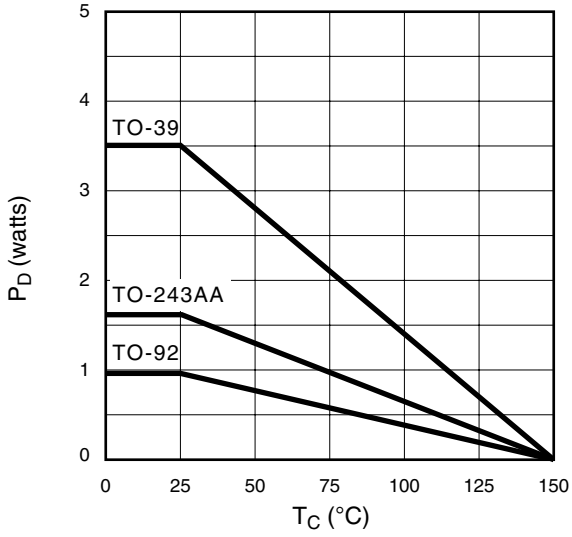
Saturation Characteristics



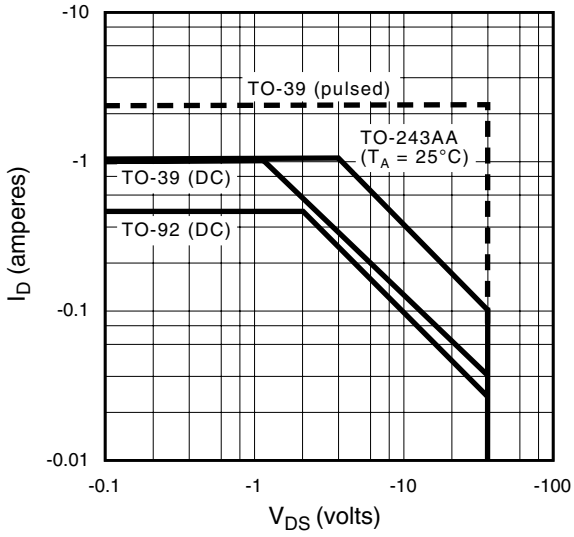
Transconductance vs. Drain Current



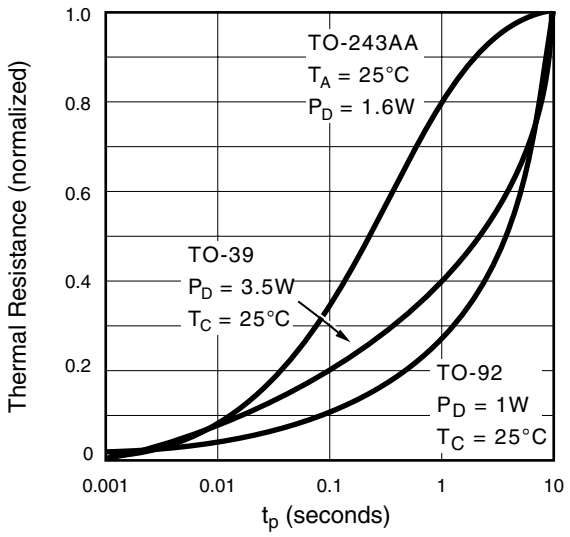
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



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Typical Performance Curves

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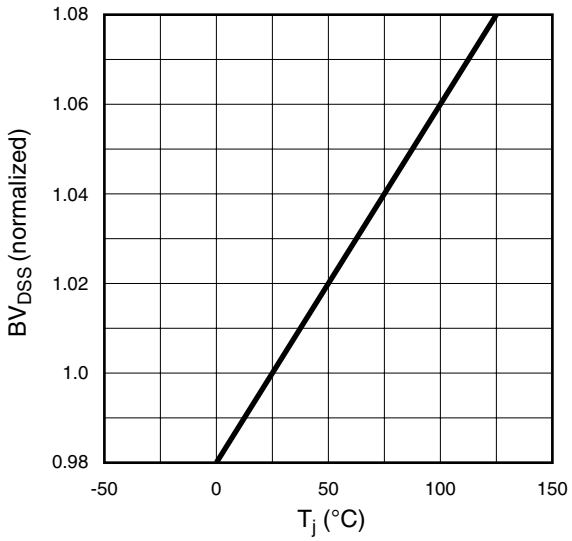
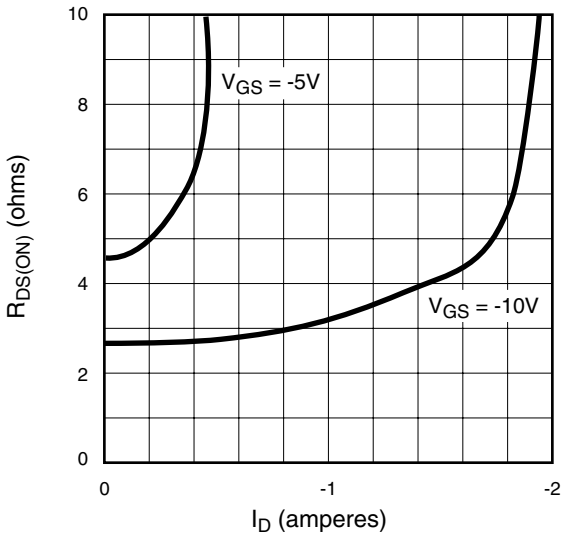
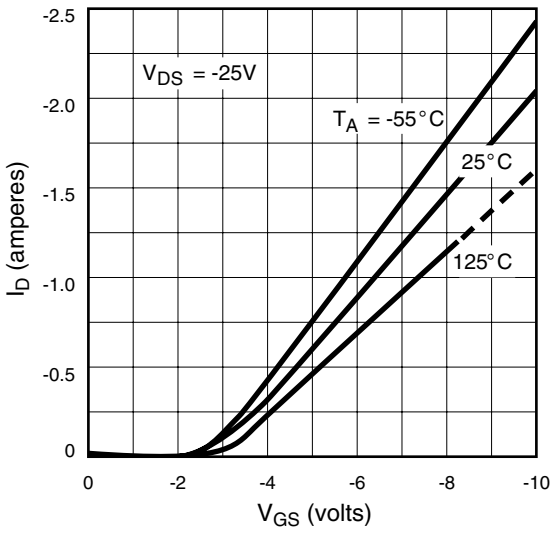
BV$_{DSS}$ Variation with Temperature



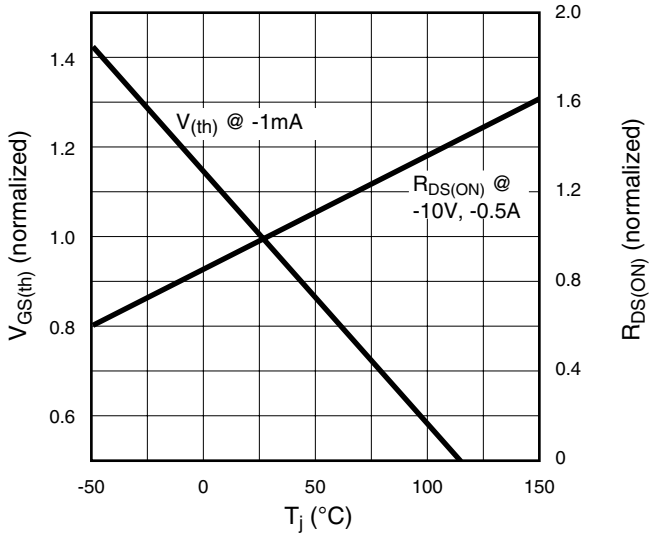
On-Resistance vs. Drain Current



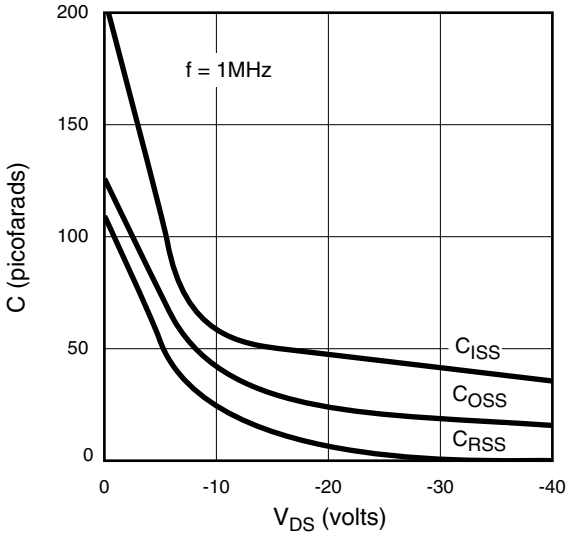
Transfer Characteristics



V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics