Supertex inc.

P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	DICE
-20V	4.0Ω	-0.85A	TP0102N2	TP0102N3	TP0102ND
-40V	4.0Ω	-0.85A	TP0104N2	TP0104N3	TP0104ND

Features

- ☐ Low threshold
- ☐ High input impedance
- ☐ Low input capacitance
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Freedom from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Advanced DMOS Technology

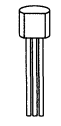
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

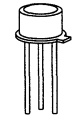
Applications

- ☐ Logic level interface
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switch
- ☐ General purpose line driver

Package Options (Note 1)



TO-92



TO-39

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-39	-0.9A	-2.6A	3.5W	35	125	-0.9A	-2.6A
TO-92	-0.5A	-2.4A	1.0W	125	170	-0.5A	-2.4A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

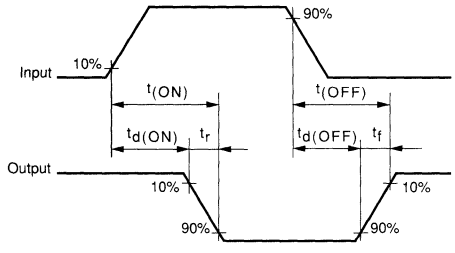
(Notes 1 and 2)

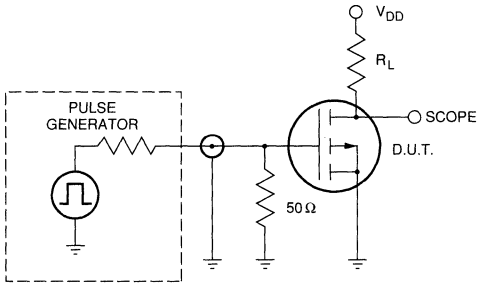
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TP0104	-40			V	V_{GS} = 0, I_D = -1.0mA
		TP0102	-20				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-2.4	V	V_{GS} = V_{DS}, I_D = -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-5.8	-6.5	mV/°C	V_{GS} = V_{DS}, I_D = -1.0mA
I_{GSS}	Gate Body Leakage			-1.0	-100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	V_{GS} = 0, V_{DS} = Max Rating
					-1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current			0.08			V_{GS} = -3V, V_{DS} = -25V
			-0.25	-0.40		A	V_{GS} = -5V, V_{DS} = -25V
			-0.85	-1.70			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			15			V_{GS} = -3V, I_D = -25mA
				5.5	7.5	Ω	V_{GS} = -5V, I_D = -0.1A
				2.5	4.0		V_{GS} = -10V, I_D = -0.5A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.55	1.0	%/°C	I_D = -0.5A, V_{GS} = -10V
G_{FS}	Forward Transconductance		225	300		m℧	V_{DS} = -25V, I_D = -0.5A
C_{ISS}	Input Capacitance			45	60	pF	V_{GS} = 0, V_{DS} = -25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			22	30		
C_{RSS}	Reverse Transfer Capacitance			3	8		
$t_{d(ON)}$	Turn-ON Delay Time			4	6	ns	V_{DD} = -25V, I_D = -1A, R_S = 50Ω
t_r	Rise Time			7	10		
$t_{d(OFF)}$	Turn-OFF Delay Time			3	5		
t_f	Fall Time			4	6		
V_{SD}	Diode Forward Voltage Drop			-1.2	-2.0	V	I_{SD} = -0.25A, V_{GS} = 0
t_{rr}	Reverse Recovery Time			300		ns	I_{SD} = -1.0A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

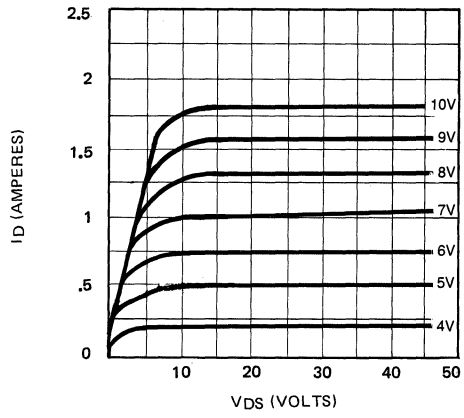
Switching Waveforms and Test Circuit



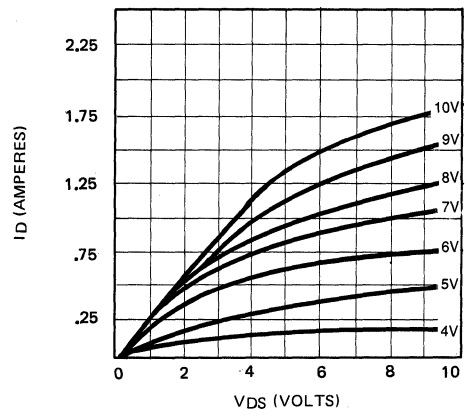


Typical Performance Curves

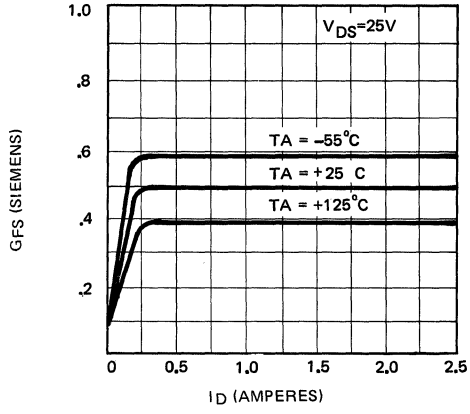
Output Characteristics



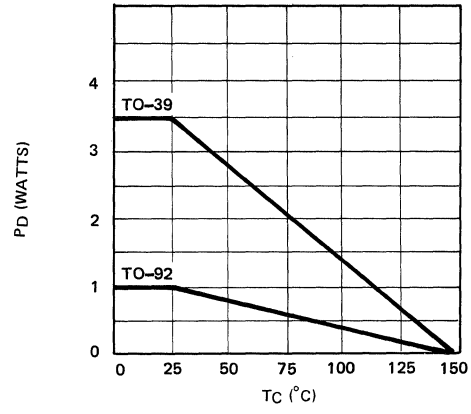
Saturation Characteristics



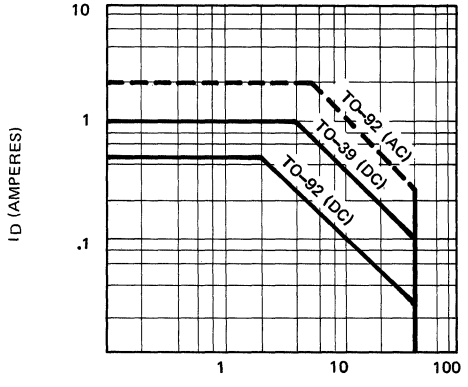
Transconductance Vs. Drain Current



Power Dissipation Vs. Case Temperature

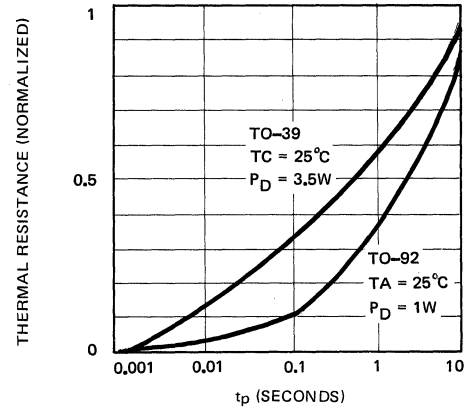


Maximum Rated Safe Operating Area



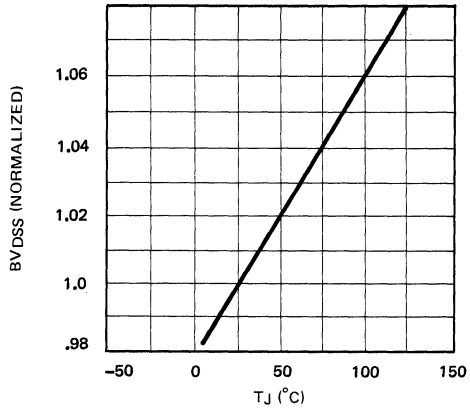
10mS Pulse @ 2V DC

Thermal Response Characteristics

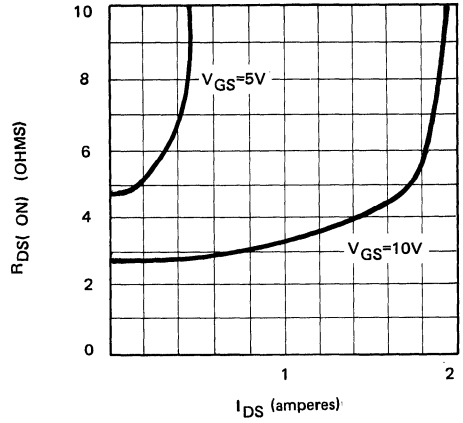


Typical Performance Curves

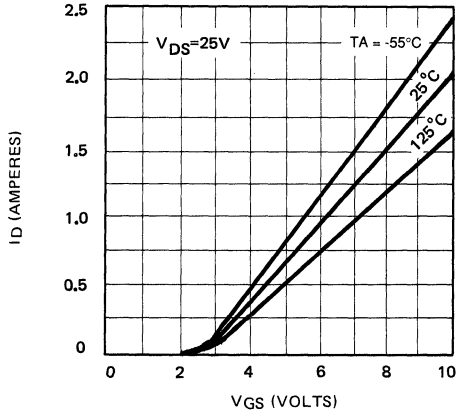
BVDSS Variation with Temperature



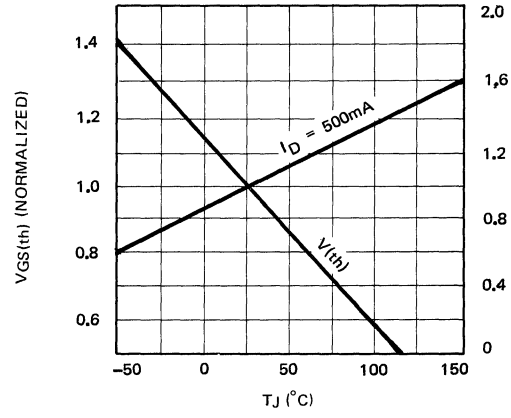
ON-Resistance Vs. Gate-to-Source Voltage



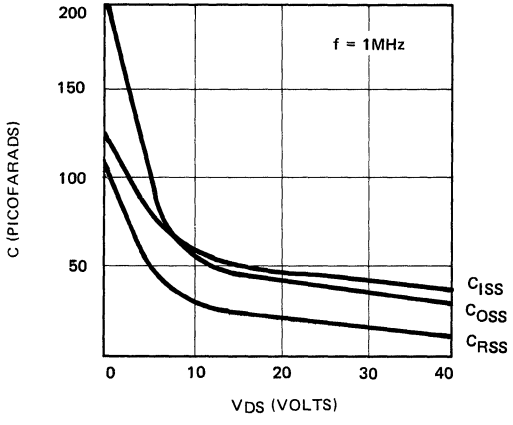
Transfer Characteristics



V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics