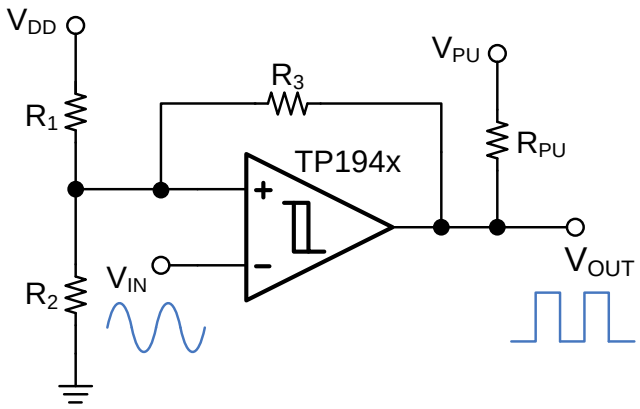
1.8V Micropower, RRIO, Open-Drain Output Comparators

Features

- **Down to 1.8V Supply Voltage: 1.8V to 5.5V**
- **Low Supply Current: 49 µA per Channel**
- **High-to-Low Propagation Delay: 70 ns**
- **Offset Voltage: ± 3.0 mV Maximum**
- **Offset Voltage Temperature Drift: 0.3 µV/°C**
- **Input Bias Current: 6 pA Typical**
- **Input Common-Mode Range Extends 200 mV**
- **Internal Hysteresis Ensures Clean Switching**
- **No Phase Reversal for Overdriven Inputs**
- **Open-Drain Output for Maximum Flexibility**
- **Green, Space-Saving SC70 Package Available**

Applications

- Threshold Detectors/Discriminators
- Sensing at Ground or Supply Line
- Peak and Zero-crossing Detectors
- Logic Level Shifting or Translation
- Window Comparators
- IR Receivers
- Clock and Data Signal Restoration
- Telecom, Portable Communications
- Portable and Battery Powered Systems



Typical Application of the TP194x Comparators

Description

The 3PEAK TP194x single/dual/quad micropower comparators feature rail-to-rail inputs and outputs, and fully specified single-supply operation down to +1.8V. The devices draw only 49µA per comparator while reaching 70ns high-to-low response time, and have open-drain outputs that can be pulled beyond V^- to 6V (max) above ground for maximum flexibility. In addition, their rail-to-rail input common-mode voltage range makes these comparators suitable for ultra-low-voltage operation. The input common-mode voltage range extends 200mV below ground and 200mV above supply, allowing both ground and supply sensing. The internal input hysteresis eliminates output switching due to internal input noise voltage, reducing current draw.

A +1.8V to +5.5V single-supply operating voltage range makes the TP194x family of comparators ideal for 2-cell battery-powered applications.

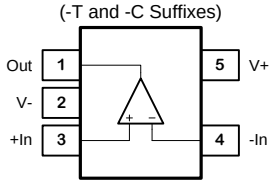
The TP1945 single comparator is available in tiny SC70 package for space-conservative designs. All chips are specified for the temperature range of –40°C to +85°C.

Related Products

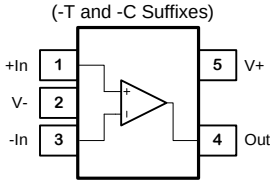
DEVICE	DESCRIPTION
TP1951/TP1951N /TP1952/TP1954	Fast 30ns, Low Power, Internal Hysteresis, ±3mV Maximum V_{OS}, – 0.2V to V_{DD} + 0.2V RRI, Push-Pull (CMOS/TTL) Output Comparators
TP1955/TP1955N /TP1956/TP1958	Fast 30ns, Low Power, Internal Hysteresis, ±3mV Maximum V_{OS}, – 0.2V to V_{DD} + 0.2V RRI, Open-Drain Output Comparators
TP1941/TP1941N /TP1942/TP1944	Fast 68ns, 46µA Micropower, Internal Hysteresis, ±3mV Maximum V_{OS}, – 0.2V to V_{DD} + 0.2V RRI, Push-Pull (CMOS/TTL) Output Comparators
TP1931 /TP1932/TP1934	950ns, 3µA, 1.8V, ±2.5mV V_{OS-MAX}, Internal Hysteresis, RRI, Push-Pull Output Comparators
TP1935 /TP1936/TP1938	950ns, 3µA, 1.8V, ±2.5mV V_{OS-MAX}, Internal Hysteresis, RRI, Open-Drain Comparators
TP2011 /TP2012/TP2014	Ultra-low 200nA, 13µs, 1.6V, ±2mV V_{OS-MAX}, Internal Hysteresis, RRI, Push-Pull (CMOS/TTL) Output Comparators
TP2015 /TP2016/TP2018	Ultra-low 200nA, 13µs, 1.6V, ±2mV V_{OS-MAX}, Internal Hysteresis, RRI, Open-Drain Output Comparators

Pin Configuration (Top View)

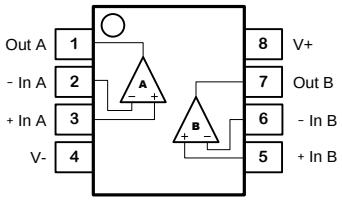
TP1945
5-Pin SOT23/SC70
(-T and -C Suffixes)



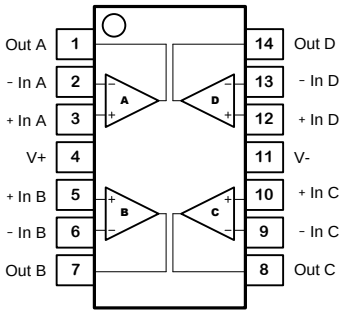
TP1945U
5-Pin SOT23/SC70
(-T and -C Suffixes)



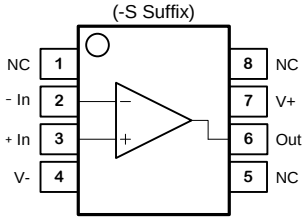
TP1946
8-Pin SOT23/SOIC/MSOP
(-T, -S and -V Suffixes)



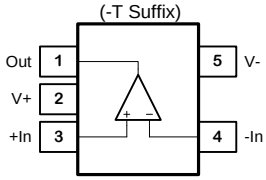
TP1948
14-Pin SOIC/TSSOP
(-S and -T Suffixes)



TP1945
8-Pin SOIC
(-S Suffix)



TP1945U2
5-Pin SOT23
(-T Suffix)



Order Information

Model Name	Order Number	Package	Transport Media, Quantity	Marking Information
TP1945	TP1945-TR	5-Pin SOT23	Tape and Reel, 3000	CT4YW (1)
	TP1945-CR	5-Pin SC70	Tape and Reel, 3000	CC4YW (1)
	TP1945-SR	8-Pin SOIC	Tape and Reel, 4000	1945S
TP1945U	TP1945U-TR	5-Pin SOT23	Tape and Reel, 3000	CA4YW (1)
	TP1945U-CR	5-Pin SC70	Tape and Reel, 3000	CB4YW (1)
TP1945U2	TP1945U2-TR	5-Pin SOT23	Tape and Reel, 3000	CE4YW (1)
TP1946	TP1946-TR	8-Pin SOT23	Tape and Reel, 3000	C46YW (1)
	TP1946-SR	8-Pin SOIC	Tape and Reel, 4000	C46S
	TP1946-VR	8-Pin MSOP	Tape and Reel, 3000	C46V
TP1948	TP1948-SR	14-Pin SOIC	Tape and Reel, 2500	1948S
	TP1948-TR	14-Pin TSSOP	Tape and Reel, 3000	1948T

Note (1): 'YW' is date coding scheme. 'Y' stands for calendar year, and 'W' stands for single workweek coding scheme.

Pin Functions

–IN: Inverting Input of the Comparator. Voltage range of this pin can go from V^- – 0.3V to V^+ + 0.3V.

+IN: Non-Inverting Input of Comparator. This pin has the same voltage range as –IN.

NC: No Connection.

V+ (V_{DD}): Positive Power Supply. Typically the voltage is from 1.8V to 5.5V. Split supplies are possible as long as the voltage between V+ and V– is between 1.8V and 5.5V. A bypass capacitor of 0.1µF as close to the part as possible should be used between power supply pins or between supply pins and ground.

V^- (V_{SS}): Negative Power Supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V^+ and V^- is from 1.8V to 5.5V. If it is not connected to ground, bypass it with a capacitor of 0.1µF as close to the part as possible.

OUT: Comparator Output. The voltage range extends to within millivolts of each supply rail.

Absolute Maximum Ratings Note 1

Supply Voltage: $V^+ – V^–$.....6.0V
Open-Drain Output..... $V^–$ + 6.0V
Input Voltage..... $V^–$ – 0.3 to V^+ + 0.3
Difference Input Voltage.....$V^–$ – 0.3 to V^+ + 0.3
Input Current: +IN, –IN, Note 2.....±10mA
Output Short-Circuit Current..... ±45mA

Output Short-Circuit Duration Note 3…..... Indefinite
Current at Output and Supply Pins..... ±50mA
Operating Temperature Range.....–40°C to 85°C
Maximum Junction Temperature..... 150°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8	8	kV
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	2	kV

Electrical Characteristics

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 27°C. V_{DD} = +1.8V to +5.5V, V_{IN+} = V_{DD}, V_{IN-} = 1.2V, R_{PU}=10kΩ, C_L =15pF.

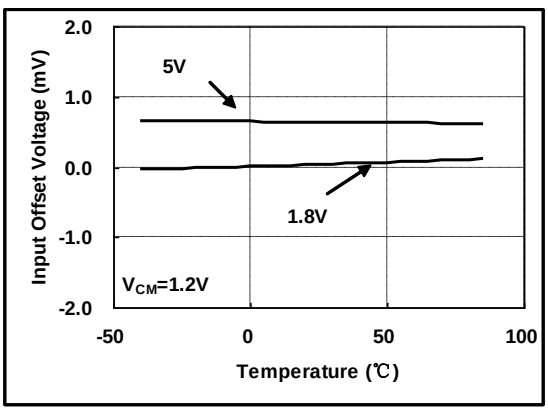
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage		●	1.8		5.5	V
V_{OS}	Input Offset Voltage Note 1	V_{CM} = 1.2V	●	-3.0	±0.6	+3.0	mV
V_{OS} TC	Input Offset Voltage Drift Note 1	V_{CM} = 1.2V	●		0.3		μV/°C
V_{HYST}	Input Hysteresis Voltage Note 1	V_{CM} = 1.2V		4	6	8	mV
V_{HYST} TC	Input Hysteresis Voltage Drift Note 1	V_{CM} = 1.2V	●		20		μV/°C
I_B	Input Bias Current	V_{CM} = 1.2V			6		pA
I_{OS}	Input Offset Current				4		pA
R_{IN}	Input Resistance				> 100		GΩ
C_{IN}	Input Capacitance	Differential Common Mode			2 4		pF
CMRR	Common Mode Rejection Ratio	V_{CM} = V_{SS} to V_{DD}	●	50	70		dB
V_{CM}	Common-mode Input Voltage Range		●	V^- - 0.2		V^+ + 0.2	V
PSRR	Power Supply Rejection Ratio		●	60	75		dB
V_{OL}	Low-Level Output Voltage	I_{OUT}=1mA	●			V^- + 0.3	V
I_{OH_leak}	High Level Output Current leakage					0.2	nA
I_{SC}	Output Short-Circuit Current	Sink or source current			25		mA
I_Q	Quiescent Current per Comparator				49	60	μA
t_F	Falling Time Note 2				5		ns
t_{PD-}	Propagation Delay (High-to-Low)	Input Overdrive=100mV, V_{IN-} = V_{SS}			70		ns

Note 1: The input offset voltage is the average of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

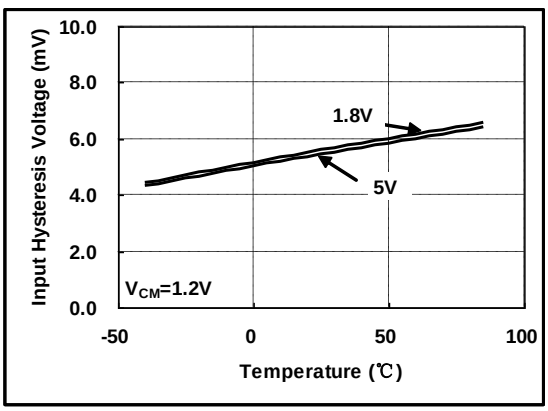
Note 2: Rising time t_R and low-to-high propagation delay t_{PD+} dependent on the pull-up resistor R_L and load capacitor C_L.

Typical Performance Characteristics

Input Offset Voltage V.S. Temperature

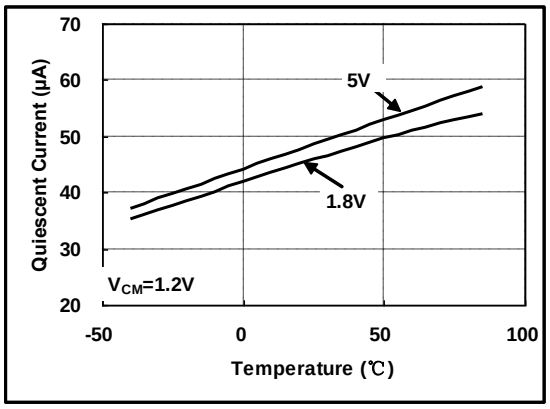


Input Hysteresis Voltage V.S. Temperature

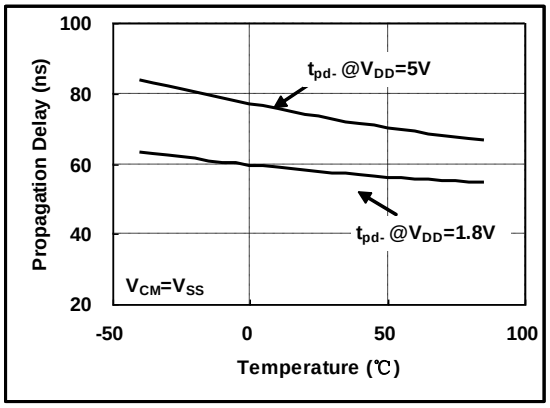


Typical Performance Characteristics

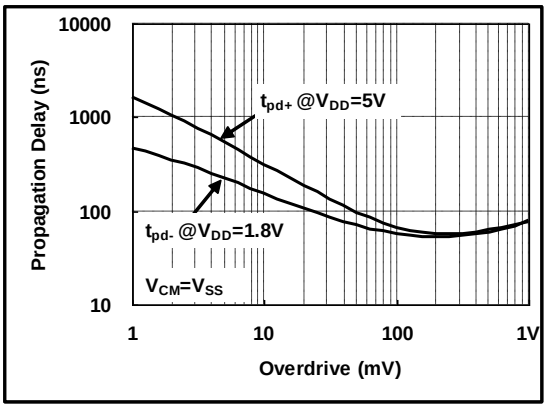
Quiescent Current V.S. Temperature



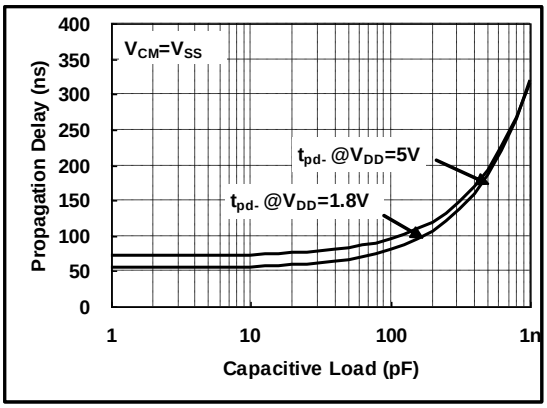
Propagation Delay V.S. Temperature



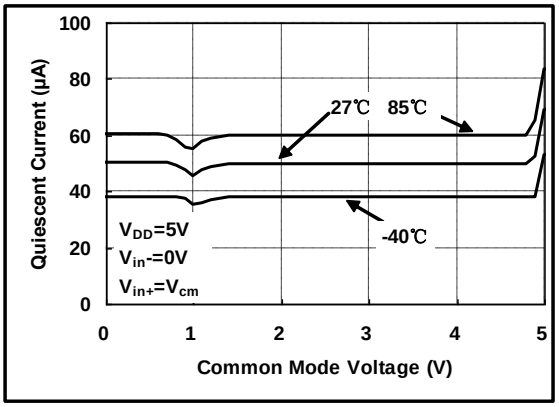
Propagation Delay V.S. Overdrive Voltage



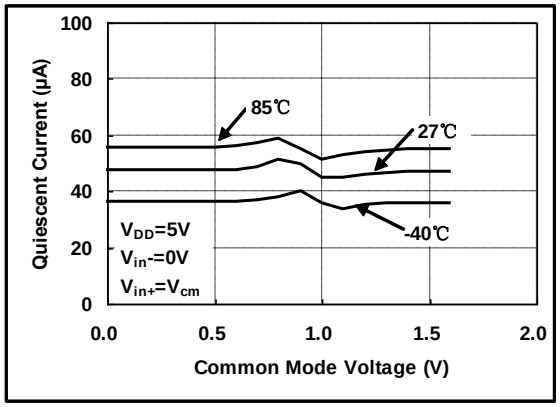
Propagation Delay V.S. Capacitor Loading



Quiescent Current V.S. Common mode Voltage

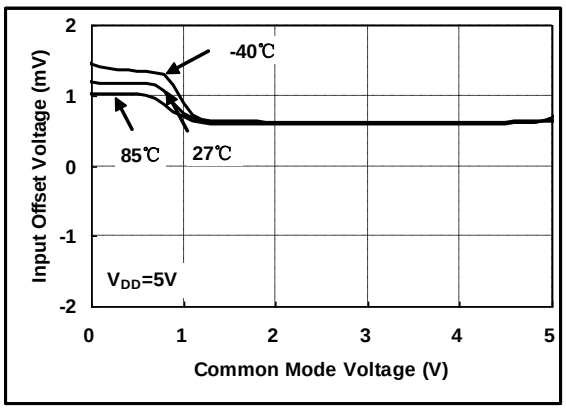


Quiescent Current V.S. Common mode Voltage

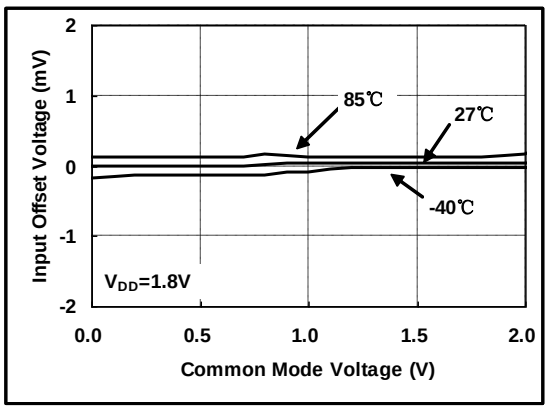


Typical Performance Characteristics

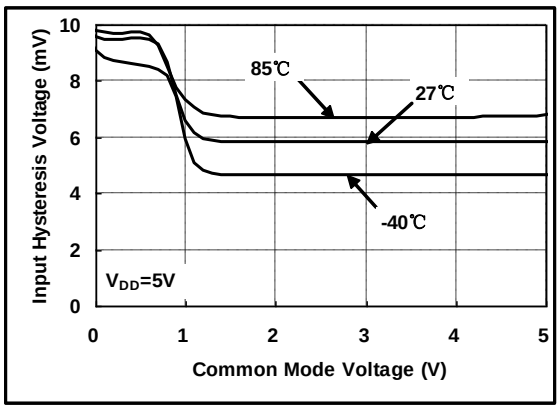
Input Offset Voltage V.S. Common mode Voltage



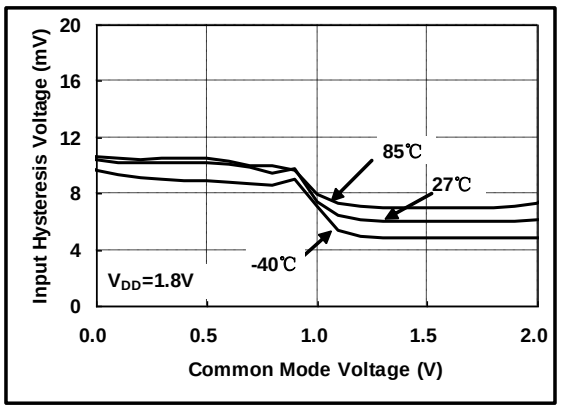
Input Offset Voltage V.S. Common mode Voltage



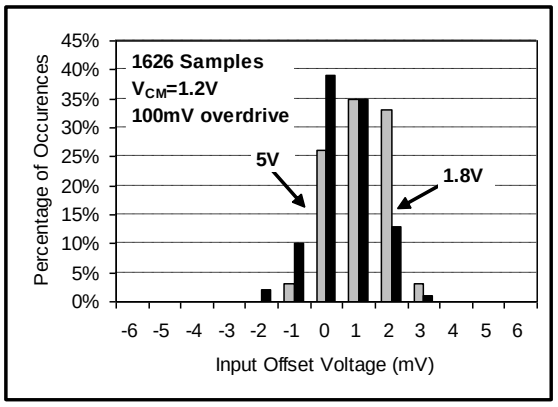
Input Hysteresis Voltage V.S. Common mode Voltage



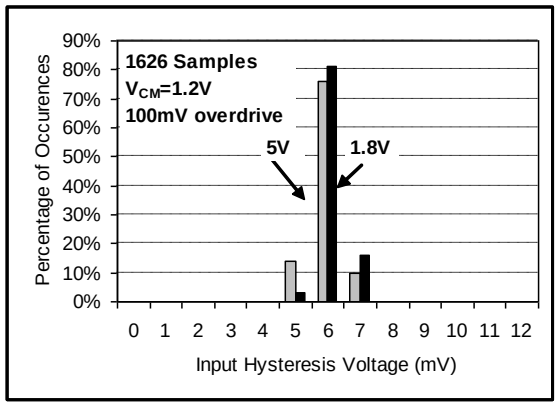
Input Hysteresis Voltage V.S. Common mode Voltage



Input Offset Voltage Distribution

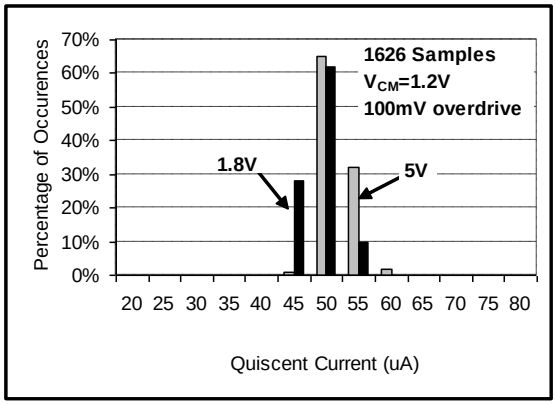


Input Hysteresis Voltage Distribution

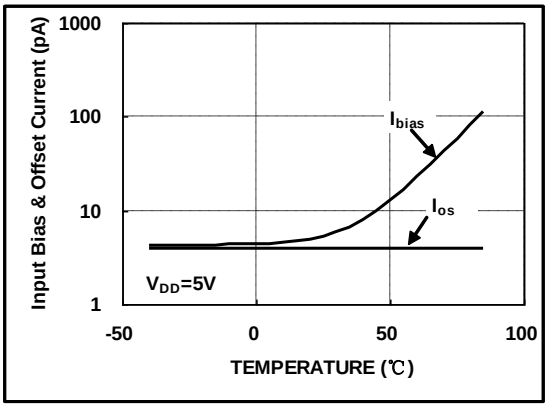


Typical Performance Characteristics

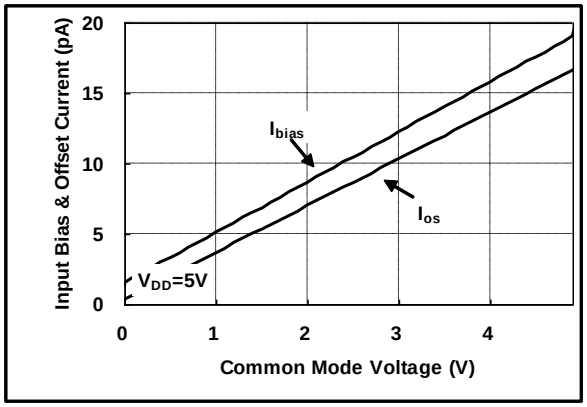
Quiescent Current Distribution



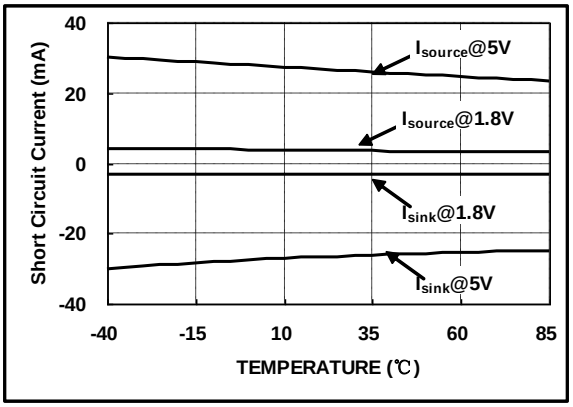
Input Bias and Offset Current V.S. Temperature



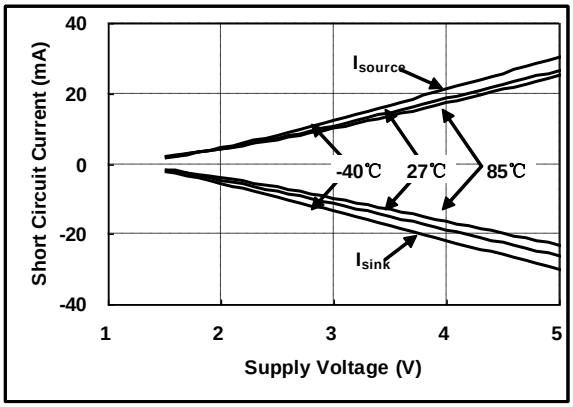
Input Bias&Offset Current V.S. Common mode Voltage



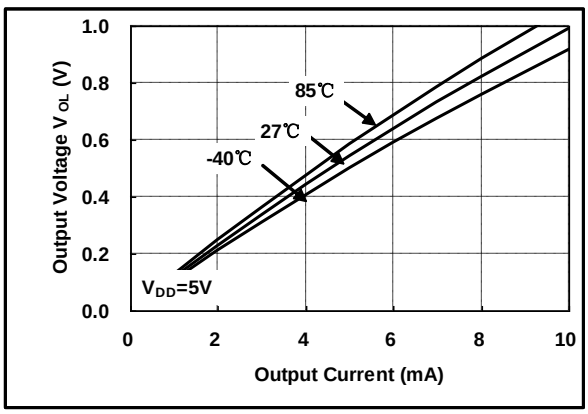
Output Short Circuit Current V.S. Temperature



Output Short Circuit Current V.S. Supply Voltage

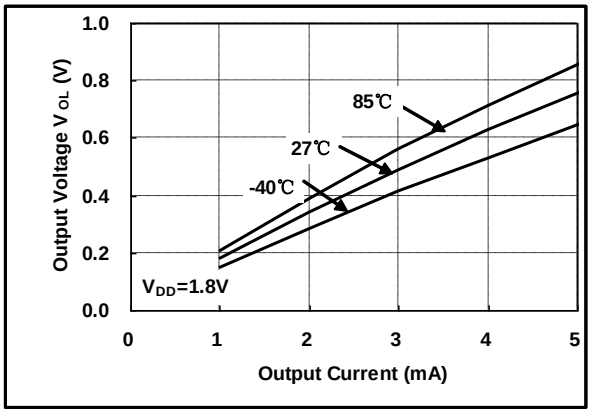


Output Voltage Headroom V.S. Output Current

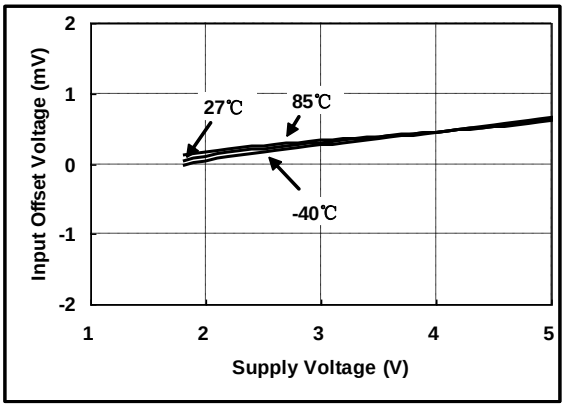


Typical Performance Characteristics

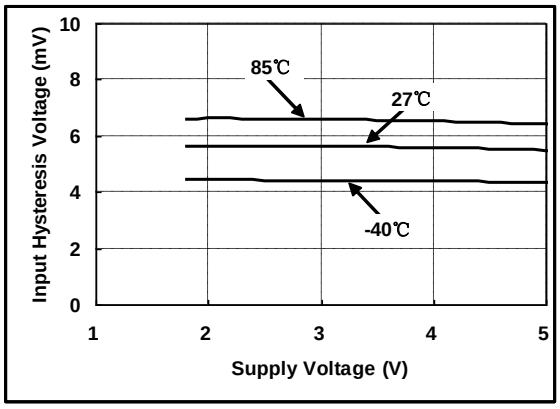
Output Voltage Headroom V.S. Output Current



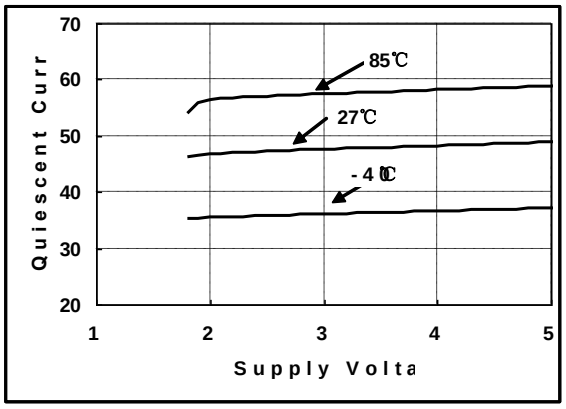
Input Offset Voltage V.S. Supply Voltage



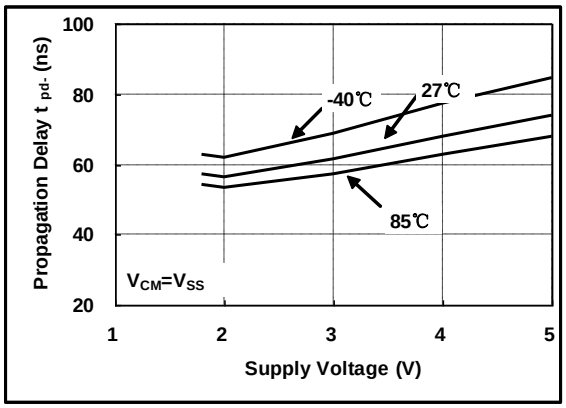
Input Hysteresis Voltage V.S. Supply Voltage



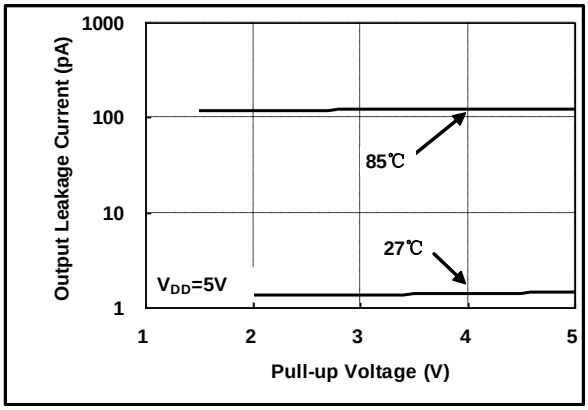
Quiescent Current V.S. Supply Voltage



High to low Propagation Delay V.S. Supply Voltage



Output Leakage Current V.S. Pull-up Voltage



Operation

The TP194x family single-supply comparators feature internal hysteresis, high speed, and low power. Input signal range extends beyond the negative and positive power supplies. The output can even extend all the way to the negative supply. The input stage is active over different ranges of common mode input voltage. Rail-to-rail input voltage range and low-voltage single-supply operation make these devices ideal for portable equipment.

Applications Information

Inputs

The TP194x comparator family uses CMOS transistors at the input which prevent phase inversion when the input pins exceed the supply voltages. Figure 1 shows an input voltage exceeding both supplies with no resulting phase inversion.

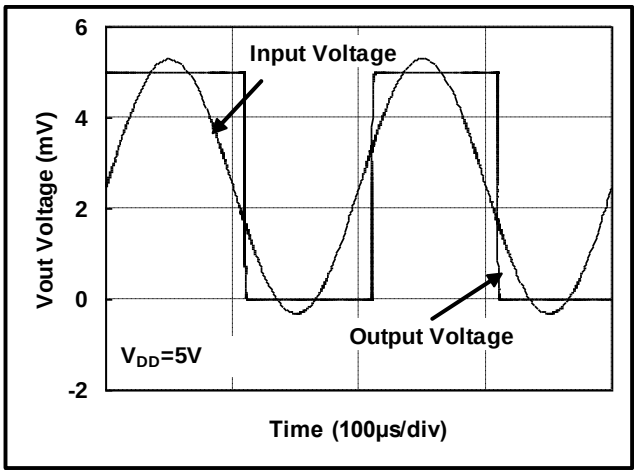


Figure 1. Comparator Response to Input Voltage

The electrostatic discharge (ESD) protection input structure of two back-to-back diodes and 1kΩ series resistors are used to limit the differential input voltage applied to the precision input of the comparator by clamping input voltages that exceed supply voltages, as shown in Figure 2. Large differential voltages exceeding the supply voltage should be avoided to prevent damage to the input stage.

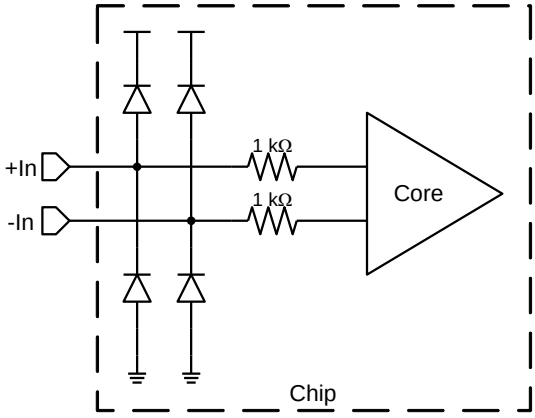


Figure 2. Equivalent Input Structure

Internal Hysteresis

Most high-speed comparators oscillate in the linear region because of noise or undesired parasitic feedback. This tends to occur when the voltage on one input is at or equal to the voltage on the other input. To counter the parasitic effects and noise, the TP194x implements internal hysteresis.

The hysteresis in a comparator creates two trip points: one for the rising input voltage and one for the falling input voltage. The difference between the trip points is the hysteresis. When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Figure 3 illustrates the case where IN- is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except the output would be inverted.

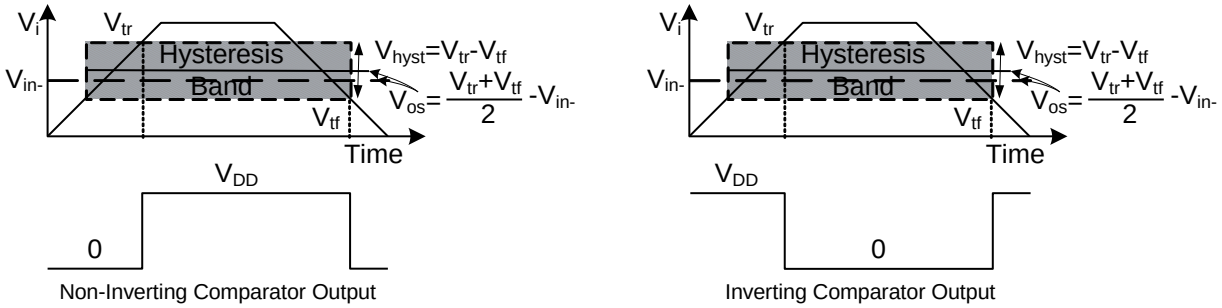


Figure 3. Comparator's hysteresis and offset

External Hysteresis

Greater flexibility in selecting hysteresis is achieved by using external resistors. Hysteresis reduces output chattering when one input is slowly moving past the other. It also helps in systems where it is best not to cycle between high and low states too frequently (e.g., air conditioner thermostatic control). Output chatter also increases the dynamic supply current.

Non-Inverting Comparator with Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network, as shown in Figure 4 and a voltage reference (V_r) at the inverting input.

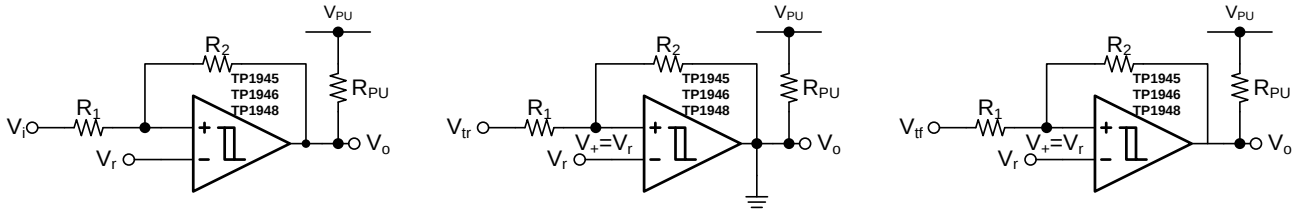


Figure 4. Non-Inverting Configuration with Hysteresis

When V_i is low, the output is also low. For the output to switch from low to high, V_i must rise up to V_{tr}. When V_i is high, the output is also high. In order for the comparator to switch back to a low state, V_i must equal V_{tf} before the non-inverting input V_+ is again equal to V_r.

$$V_r = \frac{R_2}{R_1 + R_2} V_{tr}$$

$$V_r = (V_{DD} - V_{tf}) \frac{R_1}{R_1 + R_2 + R_{PU}} + V_{tf}$$

$$V_{tr} = \frac{R_1 + R_2}{R_2} V_r$$

$$V_{tf} = \frac{R_1 + R_2 + R_{PU}}{R_2 + R_{PU}} V_r - \frac{R_1}{R_2 + R_{PU}} V_{DD}$$

$$V_{hyst} \approx \frac{R_1}{R_2 + R_{PU}} V_{DD} \quad \text{if } R_{PU} << R_2$$

Inverting Comparator with Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{DD}), as shown in Figure 5.

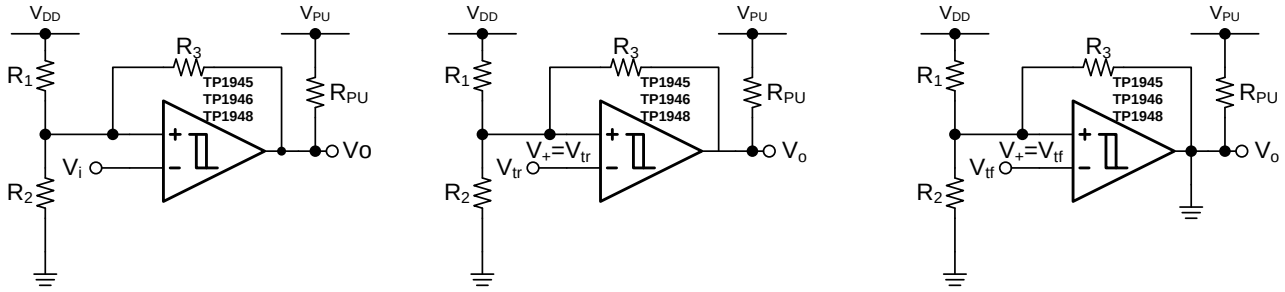


Figure 5. Inverting Configuration with Hysteresis

When V_i is greater than V_+, the output voltage is low. In this case, the three network resistors can be presented as paralleled resistor R_2 || R_3 in series with R_1. When V_i at the inverting input is less than V_+, the output voltage is high. The three network resistors can be represented as R_1 ||R_3 in series with R_2.

$$V_{tr} = \frac{R_2}{R_1 \| R_3 + R_2} V_{DD}$$

$$V_{tf} = \frac{R_2 \| R_3}{R_2 \| R_3 + R_1} V_{DD}$$

$$V_{hyst} = V_{tr} - V_{tf} = \frac{R_1 \| R_2}{R_1 \| R_2 + R_3} V_{DD}$$

Low Input Bias Current

The TP194x family is a CMOS comparator family and features very low input bias current in pA range. The low input bias current allows the comparators to be used in applications with high resistance sources. Care must be taken to minimize PCB Surface Leakage. See below section on “PCB Surface Leakage” for more details.

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5pA of current to flow,

which is greater than the TP194x's input bias current at +27°C (±6pA, typical). It is recommended to use multi-layer PCB layout and route the comparator's -IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 6 for Inverting configuration application.

1. For Non-Inverting Configuration:
   a) Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the same reference as the comparator.
2. For Inverting Configuration:
   a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the comparator (e.g., V_{DD}/2 or ground).
   b) Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

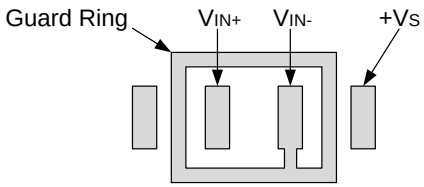


Figure 6. Example Guard Ring Layout for Inverting Comparator

Ground Sensing and Rail to Rail Output

The TP194x family implements a rail-to-rail topology that is capable of swinging to within 10mV of either rail. Since the inputs can go 300mV beyond either rail, the comparator can easily perform 'true ground' sensing.

The maximum output current is a function of total supply voltage. As the supply voltage of the comparator increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit condition. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.5V beyond either supply, otherwise current will flow through these diodes.

ESD

The TP194x family has reverse-biased ESD protection diodes on all inputs and output. Input and output pins can not be biased more than 300mV beyond either supply rail.

Power Supply Layout and Bypass

The TP194x family's power supply pin should have a local bypass capacitor (i.e., 0.01μF to 0.1μF) within 2mm for good high frequency performance. It can also use a bulk capacitor (i.e., 1μF or larger) within 100mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

Good ground layout improves performance by decreasing the amount of stray capacitance and noise at the comparator's inputs and outputs. To decrease stray capacitance, minimize PCB lengths and resistor leads, and place external components as close to the comparator' pins as possible.

Proper Board Layout

The TP194x family is a series of fast-switching, high-speed comparator and requires high-speed layout considerations. For best results, the following layout guidelines should be followed:

1. Use a printed circuit board (PCB) with a good, unbroken low-inductance ground plane.
2. Place a decoupling capacitor (0.1μF ceramic, surface-mount capacitor) as close as possible to supply.
3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
4. Solder the device directly to the PCB rather than using a socket.

5. For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. The topside ground plane should be placed between the output and inputs.

6. The ground pin ground trace should run under the device up to the bypass capacitor, thus shielding the inputs from the outputs.

Typical Applications

IR Receiver

The TP1945 is an ideal candidate to be used as an infrared receiver shown in Figure 7. The infrared photo diode creates a current relative to the amount of infrared light present. The current creates a voltage across R_D. When this voltage level cross the voltage applied by the voltage divider to the inverting input, the output transitions. Optional R_o provides additional hysteresis for noise immunity.

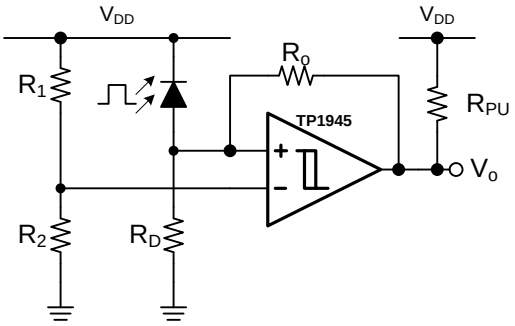


Figure 7. IR Receiver

Logic-Level Translator

Figure 8 shows an application that converts 5V logic to 3V logic levels. The TP1945/TP1946/TP1948 is powered by the +5V supply voltage, and the pull-up resistor for open-drain output is connected to the +3V supply voltage. This configuration allows the full 5V logic swing without creating overvoltage on the 3V logic inputs. For 3V to 5V logic-level translations, simply connect the 3V supply voltage to V+ and the 5V supply voltage to the pullup resistor.

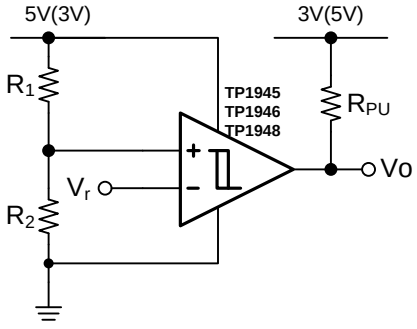


Figure 8. Logic-Level Translator

Windowed Comparator

Figure 9 shows one approach to designing a windowed comparator using a single TP201946 chip. Choose different thresholds by changing the values of R_1, R_2, and R_3. When input voltage V_i reaches the overvoltage threshold V_{OH}, the OutB gets low. Once V_i falls to the undervoltage threshold V_{UH}, the OutA gets low. When $V_{UH}<V_i<V_{OH}$, the output PowerGood gets high.

$$V_{OH} = V_r \bullet (R_1 + R_2 + R_3)/R_1 \quad (1)$$

$$V_{UH} = V_r \bullet (R_1 + R_2 + R_3)/(R_1 + R_2) \quad (2)$$

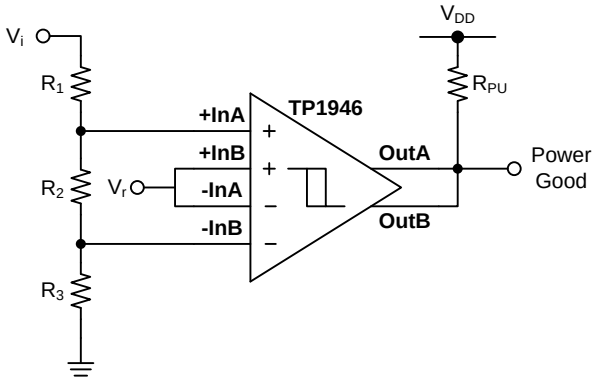
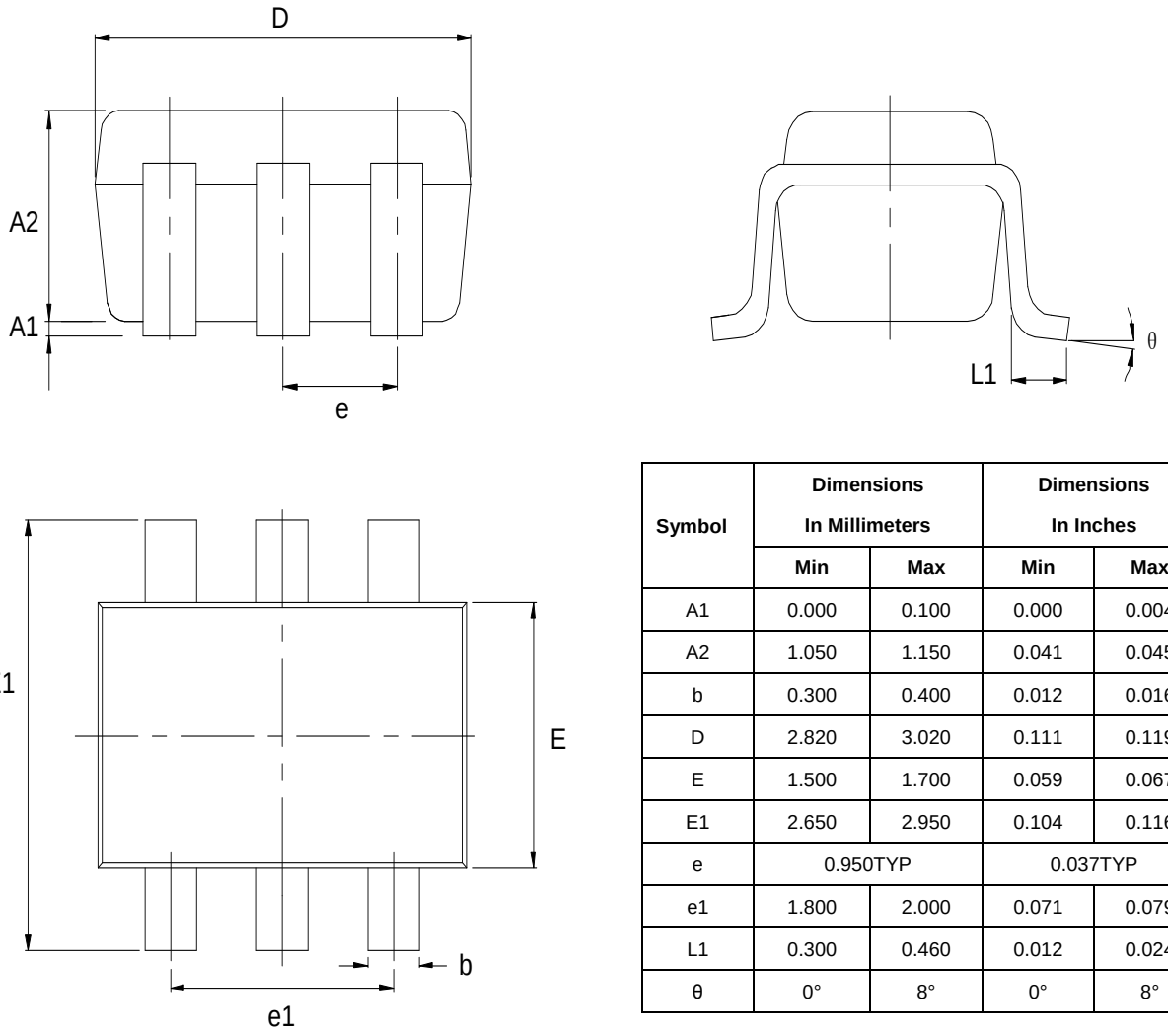


Figure 9. Windowed Comparator

Package Outline Dimensions

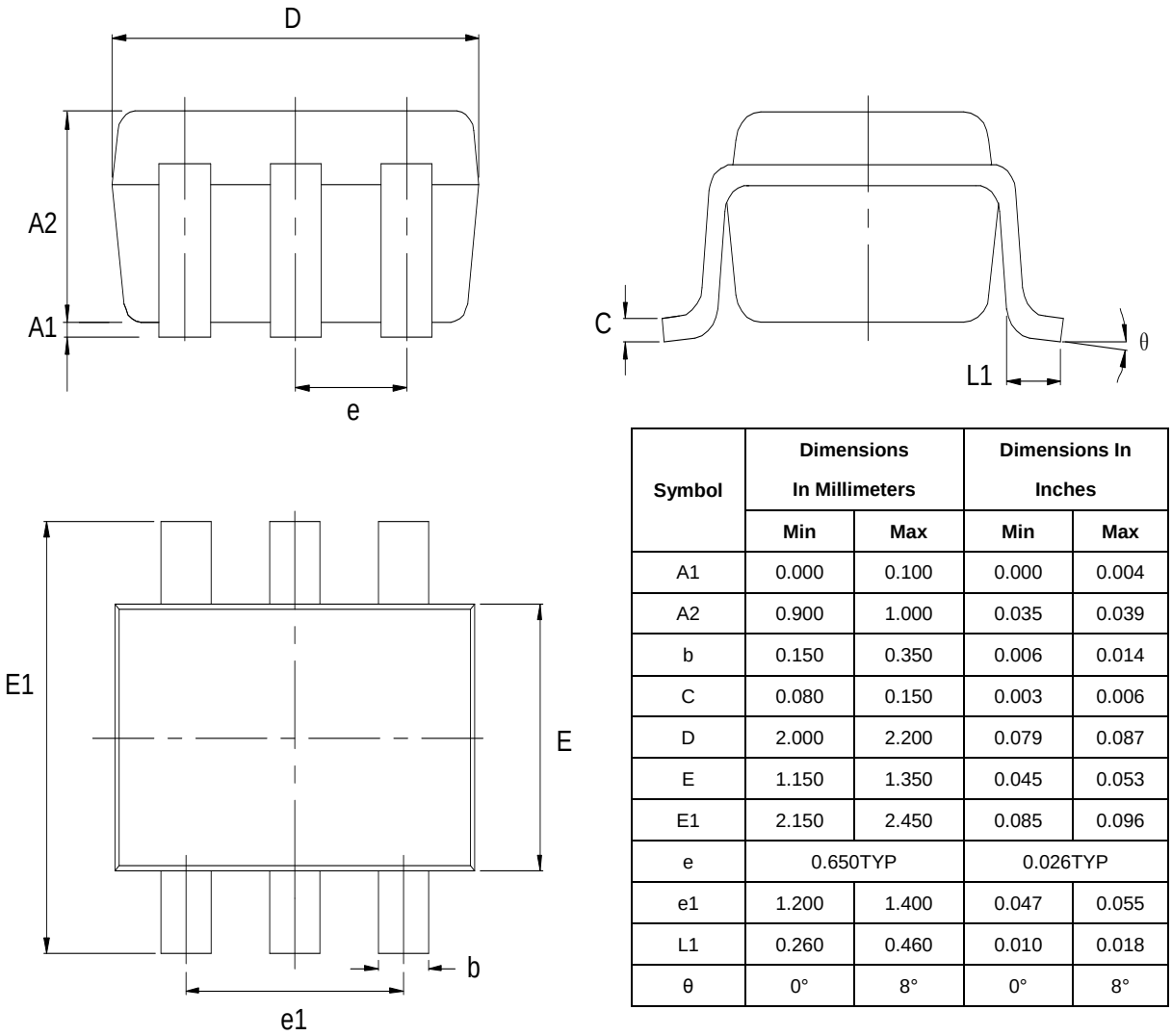
SOT23-5 / SOT23-6



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L1	0.300	0.460	0.012	0.024
θ	0°	8°	0°	8°

Package Outline Dimensions

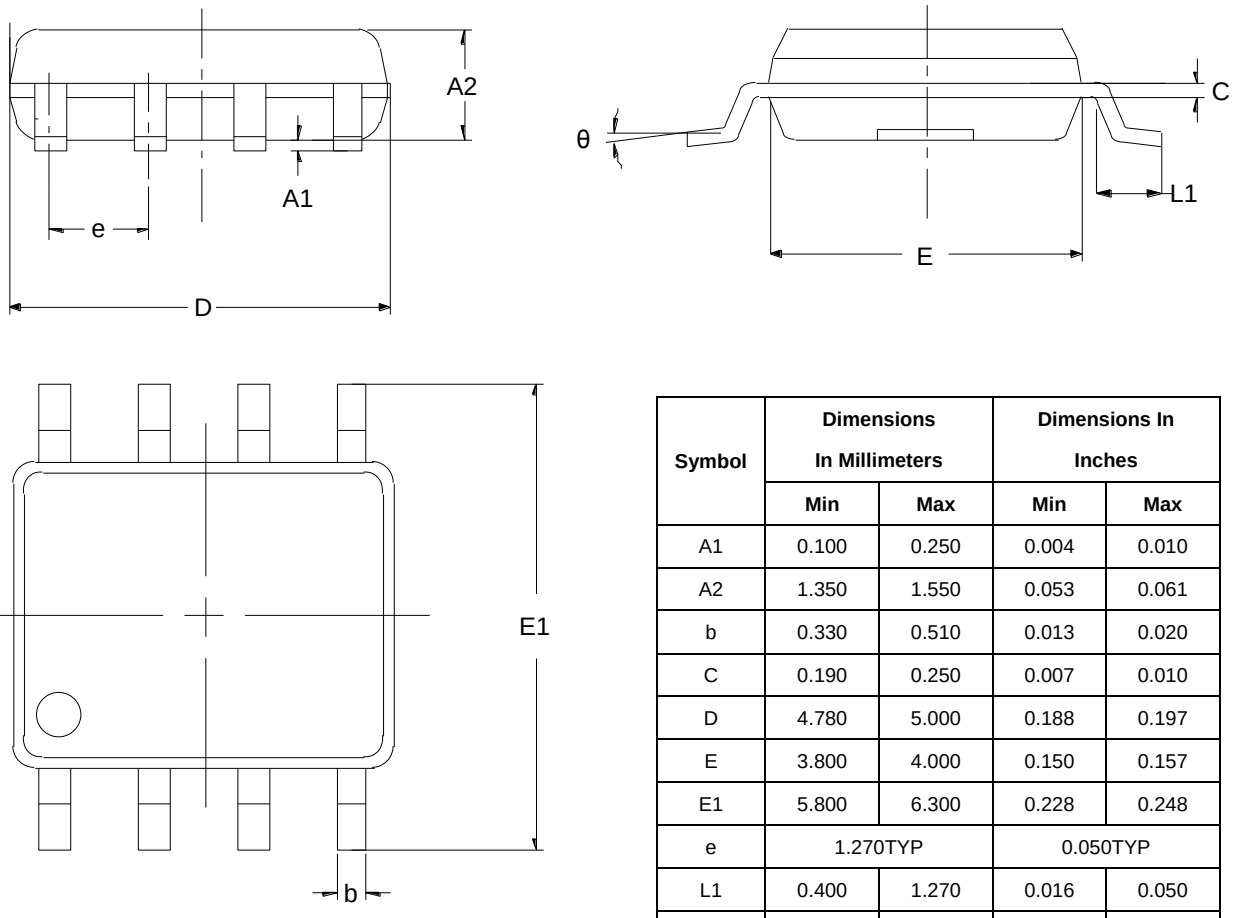
SC-70-5 / SC-70-6 (SOT353 / SOT363)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
C	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650TYP		0.026TYP	
e1	1.200	1.400	0.047	0.055
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

Package Outline Dimensions

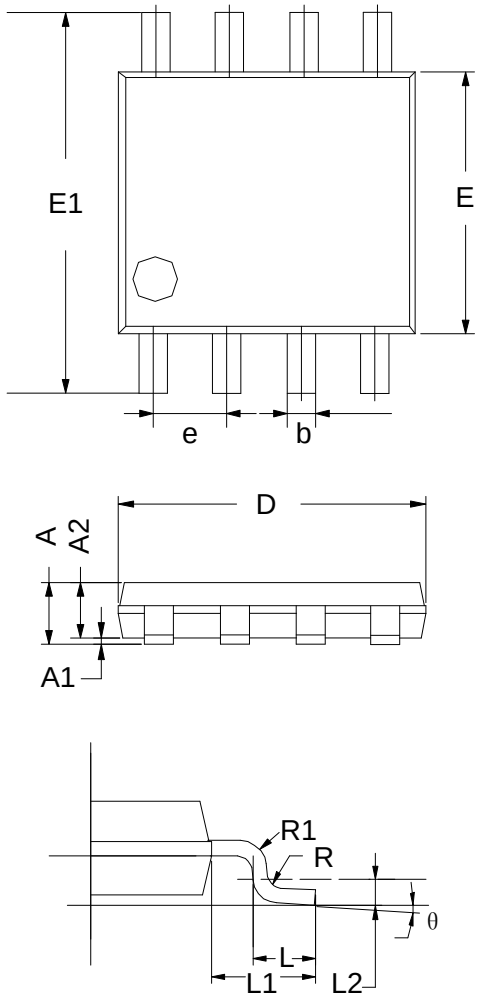
SO-8 (SOIC-8)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L1	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Outline Dimensions

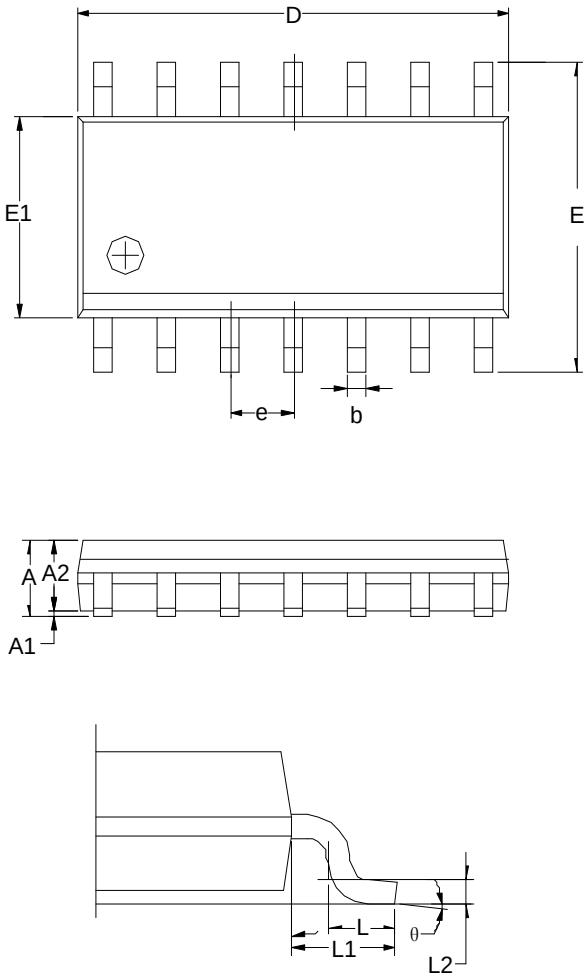
MSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
C	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L1	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°

Package Outline Dimensions

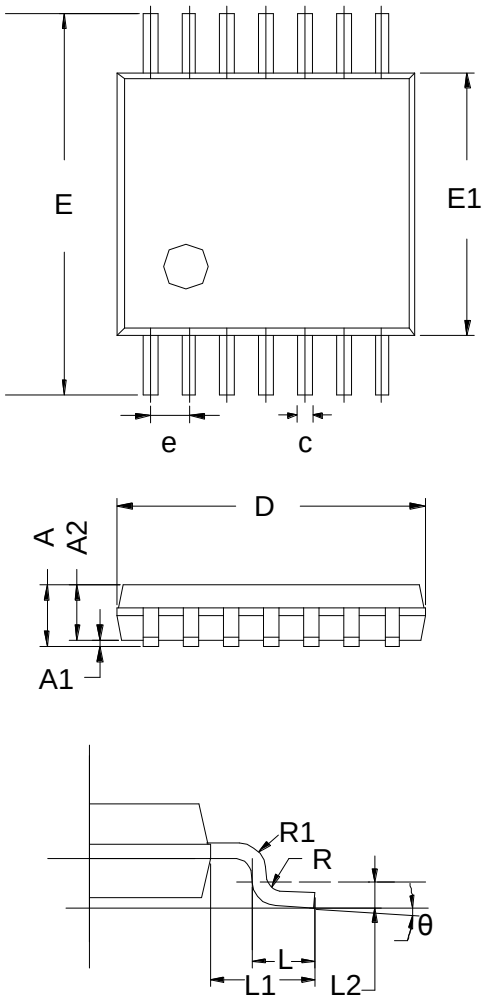
SO-14 (SOIC-14)



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
b	0.36		0.49
D	8.53	8.63	8.73
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25 BSC		
θ	0°		8°

Package Outline Dimensions

TSSOP-14



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
b	0.20	-	0.28
c	0.10	-	0.19
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
R	0.09	-	-
θ	0°	-	8°