National Semiconductor

TP3200, TP3204 SLIC-MC Magnetic Compensation SLICs

General Description

The TP3200 and TP3204 are monolithic Bipolar integrated circuits intended for use on subscriber and trunk interface cards of digital PABX and central office equipment. Each device contains a magnetic compensation circuit, a supervision circuit and three relay drivers with latched inputs.

The magnetic compensation circuit allows the use of a small, low cost line transformer by measuring the loop current, and producing an output current proportional to the d.c. value of the loop current. This output current is passed through a winding of the line transformer in such a way as to cancel the d.c. component of the magnetic flux. The transformer may be wound on a small ferrite core without an air gap.

The supervision output is used to detect off-hook, replicate dial pulses and terminate ringing on detection of ring-trip.

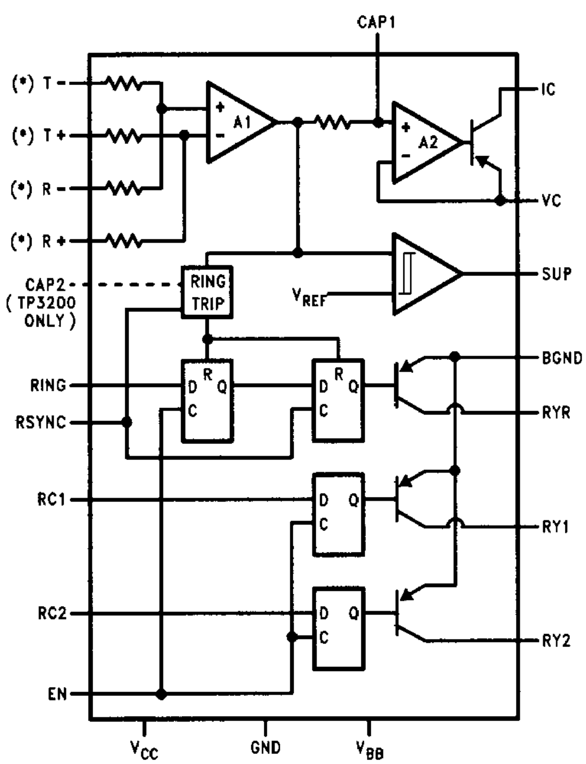
One of the three relay drivers is dedicated to the ring function, the other two are general purpose. TP3200 has PNP relay drivers, while the TP3204 has NPN relay drivers.

Features

- Magnetic Compensation Circuit allows the use of low cost ferrite core transformers
- Supervision Circuitry provides hook-switch detect, ring-trip detect and dial pulse replication
- Ring relay driver synchronized to zero-crossings
- Automatic ring-trip circuit—TP3200, TP3204
- Three Latched relay drivers
- −48 Volt relay drivers—TP3200
- +5 Volt relay drivers—TP3204
- Requires only ±5V supplies
- Thermal shutdown protection
- Power-Up reset on relay driver latches

Simplified Block Diagrams

TP3200



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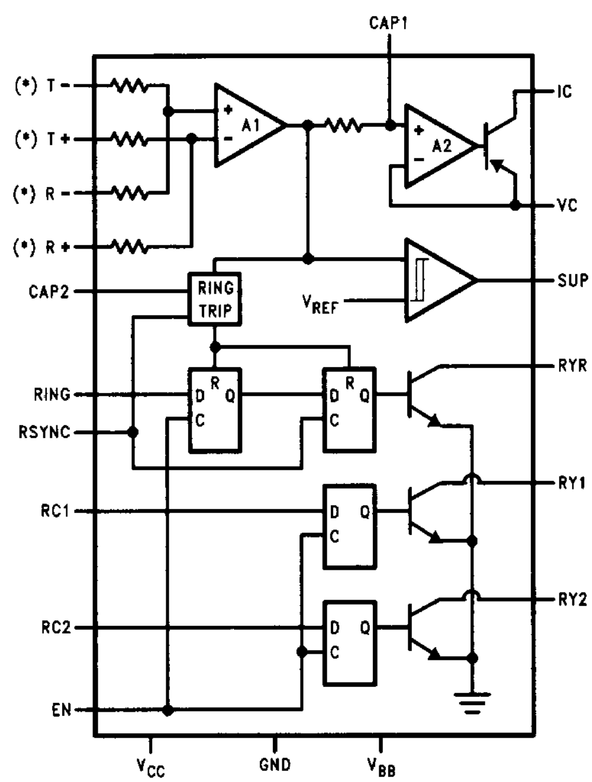
TP3204



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Operating Temperature	−25°C to +85°C
Storage Temperature	−65°C to +150°C
V_{CC} w.r.t. GND	7V
V_{BB} w.r.t. GND	−7V
V_{CC} w.r.t. V_{BB}	14V
V_{IC} w.r.t. GND	−70V
V_{RY} w.r.t. GND (TP3200)	−70V
V_{RY} w.r.t. GND (TP3204)	20V
Voltage at Sensing Inputs T+, T−, R+, R−, w.r.t. GND	300 V_{peak} (continuous)
T+, T−, R+, R− (FCC 68,302/d)	1000V (surge)
I_{RY} (TP3200)	−50 mA
I_{RY} (TP3204)	120 mA
Power Dissipation (Note 1)	1.5W
ESD (Note 2)	2 kV

Electrical Characteristics

Unless otherwise specified, Limits printed in bold characters are guaranteed for V_{CC} = +5.0V, V_{BB} = −5.0V ±5% and T_A = 0°C to 70°C by correlation with 100% production testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical values are measured at V_{CC} = +5.0V, V_{BB} = −5.0V, and T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
COMPENSATION CIRCUIT						
R_{IN}	Input Resistance	T+, T−, R+, R−		200		KΩ
V_{OS}	Offset Voltage at V_C	I_{LOOP} = 0 mA, R_S = 100Ω V_{BAT} = −48V, VC Open.	**−30**		**+30**	mV
A_V	Differential Voltage Gain	R_L = 150Ω, R_S = 100, Measure from T+, T−, R+ and R− to VC, I_{LOOP} = 10–100 mA	**0.147**		**0.153**	V/V
I_C	Maximum Compensation Current	The Output Current is Nominally Given by V_C/R_L, Where R_L is Connected from VC to GND.			25	mA
R_0	Output Resistance	Measure at CAP1	**80**	100	**120**	KΩ
VIC_{Sat}	Saturation Voltage at IC	I_C = 20 mA. Measure from VC to IC.		−0.3	**−1.5**	V
R_{IC}	IC Output Impedance	R_L = 150Ω, f = 1 kHz, I_C = 10 mA I_C = 20 mA		2 300		MΩ KΩ
N	Idle Noise	IC = 20 mA, R_L = 150Ω Connect 1500Ω from IC to V_{BAT}, Measure at IC.		0	**10**	dBrnC
SUPERVISION CIRCUITRY						
I_O	Ring-Trip Current Source	At CAP2		10		μA
I_R	Ring-Trip Threshhold	CAP2 = 0.1 μF, f = 20 Hz, R_S = 100Ω		12		mA
I+	Off-hook Positive Threshold	R_S = 100. Increase Loop Current until SUP Switches low.	**11**	13	**15**	mA
H	Off-hook Hysteresis	R_S = 100. Decrease Loop Current from I+ until SUP Switches High.		2		mA
RELAY DRIVERS						
VRY_{sat}	Relay Driver Saturation Voltage	TP3200, IRY = 30 mA TP3204, IRY = 80 mA			**−2.2** **1**	V V
DIGITAL INTERFACE (SUP, EN, RC1, RC2, RING, RSYNC)						
V_{OL}	Output Low Level	I_{OL} = 1.6 mA			**0.4**	V
V_{OH}	Output High Level	I_{OH} = 0.1 mA	**4**			V
V_{IL}	Input Low Level				**0.7**	V
V_{IH}	Input High Level		**2**			V
I_I	Input Current	0.7 < V_{IN} < 2.0	−0.1		0.1	mA
POWER DISSIPATION						
$I_{CC}0$	V_{CC} Supply I_{DLE} Current	R_L = 150Ω, R_S = 100Ω I_{LOOP} = 0 mA, All Relays Off		3	**4.5**	mA
$I_{BB}0$	V_{BB} Supply I_{DLE} Current	R_L = 150Ω, R_S = 100Ω, I_{LOOP} = 0 mA All Relays Off.		2.5	**4**	mA
$I_{CC}1$	V_{CC} Supply Active Current	R_L = 150Ω, R_S = 100Ω I_{LOOP} = 40 mA, I_{RY} = 10 mA		3	**4.7**	mA
$I_{BB}1$	V_{BB} Supply Active Current	R_L = 150Ω, R_S = 100Ω I_{LOOP} = 40 mA, I_{RY} = 10 mA		2.5	**4.2**	mA
PSRR+	Power Supply Rejection Ratio	$\Delta V_C/\Delta V_{CC}$, f = 1 kHz, CAP1 = 1 μF	**−60**	−80		dB
PSRR−		$\Delta V_C/\Delta V_{BB}$, f = 1 kHz, CAP1 = 1 μF	**−38**	−50		dB

Electrical Characteristics

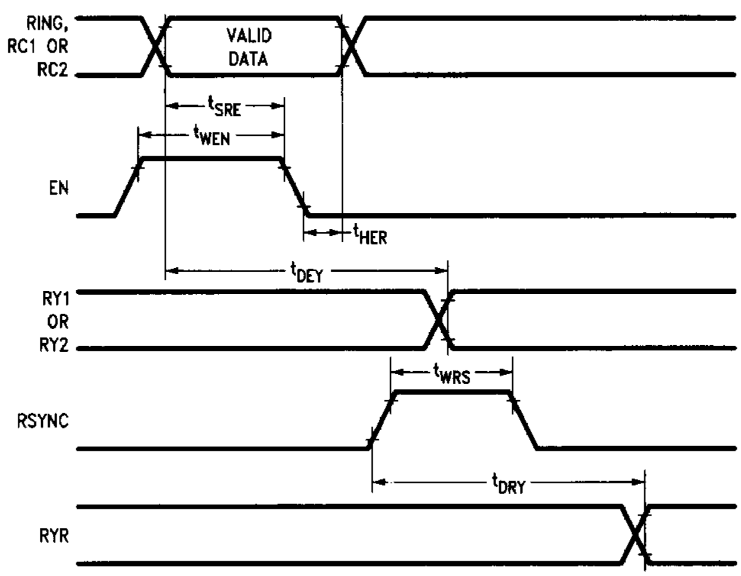
Unless otherwise specified, Limits printed in **bold** characters are guaranteed for $V_{CC} = +5.0V$, $V_{BB} = -5.0V \pm 5\%$ and $T_A = 0°C$ to $70°C$ by correlation with 100% production testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical values are measured at $V_{CC} = +5.0V$, $V_{BB} = -5.0V$, and $T_A = 25°C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TIMING (SEE DEFINITIONS AND TIMING CONVENTIONS FOR TEST METHOD INFORMATION)						
t_{SRE}	Set-up Time	Measure from RING, or RC1, RC2 Valid to EN Falling Edge.	**1**			μs
t_{HER}	Hold Time	Measure from EN Falling Edge to RING, RC1, or RC2 Invalid.	**1**			μs
t_{WEN} t_{WRS}	Input Pulse Width EN RSYNC	Active High	**2** **3**			μs μs
t_{DEY}	RY1, RY2 Drivers Delay Time	Measure from En Active and RC1, RC2, Valid to RY1, RY2 On or Off. $I_{RY\,(on)} = 10$ mA, $I_{RY\,(off)} = 0.1$ mA			20	μs
t_{DRY}	RYR Driver Delay Time	Measure from RSYNC Rising Edge to RYR On or Off. $I_{RYR\,(on)} = 10$ mA, $I_{RYR\,(off)} = 0.1$ mA			20	μs
t_{HS}	Off-Hook Detection Time	Measure from $I_{LOOP} = 20$ mA to SUP Transition from High to Low.		2.5		μs
t_R	Ring-Trip Detection Time	Measure from $I_{LOOP} = 20$ mA to, RYR Off, CAP2 = 0.1 μF, f = 20 Hz, $I_{RYR\,(on)} = 10$ mA, $I_{RYR\,(off)} = 0.1$ mA			150	ms

Note 1: Derate based on 150°C maximum junction temperature and thermal resistance of 80°C/W, junction to ambient.

Note 2: Device pins T+, T−, R+, R− are not guaranteed to meet the NSC standard requirement for ESD protection of 2000V. The functional requirements in the intended application prohibit the use of any additional components on chip for ESD protection. Maximum surge voltage for these pins is greater than 1000V, measured in accordance with FCC 68, 302/d.

Timing Diagram



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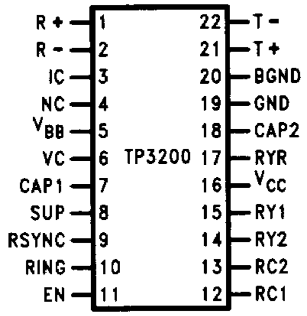
Connection Diagrams

Dual-In-Line



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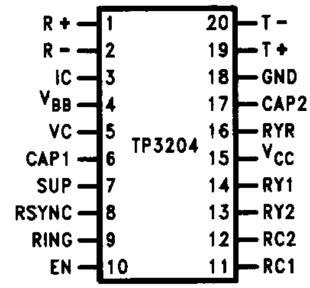
Top View

Order Number TP3200N
See NS Package Number N22A

Dual-In-Line



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Top View

Order Number TP3204N
See NS Package Number N20A

Description of Pin Functions

Name	Function
T+	Tip positive voltage sense input connected to the positive (GND) side of the Tip current sense resistor.
T−	Tip negative voltage sense input connected to the negative (line) side of the Tip current sense resistor.
BGND	Battery ground return for the relay drivers. This ground should be connected in such a way as to minimize noise due to relay switching and also to avoid large voltage transients in the presence of lightning. Preferably it should be connected to GND on the backplane.
R−	Ring negative voltage sense input connected to the negative (V_{BAT}) side of the Ring current sense resistor.
R+	Ring positive voltage sense input connected to the positive (line) side of the Ring current sense resistor.
V_{BB}	−5 volts ±5%
IC	Compensation current output. The current sourced by this output is proportional to the d.c. loop current flowing through the line transformer. By passing this current through an auxiliary winding of appropriate winding ratio, the average magnetic flux in the transformer core can be cancelled.
CAP1	External capacitor input required to filter voice frequency components from the loop current.

Name	Function
CAP2	External capacitor input required to perform charging and discharging by I_O for one cycle of ring frequency in order to perform the ring-trip function.
VC	Compensation voltage output. The output voltage at this pin is proportional to the d.c. loop current flowing through the line transformer. An external resistor R_L connected from VC to GND causes a current to flow from IC which is in turn proportional to the d.c. loop current.
GND	Analog ground.
V_{CC}	+5 volts ±5%
SUP	Supervision output indicating off-hook, Dial Pulse and Ring Trip status.
EN	Enable input. The RING, RC1 and RC2 inputs are gated in during the high state of EN and latched on the falling edge.
RC1	General purpose relay control input 1, used to turn on or off relay driver 1 (RY1) when enabled by EN.
RC2	General purpose relay control input 2 used to turn on or off relay driver 2 (RY2) when enabled by EN.
RING	Ring command input used to turn on or off the ring relay driver when enabled by EN.

Description of Pin Functions (Continued)

Name	Function
RSYNC	Ring Synchronization input used to synchronize the opening and closing of the ring relay with zero crossings of the ring signal, i.e., the minimum voltage across the relay contacts. RSYNC should nominally be a square wave generated by a zero crossing detector from the ringing signal, and should have the same frequency as the ringing signal.
RYR	Ring relay driver output.
RY1	General purpose relay driver output 1.
RY2	General purpose relay driver output 2.

Functional Description

MAGNETIC COMPENSATION CIRCUIT *(Figure 1)*

The magnetic compensation circuit measures the loop current by sensing the voltage across two matched battery feed resistors, R_S, using a high impedance thin film resistor bridge, and produces a voltage proportional to the instantaneous loop current at the output of the OpAmp, A1. This voltage is filtered by the external capacitor CAP1. The output voltage follower A2 and output transistor Q1 then reproduce this voltage at the VC output. Capacitor CAP1 is selected such that the voice frequency components of the loop current are attenuated enough to prevent the compensation current from affecting the subscriber circuit output impedance. A resistor R_L connected from VC to GND causes a current V_C/R_L to flow from the IC output. This output is connected to an auxiliary winding on the line transformer. By proper selection of resistor ratios and transformer winding ratios, the current I_C can exactly cancel the flux produced by the d.c. component of the loop current. The equation relating these parameters is:

$$NP/NC = A_V R_S / R_L$$

SUPERVISION CIRCUIT *(Figure 2)*

The supervision circuit consists of a loop current comparator with built-in hysteresis. The input of the supervision circuit is taken from the output of the Op Amp A1. The voltage at this point represents the instantaneous loop current. The output is the SUP output. During on-hook operation SUP is high. When the loop current increases beyond approximately 13 mA the SUP output goes low, indicating off-hook. When the loop current falls below approximately 11 mA SUP will go high indicating on-hook. In the presence of dial pulses, SUP will produce a square-wave replication of the dial pulses. During ringing, the comparator will detect the instantaneous ringing current through the loop, causing SUP to produce a square-wave with a mark-to-space ratio larger than 50% during the on-hook condition. When the telephone goes off-hook, the resultant dc loop current causes the mark-to-space ratio to decrease until the threshhold is reached when the duty cycle of SUP output is exactly 50%. This change in duty cycle can easily be detected digitally and the ringing terminated. This is the most flexible form of ring trip since it is frequency independent and is compatible with multi-frequency ringing. A second method of ring trip is described in the next section.

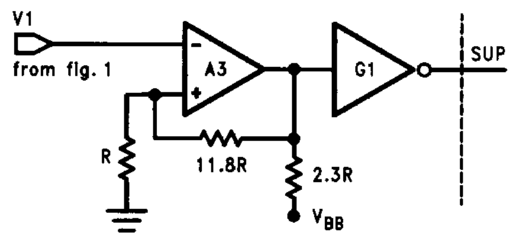

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FIGURE 2. Supervision Circuit

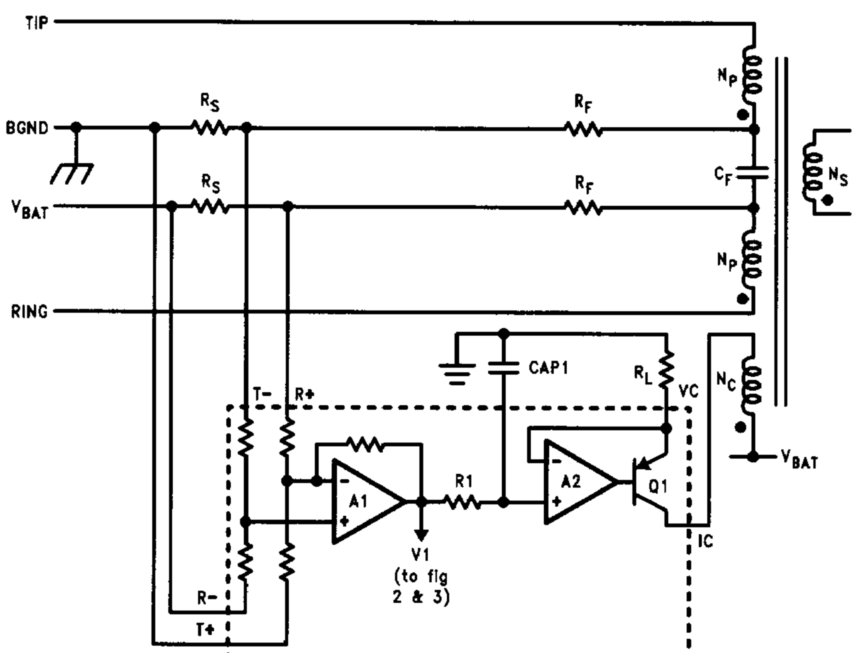

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FIGURE 1. Magnetic Compensation Circuit—Simplified Diagram

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Functional Description (Continued)

RING TRIP CIRCUIT *(Figure 3)*

The ring trip circuit takes its input from the output of A1, which represents the combination of instantaneous ringing current and DC off-hook loop current, if any. A1 output voltage is compared against a reference voltage at A4. Depending on the polarity of the comparator's output, current source I_O either sources or sinks 10 μA into CAP2. This results in the charging and discharging of CAP2. Each positive transition of RSYNC enables comparator A5 for approximately 20 μs through the one-shot circuit, after which CAP2 is discharged via Q2. Thus, the resulting voltage on CAP2 after one ring cycle indicates the average DC component of the loop current. When the threshold of approximately 12 mA is reached, comparator A5 generates a pulse output at RT which is used to reset the ring driver flip-flop at approximately the zero crossing of the ringing signal.

If multiple ring frequencies must be used on the same line, then a compromise capacitor value for CAP2 must be used. A 0.1 μF value is recommended for ringing frequencies of 16 Hz to 40 Hz, and 0.033 μF for 30 Hz to 70 Hz. Alternately, if SUP output is used to perform ring trip detect externally, CAP2 input should be grounded.

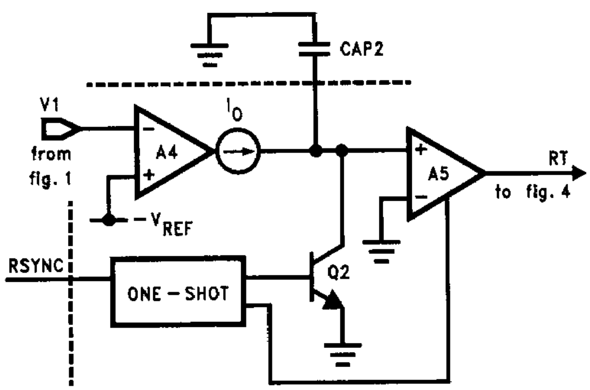

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FIGURE 3. Ring Trip Circuit

RING RELAY DRIVER *(Figure 4)*

The ring relay driver consists of the ring trip latch, a ring relay flip-flop and a relay driver output transistor. Based on the state of the ring input, the ring-trip latch is set or cleared when EN is active high, and latched on the falling edge of EN. It is also cleared by the ring trip circuit. Based on the output of the ring-trip latch, the ring relay flip-flop is set or cleared on the positive transition of RSYNC, insuring that the ring relay is turned on or off near the zero crossing of the ring signal to minimize relay contact wear. After the ring relay driver is turned on, the RING and/or EN inputs should be kept at logic low in order to prevent relay chattering.

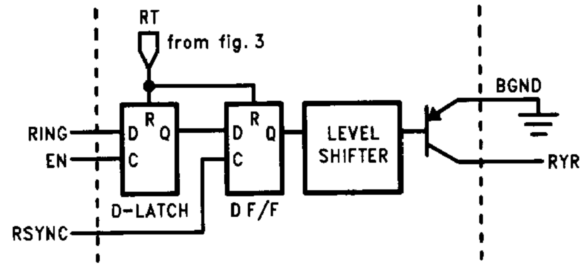

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FIGURE 4. Ring Trip Relay Driver (PNP-type)

GENERAL PURPOSE RELAY DRIVERS *(Figure 5)*

The general purpose relay drivers consist of a relay driver latch and relay driver output transistor. Depending on the state of the appropriate input RC1 or RC2, the relay driver latches are set or cleared when EN is active high, and latched on the falling edge of EN. On the TP3200 the relay driver pnp transistors operate between BGND and a negative supply as high as −70 volts, with relay currents as high as 30 mA. On the TP3204, the relay driver npn transistors operate with a positive supply voltage up to 20 volts.

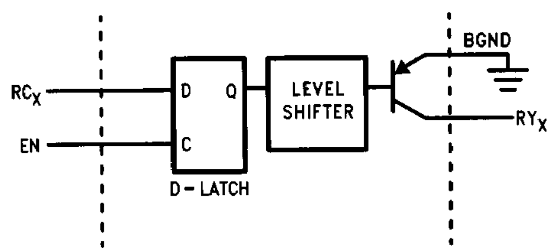

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FIGURE 5. Relay Drivers RY1 and RY2, (PNP-type)

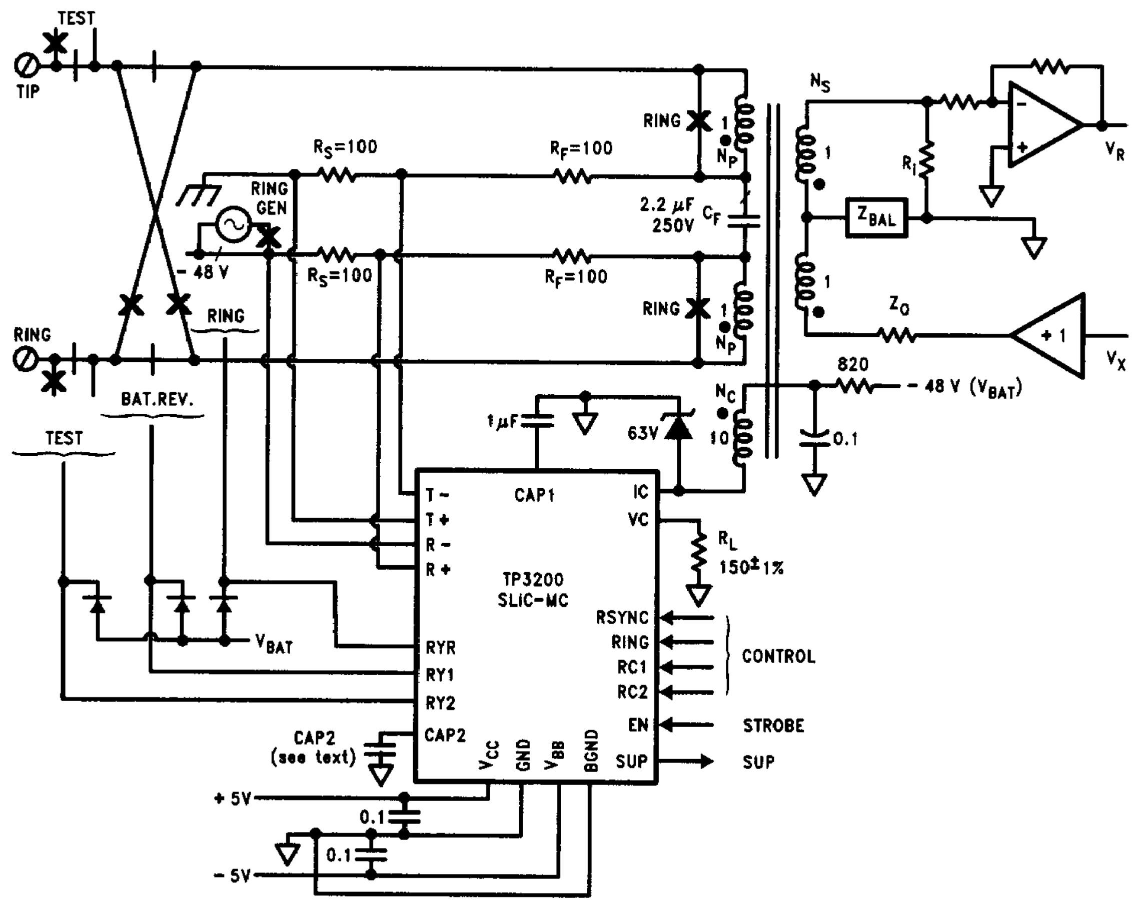

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FIGURE 6. Typical Applications Schematic

Note 1: Resistors R_S, R_F are matched to within ±0.1% to achieve 60 dB longitudinal balance.

Note 2: Transformer specifications for 600Ω Line Impedance, 5:1 cancellation ratio, $Z_o = R_i = 300\Omega$.

primary windings	N_P	210T	AWG 36
secondary windings	N_S	2x220T	AWG 38
compensation winding	N_C	2100T	AWG 42

Siemens Type RM 8-T35 core (A_L = 8400 nH/T^2)

Applications Information

Figure 6 illustrates the use of the TP3200/02/04 in one of many possible configurations. In this application, 200 ohm feed resistors ($R_S + R_F$) are used with a fixed −48 volt battery feed. 100 ohm current sense resistors in series with additional 100 ohm resistors insure that the T and R sense inputs of the device never see more than one half of any line transient voltages. The two general purpose relay drivers are used to operate a line test relay and a battery reversal relay. The a.c. line termination impedance is set by resistors R_i and Z_o (which should be equal to properly balance the hybrid), and the square of the turns ratio of the transformer, $(2N_p/N_S)^2$. The two amplifiers on the secondary side of the transformer are normally part of the PCM filter such as the TP3040, or the TP3050, TP3060, or TP3070 series of COMBO™ Codec/Filters. Z_{bal} represents the line circuit balance network. It is recommended that the IC pin be connected to the finish of the compensation winding in order to reduce the effective loading of the line impedance as well as Z_{bal} due to the reflected capacitance from the compensation winding at IC.

Ring voltage insertion is accomplished by breaking the battery feed path and superimposing the a.c. voltage upon the battery voltage. To prevent the feed decoupling capacitor from shunting ring current, a break contact is placed in series with C_F. To prevent the line transformer primary windings from attenuating the ring voltage or introducing distortion, make contacts are connected in shunt with the transformer primary.

Each relay driver output must be protected by a diode connected close to the relay coil. The IC pin must also be protected against line transients coupled through the transformer. Standard secondary transient suppression must also be connected from Tip to GND and Ring to GND.

In order to minimize errors in flux cancellation, the ratio of resistors R_S and R_L must be carefully controlled. Normally, all would reside on a common hybrid circuit. The two resistors, R_S, must be very accurately matched as must the two resistors, R_F, although R_F need not match R_S.

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Application Information (Continued)

The a.c. loop voltage will appear at IC, amplified by the ratio $N_C/(2N_p)$. A d.c. bias voltage must be provided which is sufficiently negative to prevent the compensation transistor from saturating without producing excessive power dissipation in the integrated circuit. This bias voltage can be an intermediate supply voltage or may be generated by the compensation current flowing through a resistance. The resistance may be made up of the transformer winding resistance and discrete resistances such as the filter resistor shown in *Figure 6*. If the bias voltage is generated by an IR drop, a higher supply voltage or lower compensation current ratio will be required to allow for large variations in loop current, resulting in higher circuit power dissipation.

Design Example

Assuming a 0 TLP on the line of 0 dBm into 600Ω, a 3 dB overload corresponds to a peak signal level of 1.55 volts. The peak a.c. voltage at IC is therefore 1.55N, where $N = N_C/(2N_P)$. At minimum loop current, the d.c. bias at IC must be sufficiently positive of the zener voltage to allow negative swings without clipping. Allowing for the winding resistance and reactance, a safe limit is:

$$R_C \bullet I_{LOOP}(\text{min})/N > 1.55N - V_{Z\,\text{min}} + |V_{BAT}|_{\text{max}} \quad (1)$$

where V_Z is the zener voltage, R_C is the total resistance from IC to V_{BAT}.

At the opposite extreme, the compensation transistor must not saturate with maximum loop current and positive peak swings. This corresponds to a voltage at IC of not less than

$$-VIC_{sat} + VC = 1.5 + I_{LOOP}(\text{max}) \bullet 2R_S \bullet A_V.$$

Thus we require:

$$|V_{BAT}|(\text{min}) > R_C \bullet I_{LOOP}(\text{max})/N + 1.55N - VIC_{SAT} + I_{LOOP}(\text{max}) \bullet 2R_S \bullet A_V \quad (2)$$

Substituting for R_C,

$$|V_{BAT}|(\text{min}) > (1.55N - V_{Z\text{min}} + |V_{BAT}|_{\text{max}}) \bullet I_{LOOP}(\text{max})/I_{LOOP}(\text{min}) + 1.55N + 1.5 + 30I_{LOOP}(\text{max})$$

Thus for a minimum loop current of 20 mA and a maximum of 100 mA, with a minimum zener voltage of 58 volts, and battery voltage from −42V to −54V, the maximum compensation current ratio is 6.18:1.

If N = 5 is chosen, i.e. N_C = 10 Np, the allowable range for R_C can then be calculated. From 1), R_C > 938Ω, and from 2), R_C < 1487Ω. Since the resistance of the compensation winding may typically be 600Ω, an additional 820Ω can safely be added in series to form a high frequency filter on the battery supply.

Finally, from $Np/Nc = A_V \bullet R_S/R_L$, R_L = 150Ω.

Further Information

For additional information on design of suitable transformers see National Semiconductor Application Note AN-439.

For information on the design of matched attenuators suitable for setting Receive TLP levels, see the data sheet "TP3052 Family of COMBO™ Devices".