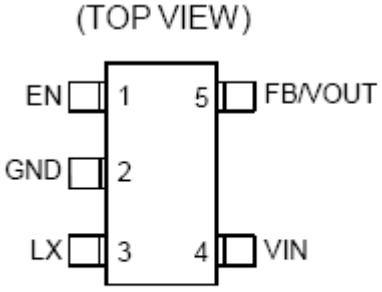
1.5MHz, 600mA, High Efficiency PWM Step-Down DC/DC Converter

General Description

The TP3406 is a high-efficiency pulse-width-modulated(PWM) step-down DC-DC converter. Capable of delivering600mA output current over a wide input voltage range from2.5V to 5.5V, the TP3406 is ideally suited for port -ableelectronic devices that are powered from 1-cell Li-ion battery or from other power sources within the range suchas cellular phones, PDAs and handy-terminals.
Internal synchronous rectifier with low RDS(ON) dramatically reduces cond -uction loss at PWM mode. No external Schottky diode is required in prac -tical application. The TP3406 automatically turns off the synchronous rec -tifier while the inductor current is low and enters discontinuous PWM mode. This can increase efficiency at light load condition.
The TP3406 enters Low-Dropout mode when normal PWM cannot provide regulated output voltage by continuously turning on the upper P-MOSFET.
TP3406 enter shutdown mode and consumes less than 0.1mA when EN pin is pulled low.
The switching ripple is easily smoothed-out by small package filtering elem -ents due to a fixed operation frequency of 1.5MHz. This along with small SOT-23-5 and TSOT-23-5 package provides small PCB area application.
Other features include soft start, lower internal reference voltage with 2% accuracy, over temperature protection,and over current protection

Pin Configurations



SOT-23-5/TSOT-23-5

Features

- +2.5V to +5.5V Input Range
- Adjustable Output From 0.6V to VIN
- 1.0V, 1.2V, 1.5V, 1.8V, 2.5V and 3.3V Fixed/ Adjustable Output Voltage
- 600mA Output Current, 1A Peak Current
- 95% Efficiency

- No Schottky Diode Required
- 1.5MHz Fixed-Frequency PWM Operation
- Small SOT-23-5 and TSOT-23-5 Package
- RoHS Compliant and 100% Lead (Pb)-Free

Applications

- Cellular Telephones
- Personal Information Appliances
- Wireless and DSL Modems
- MP3 Players
- Portable Instruments

Typical Application Circuit

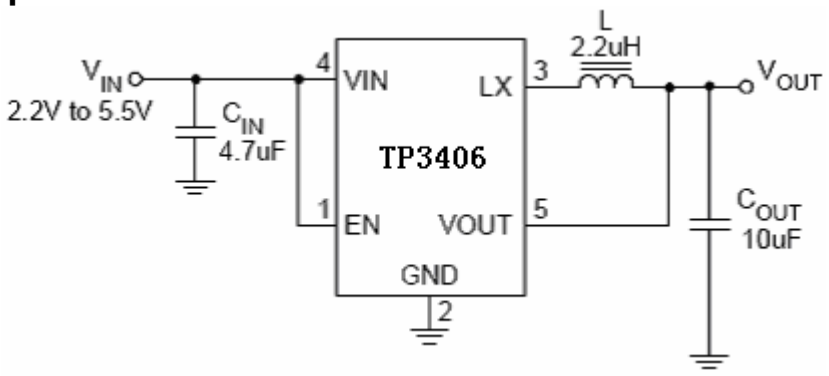


Figure 1. Fixed Voltage Regulator

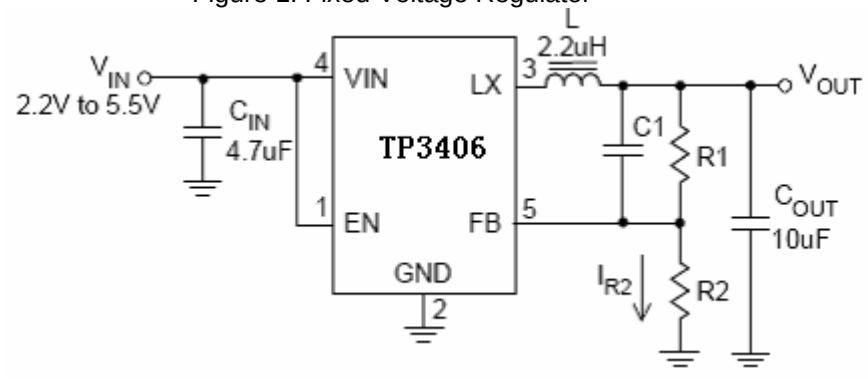


Figure 2. Adjustable Voltage Regulator

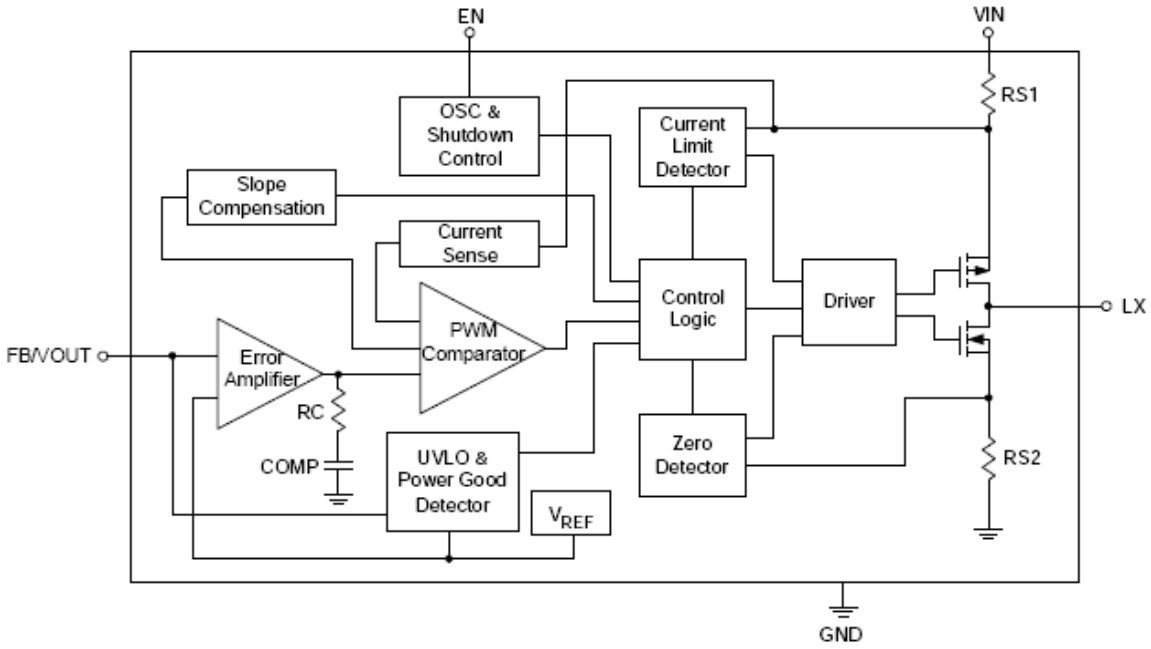
$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

with R2 = 300kΩ to 60kΩ so the IR2 = 2μA to 10μA,
and (R1 x C1) should be in the range between 3x10-6 and 6x10-6 for component selection.

Functional Pin Description

Pin Number	Pin Name	Pin Function
1	EN	Chip Enable (Active High, do not leave EN pin floating, and V_{EN} < V_{IN} + 0.6V>
2	GND	Ground.
3	LX	Pin for Switching.
4	VIN	Power Input.
5	FB/VOUT	Feedback Input Pin.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- 6.5V
- Enable, FB Voltage---------- V_{IN} + 0.6V
- Power Dissipation, P_D @ T_A = 25°C

SOT-23-5, TSOT-23-5 ---------- 0.4W

- Package Thermal Resistance (Note 4)

SOT-23-5, TSOT-23-5, θ_{JA} ---------- 250°C/W
SOT-23-5, TSOT-23-5, θ_{JC} ---------- 130°C/W

- Junction Temperature Range ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 2)

HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Supply Input Voltage ---------- 2.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.6V, V_{OUT} = 2.5V, V_{REF} = 0.6V, L = 2.2μH, C_{IN} = 4.7μF, C_{OUT} = 10μF, T_A = 25°C, I_{MAX} = 600mA unless otherwise specified)

Parameter		Symbol	Test Conditions		Min	Typ	Max	Units
Input Voltage Range		V_{IN}			2.5		5.5	V
Quiescent Current		I_Q	I_{OUT} = 0mA, V_{FB} = V_{REF} + 5%			50	100	μA
Shutdown Current		I_{SHDN}	EN = GND			0.1	1	μA
Reference Voltage		V_{REF}	For adjustable output voltage		0.588	0.6	0.612	V
Adjustable Output Range		V_{OUT}			V_{REF}		V_{IN}–0.2	V
Output Voltage Accuracy	Fix	ΔV_{OUT}	V_{IN} = 2.2 to 5.5V, V_{OUT} = 1.0V 0A < I_{OUT} < 600mA		–3		+3	%
			V_{IN} = 2.2 to 5.5V, V_{OUT} = 1.2V 0A < I_{OUT} < 600mA		–3		+3	%
			V_{IN} = 2.2 to 5.5V, V_{OUT} = 1.5V 0A < I_{OUT} < 600mA		–3		+3	%
			V_{IN} = 2.2 to 5.5V, V_{OUT} = 1.8V 0A < I_{OUT} < 600mA		–3		+3	%
			V_{IN} = 2.2 to 5.5V, V_{OUT} = 2.5V 0A < I_{OUT} < 600mA		–3		+3	%
			V_{IN} = 2.2 to 5.5V, V_{OUT} = 3.3V 0A < I_{OUT} < 600mA		–3		+3	%
	Adjustable	ΔV_{OUT}	V_{IN} = V_{OUT} + 0.2V to 5.5V, V_{IN} ≧ 3.5V		–3		+3	%
			V_{IN} = V_{OUT} + 0.4V to 5.5V, V_{IN} ≧ 2.2V		–3		+3	%
FB Input Current		I_{FB}	V_{FB} = V_{IN}		–50		50	nA
PMOSFET R_{ON}		$R_{DS(ON)}$	I_{OUT} = 200mA	V_{IN} = 3.6V		0.3		Ω
				V_{IN} = 2.5V		0.4		
NMOSFET R_{ON}		$N_{RDS(ON)}$	I_{OUT} = 200mA	V_{IN} = 3.6V		0.25		Ω
				V_{IN} = 2.5V		0.35		
P-Channel Current Limit		$I_{P(LM)}$	V_{IN} = 2.5V to 5.5 V		1		1.8	A
EN High-Level Input Voltage		V_{ENH}	V_{IN} = 2.5V to 5.5V		1.5			V
EN Low-Level Input Voltage		V_{ENL}	V_{IN} = 2.5V to 5.5V				0.4	V
Undervoltage Lock Out threshold						1.8		V
Hysteresis						0.1		V
Oscillator Frequency		f_{OSC}	V_{IN} = 3.6V, I_{OUT} = 100mA		1.2	1.5	1.8	MHz
Thermal Shutdown Temperature		T_{SD}				160		℃
Min. On Time						50		ns
Max. Duty Cycle					100			%
LX Leakage Current			V_{IN} = 3.6V, V_{LX} = 0V or V_{LX} = 3.6V		–1		1	μA

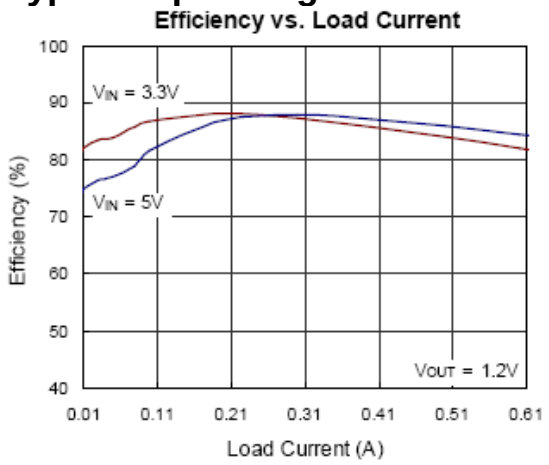
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

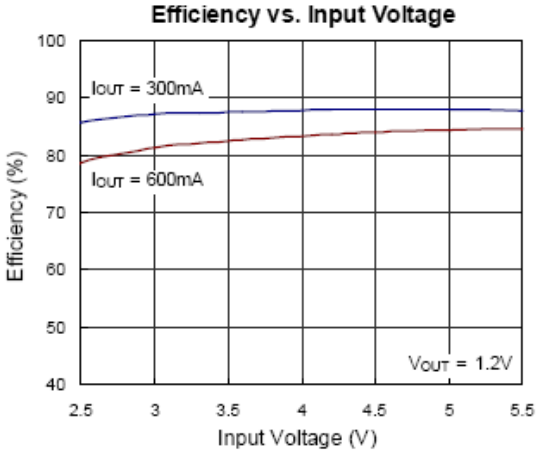
Note 2. Devices are ESD sensitive. Handling precaution recommended.

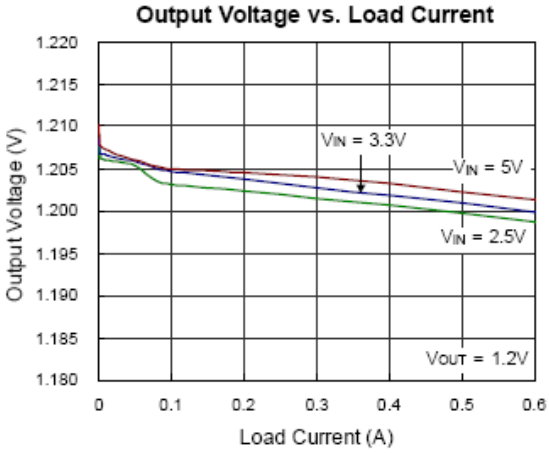
Note 3. The device is not guaranteed to function outside its operating conditions.

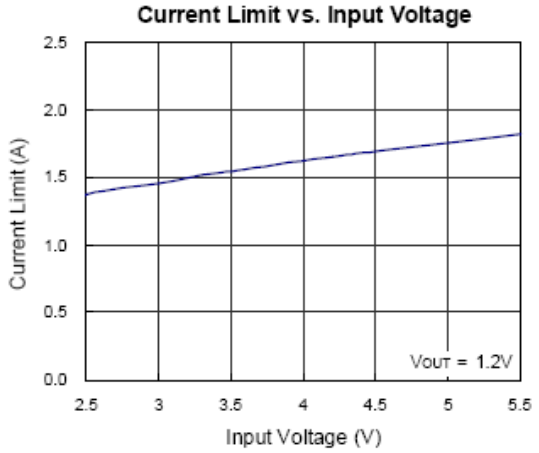
Note 4. JA is measured in the natural convection at TA = 25 C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Pin 2 of SOT-23-5/TSOT-23-5 packages is the case position for JC measurement.

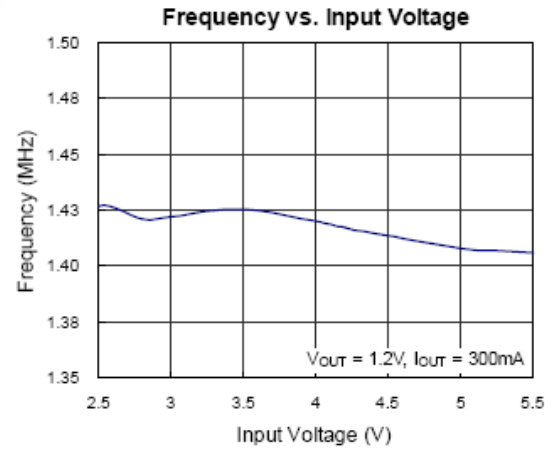
Typical Operating Characteristics

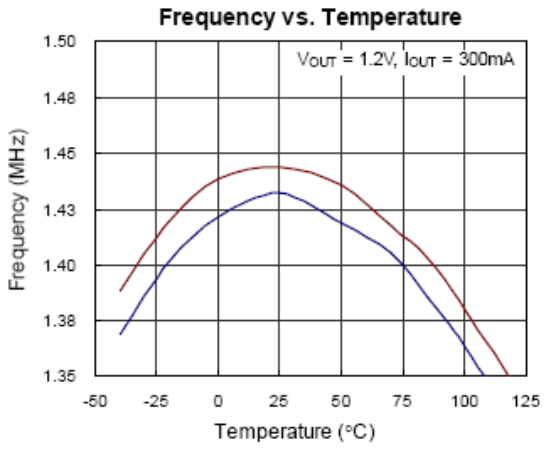


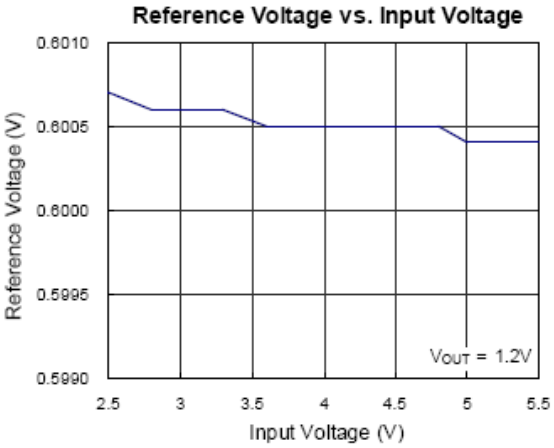


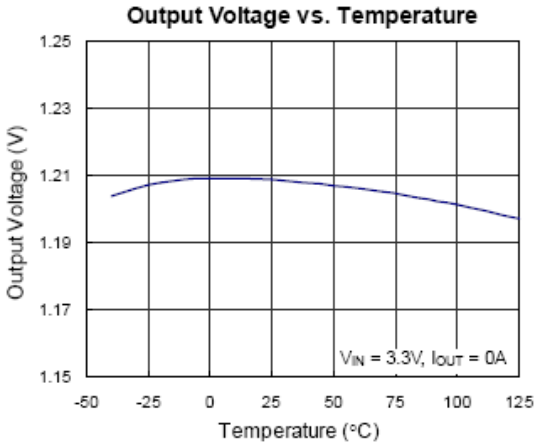












Applications Information

The basic TP3406 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by CIN and COUT.

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔIL increases with higher VIN and decreases with higher inducta -nce.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right]\left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor.

A reasonable starting point for selecting the ripple current is ΔIL = 0.4(IMAX). The largest ripple current occurs at the highest VIN. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right]\left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores,forcing the use of more expensive ferrite or mollypermalloy cores. Actual core loss is independent of core size for a
fixed inductor value but it is very dependent on the inductance selected. As the inductance increa -ses, corelosses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losseswill increase. Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard”, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!
Different core materials and shapes will change the size/current and price/current relationship of an inductor.
Toroid or shielded pot cores in ferrite or permalloy materials are small and don’ t radiate energy but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price vs size requirements and any radiated field/EMI requirements.

CIN and COUT Selection

The input capacitance, CIN, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at VIN = 2VOUT, where IRMS = IOUT/2. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.
The selection of COUT is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, ΔVOUT, is determined by :

$$\Delta V_{OUT} \le \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple is highest at maximum input voltage since ΔIL increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are
all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors

have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost –sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductan –ce can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input andoutput. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, VIN. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at VIN large enough to damage the
part.

Output Voltage Programming

The resistive divider allows the VFB pin to sense a fraction of the output voltage as shown in Figure 4.

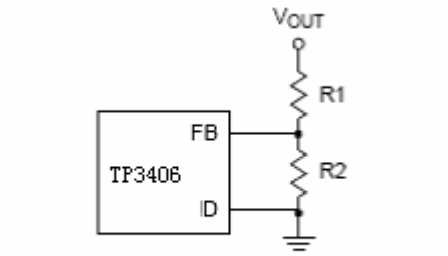


Figure 4. Setting the Output Voltage

For adjustable about voltage mode, the output voltage is set by an external resistive divider according to the following equation : $V_{OUT} = V_{REF}(1+\frac{R1}{R2})$

where VREF is the internal reference voltage (0.6V typ.)

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as :

Efficiency = 100% – (L1+ L2+ L3+ ...)

where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses : VIN quiescent current and I2R losses. The VIN quiescent current loss dominates the efficiency loss at very low load currents whereas the I2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents

can be misleading since theactual power lost is of no consequence.
1. The VIN quiescent current is due to two components : the DC bias current as given in the elect -rical characteristics and the internal main switch and synchronous switch gate charge current -s. The gate charge current results from switching the gate capacitance of the internal power MOSFE -T switches. Each time the gate is switched from high to low to high again, a packet of charge ΔQ movesfrom VIN to ground.
The resulting ΔQ/Δt is the current out of VIN that is typically larger than the DC bias current. In cont -inuous mode,
IGATECHG = f(QT+QB)
where QT and QB are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to VIN and thus their effects will be more pronounced at higher supply voltages.
2. I2R losses are calculated from the resistances of the internal switches, RSW and externalinductor RL. In continuous mode the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the LX pin is a function of both top and bottomMOSFET RDS(ON) and the duty cycle (DC) as follows :
RSW = RDS(ON)TOP x DC + RDS(ON)BOT x (1−DC)
The RDS(ON) for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I2R losses, simply add RSW to RL and multiply the result by the square of the average outputcurrent.
Other losses including CIN and COUT ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

Thermal Considerations

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maxi -mum power dissipation can be calculated by following formula :
PD(MAX) = (TJ(MAX) - TA) / θJA
Where TJ(MAX) is the maximum operation junction temperature 125°C, TA is the ambient tempera -ture and theθJA is the junction to ambient thermal resistance.
For recommended operating conditions specification of TP3406 DC/DC converter, where TJ (MAX) is the maximum junction temperature of the die (125°C) and TA is the maximum ambient tempera -ture. The junction to ambient thermal resistance θJA is layout dependent. For SOT-23-5/TSOT-23 -5 packages, the thermal resistance θJA is 250°C/W on the standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at TA = 25°C can be calculated by following formula :
PD(MAX) = (125°C - 25°C) / 250 = 0.4 W for SOT-23-5/TSOT-23-5 packages
The maximum power dissipation depends on operating ambient temperature for fixed TJ(MAX) and thermal resistance θJA. For RT8008 packages, the Figure 5 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.
The value of junction to case thermal resistance θJC is popular for users. This

thermal parameter is convenient for users to estimate the internal junction operated temperature of packages while IC operating. It's independent of PCB layout, the surroundings airflow effects and temperature differe -nce between junction to ambient. The operated junction temperature can be calculated by following formula :

TJ = TC + PD x θJC

Where TC is the package case (Pin 2 of package leads) temperature measured by thermal sensor, PD is the power dissipation defined by user's function and the θJC is the junction to case thermal resistance provided by IC manufacturer. Therefore it's easy to estimate the junction temperature by any condition.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, VOUT immediately shifts by an amount equal to ΔILOAD (ESR), where ESR is the effective series resistan -ce of COUT. ΔILOAD also begins to charge or discharge COUT generating a feedback error signal used by the regulator to return VOUT to its steady-state value. During this recovery time, VOUT can be monitored for overshoot or ringing that would indicate a stability problem.

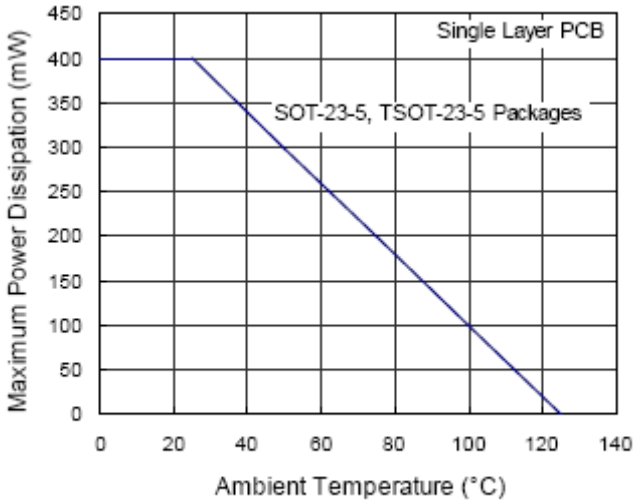
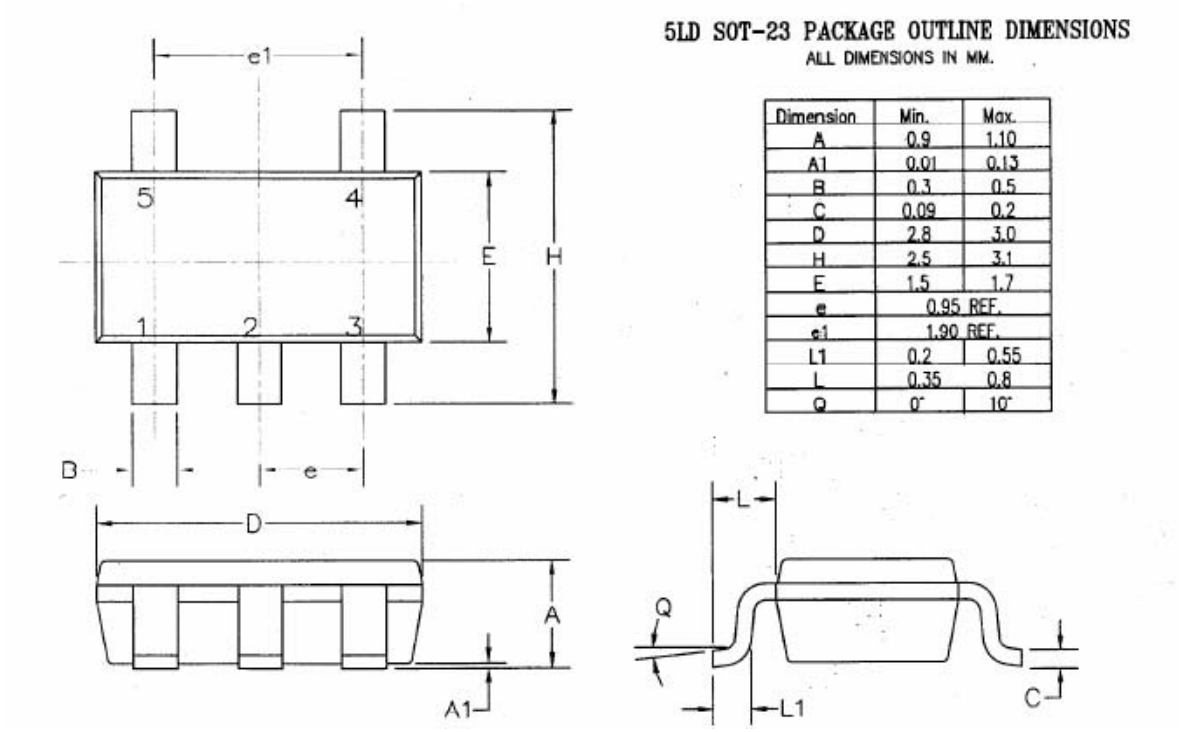


Figure 5. Derating Curves for RT8008 Package

Package Description



Note: Package outline exclusive of mold flash and metal burr.