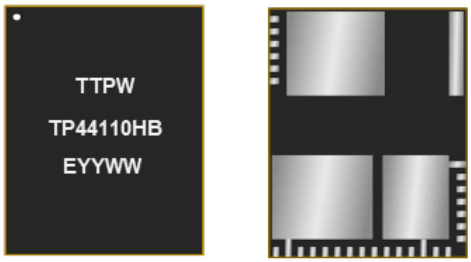
TP44110HB – 650 V GaN Half-Bridge, 90 mΩ (LS) and 90 mΩ (HS)

1.0 Features

- 650 V enhancement mode power HEMTs
- R_{DSON}: 90 mΩ (Low-side) and 90 mΩ (High-side)
- I_{DS}: 19 A (max) / $I_{DSpulse}$: 30 A (max)
- Adjustable turn-on/off speed
- Reverse conduction capability
- Zero reverse-recovery loss
- High switching frequency capability
- Interfaces with 6 V and ≥12 V drivers (see Application Information)
- Low-side thermal-pad LV-isolated from the source for better thermal connection even with current-sense resistors



(Top View) (Bottom View)

Figure 1 Device Image
(30 pin 8×10×0.8 mm QFN Package)

2.0 Topologies and Applications

- Ac-dc, dc-dc, dc-ac converters
- Totem-pole and bi-directional PFCs
- Half- and full-bridge LLC converters
- High-frequency electronic transformers
- Mobile chargers and laptop adapters
- EV chargers and power tools
- LED and motor drives
- Server power supplies

RoHS/REACH/Halogen Free Compliance

3.0 Description

The TP44110HB is a half-bridge IC consisting of two 650 V GaN HEMT power devices. The low-side (LS) and the high-side (HS) devices are of 90 mΩ each. This co-packaged solution minimizes inductance in the power loop enabling clean switching even at high-current high-frequency operations. As provided in the application information, simple external interface circuits can be used to drive this part both from dedicated 6 V GaN drivers as well as more traditional 12 V drivers. Resistors in the individual gate path can be used to control the switching speeds of the low-side/high-side for the best EMI performance. The solution is well suited for all half-bridge applications with a view towards high performance and compact solution.

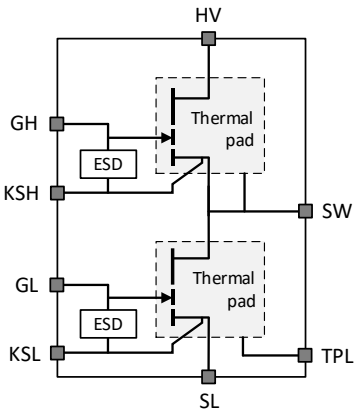


Figure 2 Functional Block Diagram

4.0 Ordering Information

Table 1 Ordering Information

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TP44110HB	30 Pin 8×10×0.8 mm QFN	Tape and Reel	1000	13” (330 mm)	18 mm	TP44110HBTRPBF

5.0 Pin Definition

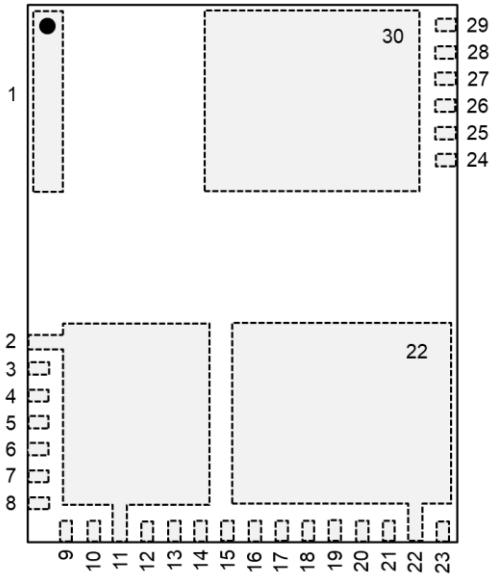


Figure 3 Pin Location
(Package Top View)

Table 2 Pin Definition

Pin Number	Pin Name	Pin Type	Description
1	HV	PWR	Drain of the high-side HEMT.
2, 11	PADL	NC	No connect. These may be connected to TPL (Pin-22) for better PCB layout.
3–10, 12, 13, 23	NCL	NC	
14	GL	AI	Gate of the low-side.
15	KSL	AI	Kelvin-source of the low-side.
16–21	SL	PWR	Source of the low-side.
22	TPL	Thermal	Exposed thermal pad of the low-side. Must have good thermal path to the PCB thermal plane. Also, voltage difference between this pin and SL (Pin-16 to 21) shall be limited within ±20 V. See the section on Application Information for more details.
24	GH	AI	Gate of the high-side.
25	KSH	AI	Kelvin-source of the high-side.
26–29	NCH	NC	No connect. These may be connected to SW (Pin-30) for better PCB layout.
30	SW	PWR	Half-bridge switching-node. Also exposed thermal pad of the high-side. Must connect to sufficient area of thermal plane either directly or through multiple thermal vias for effective cooling. See the section on Application Information for more details.

Abbreviations: NC = not connected; AI = analog input; PWR = power

6.0 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings [1] @T_J = +25 °C, unless otherwise specified.

The low-side and the high-side power devices are the same, and each of the parameter values, including electrical and thermal is for one of the individual devices, except if mentioned otherwise.

Parameter	Symbol	Value	Unit
Electrical Ratings			
Drain to source voltage of GaN power HEMT	V_{DS}	650	V
Transient drain to source voltage [2]	V_{TDS}	750	V
Continuous drain current (at Tc = 25 °C)	I_{DS}	19	A
Continuous drain current (at Tc = 100 °C)	I_{DS}	12	A
Pulsed drain current (at T_J = 25 °C) [3]	$I_{DSpulse}$	30	A
Drain to source voltage slew-rate	$(dv/dt)_{DS}$	200	V/ns
Input gate voltage with respect to the respective Kelvin-source	V_{GS}	-0.5 to +6.5	V
Transient input gate voltage with respect to the respective Kelvin-source	$V_{GS(Transient)}$	+9.0	V
Voltage difference of TPL pad to SL Pin	$\Delta V_{TPL\text{-}Source}$	±20	V
Storage temperature range	T_{st}	−55 to +150	°C
Operating temperature range	T_{op}	−55 to +150	°C
Maximum junction temperature	T_J	+150	°C
Thermal Ratings			
Thermal resistance (junction-to-case) – bottom side [4]	$R_{\theta JC}$	1.2	°C/W
Thermal resistance (junction-to-ambient) [4]	$R_{\theta JA}$	40	°C/W
Soldering temperature	T_{SOLD}	260	°C
ESD Ratings			
Human body model (HBM) per JS-001-2017	Level 2	>3000	V
Charged device model (CDM) per JS-002-2014	Level C3	≥1000	V
Moisture Rating			
Moisture sensitivity level (per J-STD-020D.1)	MSL	1	-

Note:

[1] These are stress ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to the surrounding circuit.

[2] For duration < 1ms, provided to indicate robustness and not recommended for normal operation.

[3] For duration < 10us, followed by sufficient time for the device to cool off.

[4] As measured on DUT soldered on 2 oz Cu (FR4) PCB of size 1 square inch.

7.0 Recommended Operating Conditions

Table 4 Recommended Operating Conditions [1] @T_J = +25 °C, unless otherwise specified.

Parameter	Symbol	Min	Nominal	Max	Unit
Input gate to Kelvin-source voltage	V_{GS}	0		6.0	V
Pull-up resistor — with 12V drive [2]	R_U	15			Ω
Pull-up resistor — with 6V drive [2]		5			Ω
Operating case temperature	T_C	-40		+125	°C

Note:

[1] Operating for extended periods of time at conditions beyond the recommended range might affect device reliability.

[2] The recommended value of this resistor depends on the drive type and the interface circuit. See the section on Application Information for more details.

8.0 Electrical Specifications

Table 5 Electrical Specifications [1] @T_J= + 25°C, unless otherwise specified.

Parameter	Description	Condition	Minimum	Typical	Maximum	Unit
Static Characteristics						
R_{DSON}	Drain to source resistance	I_{DS} = 0.5 A DC, V_{GS} = 6 V, T_J = +25 °C		90	118	mΩ
		I_{DS} = 0.5 A DC, V_{GS} = 6 V, T_J = +150 °C		220		
I_{DSS}	Drain to source leakage current	V_{DS}= 650 V, V_{GS} = 0 V, T_J = +25 °C		0.4		µA
		V_{DS} = 650 V, V_{GS} = 0 V, T_J = +150 °C		60.0		
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_{DS} = 11 mA		1.7	2.5	V
I_{GS}	Gate to source current	V_{DS} = 0 V, V_{GS} = 6 V		25		µA
Dynamic Characteristics						
C_{ISS}	Input capacitance	V_{DS} = 400 V, V_{GS} = 0 V, Freq = 100 kHz		110		pF
C_{RSS}	Reverse transfer capacitance			0.65		pF
C_{OSS}	Output capacitance			35		pF
$C_{O(ER)}$ [2]	Effective output capacitance – energy related	V_{DS} = 0 to 400 V, V_{GS} = 0 V		53		pF
$C_{O(TR)}$ [3]	Effective output capacitance – time related	V_{DS} = 0 to 400 V, V_{GS} = 0 V		80		pF
Q_{OSS}	Output charge	V_{DS} = 400 V, V_{GS} = 0 V		32		nC

E_{OSS}	Output capacitance stored energy	V_{DS} = 400 V, V_{GS} = 0 V, Freq = 100 kHz		4.8		µJ
Gate Characteristics						
Q_G	Gate charge – total	V_{DS} = 400 V V_{GS} = 0 to 6 V		3.0		nC
Q_{GS}	Gate to source charge			0.5		nC
Q_{GD}	Gate to drain charge			1.5		nC
V_{GPLAT}	Gate plateau voltage	V_{DS} = 400 V I_{DS} = 7.5 A		2.5		V
Reverse Conduction Characteristics						
Q_{RR} [4]	Reverse recovery charge			0		nC
t_{RR}	Reverse recovery time			0		ns
V_{SD}	Reverse conduction voltage	I_{SD} = 4 A, V_{GS} = 0 V		2.5		V
		I_{SD} = 12 A, V_{GS} = 0 V		4.0		
Switching Time (Refer to Figure 4 and Figure 5)						
t_r	Rise time	V_{DS} = 400 V, I_{DS} = 8 A, R_U = 5 Ω, R_D = 5 Ω		9		ns
t_f	Fall time			4		ns
$t_{prop-on}$	Turn-on propagation delay			8		ns
$t_{prop-off}$	Turn-off propagation delay			15		ns

Note:

[1] All V_{GS} refer to the gate-to-source voltage of the respective power device. Note that the source and the Kelvin-source terminals are internally connected for each device.

[2] $C_{O(ER)}$ is an equivalent (fixed) capacitance that gives the same energy as C_{OSS} while V_{DS} rises from zero volt to the stated V_{DS}.

[3] $C_{O(TR)}$ is an equivalent (fixed) capacitance that gives the charging time as C_{OSS} while V_{DS} rises from zero volt to the stated V_{DS}.

[4] Q_{RR} computation excludes Q_{OSS}.

9.0 About Gate Drive Requirements of GaN Power HEMT

9.1 Gate Drive Voltage Level, Slew-rate Control

The GaN HEMT has a recommended gate drive high voltage of +6 V, and hence the gate should operate between 0 to 6 V. A lower than optimum on-state gate drive high voltage, say 5.5 V or 5 V will result into a slightly higher R_{DSON}. Before settling to a 6 V on-state voltage, if the gate voltage has some transient ringing (say, within 0.5 V), then the device can tolerate this without much adverse effect to the gate reliability. However, excessive ringing shall be avoided by minimizing the inductance of the gate drive loop. For a high-performance gate drive, the pull-up path and the pull-down path shall be kept separate,

where the pull-up path resistor can be selected for controlling the turn-on slew-rate. This is similar to what is used for a common silicon power MOSFET. Recommended gate drive interface circuits both with 6 V and 12 V drivers are shown in the section Application Information.

9.2 Immunity Against Parasitic Turn-on, and Use of Negative Gate Drive

Switching produces dv/dt at the switch node, which in the case of GaN can be large. Apart from EMI issues, these large dv/dt may also lead to what is known as parasitic turn-on or Miller turn-on. The way this happens is that when one of the devices in H-bridge configuration turns-on under hard-switching, the drain-source voltage across the other device undergoes a rapid rise. This positive dv/dt on the drain of the other device (with respect to the gate/source) tries to turn it on through the parasitic gate-to-drain capacitance $C_{GD.}$ This parasitic turn-on is highly undesirable as it can cause catastrophic amount of shoot-through or crowbar current. An effective way to avoid such turn-on is to use low (or zero) pull-down resistance and to keep the inductance of the turn-off path low.

One way to avoid parasitic turn-on in GaN HEMT devices is to use a negative-swing gate-drive where under the off condition, the gate drive voltage is a negative voltage in the range of −2 V to −4 V. However, such a drive is more complex to implement and also causes higher losses under reverse conduction. The suggested way to avoid parasitic turn-on for Tagore's TP44110HB devices is to minimize the resistance and the loop inductance of the turn-off path. A good approach to minimize the turn-off resistance is to use a driver with a separate (and strong) turn-off path and use no external resistance in this path.

9.3 Thermal Pad Connection

In TP44110HB, there are two exposed thermal pads, both of which are available at the bottom side. The pad named TPL (Pin-22) is for the low-side device, and the pad named SW (Pin-30) is for the high-side device. For a desirable level of thermal performance, each of these pads need to be connected to a suitable heat-sink arrangement, or to (their own) large enough PCB islands. The connections can be either direct or through thermal vias with a pattern as shown in Figure 21. For the low-side device, it shall be noted that the thermal pad is connected to the device's substrate whereas the source connection of the device is brought out separately on Pins 16−21. This allows for insertion of current sense resistor at the low-side source without cutting the thermal path. However, care shall be exercised that the voltage difference between the TPL pad and Pins 16−21 shall not exceed ±20 V. For the high-side device, the pin SW is already connected both to the device's substrate and the source, and hence no special care is needed.

9.4 Kelvin Source for Gate Drive Loop

TP44110HB has separate Kelvin-source pins available for both the low-side and the high-side devices. These pins shall be used in the respective driver return paths for the best de-coupling of the gate-loops from the power-loops.

9.5 Parallel Operation for Higher Current

The device has a maximum current rating as given in Table 3. Higher current operation is possible if two or more TP44110HB devices are connected in parallel. For parallel operation, there are two main challenges. (1) One is the possibility of parasitic divergent oscillations between the parallel devices leading to permanent failure of devices. Such oscillations can happen in any type of two parallel power devices, but due to the extra-high speed of GaN devices, more care is needed. A major part of fixing such oscillations is to use individual gate resistors for each of the parallel devices (as opposed to using a single common resistor). Further, each individual Kelvin-source shall have a series resistor. (2) The other challenge of paralleling power devices is the imbalance of currents between the devices during the operation. Fortunately, GaN devices have a R_{DSON} which has a positive temperature co-efficient. Therefore, between parallel devices, any imbalance in current is limited due to the negative feedback arising from this behavior. To aid dynamic balancing of current, it is highly recommended to make the layout as symmetric as possible. The individual series resistor of Kelvin-source further aids with this balancing. Finally, as with any arrangement of parallel devices, some derating shall be allowed.

10.0 Switching Time Measurement Information

The switching time parameters are measured using the test circuit shown in Figure 4. Here a TP44110HB device is configured in the well-known arrangement of double-pulse-test (DPT). The pin SW is connected to a 400 V DC bus supply through an inductor. The low-side power device is used as a controlled device, whereas the high-side power device is used in a freewheeling/clamp-diode mode (i.e., its gate GH is shorted to its Kelvin-source terminal KSH). The two resistors R_U and R_D as shown in the figure are used for controlling the switching speed.

When the gate pin GL of the low-side of TP44110HB is supplied with a 6V signal, the low-side HEMT device turns on and the switch-node SW goes down to a low voltage as shown in Figure 5. During this time, the inductor current starts to increase. When the gate signal at GL is made low, the low-side HEMT device turns off, and hence, the switch-node SW starts to increase with a slew rate which depends on the inductor current and the switch-node capacitance. Once the switch-node reaches the DC bus and crosses it by about $V_{GS(th)}$, the high-side of TP44110HB turns on. Then, the switch-node voltage gets clamped to the DC bus voltage and remains so till the inductor current reaches zero.

The various switching including propagation delays are defined in Figure 5.

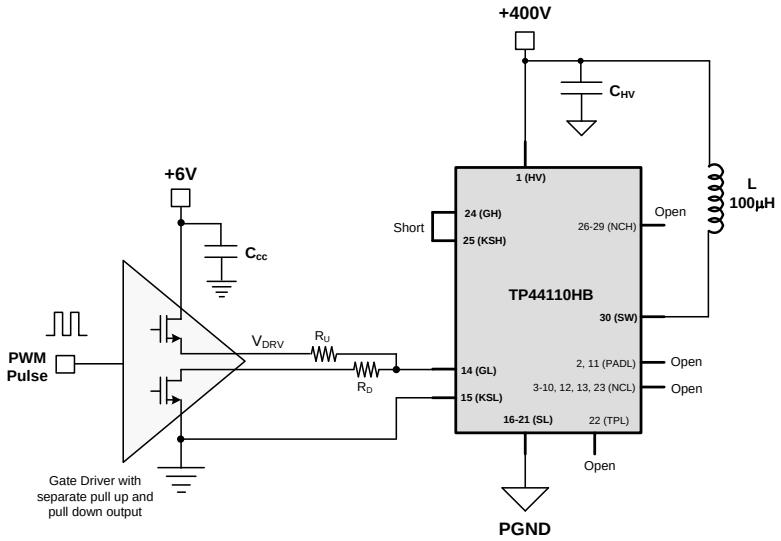


Figure 4 Switching Time Measurement Circuit

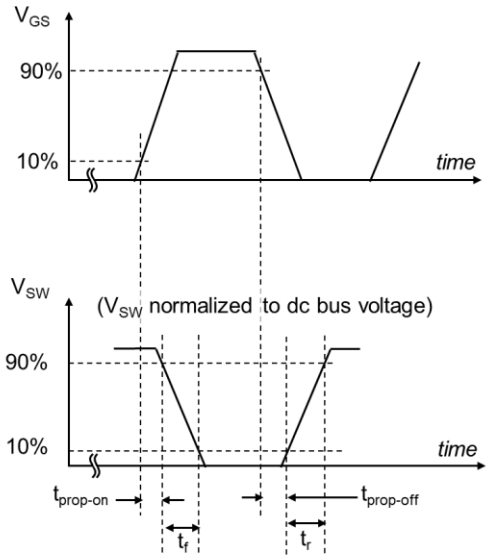


Figure 5 Switching Time Waveform and Definition of Parameters

11.0 Typical Characteristics

Conditions: @T_J = +25 °C unless otherwise specified. Plots show behavior of a single device.

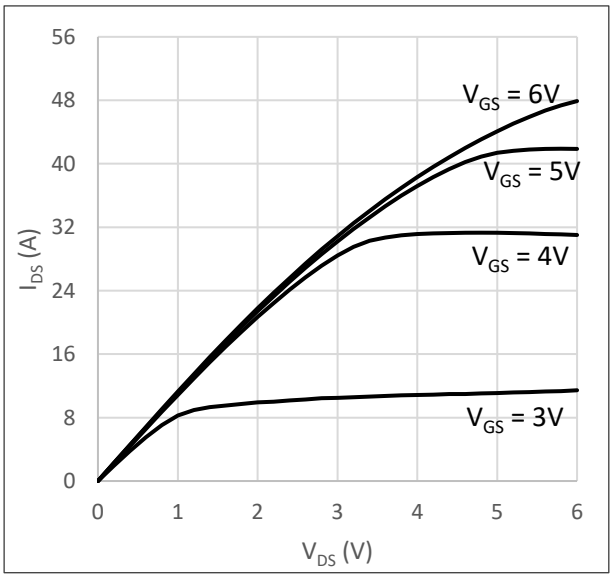


Figure 6 Forward Conduction of GaN HEMT $I_{DS} = f(V_{DS}, V_{GS})$

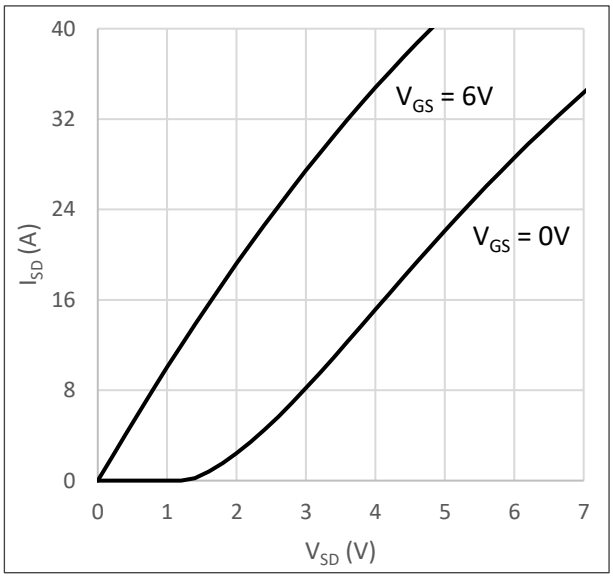


Figure 7 Reverse Conduction of GaN HEMT $I_{SD} = f(V_{SD}, V_{GS})$

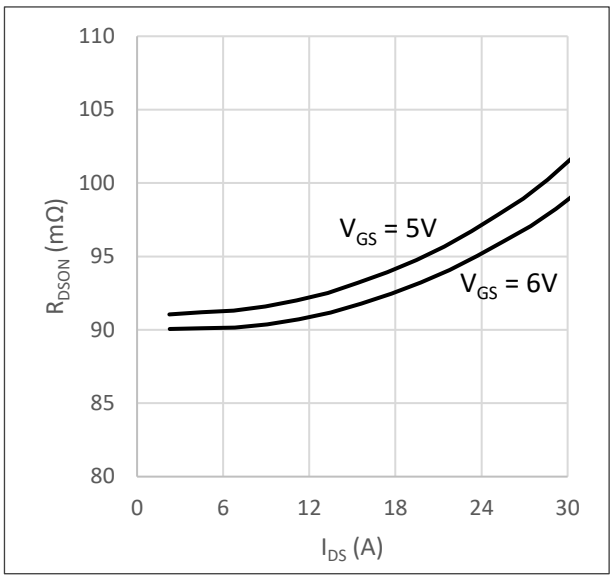


Figure 8 On-state Resistance of GaN HEMT $R_{DSON} = f(I_{DS}, V_{GS})$

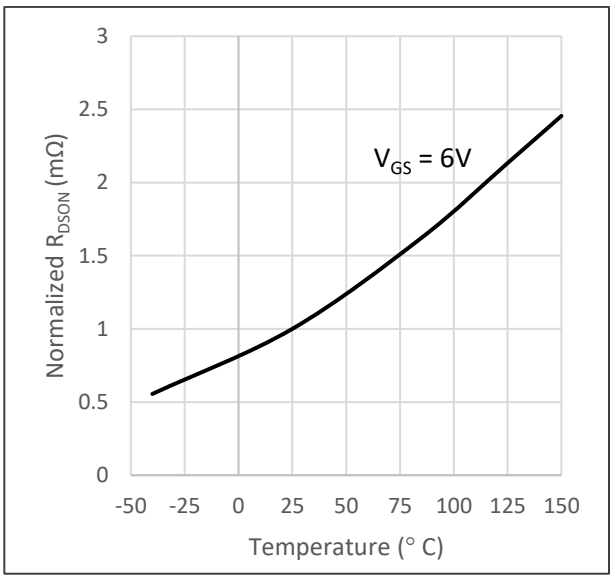


Figure 9 Normalized R_{DSON} vs. Junction Temperature at I_{DS} = 1 A

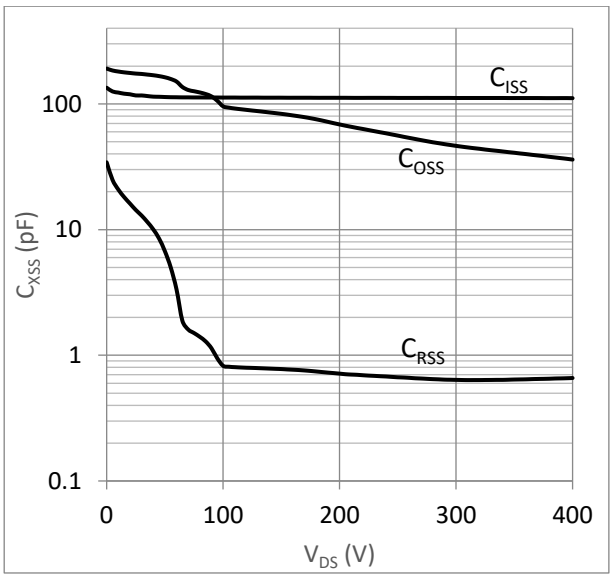


Figure 10 C_{XSS} vs. V_{DS}

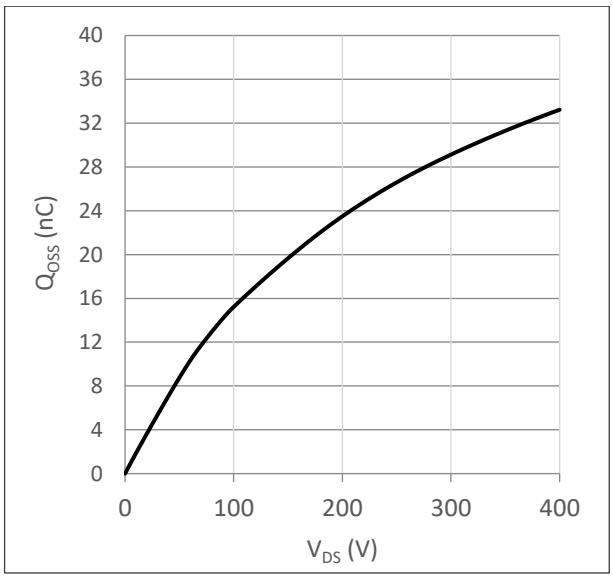


Figure 11 Q_{OSS} vs. V_{DS}

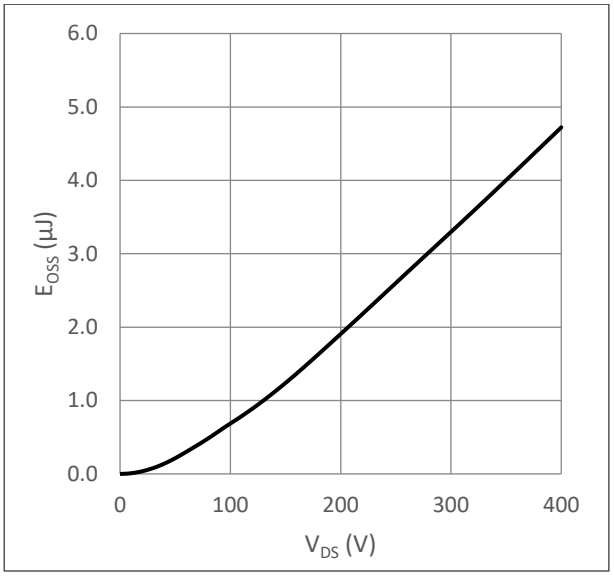


Figure 12 E_{OSS} vs. V_{DS}

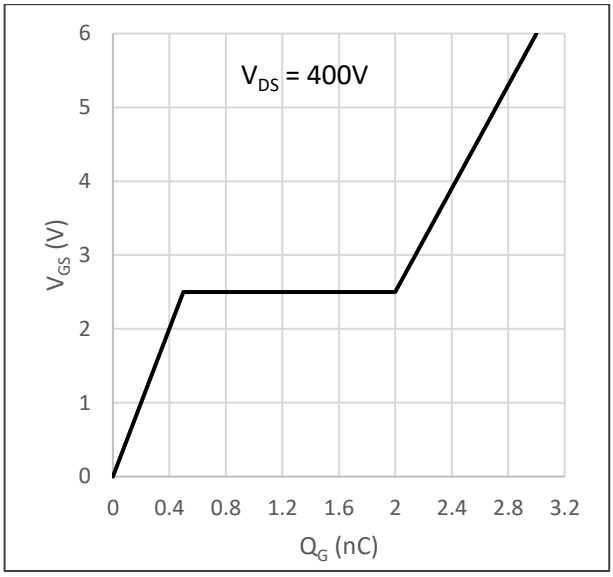


Figure 13 V_{GS} vs. Q_G

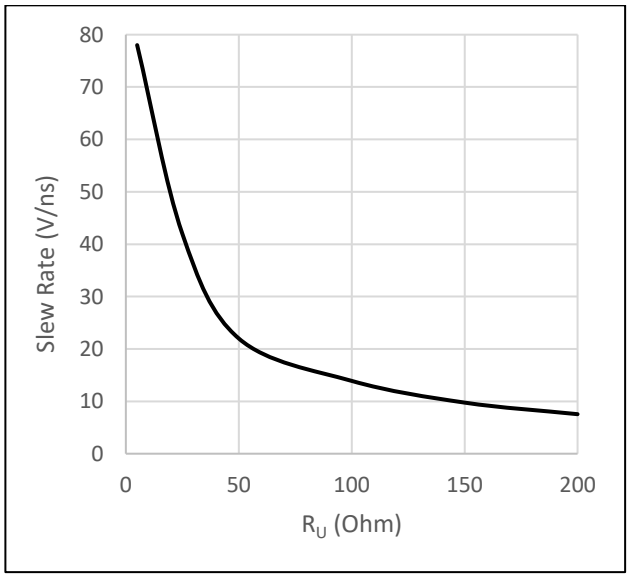


Figure 14 Drain Slew-Rate Variation vs. R_U Resistor at Turn-On Transition [1]

Note:

[1] The measurement setup is as per Figure 4 and Figure 5. The slew-rate corresponds to the region where SW drops from 90% to 10% of the bus voltage during its falling edge transition, and the value of I_{DS} at the transition is 8 A.

12.0 Application Information

12.1 Interface for 6 V Drive

A TP44110HB device can be directly driven with a 6 V driver. However, typically, one needs to control turn-on/off speeds, for which resistors are used. For the common case of a driver with a single output (i.e., no dedicated pull-up and pull-down paths), the interface circuit is shown in the left-side diagram in Figure 15. The resistor R_U provides the path for turn-on, and its value can be selected for a desirable slew-rate. The turn-off path consists of R_U in parallel with a (Schottky + R_D) combination. The job of the Schottky diode is to ensure that R_D only conducts during the turn off. Typically, a low value of R_D is preferred in order to avoid Miller turn-on as explained in Section 9.1. For the highest turn-off speed, the resistor R_D may be replaced by a short.

Some drivers have separate pull-up and pull-down paths. In such cases, no Schottky diode is needed, and the interface circuit simplifies to what was shown in Figure 4.

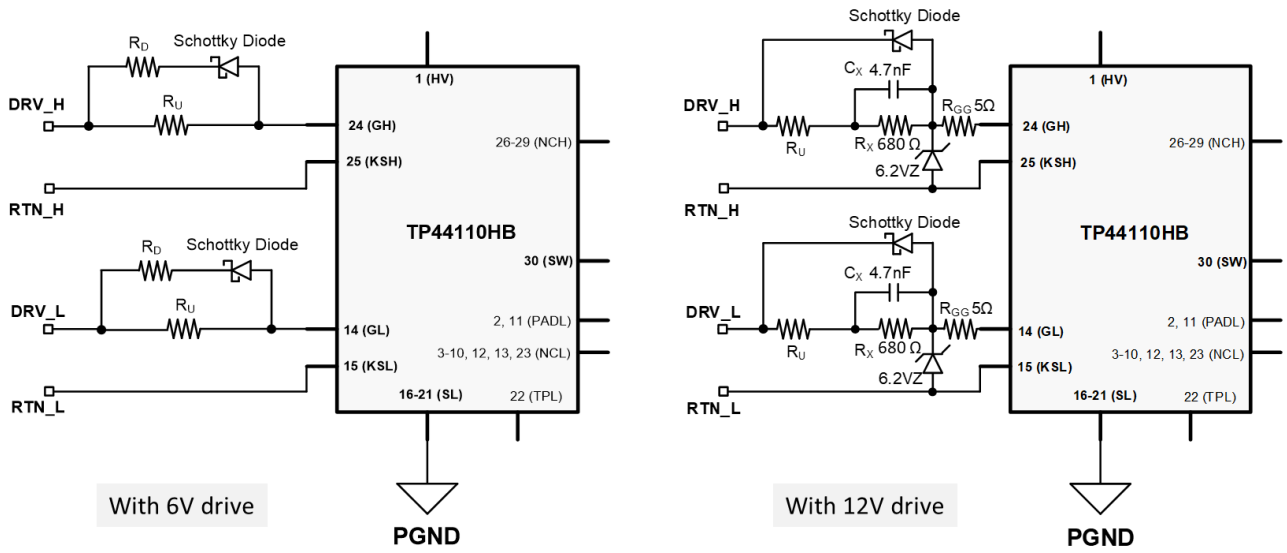


Figure 15 Gate Drive Interface (Left) for 6 V Drive, (Right) for ≥12 V Drive

12.2 Interface for ≥12 V Drive

When using a higher than 6 V drive (say a standard 12 V or higher), one can use an interface circuit shown in the right-side diagram in Figure 15. Zener diodes of 6.2 V serve the purpose of limiting the voltage between the gates and the Kelvin sources of both of the low-side or the high-side devices. The 5 Ω resistors R_{GG} connected to pins GL/GH are to avoid parasitic oscillation between the GaN device and the Zener diodes. For ZVS operation, these R_{GG} resistors are optional and may be removed by shorting. The resistors R_U, once again, are for setting the turn-on speed. In this diagram, for the maximum turn-off speed, R_D has been removed by shorting. The Schottky diodes remain to provide the fast turn-off path. Finally, within the resistor-capacitor pair R_X-C_X, the resistor limits the Zener current during gate high periods. And the purpose of the capacitor C_X is to bypass R_X during transients so that the turn-on/off speed are not affected by R_X. This interface circuit can be used for other drive voltages which are higher than 6 V e.g., 9 V, 12V, 15 V etc. The value of R_X needs to be adjusted accordingly.

12.3 Example Application: AC-DC Power Conversion

This section presents the application of TP44110HB in ac-dc power conversion using a PFC followed by an LLC topology as shown in Figure 16. The combo-controller IC TEA2016AAT drives both the PFC and the LLC devices. The half-bridge LLC resonant converter needs two switching devices, for which this half-bridge GaN IC TP44110HB is used. Compared to a two discrete power devices solution, the single half-bridge IC significantly simplifies the PCB layout complexities, occupies less PCB foot-print area, reduces BOM part count and enables higher switching-frequency operation.

In the PFC section, Tagore's GaN HEMT TP44100SG can be used as the main switching device.

The combo-controller IC TEA2016AAT outputs +12V/0V gate drive pulses for both the high- and low-side devices. The GaN half-bridge IC and the stand-alone GaN IC, however, need +6V/0V gate drive. To meet this requirement, the interface circuit of Section 12.2 has been used as shown in Figure 16. The turn-on speed of the GaN devices can be easily controlled through the resistor R_U.

The secondary side of the LLC resonant converter is shown to have diode rectifiers D1 and D2. If desired, these diodes can be replaced with synchronous rectification FETs to achieve higher efficiency and better thermal performance.

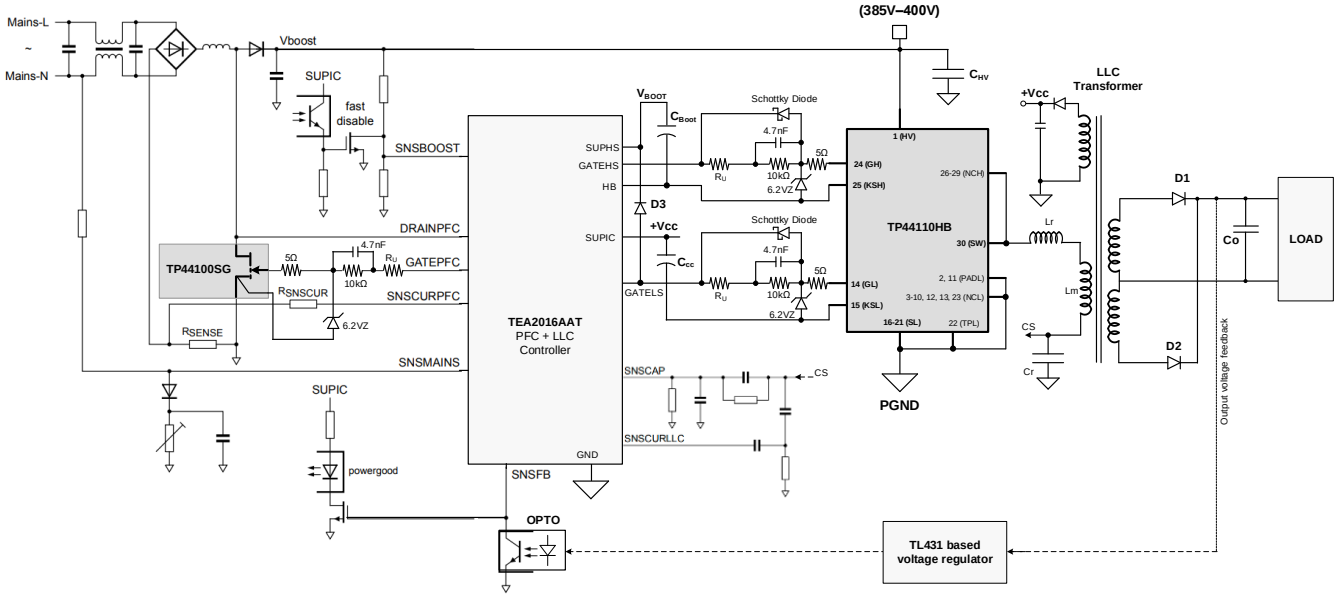
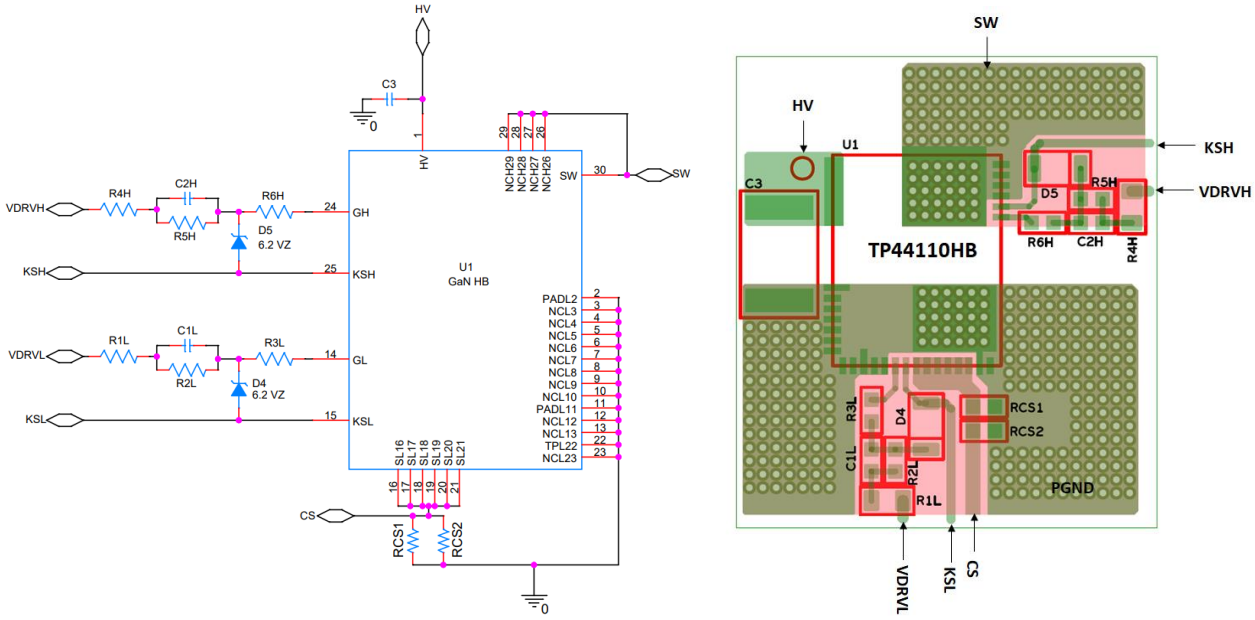


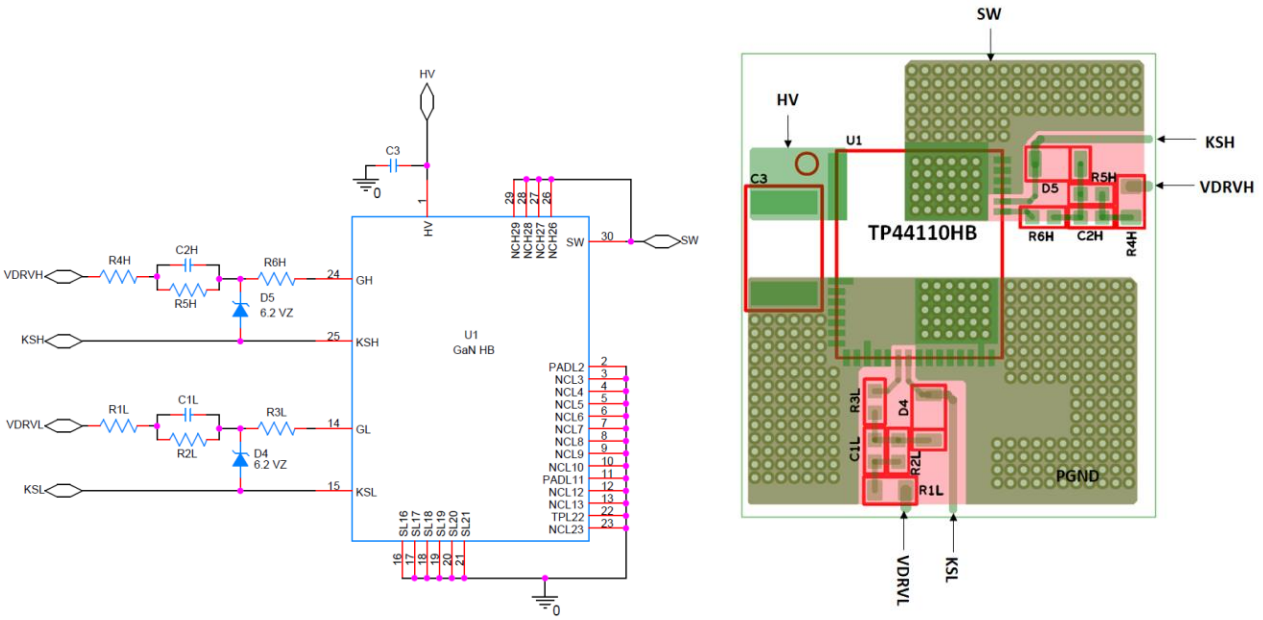
Figure 16 AC-DC Power Converter Using a TP44110HB Part

12.4 PCB Layout with and without Current-Sense Resistor

In a half-bridge, it is quite common to use a current sense resistor at the source side of the low-side device. Such as arrangement is shown in the top left drawing in Figure 17. While doing the layout for such cases, the thermal pad TPL (Pin-22) shall be connected to a large enough area on the PCB (the thermal plane) for heat dissipation. Usually, power-ground (PGND) is the largest copper area available, and the recommended layout is shown in the top right drawing in Figure 17 where PGND acts as the thermal plane. Note that with Tagore's TP44110HB parts, even with the sense resistors between the source pins and the thermal plane, the thermal performance of the low-side device is minimally affected. For the case when no sense resistors are used, one could short all the source pins with TPL (Pin-22) and use a layout as shown in the bottom right drawing in Figure 17.



(a) With current-sense resistors. IC sits on the green layer of PCB.



(b) Without current-sense resistors. IC sits on the green layer of PCB.

Figure 17 Layout Guidelines for (a) With the Current-Sense Resistors, and (b) Without the Current-Sense Resistors

13.0 Device Package Information

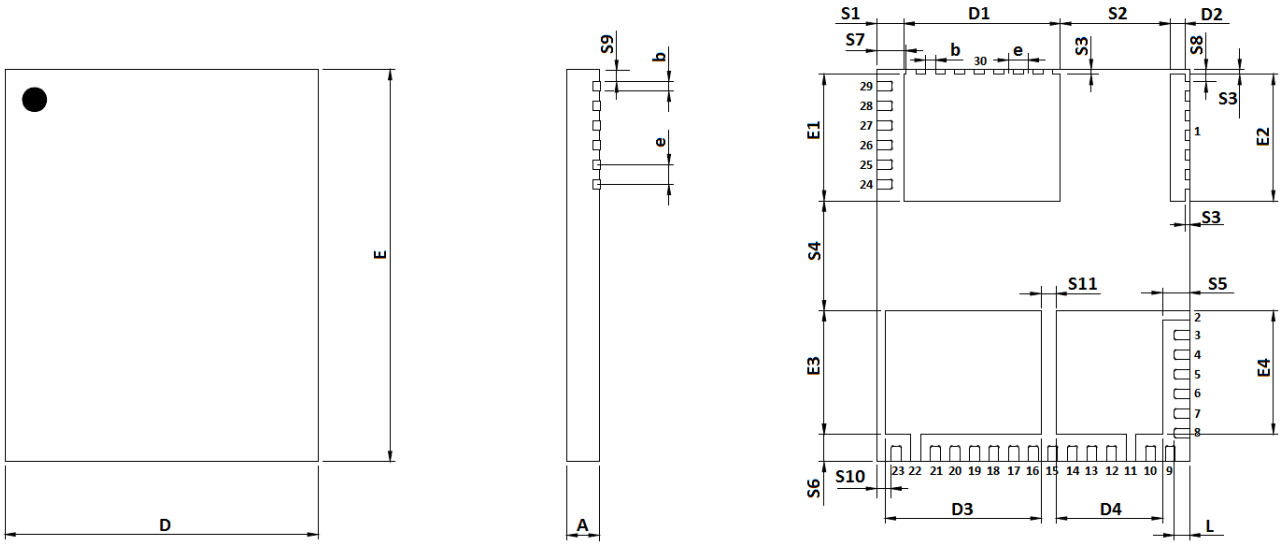


Figure 18 Device Package Drawing
(All dimensions are in mm)

Table 6 Device Package Dimensions

Dimension	**Value** (mm)	**Tolerance** (mm)	**Dimension**	**Value** (mm)	**Tolerance** (mm)
A	0.80	±0.05	L	0.40	±0.05
b	0.25	+0.05/-0.07	S1	0.70	±0.05
D	8.00 BSC	±0.05	S2	2.80	±0.05
D1	4.00	±0.05	S3	0.12	±0.05
D2	0.38	±0.05	S4	2.80	±0.05
D3	3.98	±0.05	S5	0.70	±0.05
D4	2.70	±0.05	S6	0.70	±0.05
e	0.50 BSC	±0.05	S7	0.75	±0.05
E	10.00 BSC	±0.05	S8	0.30	±0.05
E1	3.23	±0.05	S9	0.30	±0.05
E2	3.23	±0.05	S10	0.375	±0.05
E3	3.15	±0.05	S11	0.40	±0.05
E4	3.15	±0.05	-	-	-

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5 μm ~ 20 μm (Typical 10 μm ~ 12 μm)

Attention:
Please refer to application notes *TN-001* and *TN-002* at http://www.tagoretech.com for PCB and soldering related guidelines.

14.0 PCB Land Design

Guidelines:

[1] A 4-layer PCB is recommended.
[2] Via diameter is recommended to be 0.3 mm to prevent solder wicking inside the vias.
[3] Thermal vias shall only be placed on pad A, B, and C.
[4] The maximum via number for pads A, B, and C are 6(X)×5(Y)=30, 6(X)×5(Y)=30 and 4(X)×5(Y)=20, respectively.

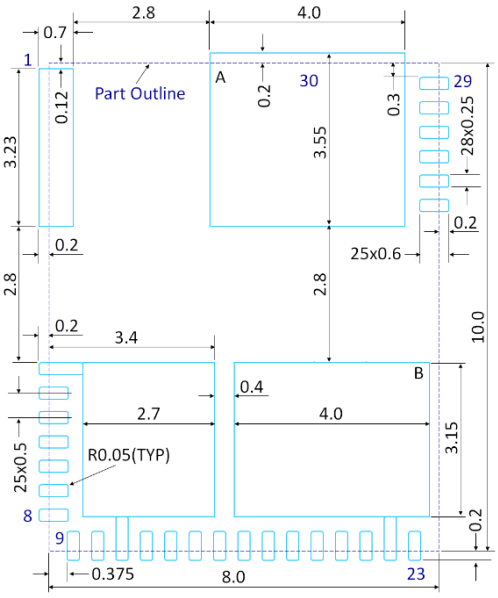
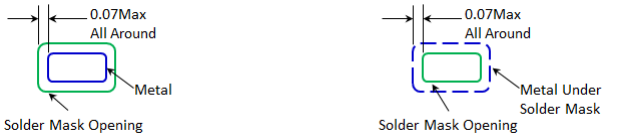


Figure 19 PCB Land Pattern
(Dimensions are in mm)



Non-Solder Mask Defined
(Preferred)

Solder Mask Defined

Figure 20 Solder Mask Pattern
(Dimensions are in mm)

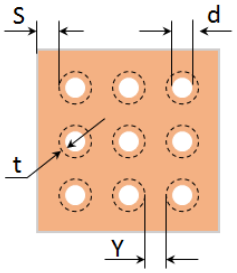


Figure 21 Thermal Via Pattern
(Recommended Values: S ≥ 0.15 mm; Y ≥ 0.20 mm; d = 0.3 mm; Plating Thickness t = 25 µm or 50 µm)

15.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125 μm.

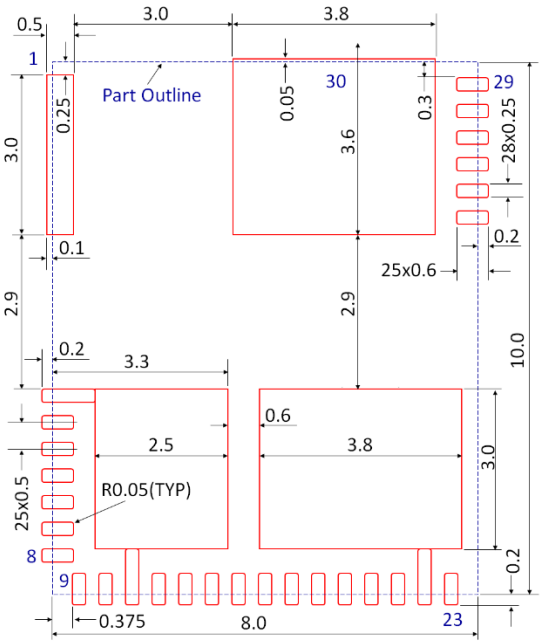


Figure 22 Stencil Openings
(Dimensions are in mm)

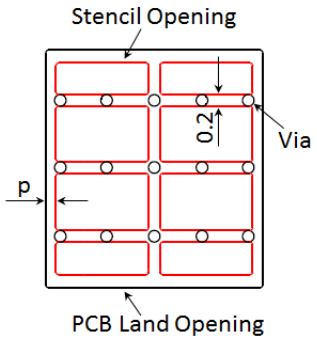


Figure 23 Stencil Openings (Shall Not Cover Via Areas if Possible)
(Dimensions are in mm)

16.0 Tape and Reel Information

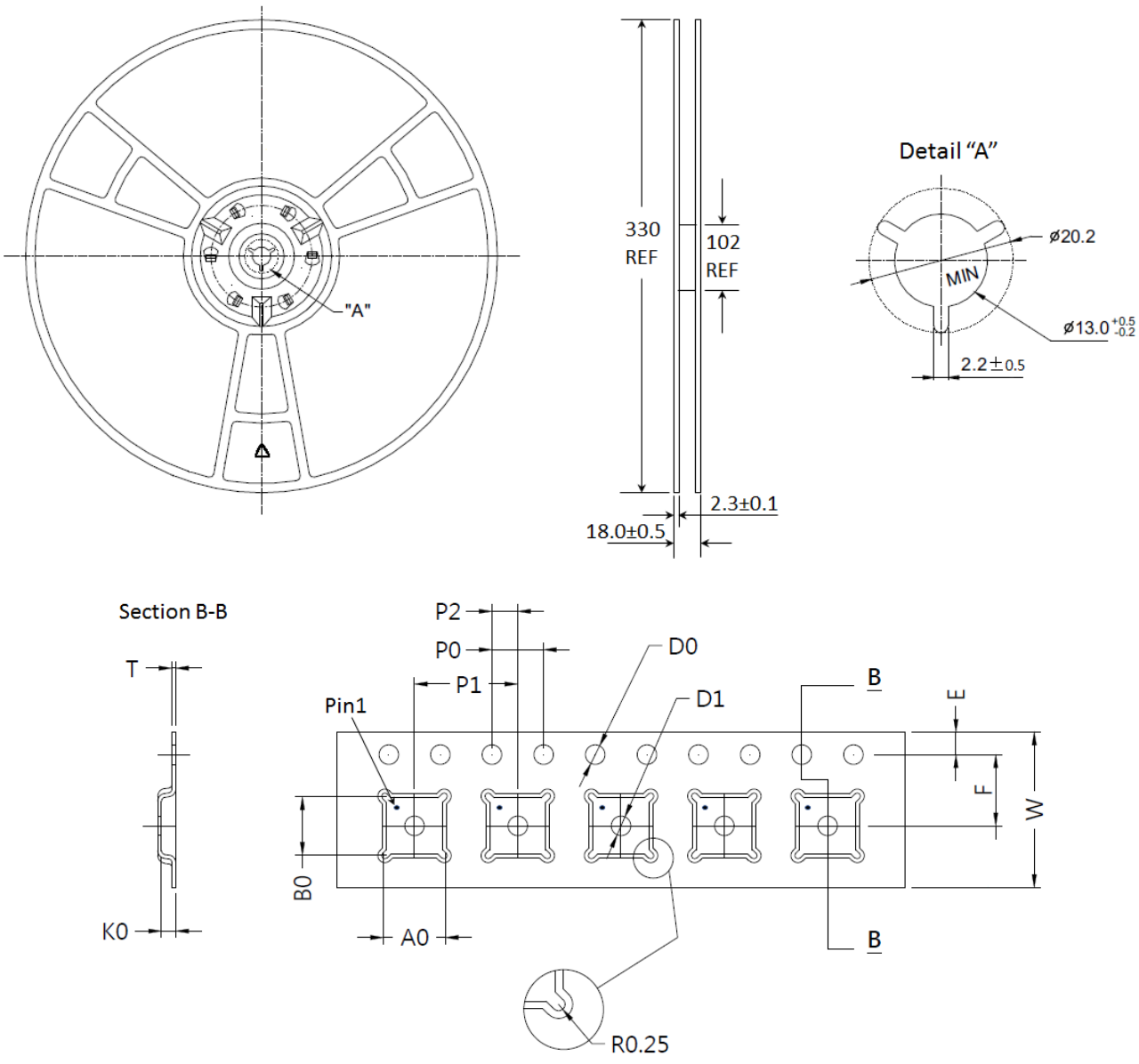


Figure 24 Tape and Reel Drawing

Table 7 Tape and Reel Dimensions

Dimension	**Value** (mm)	**Tolerance** (mm)	**Dimension**	**Value** (mm)	**Tolerance** (mm)
A0	10.35	±0.10	K0	1.10	±0.10
B0	8.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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