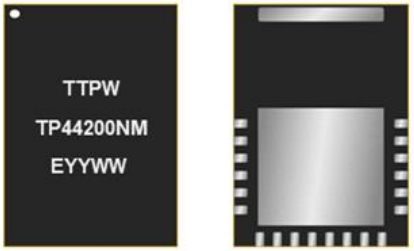
TP44200NM – 180 mΩ, 650 V GaN HEMT with Integrated Driver and Protection

1.0 Features

- 650 V enhancement mode HEMT with integrated driver
- R_{DSON}: 180 mΩ
- I_{DS}: 10 A (max) / $I_{DSpulse}$: 15 A (max)
- 5 V PWM input
- UVLO protection
- Zero reverse recovery
- Low quiescent current driver
- Adjustable turn-on slew rate
- Dv/Dt immunity both with/without driver-supply
- Low propagation delay for up to 2 MHz operation
- Thermal pad (LV) isolated from the source for better thermal connection even with sense resistors



(Top view) (Bottom View)

Figure 1 Device Image
(22pin 5×7×0.85 mm QFN Package)

2.0 Topologies and Applications

- As switching FETs in singles, or in pairs as half-bridges
- AC-DC, DC-DC, DC-AC converters
- PFC applications (totem-pole and standard)
- High frequency LLC converters
- Mobile chargers and laptop adapters
- LED and motor drives
- Server power supplies

RoHS/REACH/Halogen Free Compliance

3.0 Description

The TP44200NM is a 180 mΩ, 650 V GaN HEMT device with integrated driver circuit. The monolithic integration of driver minimizes inductance in the gate loop enabling safe and clean switching even at high-voltage high-frequency operations. This device makes the applications more efficient and reliable, and also helps reduce the size of the magnetic components. UVLO function of the device turns-off the HEMT in case V_{DD} voltage droops below its threshold voltage. A proprietary dv/dt protection circuit protects the HEMT from drain-source dv/dt induced false turn-on even in the absence of V_{DD} supply. An external resistance between V_{reg} and RG allows control of drain voltage slew rate for best EMI performance.

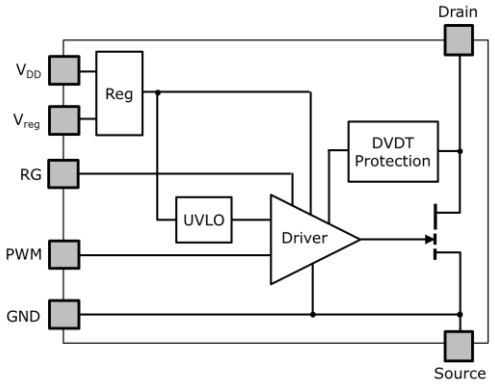


Figure 2 Functional Block Diagram

4.0 Ordering Information

Table 1 Ordering Information

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TP44200NM	22 Pin 5×7×0.8mm QFN	Tape and Reel	1000	13” (330mm)	18mm	TP44200NMTRPBF

5.0 Pin Definition

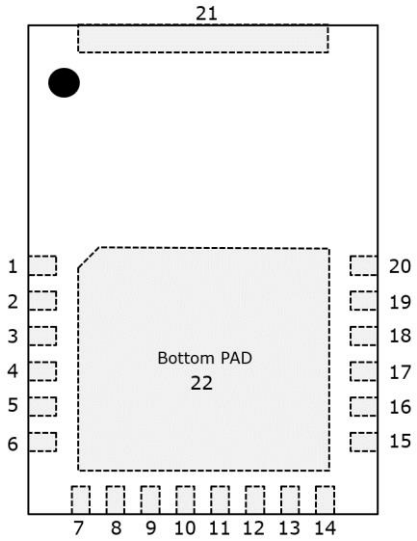


Figure 3 Pin Location
(Package Top View)

Table 2 Pin Definition

Pin Number	Pin Name	Pin Type	Description
1, 7, 14–20	NC		No connect. Pins 14–20 can be connected to TP (Pin-22) for better PCB layout. **Pin 1 and Pin 7 must be left open.**
2	V_{DD}	LV-PWR	V_{DD} supply for the driver. Connect to the driver bias-supply as shown in the section on Application Information. Also, bypass with a capacitor of 100 nF.
3	V_{reg}	AO	Regulated voltage at the driver. Connect to the interface circuit as shown in the section on Application Information. Also, bypass with a capacitor of a minimum value of 10nF.
4	RG	AI	Connect a suitable resistor between RG and V_{reg} for controlling the drain voltage slew rate during the turn on.
5	PWM	DI	PWM input. Optional RC filter may be used.
6	GND	GND	Ground pin of the driver (internally Kelvin connected to the source of the 650 V GaN HEMT). Bypass capacitors of V_{DD}, V_{reg}, and PWM (if any) shall be referenced to this pin.
21	Drain	HV-PWR	Drain of 650 V GaN HEMT
8–13	Source		Source of 650 V GaN HEMT
22 (Back Pad)	TP		Exposed thermal Pad. Must connect to the PCB thermal plane either directly or through multiple thermal vias. See the section on Application Information for more details.

Abbreviations: NC = not connected; LV-PWR = low-voltage power; AO = analog output; AI = analog input; DI = digital input; GND = ground; HV-PWR = high-voltage power

6.0 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings [1] @T_J = +25 °C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Drain to Source Voltage of GaN HEMT	V_{DS}	650	V
Transient Drain to Source Voltage [2]	V_{TDS}	750	V
Continuous Drain Current (at Tc = 25 °C)	I_{DS}	10	A
Continuous Drain Current (at Tc = 100 °C)	I_{DS}	6.5	A
Pulsed Drain Current (at T_J = 25 °C) [3]	$I_{DSpulse}$	15	A
Drain to Source Voltage Slew Rate	$(dv/dt)_{DS}$	200	V/ns
V_{DD} Supply Voltage	V_{DD}	9.0	V
Input PWM Voltage	V_{PWM}	6.5	V
Transient Input PWM Voltage	$V_{PWM(Transient)}$	+9.0	V
Voltage Difference of Thermal-Pad to Source Pin	$\Delta V_{TP\text{-}Source}$	±20	V
Storage Temperature Range	T_{st}	−55 to +150	°C
Operating Temperature Range	T_{op}	−55 to +150	°C
Maximum Junction Temperature	T_J	+150	°C
Thermal Ratings			
Thermal Resistance (junction-to-case) [4] – Bottom side	$R_{\theta JC}$	2.0	°C/W
Thermal Resistance (junction-to-ambient) [4]	$R_{\theta JA}$	45	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM) per JS-001-2017	Level 1C	1000 to <2000	V
Charged Device Model (CDM) per JS-002-2014	Level C3	≥1000	V
Moisture Rating			
Moisture Sensitivity Level (per J-STD-020D.1)	MSL	1	-

Note:

[1] These are stress ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damages to the device and/or to the surrounding circuit.

[2] For duration < 1ms, provided to indicate robustness and not recommended for normal operation.

[3] For duration < 10us, followed by sufficient time for the device to cool off.

[4] As measured on DUT soldered on 2 oz Cu (FR4) PCB of size 1 square inch.

7.0 Recommended Operating Conditions

Table 4 Recommended Operating Conditions [1][2] @T_J =+25 °C, Unless Otherwise Specified

Parameter	Symbol	Min	Nominal	Max	Unit
V_{reg} Regulated Voltage	V_{reg}	5.7	6.0	6.5	V
Input PWM Voltage	V_{PWM}	0		6.0	V
Drain Slew-Rate Control Resistor	Rg	0		300	Ω
Bypass capacitor at V_{DD} pin	C_{VDD}		100		nF
Bypass Capacitor at V_{reg} pin	C_{Vreg}	10	100		nF
Operating Case Temperature	T_C	-40		+125	°C

Note:

[1] Operating for extended periods of time at conditions beyond the recommended range might affect device reliability.

[2] All voltages are with respect to GND pin which is internally Kelvin connected to Source pin.

8.0 Electrical Specifications

Table 5 Electrical Specifications [1] @T_J=+25 °C, V_{reg} =6.0 V, Rg =0 Ω, unless otherwise specified

Parameter	Description	Condition	Minimum	Typical	Maximum	Unit
650 V GaN HEMT						
R_{DSON}	Drain to source resistance	I_{DS}=0.5 A DC		180	236	mΩ
		I_{DS}=0.5 A DC, T_J=+150 °C		440		
I_{DSS}	Drain to source leakage current	V_{DS}=650 V, V_{PWM}=0 V		0.2		μA
		V_{DS}=650 V, V_{PWM}=0 V, T_J=+150 °C		30.0		
C_{OSS}	Output capacitance	V_{DS}=400 V, V_{PWM}=0 V, Freq = 100 kHz		18		pF
$C_{O(ER)}$ [2]	Effective output capacitance – energy related	V_{DS} = 0 to 400 V, V_{PWM} = 0 V		26		pF
$C_{O(TR)}$ [3]	Effective output capacitance – time related	V_{DS} = 0 to 400 V, V_{PWM} = 0 V		40		pF
Q_{OSS}	Output charge	V_{DS}=400 V, V_{PWM} = 0 V		16		nC
Q_{RR} [4]	Reverse recovery charge			0		nC
V_{SD}	Reverse conduction voltage	I_{SD}=2 A, V_{PWM}=0 V		2.5		V
		I_{SD}=6 A, V_{PWM}=0 V		4.0		
Driver						
I_q	Quiescent current from V_{DD}	V_{DS} open, V_{PWM}=0		1.8		mA
I_{sw0}	Switching current from V_{DD}	V_{DS} open, V_{PWM} switching at 50% duty cycle, 1 MHz freq.		3.0		mA

$V_{DD\_UVLO-High}$	UVLO threshold while V_{DD} rising	V_{DD} =0V to 7.5V		4.6		V
$V_{DD\_UVLO-Low}$	UVLO threshold while V_{DD} falling	V_{DD}=7.5V to 0V		4.3		V
$UVLO_{hyst}$	UVLO hysteresis			0.3		V
V_{IH}	PWM input voltage to turn on				3.0	V
V_{IL}	PWM input voltage to turn off		0.7			V
DVDT Immunity						
$(dv/dt)_{DS}$	Max drain-source dv/dt	V_{DD} = 0V to 8V			200	V/ns
Switching Time @ R_G = 0Ω (Refer to Figure 5 and Figure 6)						
t_r	Rise time	V_{DS}=400V, I_{DS}=4A,		11		ns
		V_{DS}=400V, I_{DS}=4A, T_J=+150°C		11		
t_f	Fall time	V_{DS}=400V, I_{DS}=4A		4		ns
		V_{DS}=400V, I_{DS}=4A, T_J=+150°C		7		
$t_{prop-on}$	Turn-on propagation delay	V_{DS}=400V, I_{DS}=4A		14		ns
		V_{DS}=400V, I_{DS}=4A, T_J=+150°C		17		
$t_{prop-off}$	Turn-off propagation delay	V_{DS}=400V, I_{DS}=4A		19		ns
		V_{DS}=400V, I_{DS}=4A, T_J=+150°C		23		

Note:

[1] All voltages are with respect to GND pin which is internally Kelvin connected to Source pin.

[2] $C_{O(ER)}$ is an equivalent (fixed) capacitance that gives the same energy as C_{OSS} while V_{DS} rises from zero volt to the stated V_{DS}.

[3] $C_{O(TR)}$ is an equivalent (fixed) capacitance that gives the charging time as C_{OSS} while V_{DS} rises from zero volt to the stated V_{DS}.

[4] Q_{RR} computation excludes Q_{OSS}.

9.0 Detailed Description of Functions

9.1 UVLO Function

UVLO (Under Voltage Lock Out) controls the driver functionality. When the V_{DD} voltage is relatively low, such as during the system startup, the 650V GaN HEMT might turn on unintentionally due to various parasitic coupling. To address this, for V_{DD} below a certain threshold, UVLO forces the driver to keep the HEMT off and the PWM signal is ignored. As the V_{DD} voltage crosses the threshold above which the driver functions properly as shown in Figure 4, the UVLO releases the control, and the driver turns on and off the HEMT device according to the PWM input. It should be noted that for a reliable and efficient operation of the HEMT, the value of V_{DD} must be such that V_{reg} lies within the range given in the recommended operating conditions.

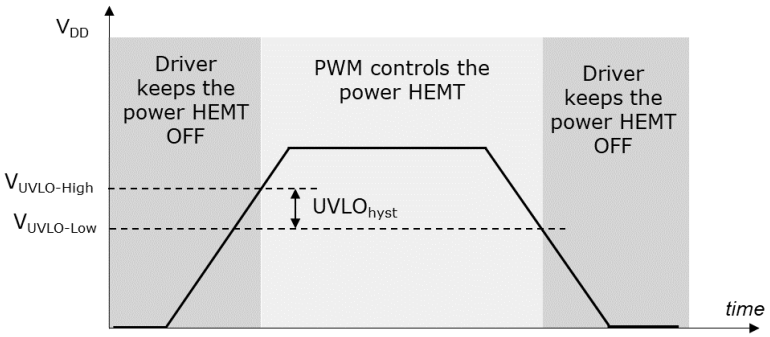


Figure 4 UVLO Functionality Diagram

9.2 DvDt Immunity Function

Large dv/dt at the drain pin is normal during the operation of converter. Such dv/dt may arise due to the usual switching actions, or due to the first-time hook-up of the converter system to the main supply of the power-stage. A positive dv/dt on the drain (with respect to the gate/source) will try to turn on the HEMT device through the parasitic gate-to-drain capacitance C_{GD}. This parasitic turn-on, also known as Miller turn-on or false turn-on, is highly undesirable, and might even cause catastrophic amount of shoot-through or crowbar current.

Usually, the driver is able to keep the HEMT off in the face of such dv/dt events, but for this to work properly, the driver requires its own supply to be up and steady. However, in many cases, the driver supply, which is derived from the main supply, may not be present at the first-time hookup of the main supply, which will lead to the HEMT device getting parasitically turn on.

The DvDt immunity function of TP44200NM device is a proprietary design which keeps the HEMT immune to such dv/dt induced turn-ons irrespective of whether V_{DD} supply is present or not. Also, this function works irrespective of usage of the device either on the low-side or the high-side of a half-bridge.

9.3 Adjustable Turn-On Slew Rate Function

An adjustable slew-rate of the drain voltage during turn-on is a useful feature which helps control EMI and limits the magnitude of ringing on the switch node in a converter. For this feature, TP44200NM uses an external resistor Rg of user selectable value between the pins RG and V_{reg} as shown in Figure 5. A typical plot of slew rate versus Rg value has been shown in Figure 15. It shall be noted that the switching-time numbers given in Table 5 are for the default value of Rg = 0 Ω.

10.0 Switching Time Measurement Information

The switching time parameters are measured using the test circuit shown in Figure 5, where two TP44200NM devices are used. The low-side TP44200NM is the device under test (DUT) and works as the switching device. Its V_{DD} pin is connected to a 15V DC supply through a current limiting resistor RDD of value 2.4 kΩ. Another resistor RG of 0 Ω is connected between pins R_G and V_{reg}. The high-side TP44200NM is used as a freewheeling/clamp-diode in the reverse direction. Its terminals 2–4 have been

kept open for simplicity and pin 5 is shorted to pin 6. For both the low-side and the high-side devices, pin 1 and pin 7 are open. Also, their pins 14–20 are shorted to their respective TP pins. The junction point of the drain of the low-side and the source of the high-side forms the switching node, and this is connected to a 400V DC bus supply through an inductive load.

When the PWM input pin of the low-side TP44200NM is supplied with a 5V pulse, the HEMT device turns on and its drain to source voltage (V_{DS}) goes down as shown in Figure 6. During this time, the inductor current starts to increase. When the PWM signal goes low, the HEMT device turns off, and hence, V_{DS} starts to increase with the slew rate depending on the values of the inductor current and the switch-node capacitance. The drain to source voltage V_{DS} gets clamped to the DC bus voltage because of the clamp diode, and the diode will conduct till the inductor current reaches zero.

The rise and fall times, and the propagation delays of PWM are defined as shown in Figure 6. The propagation delay to turn on the device is defined as the time from 50% of PWM rising edge to V_{DS} falling by 10% of the DC bus voltage at the given current. Similarly, propagation delay to turn off is defined as the time from 50% of PWM falling edge to V_{DS} rising by 10% of its bus voltage at the given current.

The rise time t_r is defined as the time it takes V_{DS} to go from 10% to 90% of the DC bus voltage during rising edge at the given drain current, while the fall time t_f is defined as the time it takes V_{DS} to drop from 90% to 10% of the DC bus voltage during the falling edge at the given drain current.

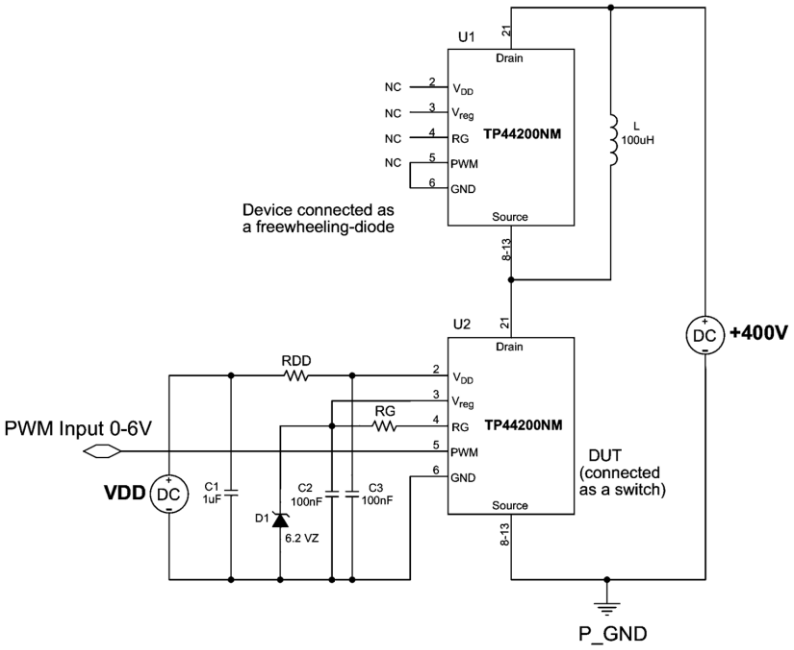


Figure 5 Switching Time Measurement Circuit

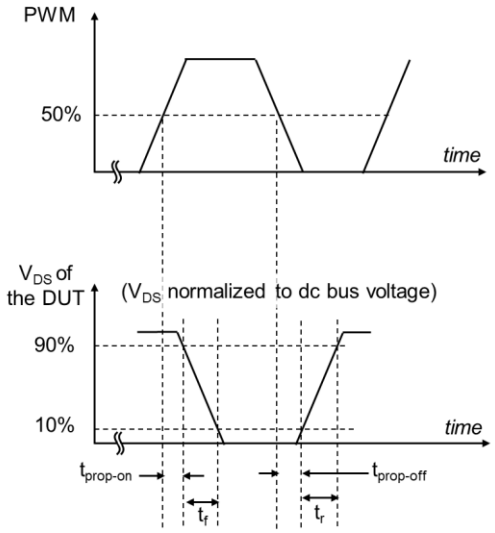


Figure 6 Switching Time Waveform and Definition of Parameters

11.0 Typical Characteristics

Conditions: @T_J = +25°C, V_{DD} = +7.5V, Rg = 0Ω, unless otherwise specified.

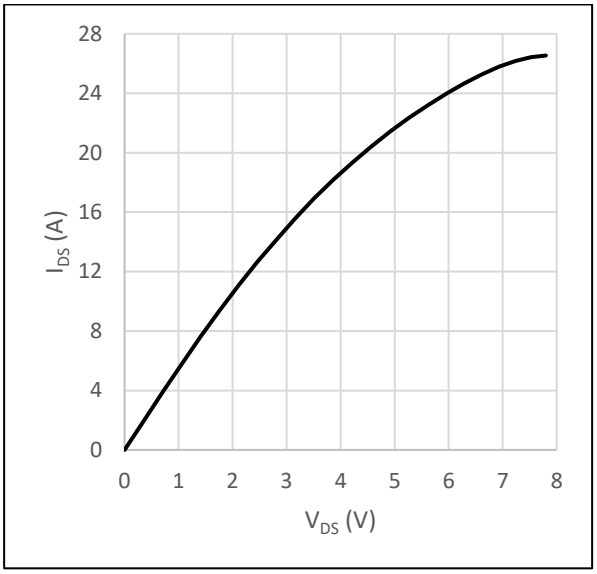


Figure 7 Forward Conduction of 650V HEMT I_{DS} vs. V_{DS}

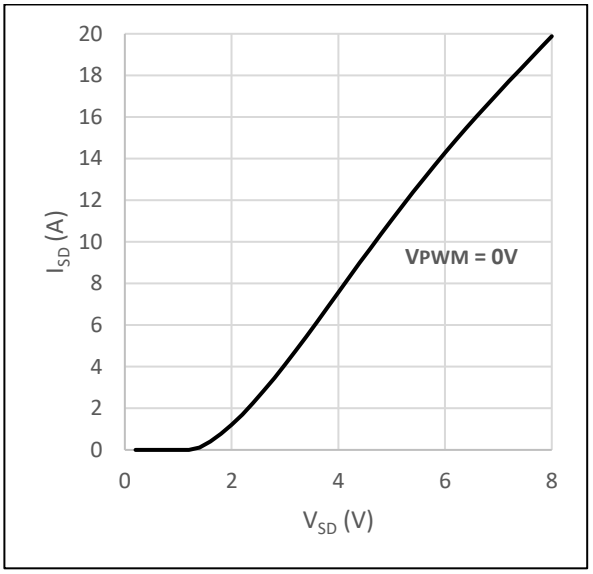


Figure 8 Reverse Conduction of 650V HEMT I_{SD} vs. V_{SD}

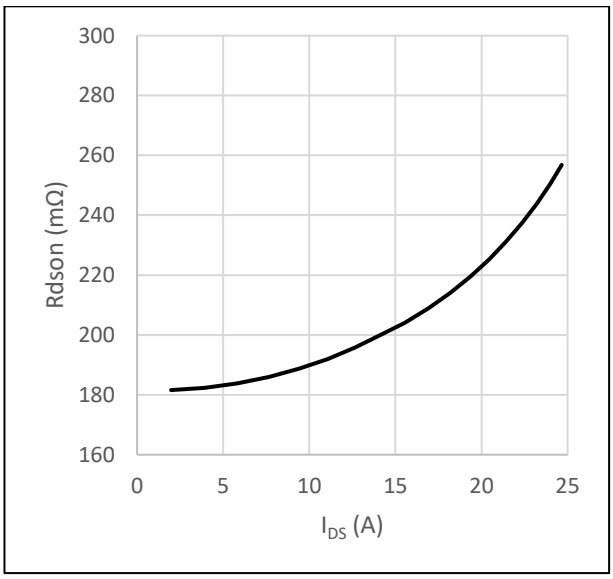


Figure 9 R_{DSON} vs. I_{DS}

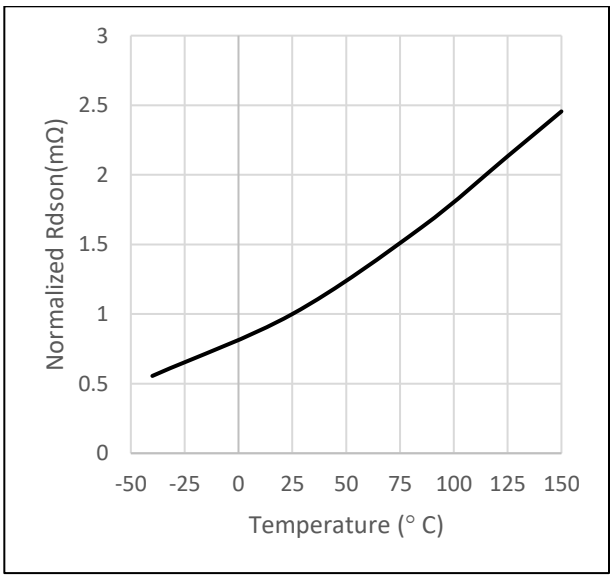


Figure 10 Normalized R_{DSON} vs. T_J @ I_{DS} = 1 A

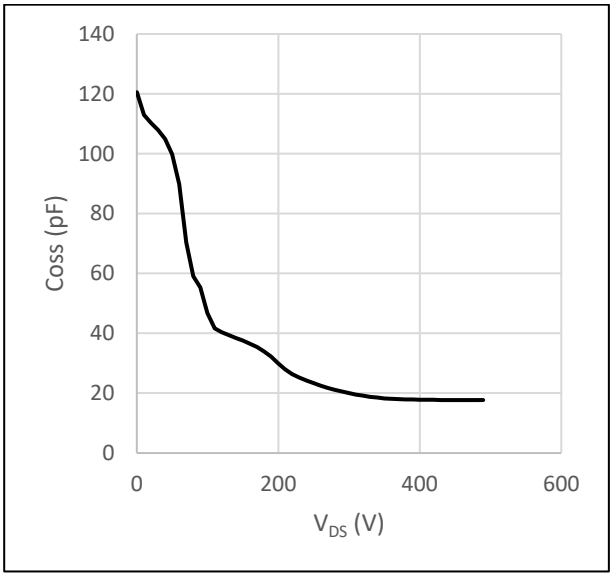


Figure 11 C_{OSS} vs. V_{DS}

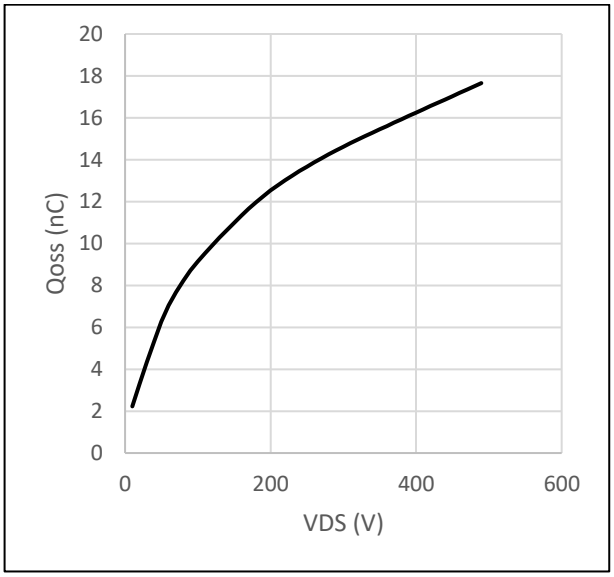


Figure 12 Q_{OSS} vs. V_{DS}

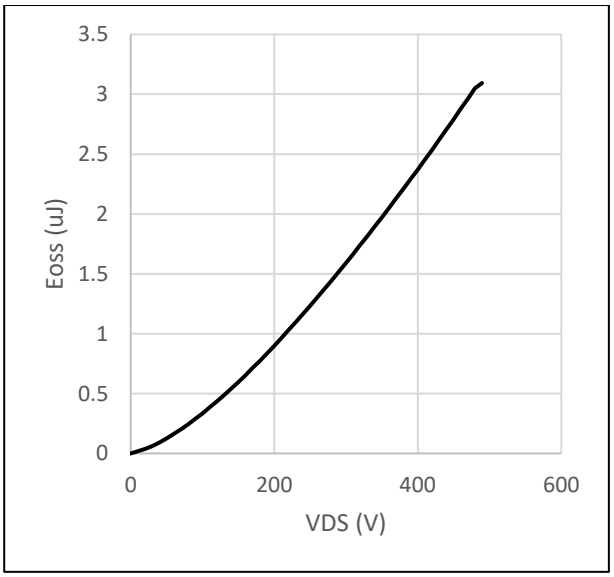


Figure 13 E_{OSS} vs. V_{DS}

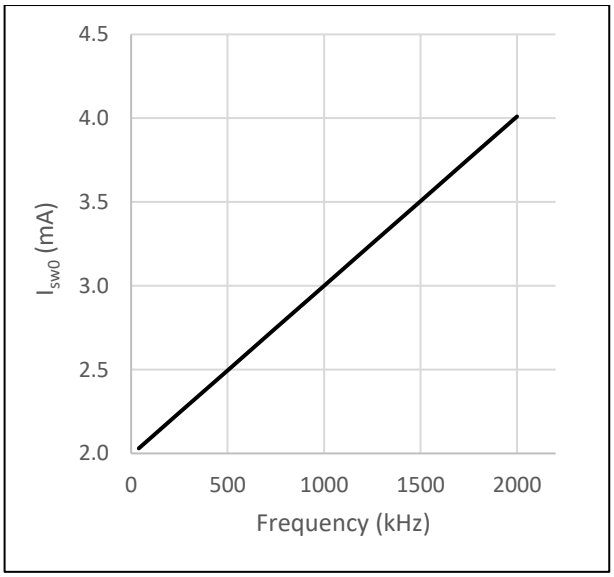


Figure 14 Driver Supply Current I_{sw0} vs. PWM Frequency under Open Drain Condition @50% duty cycle

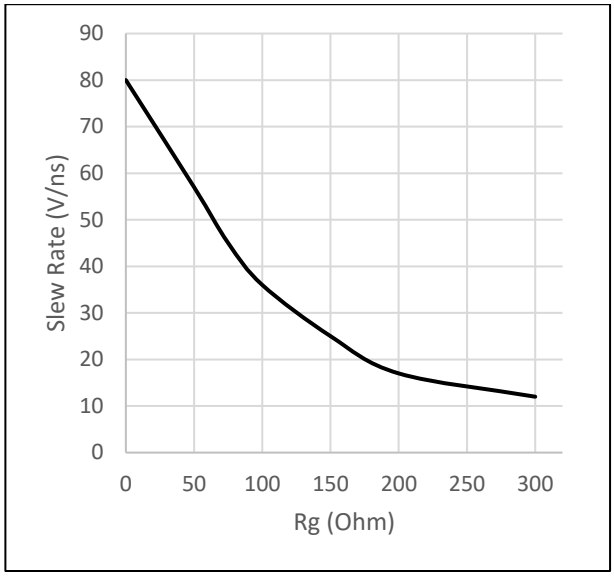


Figure 15 Drain Slew-Rate Variation vs. Rg Resistor at Turn-On Transition [1]

Note:

[1] The measurement setup is as per Figure 5 and Figure 6. The slew-rate corresponds to the region where V_{DS} drops from 90% to 10% of the bus voltage during its falling edge transition, and the value of I_{DS} at the transition edge is 4A.

12.0 Application Information

12.1 Half-bridge Configuration

Two TP44200NM devices can be configured in a half bridge topology as shown in Figure 16, where the setup is for a generic boost converter application. In here, Zener diodes and RDDL and RDDH resistors are used for regulating the voltage at V_{reg} of the respective parts. For the low-side device, VCC is directly connected to RDDL. For the high-side device, the connection to RDDH is through the bootstrap diode D3 (as shown), though one could also use an isolated DC-DC converter (not shown).

The resistor RDDL/RDDH should be chosen such that for the range of VCC, it should allow enough Iq for the operation. In an alternate arrangement, one could use an LDO in a feedback loop to regulate V_{reg} in which case LDO's output current will get automatically adjusted. See application note for TP44200NM device for more details.

An optional R-C filter (100 Ω, 100 pF, not shown in the diagram) can be added at the PWM pin of both the low-side and the high-side devices. The filter-capacitors shall be referenced to the respective GND pins of the low-side and the high-side.

The PWM input signal to the low-side module can be directly fed from the PWM output of a controller or a microcontroller (sitting on the low-side device ground), while the PWM for the high-side module can be supplied through a digital isolator as shown in the figure. The digital isolator shall have sufficient immunity against the expected high dv/dt rates of the switching node. The bias supplies for the primary and the secondary sides of the digital isolator can be derived from the V_{reg} pins as shown in the figure, and diodes may be inserted in the path to lower the voltages to the desired levels for the digital isolator. The RGL/RGH resistors may be chosen for the desired turn-on speed as per Figure 15.

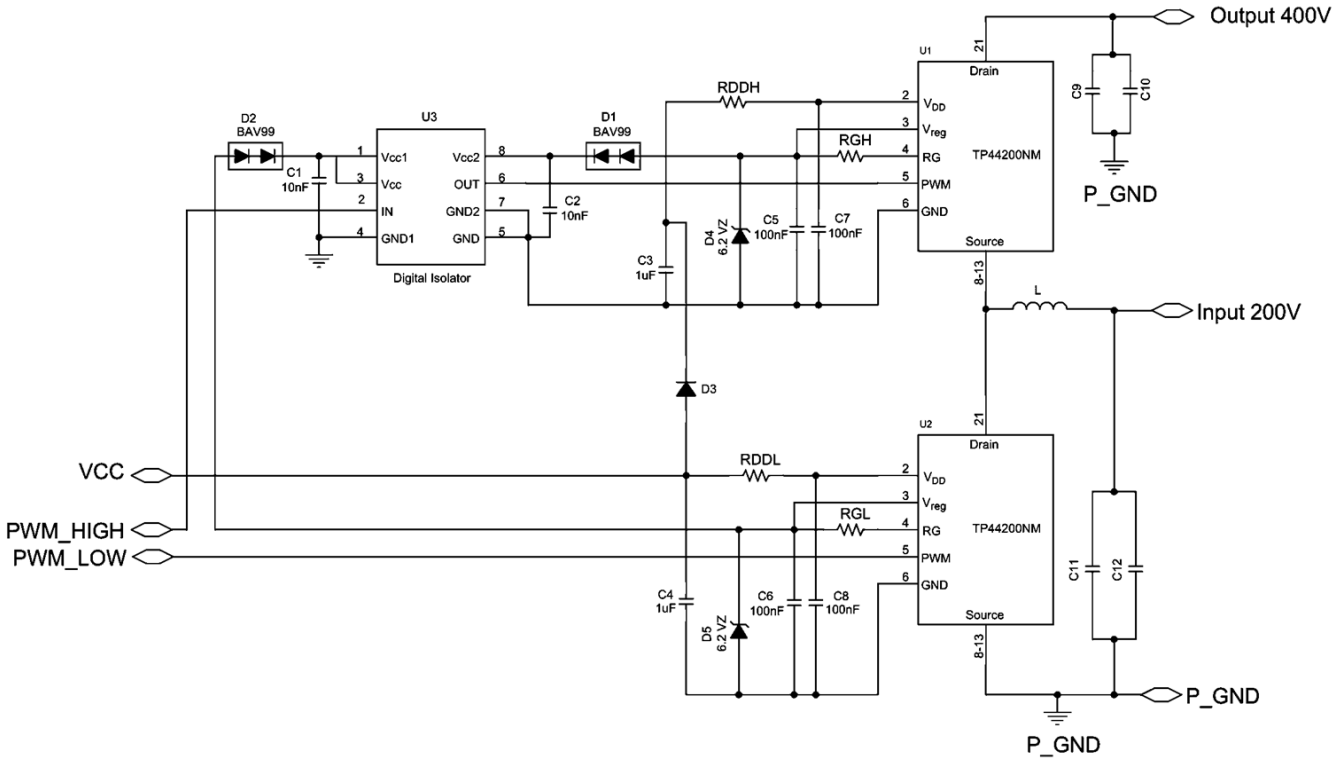


Figure 16 Boost Converter Application Circuit

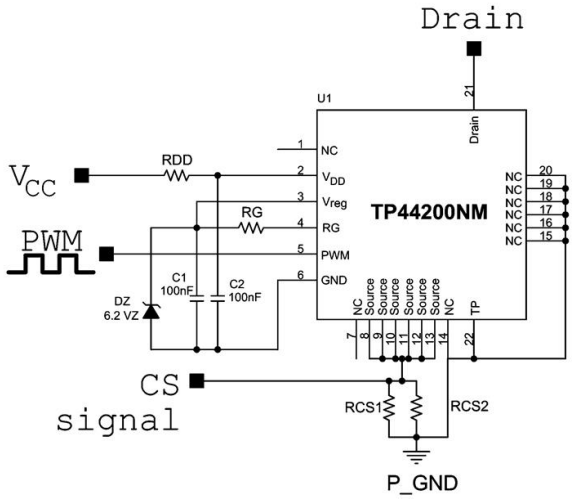
In Figure 16, some of the pins have not been shown for retaining clarity. The details of these pins are here: For both the low-side and the high-side devices, pin 1 and pin 7 are open. Also, for both the low-side and the high-side devices, pins 14–20 are shorted to their respective TP pins. For the connection of the TP, see the next section on the layout.

12.2 Layout with and without Current-Sense Resistor

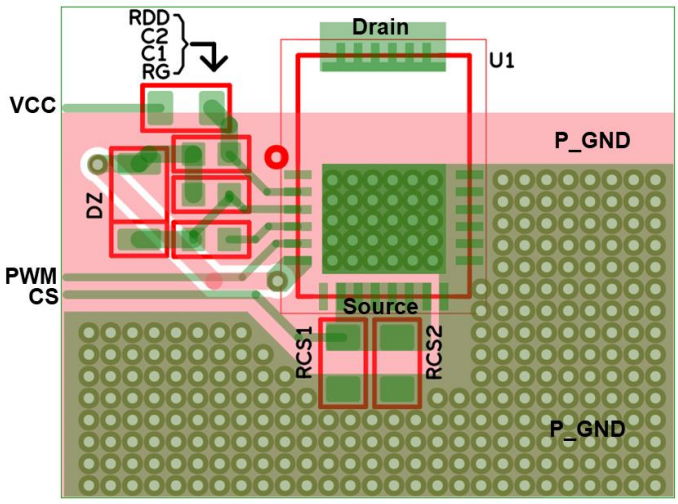
It is quite common to use a sense resistor at the source side of the low-side device for sensing the current. Such as arrangement is shown in the top left drawing of Figure 17. While doing the layout, the thermal pad TP shall always be connected to a large enough area on the PCB (the thermal plane) for heat

dissipation. Usually, P_GND is the largest copper area available, and the recommended layout is shown in the top right drawing of Figure 17 where P_GND acts as the thermal plane. Note that one of the advantages with Tagore's TP44200NM parts is that, even if we put the sense resistors between the source pins and the thermal plane, this only minimally affects the thermal performance of the device as the thermal pad TP has a direct and wide enough path to the thermal plane of the PCB.

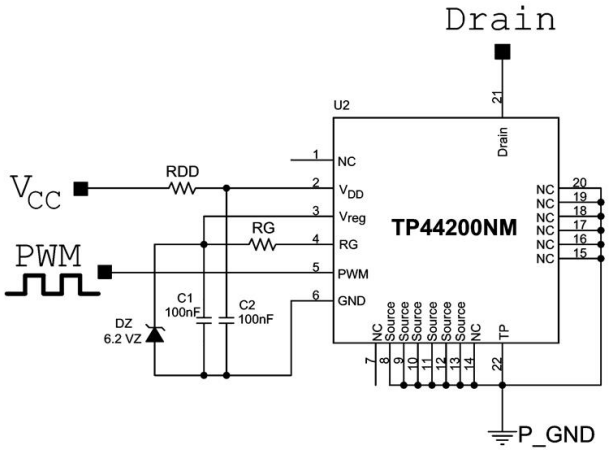
For the case when there are no sense resistors, one could short all the source pins with the TP and use a layout as shown in the bottom right drawing of Figure 17.



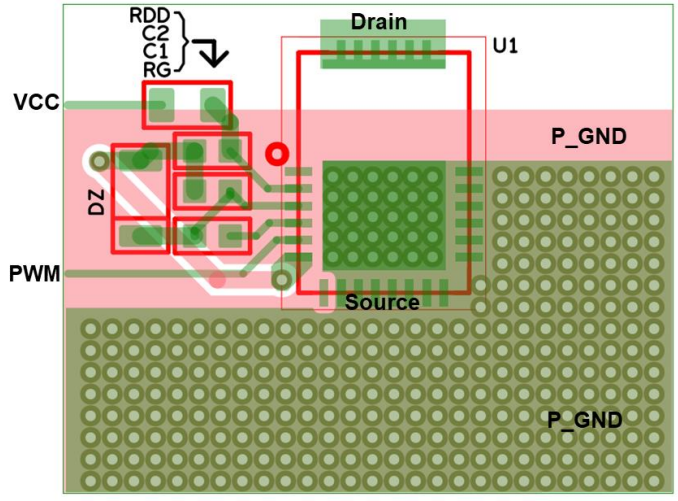
With Current Sensing Resistors



With Current Sense Resistors (IC sits on the green layer.)



Without Current Sensing Resistors



Without Current Sense Resistor (IC sits on the green layer.)

Figure 17 Layout Guidelines for with and without the Current Sense Resistors

13.0 Device Package Information

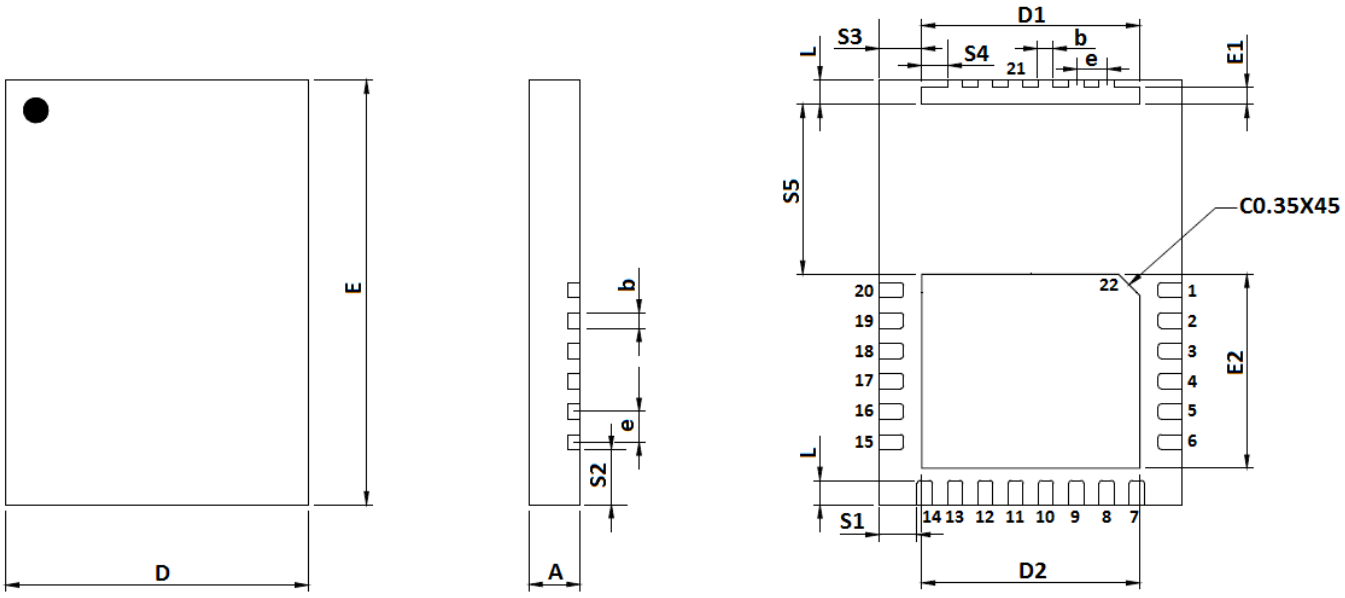


Figure 18 Device Package Drawing
(All dimensions are in mm)

Table 6 Device Package Dimensions

Dimension (mm)	Value (mm)	Tolerance (mm)	Dimension (mm)	Value (mm)	Tolerance (mm)
A	0.80	±0.05	E2	3.20	±0.05
b	0.25	+0.05/-0.07	L	0.40	±0.05
D	5.00 BSC	±0.05	S1	0.625	±0.05
D1	3.60	±0.05	S2	0.91	±0.05
D2	3.60	±0.05	S3	0.70	±0.05
e	0.50 BSC	±0.05	S4	0.425	±0.05
E	7.00 BSC	±0.05	S5	2.80	±0.05
E1	0.28	±0.05	-	-	-

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5μm ~ 20μm (Typical 10μm ~ 12μm)

Attention:
Please refer to application notes *TN-001* and *TN-002* at http://www.tagoretech.com for PCB and soldering related guidelines.

14.0 PCB Land Design

Guidelines:

[1] A 4-layer PCB is recommended.
[2] Via diameter is recommended to be 0.3mm to prevent solder wicking inside the vias.
[3] Thermal vias shall only be placed on pad A.
[4] The maximum via number for pad A is 6(X) × 5(Y) = 30 units.

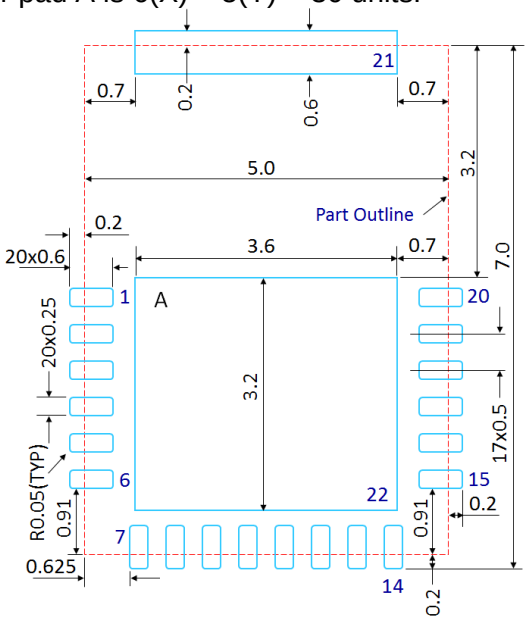


Figure 19 PCB Land Pattern
(Dimensions are in mm)

Non-Solder Mask Defined
(Preferred)

Solder Mask Defined

Figure 20 Solder Mask Pattern
(Dimensions are in mm)

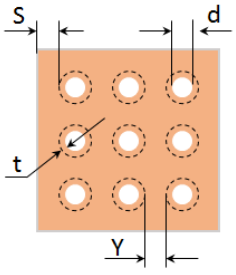


Figure 21 Thermal Via Pattern
(Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.3mm; Plating Thickness t=25μm or 50μm)

15.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125μm.

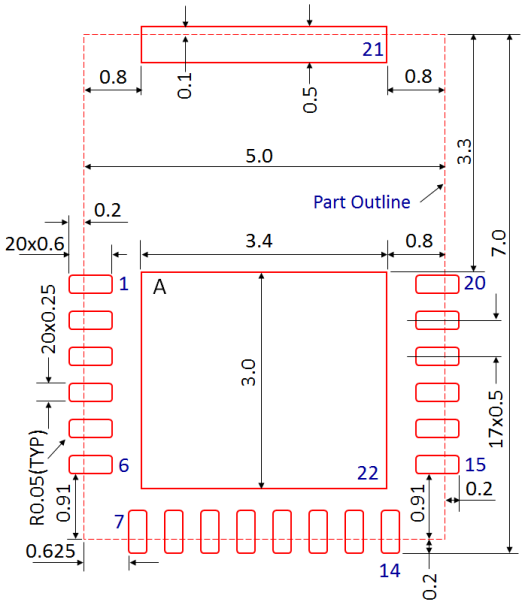


Figure 22 Stencil Openings
(Dimensions are in mm)

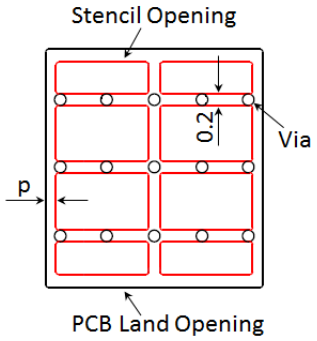


Figure 23 Stencil Openings (Shall Not Cover Via Areas if Possible)
(Dimensions are in mm)

16.0 Tape and Reel Information

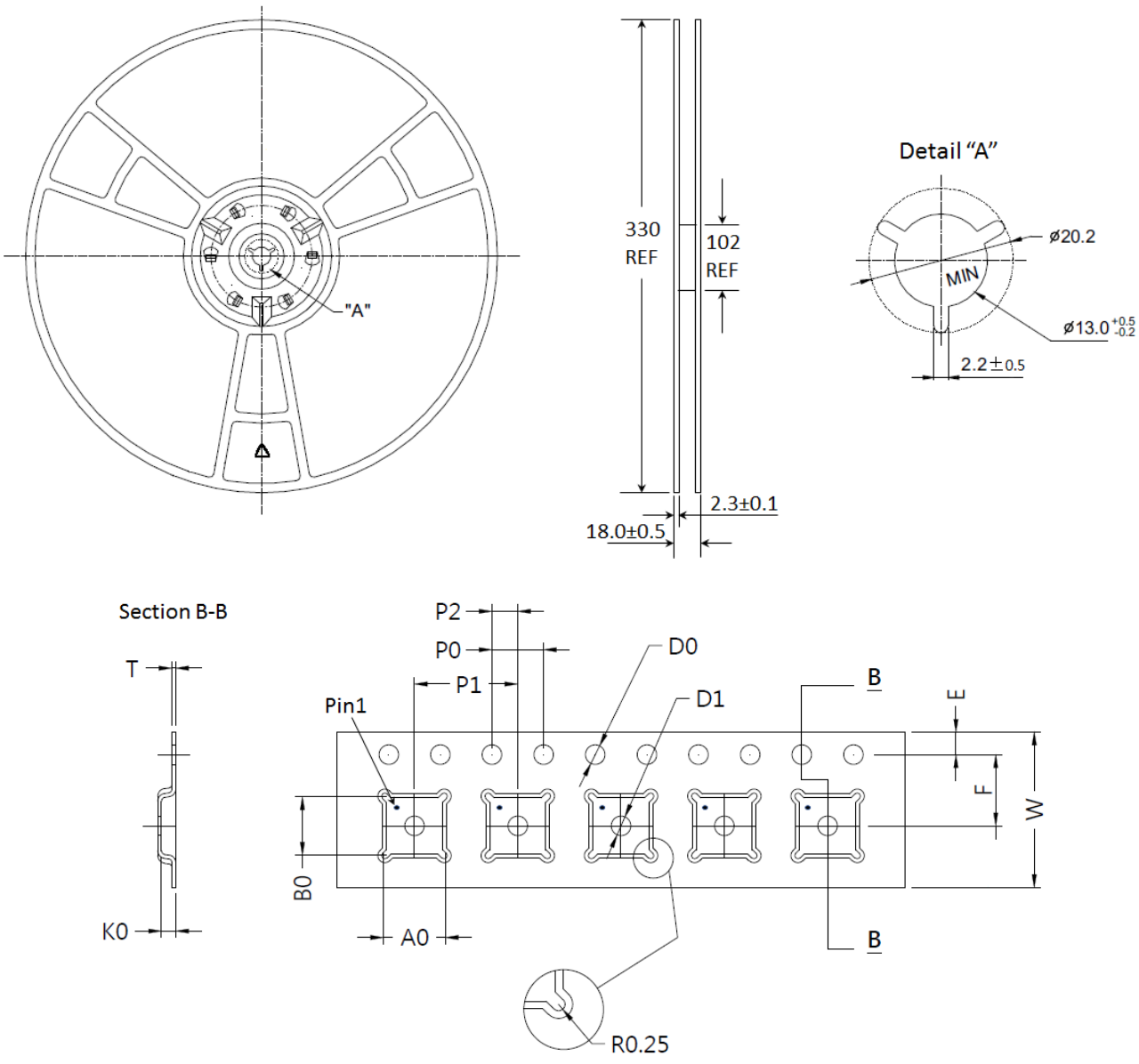


Figure 24 Tape and Reel Drawing

Table 7 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	5.35	±0.10	K0	1.10	±0.10
B0	7.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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