Features

- Full compliance with the USB Specification v1.1
- Support the RS232 Serial interface
- Support automatic handshake mode
- Over 1Mbps transfer rate
- Support remote wake-up and power management
- Dual data buffers for upstream and downstream data flow
- Support default ROM or external EEPROM for device configuration
- On chip USB transceiver
- On chip crystal oscillator running at 12M Hz
- 28 Pins SSOP package

Order Information

- TP561: 56K modem USB Chip

General Description

The TP561 operates as a bridge between one USB port and one standard RS232 Serial port, especially for TP560x modem chip. There are two large on-chip buffers accommodate the data flow from two different buses. The USB bulk-type data is adopted for maximum data transfer. Automatic handshake is supported at the Serial port. This device is also compliant with USB power management and remote wakeup scheme. Only minimum power is consumed from the host during suspend. By integrating all the functions into the SSOP-28 package, this chip is suitable for cable embedding. Users just simply hook the cable into PC or Hub's USB port, then they can connect to any RS-232 devices.

System Block Diagram

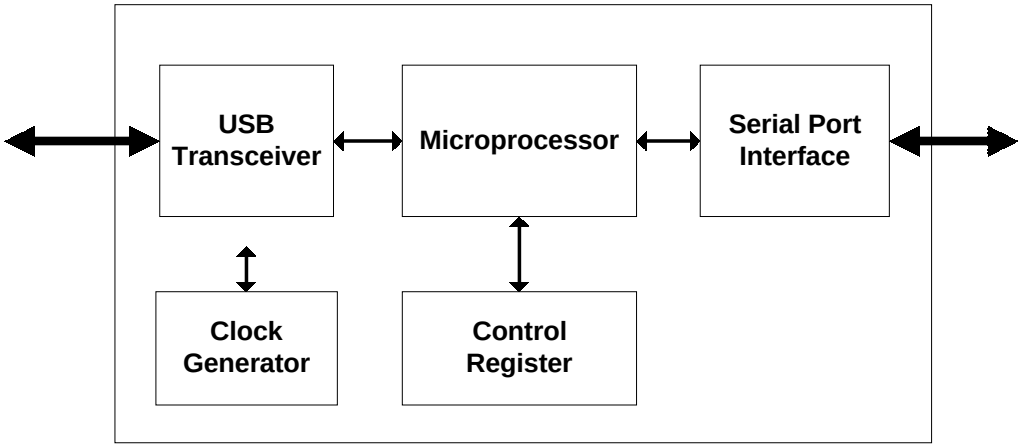

Figure 1. Block Diagram

PIN Assignments

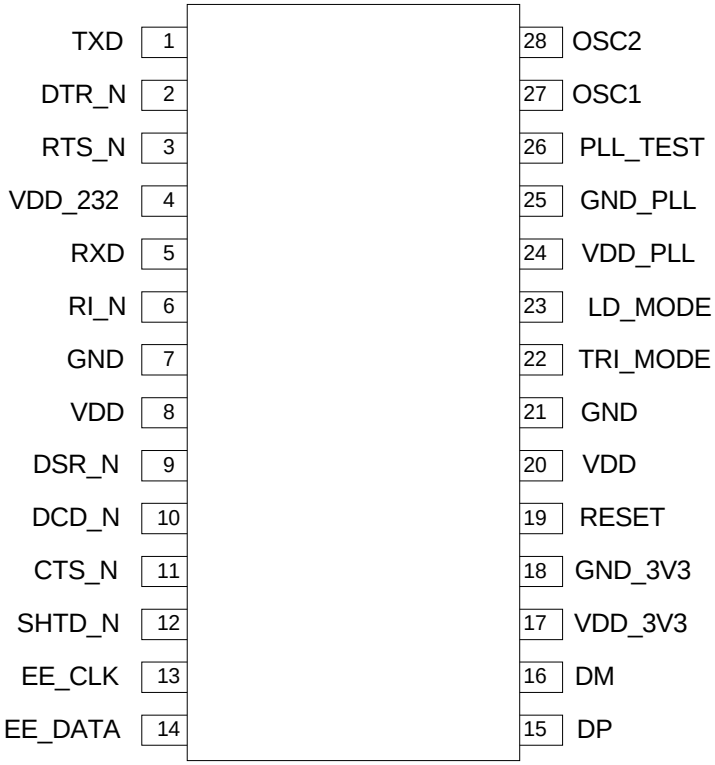

Figure 2. TP561 Pin Assignments

PIN Description

Pin No.	Symbol	I/O	Description
1	TXD	O*	Data output to Serial port
2	DTR_N	O*	Data Terminal Ready, active low
3	RTS_N	O*	Request To Send, active low
4	VDD_232	P	RS-232 VDD. The RS-232 output signals (Pin 1 ~ Pin 3) are designed for 5V, 3.3V or 3V operation. VDD_232 should be connected to the same power level of the RS-232 interface. (The RS-232 input signals are always 5V~3V tolerant.)
5	RXD	I*	Data input from Serial Bus
6	RI_N	I*	Ring Indicator, active low
7	GND	P	Ground
8	VDD	P	Power
9	DSR_N	I*	Data Set Ready, active low
10	DCD_N	I*	Data Carrier Detect, active low
11	CTS_N	I*	Clear To Send, active low
12	SHTD_N	O	Shut Down RS232 Transceiver
13	EE_CLK	I/O	During Reset, this pin is input for simulation purpose. During normal operation, this pin is Serial ROM clock
14	EE_DATA	I/O	Serial ROM data signal
15	DP	I/O	USB DPLUS signal
16	DM	I/O	USB DMINUS signal
17	VDD_3V3	O	3.3V power output from internal voltage regulator
18	GND_3V3	P	3.3V ground
19	RESET	I	System Reset
20	VDD	P	Power
21	GND	P	Ground
22	TRI_MODE	I	RS232 Tri-state output control during Suspend
23	LD_MODE	I	Load Mode. At reset, LD_MODE is used to decide if this is a heavy load or light load device. High: indicates this is a 500mA device. Low: indicates this is a 100mA device.
24	VDD_PLL	P	5V power for PLL
25	GND_PLL	P	Ground for PLL
26	PLL_TEST	I	PLL test mode control
27	OSC1	I	Crystal oscillator input
28	OSC2	O	Crystal oscillator output

Table 1. TP561 Pin Description

External EEPROM and Device Configuration

TP561 allows storing the configuration data in an external EEPROM. After reset, the first two bytes of EEPROM are checked. If their value is 067Bh, the EEPROM is valid and the contents of the EEPROM is loaded as the chip's default parameters. Otherwise, the chip's default setting is used. The content of EEPROM is shown in Table 2 below.
The Device Configuration Register is used to control some vendor-specific functions. The meaning of each bit in Device Configuration Register is shown in Table 3. Reserved and unused pins always set to the default value.

Bytes	Name	Description
1: 0	EECHK	When the EEPROM is programmed, these two bytes is configured as 067B. After reset, they will be checked for the value. If matched, the following information will be loaded as the default parameters.
3: 2	VID	USB Vendor ID.
5: 4	PID	Product ID.
7: 6	RN	Release number (BCD).
10: 8	DCR	Device Configuration Register.

Table 2. EEPROM Content

Name	Bits	Definition	Default
23	RESERVED	Reserved.	0
22	TRI_OUT	RS-232 Output Tri-state: 1: RS-232 output Tri-state 0: RS-232 output in output mode	0
21	RESERVED	Reserved.	0
20	WURX	Enable Wake Up Trigger on RXD: 0 – Disabled; 1 – Enable Wake Up Trigger on RXD state changes.	0
19	WUDSR	Enable Wake Up Trigger on DSR: 0 – Disabled; 1 – Enable Wake Up Trigger on DSR state changes.	0
18	WURI	Enable Wake Up Trigger on RI: 0 – Disabled; 1 – Enable Wake Up Trigger on RI state changes.	0
17	WUDCD	Enable Wake Up Trigger on DCD: 0 – Disabled; 1 – Enable Wake Up Trigger on DCD state changes.	0
16	WUCTS	Enable Wake Up Trigger on CTS: 0 – Disabled; 1 – Enable Wake Up Trigger on CTS state changes.	0
15	RESERVED	Always set to one	1
14	RESERVED	Always set to one	1
13 : 1	RESERVED	Always set to zero	0's
0	RSPDM	RS-232 Transceiver Shut-Down Mode: 1: Shut down the transceiver when USB SUSPEND is engaged 0: Do not shut down the transceiver even when USB SUSPEND is engaged	0

Table 3. Device Configuration Register

Electrical Characteristics

Absolute Maximum Rating

Power supply voltage	-0.3V to 6.0V
Operating temperature under bias	0℃ to 70℃
Storage temperature	-55℃ to 150℃
Applied voltage on any pin	-0.3V≦VIN≦VDD+0.3V

Table 4. Absolute Maximum Rating

DC Electrical Characteristics (VDD=5V, GND=0V, TA=0℃ to 70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
VDD5V	Operation Voltage	4.75	5.0	5.25	V	
IDD	Operation Current		19	24	mA	
VIH	Input High Voltage	2.0			V	
VIL	Input Low Voltage			+0.8	V	
ILI	Input Leakage	-10		10	uA	VIN =0, 5.25V
VOH	Output High Voltage	3.5			V	IOH=-0.5mA
VOL	Output Low Voltage			+0.4	V	IOL=1.5mA
CIN	Input Capacitance		3.0		pF	

Table 5. DC electrical characteristics

USB Transceiver Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Rise and Fall Times: (10%—90%) (90%—10%)	 TR TF	 4 4	 8 8	 15 15	 ns ns
Cross Point	Vcr	1.3	--	2.0	V
Output Impedance	RD	23	28	33	ohm
High Level Output	VOH	2.8	--	--	V
Low Level Output	VOL	--	--	0.7	V
High Level Iutput	VIH	2.0	--	--	V
Low Level Iutput	VIL	--	--	0.8	V

- CL :50pf

Clock Characteristics

Parameter	Min	Typ	Max	Units
Frequency of Operation	11.976	12.000	12.024	MHz
Clock Period	83.1	83.3	83.5	ns
Duty Cycle	45	50	55	%

Package Dimensions (28-Pin SSOP)

Symbol	Millimeters			Inch		
	Min	Nom	Max	Min	Nom	Max
b	0.22		0.38	0.009		0.015
E	7.40	7.80	8.20	0.291	0.307	0.323
E1	5.00	5.30	5.60	0.197	0.209	0.220
L	0.55	0.75	0.95	0.021	0.030	0.037
R1	0.09			0.004		
D	9.9	10.2	10.5	0.390	0.402	0.413
A			2.0			0.079
e		0.65			0.0256	
L1		1.25			0.050	
A1	0.05			0.020		
A2	1.65	1.75	1.85	0.065	0.069	0.073