



# TP6311QG

## *1/8 - 1/16 Duty VFD Controller/ Driver*

# *DataSheet*

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# TP6311QG

## *1/8 - 1/16 Duty VFD Controller/Driver*

### General Specification

The TP6311QG is a FIP (Fluorescent indicator Panel or Vacuum Fluorescent Display) controller/driver that is driven on a 1/8 – to 1/16 duty factor. It consists of 12 segment output lines, 8 grid output lines, 8 segment/grid output drive lines, a display memory, a control circuit, and a key scan circuit. Serial data is input to the TP6311QG through a three-line serial interface. This FIP controller/driver is ideal as a peripheral device of a single-chip microcomputer.

### FEATURE

- Many display modes (12-segment & 16-digit to 20-segment & 8-digit)
- Key scanning (12 × 4 matrices)
- Dimming circuit (eight steps)
- High-voltage output ( $V_{DD} - 35V$  max)
- LED ports (5 chs, 20 mA max)
- General-purpose input port (4 bits)
- No external resistor necessary for driver outputs (P-ch open-drain + pull-down resistor output)
- Serial interface (CLK, STB,  $D_{IN}$ ,  $D_{OUT}$ )



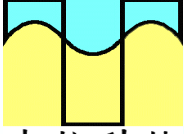
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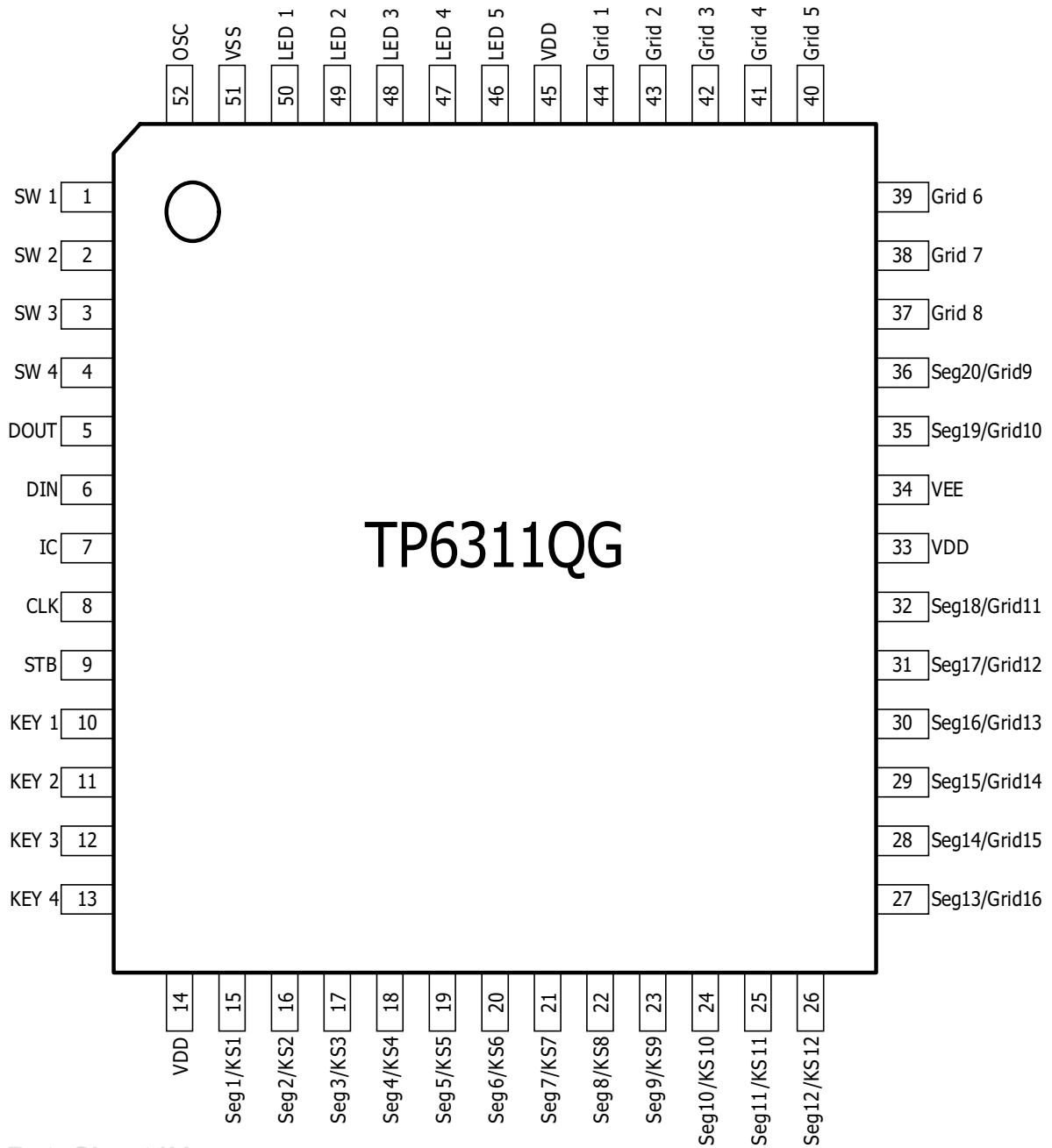


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### Pin Configurations and Package Type



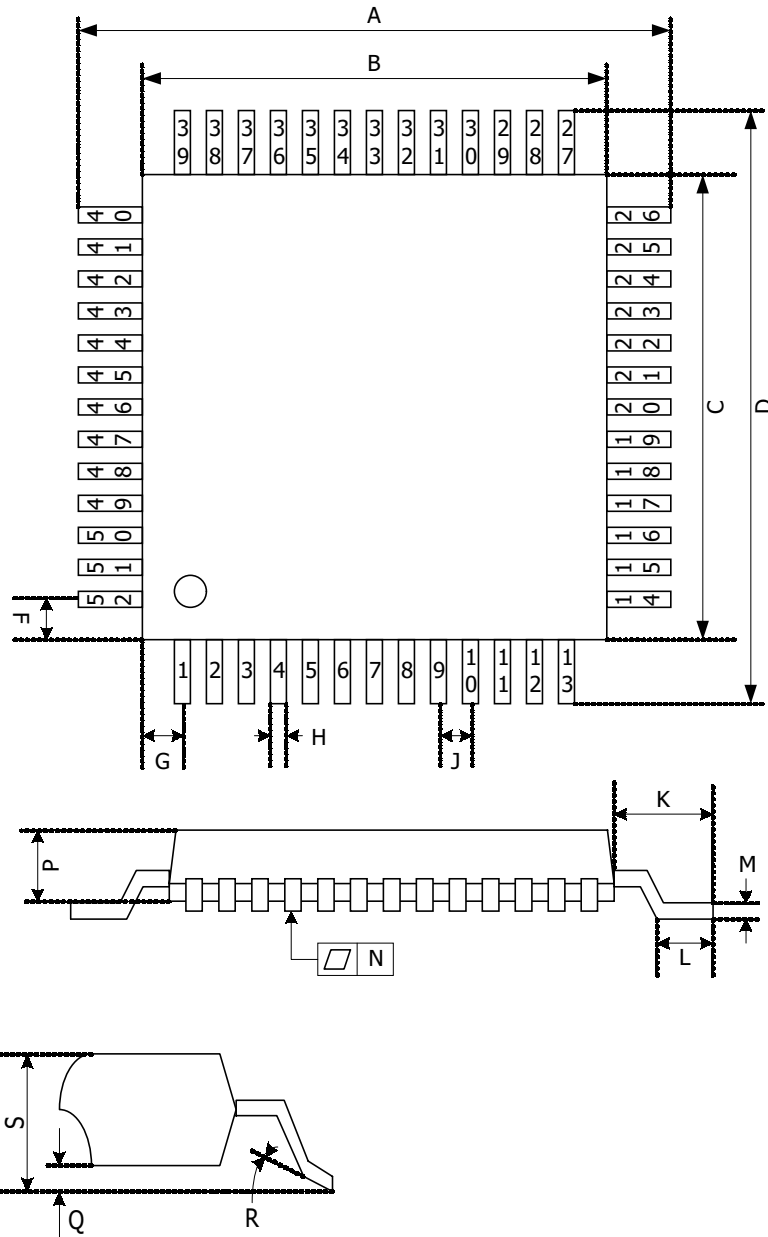
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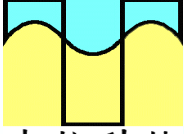
Use all the power pins. Leave the IC pin open.

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52 PIN PLASTIC QFP (14 × 14)



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ITEM	MILLMETERS	INCHES		ITEM	MILLMETERS	INCHES	
A	17.6± 0.4	0.693± 0.016		K	1.8± 0.2	0.071	+0.008 -0.009
B	14.0± 0.2	0.551	+0.009 -0.008	L	0.8± 0.2	0.031	+0.009 -0.008
C	14.0± 0.2	0.551	+0.009 -0.008	M	0.15	+0.10 -0.05	0.006 +0.004 -0.003
D	17.6± 0.4	0.693± 0.016		N	0.10	0.004	
F	1.0	0.039		P	2.6	0.102	
G	1.0	0.039		Q	0.1± 0.1	0.004± 0.004	
H	0.40± 0.10	0.016	+0.004 -0.005	R	5° ± 5°	5° ± 5°	
I	0.20	0.008		S	3.0 MAX.	0.119 MAX.	
J	1.0 (T.P.)	0.039 (T.P.)					

# TP6311QG

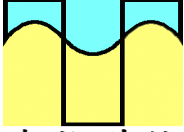
## *1/8 - 1/16 Duty VFD Controller/ Driver*

### Pin Descriptions

#### Pin Function

Pin No	Symbol	Pin Name	Description
6	DIN	Date input	Input serial data at rising edge of shift clock, starting from lower bit.
5	DOUT	Date output	Outputs serial data at falling edge of shift clock, starting from lower bit. This is N-ch open-drain output pin.
9	STB	Strobe	Initializes serial interface at rising or falling edge to make TP6311QG waiting for reception of command. Data input after STB has fallen is processed as command. While command data is processed, current processing is stopped, and serial interface is initialized . While STB is high, CLK is ignored.
8	CLK	Clock input	Reads serial data at rising edge, and outputs data at falling edge.
52	OSC	Oscillator pin	Connect resistor for determining oscillation frequency to this pin.
15 to 26	Seg1/KS1 to Seg12/KS12	High-voltage output (segment)	Segment output pins (Dual function as key source)
44 to 37	Grid1 to Grid8	High-voltage output (grid)	Grid output pins
27 to 32 35 to 36	Seg13/Grid16 to Seg20/Grid9	High-voltage output (segment/grid)	These pins are selectable for segment or grid output.
50 to 46	LED1 to LED5	LED output	CMOS output. +20 mA max
10 to 13	Key1 to Key4	Key data input	Data input to these pins is latched at end of display cycle.
1 to 4	SW1 to SW4	Switch input	These pins constitute 4-bit general-purpose input port.

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## *1/8 - 1/16 Duty VFD Controller/ Driver*

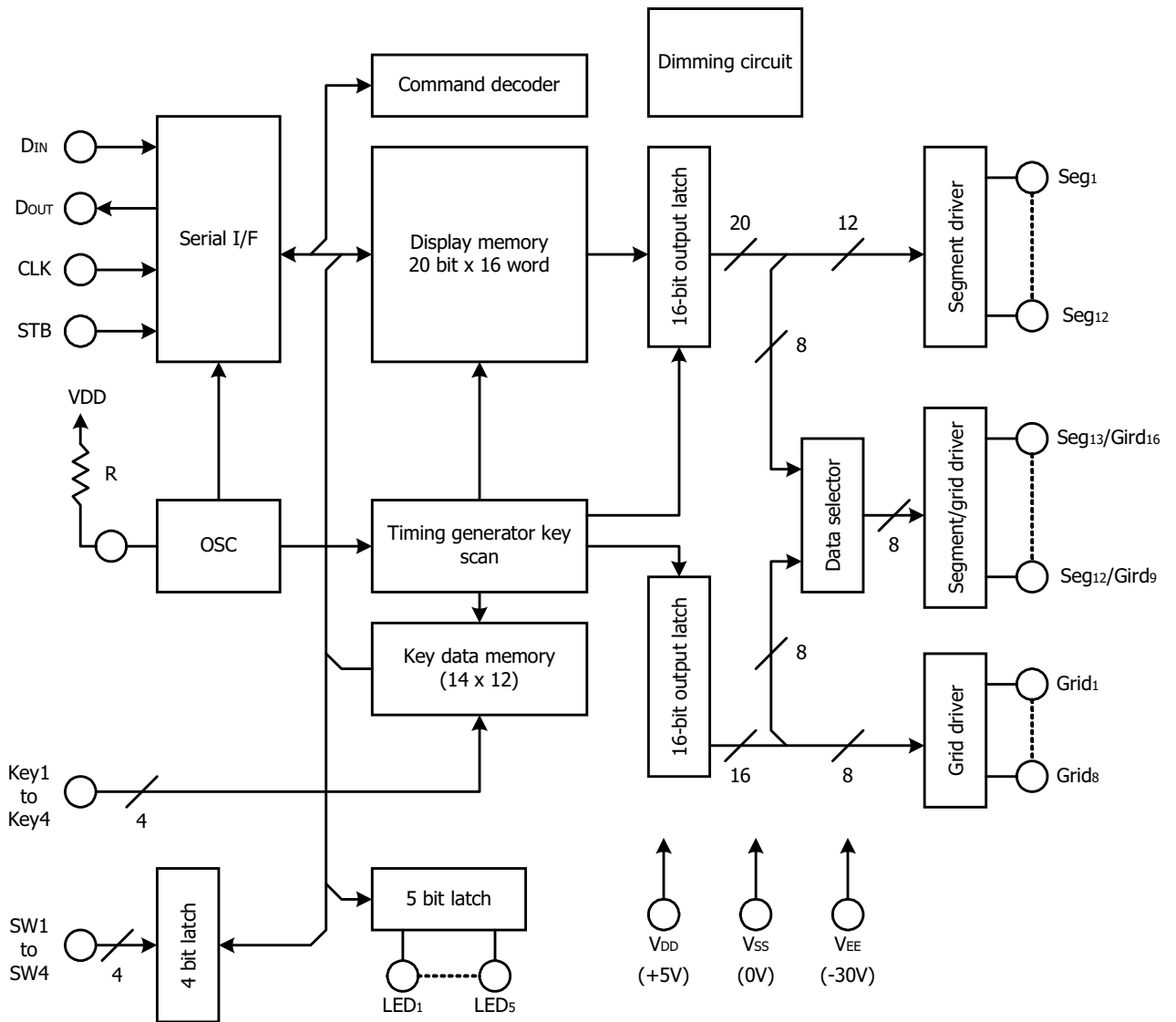
14, 33,45	VDD	Logic power	5V $\pm$ 10%
51	VSS	Logic ground	Connect this pin to GND of system.
34	VEE	Pull-down level	VDD – 35 V max
7	IC	Internally connected	Be sure to leave this pin open (this pin is at VDD level).



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## 1/8 - 1/16 Duty VFD Controller/Driver

### Functional Block Diagram





# TP6311QG

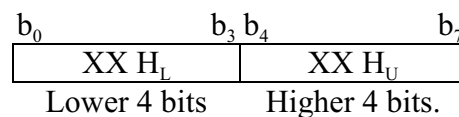
## 1/8 - 1/16 Duty VFD Controller/Driver

### Function Descriptions

#### Display RAM Address and Display Mode

The display RAM stores the data transmitted from an external device to the TP6311QG through the serial interface, and is assigned addresses as follows, in units of 8 bits:

Seg <sub>1</sub>	Seg <sub>4</sub>	Seg <sub>8</sub>	Seg <sub>12</sub>	Seg <sub>16</sub>	Seg <sub>20</sub>	
00H <sub>L</sub>	00H <sub>U</sub>	01H <sub>L</sub>	01H <sub>U</sub>	02H <sub>L</sub>		DIG1
03H <sub>L</sub>	03H <sub>U</sub>	04H <sub>L</sub>	04H <sub>U</sub>	05H <sub>L</sub>		DIG2
06H <sub>L</sub>	06H <sub>U</sub>	07H <sub>L</sub>	07H <sub>U</sub>	08H <sub>L</sub>		DIG3
09H <sub>L</sub>	09H <sub>U</sub>	0AH <sub>L</sub>	0AH <sub>U</sub>	0BH <sub>L</sub>		DIG4
0CH <sub>L</sub>	0CH <sub>U</sub>	0DH <sub>L</sub>	0DH <sub>U</sub>	0EH <sub>L</sub>		DIG5
0FH <sub>L</sub>	0FH <sub>U</sub>	10H <sub>L</sub>	10H <sub>U</sub>	11H <sub>L</sub>		DIG
12H <sub>L</sub>	12H <sub>U</sub>	13H <sub>L</sub>	13H <sub>U</sub>	14H <sub>L</sub>		DIG7
15H <sub>L</sub>	15H <sub>U</sub>	16H <sub>L</sub>	16H <sub>U</sub>	17H <sub>L</sub>		DIG8
18H <sub>L</sub>	18H <sub>U</sub>	19H <sub>L</sub>	19H <sub>U</sub>	1AH <sub>L</sub>		DIG9
1BH <sub>L</sub>	1BH <sub>U</sub>	1CH <sub>L</sub>	1CH <sub>U</sub>	1DH <sub>L</sub>		DIG10
1EH <sub>L</sub>	1EH <sub>U</sub>	1FH <sub>L</sub>	1FH <sub>U</sub>	20H <sub>L</sub>		DIG11
21H <sub>L</sub>	21H <sub>U</sub>	22H <sub>L</sub>	22H <sub>U</sub>	23H <sub>L</sub>		DIG12
24H <sub>L</sub>	24H <sub>U</sub>	25H <sub>L</sub>	25H <sub>U</sub>	26H <sub>L</sub>		DIG13
27H <sub>L</sub>	27H <sub>U</sub>	28H <sub>L</sub>	28H <sub>U</sub>	29H <sub>L</sub>		DIG14
2AH <sub>L</sub>	2AH <sub>U</sub>	2BH <sub>L</sub>	2BH <sub>U</sub>	2CH <sub>L</sub>		DIG15
2DH <sub>L</sub>	2DH <sub>U</sub>	2EH <sub>L</sub>	2EH <sub>U</sub>	2FH <sub>L</sub>		DIG16



Only the lower 4 bits of the addresses assigned to Seg17 through Seg20 are valid, and the higher 4 bits are ignored.

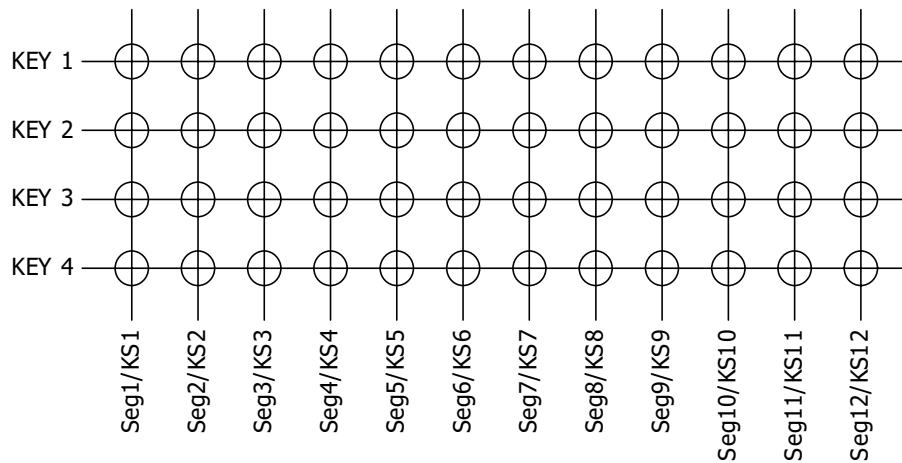


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### Key Matrix and Key-Input Data Storage RAM

The key matrix is of 12 × 4 configuration, as shown below.



The data of each key is stored as illustrated below, and is read by a read command, starting from the least significant bit.

KEY <sub>1</sub> .....	KEY <sub>4</sub>	KEY <sub>1</sub> .....	KEY <sub>4</sub>	
Seg <sub>1</sub> / KS <sub>1</sub>	Seg <sub>2</sub> / KS <sub>2</sub>	Reading sequenc	Seg <sub>3</sub> / KS <sub>3</sub>	
Seg <sub>3</sub> / KS <sub>3</sub>	Seg <sub>4</sub> / KS <sub>4</sub>		Seg <sub>5</sub> / KS <sub>5</sub>	Seg <sub>6</sub> / KS <sub>6</sub>
Seg <sub>5</sub> / KS <sub>5</sub>	Seg <sub>6</sub> / KS <sub>6</sub>		Seg <sub>7</sub> / KS <sub>7</sub>	Seg <sub>8</sub> / KS <sub>8</sub>
Seg <sub>7</sub> / KS <sub>7</sub>	Seg <sub>8</sub> / KS <sub>8</sub>		Seg <sub>9</sub> / KS <sub>9</sub>	Seg <sub>10</sub> / KS <sub>10</sub>
Seg <sub>9</sub> / KS <sub>9</sub>	Seg <sub>10</sub> / KS <sub>10</sub>		Seg <sub>11</sub> / KS <sub>11</sub>	Seg <sub>12</sub> / KS <sub>12</sub>
Seg <sub>11</sub> / KS <sub>11</sub>	Seg <sub>12</sub> / KS <sub>12</sub>			

b0 ..... b3      b4 ..... b7

When the most significant bit of data (Seg12 b7) has been read, the least significant bit of the next data (Seg1 b0) is read.

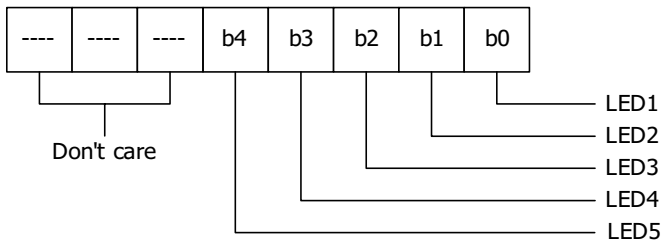


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## 1/8 - 1/16 Duty VFD Controller/Driver

### LED PORT

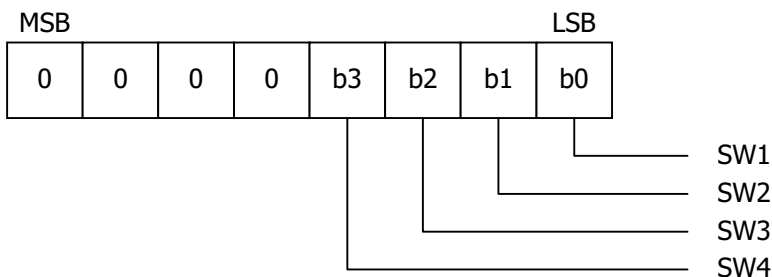
Data is written to the LED port by a write command, starting from the least significant bit of the port. When a bit of this port is 0, the corresponding LED lights ; when the bit is 1, the LED goes off. The data of bits 6 through 8 is ignored.



On power application, all the LEDs remain dark.

### SW Data

The SW data is read by a read command, starting from the least significant bit. Bits 5 through 8 of the SW data are 0.





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## 1/8 - 1/16 Duty VFD Controller/Driver

### Command

A command sets the display mode and status of the FIP driver.

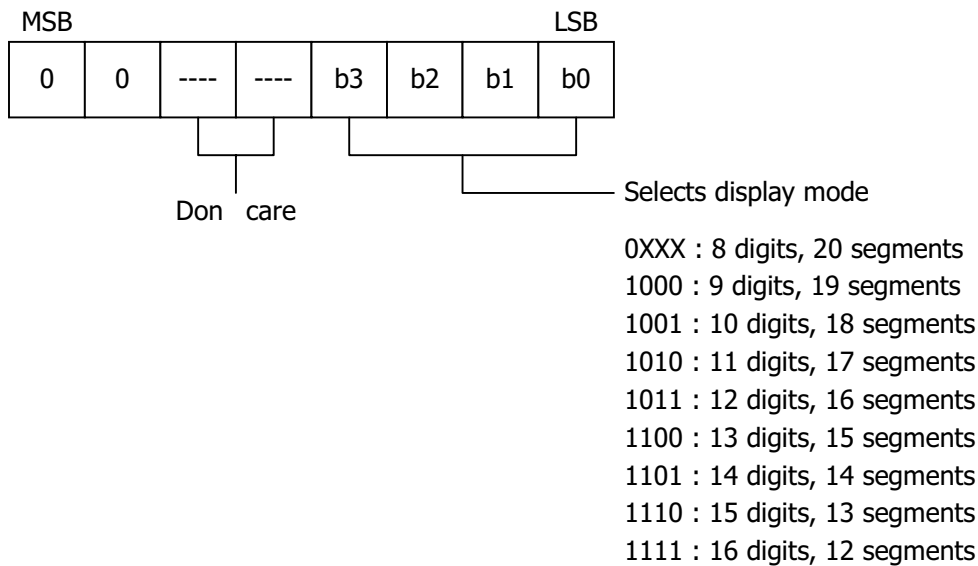
The first 1 byte input to the TP6311QG through the Din pin after the STB pin has fallen is regarded as a command.

If STB is made high while a command/data is transmitted, serial communication is initialized, and the command/data being transmitted is invalid (however, the command/data already transmitted remains valid).

#### (1) Display mode setting command

This command initializes the TP6311QG and selects the number of segments and number of grids (1/8 to 1/16 duty, 12 segments to 20 segments).

On power application, the 16-digit, 12-segment mode is selected.

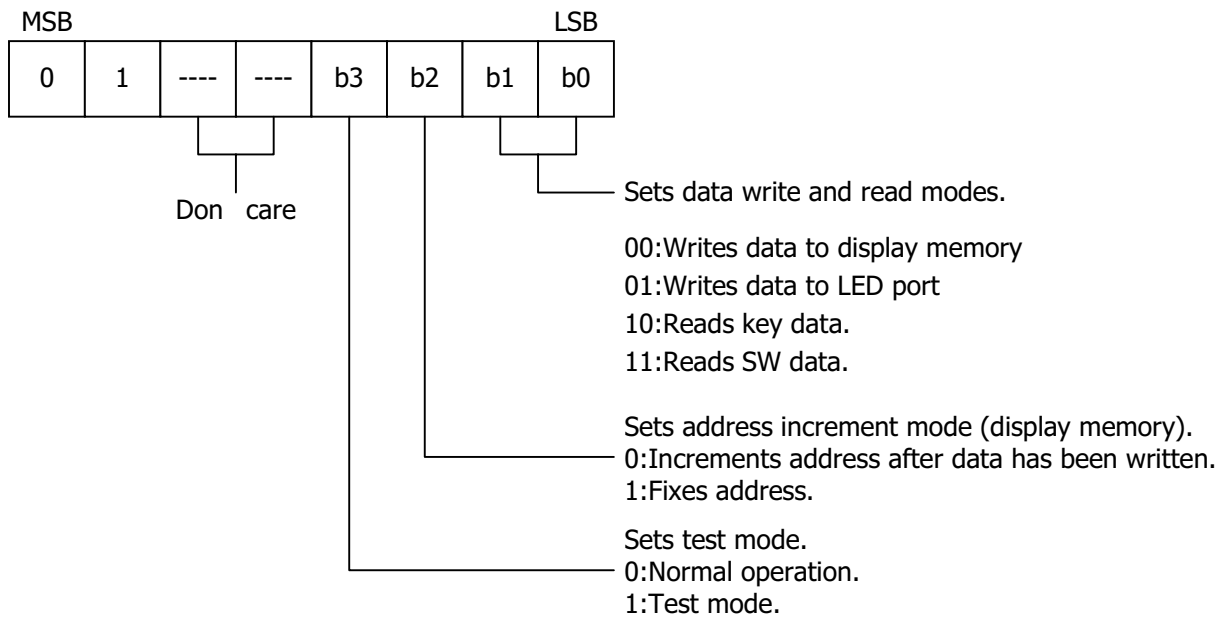


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## 1/8 - 1/16 Duty VFD Controller/Driver

### (2) Data setting command

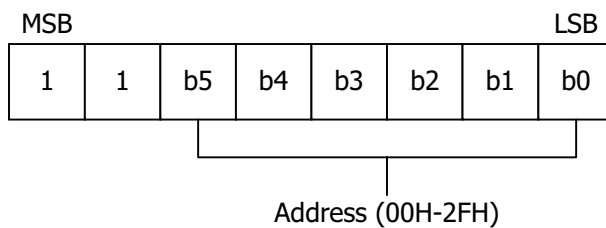
This command sets data write and read modes.



On power application, the normal operation mode and address increment mode set.

### (3) Address setting command

This command sets an address of the display memory.



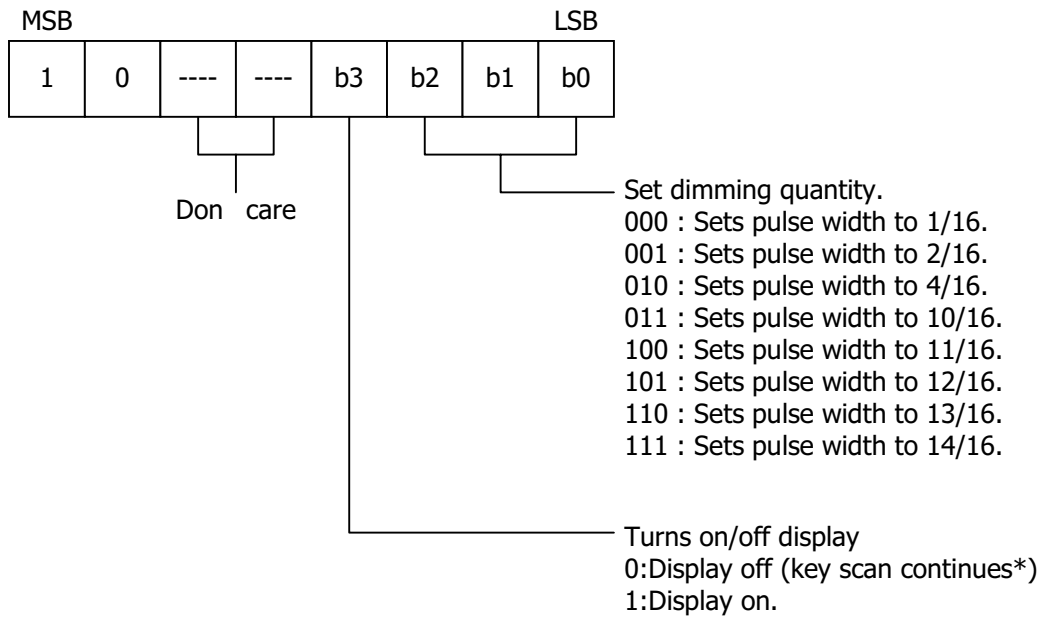
If address 30H or higher is set, the data is ignored, until a correct address is set.

On power application, the address is set to 00H.

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## 1/8 - 1/16 Duty VFD Controller/ Driver

### (4) Display control command



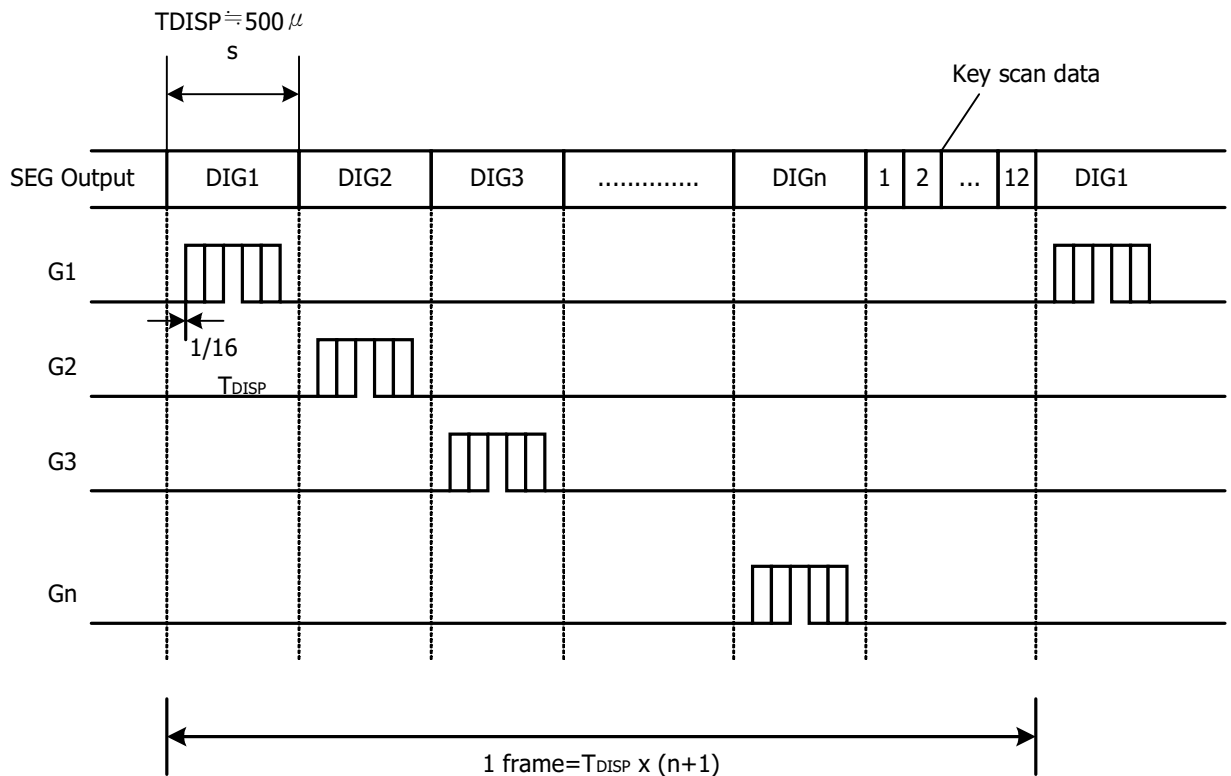
On power application, the 14/16-pulse width is set and the display is turned off.

\* : On power application, key scanning is stopped..

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## 1/8 - 1/16 Duty VFD Controller/Driver

### Key Scanning and Display Timing



One cycle of key scanning consists of two frames, and data of  $12 \times 4$  matrices is stored in RAM.

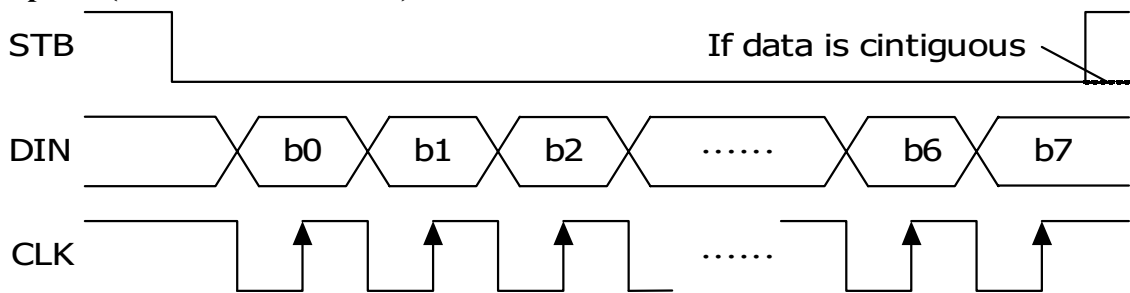


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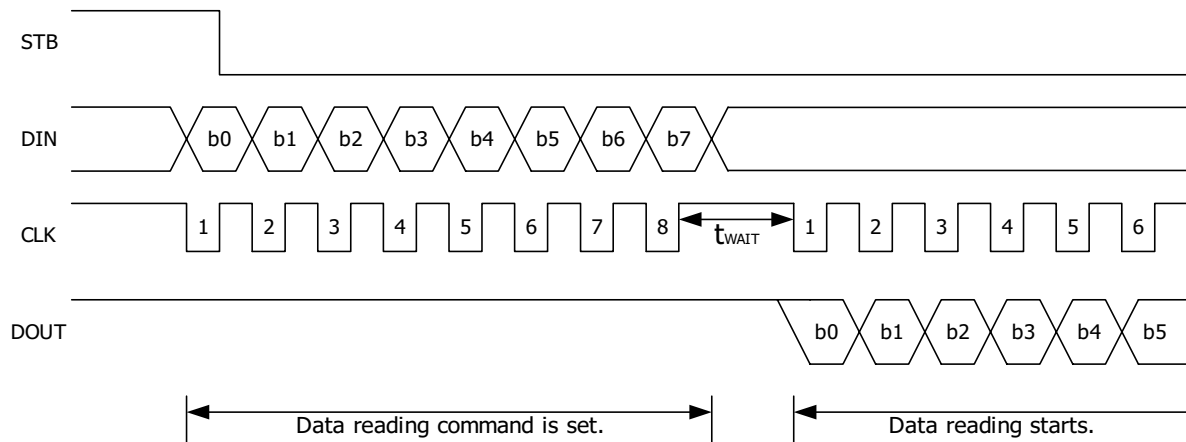
## 1/8 - 1/16 Duty VFD Controller/Driver

### Serial Communication Format

#### Reception (command/data write)



#### Transmission (data read)



Because the DOUT pin is an N-ch, open-drain output pin, be sure to connect an external pull-up resistor to this pin (1k $\Omega$  to 10 k $\Omega$ ).

\*:When data is read, a wait time  $t_{WAIT}$  of 1 $\mu$ s is necessary since the rising of the eighth clock that has set the command, until the falling of the first clock that has read the data.



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## 1/8 - 1/16 Duty VFD Controller/ Driver

### Absolute Maximum Ratings

**ABSOLUTE MAXIMUM RATING (Ta=25°C, Vss=0 V)**

PARAMETER	SYMBOL	RATINGS	UNIT
Logic Supply Voltage	V <sub>DD</sub>	-0.5 to + 7.0	V
Driver Supply Voltage	V <sub>EE</sub>	V <sub>DD</sub> +0.5 to V <sub>DD</sub> -40	V
Logic Input Voltage	V <sub>i1</sub>	-0.5 to V <sub>DD</sub> +0.5	V
FIP Driver Output Voltage	V <sub>o2</sub>	V <sub>EE</sub> -0.5 to V <sub>DD</sub> +0.5	V
LED Driver Output Current	I <sub>o1</sub>	25	mA
FIP Driver Output Current	I <sub>o2</sub>	-40 (grid) -15 (segment)	mA
Power Dissipation	P <sub>D</sub>	1200*	mW
Operating Ambient Temperature	T <sub>opt</sub>	-40 to +85	°C
Storage Temperature	T <sub>stg</sub>	-65 to +150	°C

\* Derate at -9.6 mW/°C at Ta=25°C or higher.



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## 1/8 - 1/16 Duty VFD Controller/Driver

### DC Electrical Characteristic

#### RECOMMENDED OPERATING CONDITION (Ta=-20

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Logic Supply Voltage	VDD	4.5	5	5.5	V	
High-Level input Voltage	Vih	0.6VDD		VDD	V	
Low-Level input Voltage	Vil	0		0.3VDD	V	
Driver Supply Voltage	VEE	0		VDD-35	V	

Maximum power consumption  $P_{max.} = \text{FIP driver dissipation} + R_L \text{ dissipation} + \text{LED driver dissipation} + \text{dynamic power consumption.}$

Where segment current = 3 mA, grid current = 15ma, and LED current = 20 mA,

FIP driver dissipation = number of segments x 6 + number of grids/(number of grids + 1) x 30 (mW)

$R_L \text{ dissipation} = (V_{DD} - V_{EE})^2 / 50 \times (\text{segment} + 1) \text{ (mW)}$

LED driver dissipation = number of LEDs x 20(mW)

Dynamic power consumption =  $V_{DD} \times 5 \text{ (mW)}$



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## 1/8 - 1/16 Duty VFD Controller/Driver

### Example

Where  $V_{EE} = -30\text{ V}$ ,  $V_{DD} = 5\text{ V}$ , and in 16-segment and 12-digit modes,

FIP driver dissipation = $16 \times 6 + 12/13 \times 35 =$	128
$R_L$ dissipation = $35^2/50 \times 17 =$	417
LED driver dissipation = $5 \times 20 =$	100
Dynamic power consumption = $5 \times 5 =$	25

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Total 670 mW

### ELECTRICAL SPECIFICATIONS(Ta= -20 to + 70°C ,VDD= 4.5 to 5.5V ,VS

=0V,VEE =VDD - 35V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
High-Level Output Voltage	$V_{OH1}$	$0.9 V_{DD}$			V	LED <sub>1</sub> - LED <sub>5</sub> , $I_{OH1} = -1\text{ mA}$
Low-Level Output Voltage	$V_{OL1}$			1	V	LED <sub>1</sub> - LED <sub>5</sub> , $I_{OL1} = 20\text{ mA}$
Low-Level Output Voltage	$V_{OL2}$			0.4	V	D <sub>OUT</sub> , $I_{OL2} = 4\text{ mA}$
High-Level Output Current	$I_{OH21}$	-3			mA	$V_o = V_{DD} - 2\text{V}$ , Seg <sub>1</sub> to Seg <sub>12</sub>
High-Level Output Current	$I_{OH22}$	-15			mA	$V_o = V_{DD} - 2\text{V}$ , Grid <sub>1</sub> to Grid <sub>8</sub> , Seg <sub>13</sub> /Seg <sub>16</sub> to Seg <sub>20</sub> /Seg <sub>9</sub>
Driver Leakage Current	$I_{OLEAK}$			-10	μA	$V_o = V_{DD} - 35\text{V}$ , Driver off
Output Pull-Down Resistor	$R_L$	50	100	150	kΩ	Driver output
Input Current	$I_i$			±1	μA	$V_i = V_{DD} - V_{SS}$
High-Level Output Voltage	$V_{IH}$	$0.6 V_{DD}$			V	
Low-Level Output Voltage	$V_{IL}$			$0.3 V_{DD}$	V	
Hysteresis Voltage	$V_H$		0.35		V	CLK, DIN, STB
Dynamic Current Consumption	$I_{DDdyn}$			5	mA	Under no load, display off



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## 1/8 - 1/16 Duty VFD Controller/Driver

### AC Electrical Characteristic

**SWITCHING CHARACTERISTICS**( $T_a = -20$  to  $+70^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{EE} = -30\text{V}$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Oscillation Frequency	$t_{OSC}$	350	500	650	kHz	$R = 56\text{k}\Omega$
Propagation Delay Time	$t_{PLZ}$			300	ns	CLK $\Rightarrow$ DOUT CL = 15pF, RL = 10k $\Omega$
	$t_{PZL}$			100	ns	
Rise Time	$t_{TZH1}$			2	$\mu\text{s}$	CL = 300 PF Seg1 to Seg12 Grid1 to Grid8 Seg13/Grid15 to Seg20/Grid9
	$t_{TZH2}$			0.5	$\mu\text{s}$	
Fall Time	$t_{THZ}$			120	$\mu\text{s}$	CL = 300 pF, Segn, Gridn
Maximum Clock Frequency	$f_{max}$	1			MHZ	Duty = 50%
Input Capacitance	C1			15	pF	

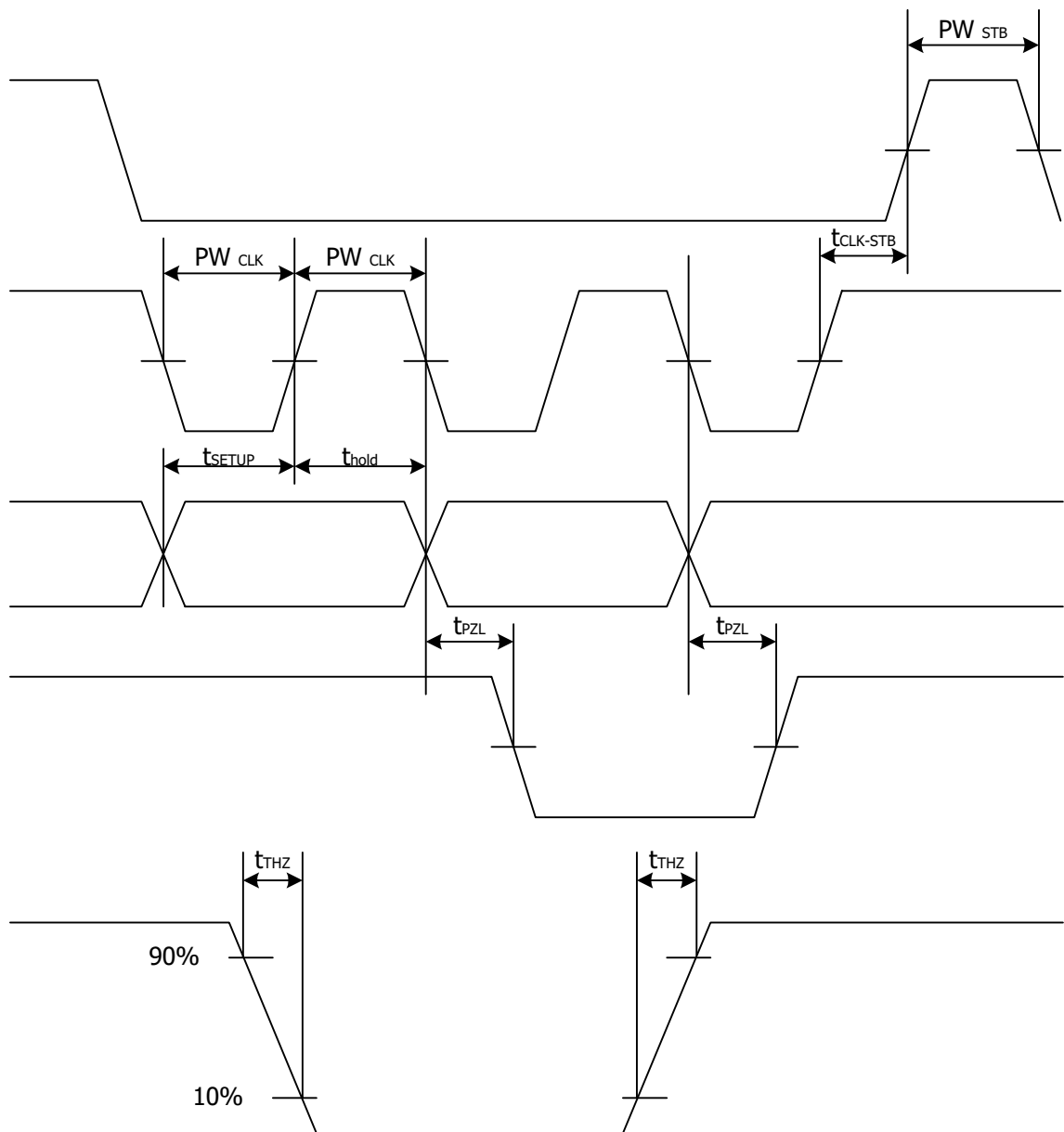
**TIMING CONDITIONS**( $T_a = -20$  to  $+70^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Clock Pulse Width	$PW_{CLK}$	400			ns	
Strobe Pulse Width	$PW_{STB}$	1			$\mu\text{s}$	
Data Setup Time	$t_{SETUP}$	100			ns	
Data Hold Time	$t_{HOLD}$	100			ns	
Clock-Strobe Time	$t_{CLK-STB}$	1			$\mu\text{s}$	CLK $\uparrow \rightarrow$ STB $\uparrow$
Wait Time	$t_{WAIT}$	1			$\mu\text{s}$	CLK $\uparrow \rightarrow$ CLK $\downarrow$

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## 1/8 - 1/16 Duty VFD Controller/Driver

### Switching Characteristic Waveform



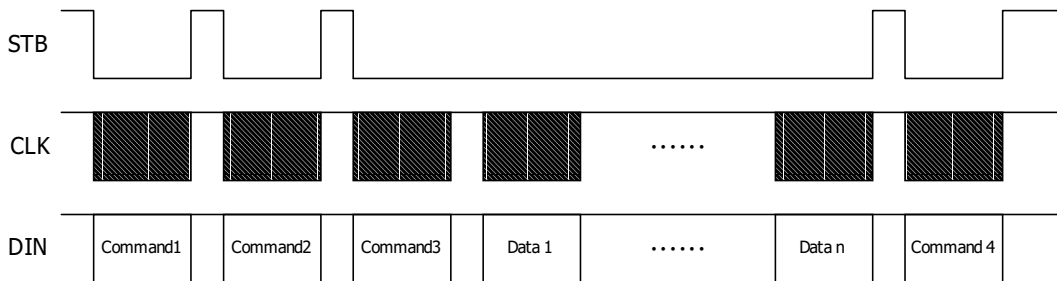


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## 1/8 - 1/16 Duty VFD Controller/Driver

### Application Notes

#### Updating display memory by incrementing address.



Command1: sets display mode

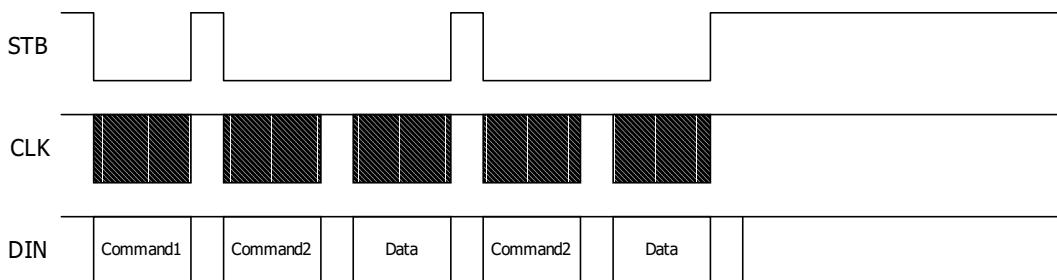
Command2: sets data

Command3: sets address

Data 1 to n : transfers display data (48 bytes max.)

Command4: controls display

#### Updating specific address



Command1: sets data

Command2: sets address

Data: display data